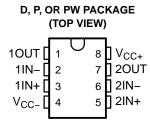
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FEATURES

- Operating Voltage...±2 V to ±18 V
- Low Offset Voltage...1 mV Max at 25°C, TL5580A
- Wide GBW...12 MHz Typ
- Slew Rate...5 V/μs Typ
- Low THD...0.0005% Typ
- Low-Noise Voltage...7 nV/√Hz at 1 kHz Typ

APPLICATIONS

- Audio
- Test Equipment
- Industrial Process Controls
- Data-Acquisition Systems
- Active Filters
- Power-Supply Regulation



DESCRIPTION/ORDERING INFORMATION

The TL5580 is a dual bipolar operational amplifier that combines both high dc and ac performance with its low offset voltage, high-gain bandwidth, low harmonic distortion, and low-noise characteristics. In addition, its output is capable of driving $600-\Omega$ loads. All these characteristics make the device ideally suited for use in audio, active filtering, and industrial measurement applications.

ORDERING INFORMATION

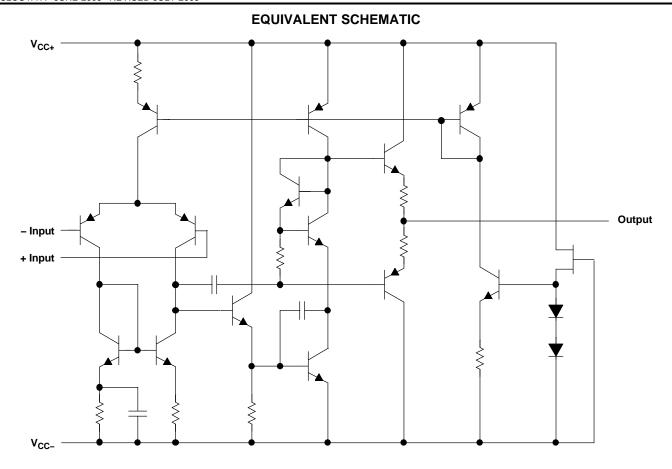
T _A	V _{IO} (25°C, MAX)	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
		PDIP – P	Tube of 50	TL5580IP	TL5580IP
		SOIC - D	Tube of 75	TL5580ID	75500
	Standard grade 1.5 mV	30IC - D	Reel of 2500	TL5580IDR	Z5580
		TSSOP – PW	Tube of 150	TL5580IPW	Z5580
–40°C to 85°C		1330P – PW	Reel of 2000	TL5580IPWR	25560
-40 C to 65 C		PDIP – P	Tube of 50	TL5580AIP	TL5580AIP
		SOIC - D	Tube of 75	TL5580AID	755004
	A grade 1 mV	30IC - D	Reel of 2500	TL5580AIDR	Z5580A
		TSSOP – PW	Tube of 150	TL5580AIPW	Z5580A
		1330P - FW	Reel of 2000	TL5580AIPWR	2000A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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TL5580, TL5580A **DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER**

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage			±18	V
VI	Input voltage (any input)			±15	V
V_{ID}	Differential input voltage			±30	V
Io	Output current			±50	mA
		D package		97	
θ_{JA}	Package thermal impedance (2)(3)	P package		85	°C/W
		P package PW package		149	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		-60	125	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating" conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC+}	Cumply voltage	2	16	\/
V _{CC} -	Supply voltage	-2	-16	V
T _A	Operating free-air temperature	-40	85	°C

Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. The package thermal impedance is calculated in accordance with JESD 51-7.

TL5580, TL5580A DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER

SLOS477A-JUNE 2005-REVISED JULY 2005



Electrical Characteristics

 $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
		TI FEROA		25°C		0.3	1	
.,	land offert college	TL5580A	D <4010	-40°C to 85°C			1.35	\/
V _{IO}	o Input offset voltage	TI 5500	$R_S \le 10 \text{ k}\Omega$	25°C		0.3	1.5	mV
		TL5580		-40°C to 85°C			2	
αV_{IO}	Average temperature coeff offset voltage	icient of input		-40°C to 85°C		1.8	5	μV/°C
-	land offers and an armount			25°C		5	75	A
I _{IO}	Input offset current			-40°C to 85°C			100	nA
	IB Input bias current			25°C		100	500	A
IB				-40°C to 85°C			800	nA
۸	A _{VD} Large-signal differential-voltage amplification		D > 2 kO V 140 V	25°C	90	110		dB
A _{VD}			$R_L \ge 2 \text{ k}\Omega, V_O = \pm 10 \text{ V}$	-40°C to 85°C	87			ив
	Outrout valta na avvia a		D > 0 lo	25°C	12.75 - 12.25	±13.5		V
V _{OM}	Output voltage swing		$R_L \ge 2 k\Omega$	-40°C to 85°C	12.5 –12			V
.,	Common model innut valte			25°C	±13	±13.5		V
V_{ICR}	Common-mode input voltage	ge range		-40°C to 85°C	±12			V
OMPD	0		$R_S \le 10 \text{ k}\Omega$,	25°C	90	110		-ID
CMRR	CMRR Common-mode rejection ratio		$V_{ICR} = -12 \text{ V to } 12 \text{ V}$	-40°C to 85°C	85			dB
ı. (1)	VR ⁽¹⁾ Supply-voltage rejection ratio		D <4010	25°C	85	110		٩D
K _{SVR} (1)			$R_{S} \le 10 \text{ k}\Omega$	-40°C to 85°C	83			dB
	Cumply gurrent (all generalities	" "		25°C		6	9	m A
Icc	Supply current (all amplifie	rs)		-40°C to 85°C			12	mA

⁽¹⁾ Measured with $V_{CC\pm}$ varied simultaneously

Operating Characteristics

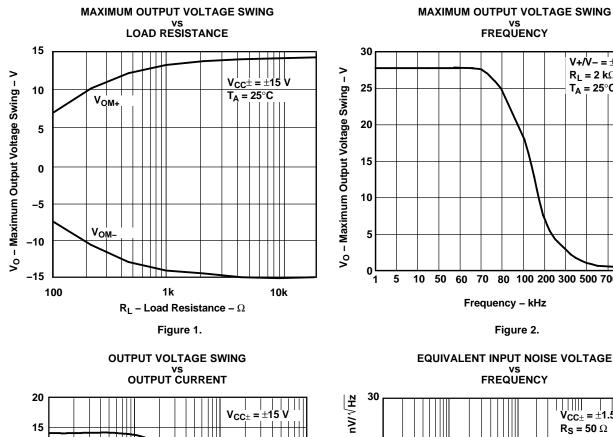
 $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

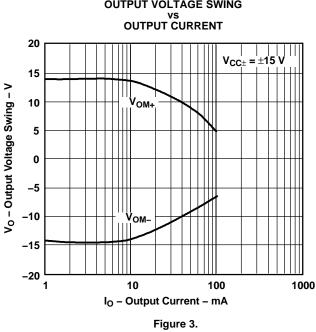
	PARAMETER	TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L \ge 2 \text{ k}\Omega$	5	V/μs
GBW	Gain bandwidth product	f = 10 kHz	12	MHz
THD	Total harmonic distortion	$V_O = 5 \text{ V}, R_L = 2 \text{ k}\Omega, f = 1 \text{ kHz}, A_{VD} = 20 \text{ dB}$	0.0005	%
V _n	Equivalent input noise voltage	f = 1 kHz	7	nV/√ Hz

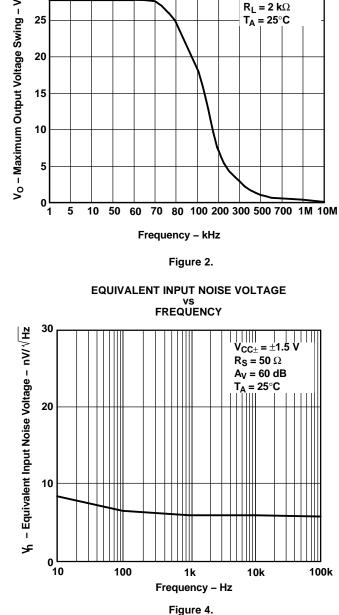
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V+/V-=±15 V

TYPICAL CHARACTERISTICS

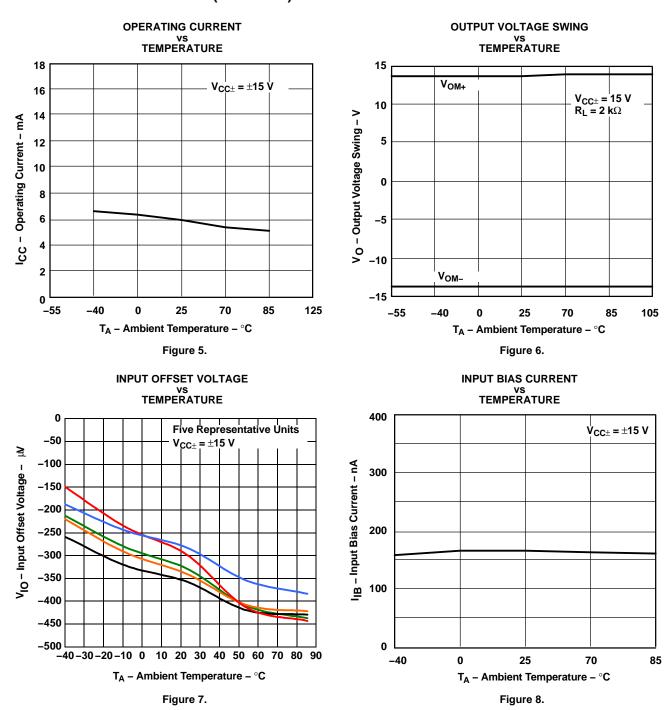








TYPICAL CHARACTERISTICS (continued)

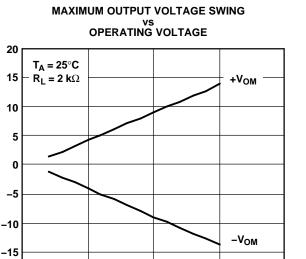




V_O- Maximum Output Voltage Swing - V

-20 L

TYPICAL CHARACTERISTICS (continued)



V_{CC+}/V_{CC-} – Operating Voltage – V Figure 9.

±10

±20

±15

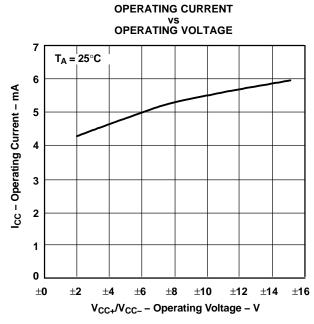


Figure 10.

TOTAL HARMONIC DISTORTION VS OUTPUT VOLTAGE

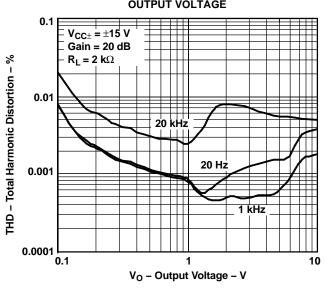


Figure 11.

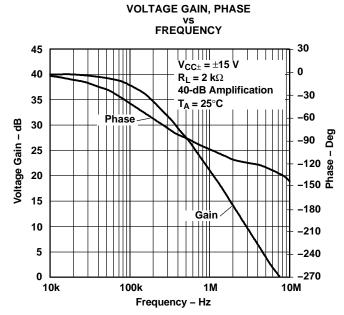


Figure 12.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TL5580AID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	Z5580A
TL5580AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A
TL5580AIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A
TL5580AIP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL5580AIP
TL5580AIP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL5580AIP
TL5580AIPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A
TL5580AIPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580A
TL5580IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580
TL5580IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580
TL5580IDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL5580IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL5580IP
TL5580IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL5580IP
TL5580IPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580
TL5580IPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z5580

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL5580AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5580AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL5580IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5580IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1



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*All dimensions are nominal

7 111 41111011010110 41 0 11011111141							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL5580AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TL5580AIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL5580IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL5580IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL5580AIP	Р	PDIP	8	50	506	13.97	11230	4.32
TL5580AIP.A	Р	PDIP	8	50	506	13.97	11230	4.32
TL5580IP	Р	PDIP	8	50	506	13.97	11230	4.32
TL5580IP.A	Р	PDIP	8	50	506	13.97	11230	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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