TL4050-Q1 Precision Micropower Shunt Voltage Reference

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: -40°C to +125°C
- Fixed output voltages of 2.048V, 2.5V, 4.096V, 5V
- Tight output tolerances and low temperature coefficient
  - Maximum 0.1%, 50ppm/°C – A Grade
  - Maximum 0.2%, 50ppm/°C – B Grade
  - Maximum 0.5%, 50ppm/°C – C Grade
- Low output noise: 41μV_{RMS} typical
- Wide operating current range: 60µA typical to 15mA
- Stable with all capacitive loads; no output capacitor required
- Available in extended temperature range: –40°C to 125°C

2 Applications

- Data-acquisition systems
- Power supplies and power-supply monitors
- Instrumentation and test equipment
- Process controls
- Precision audio
- Automotive electronics
- Energy management
- Battery-powered equipment

3 Description

The TL4050-Q1 family of shunt voltage references are versatile easy-to-use references designed for a wide array of applications. The two-terminal fixed-output device requires no external capacitors for operation and is stable with all capacitive loads. Additionally, the reference offers low dynamic impedance, low noise, and low temperature coefficient to maintain a stable output voltage over a wide range of operating currents and temperatures.

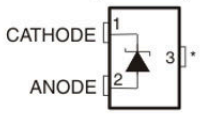
The TL4050-Q1 is available in three initial tolerances, ranging from 0.1% (maximum) for the A grade to 0.5% (maximum) for the C grade. Thus, a great deal of flexibility is available to designers in choosing the best cost-to-performance ratio for an application. Packaged in the space-saving SOT-23-3 and SC-70 packages and requiring a minimum current of 45µA (typical), the TL4050-Q1 also is designed for portable applications.

The TL4050x-Q1 characterization is for operation over an ambient temperature range of –40°C to 125°C.

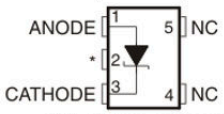
Table of Contents

4 Pin Configuration and Functions

DBZ (SOT-23-3) PACKAGE
(TOP VIEW)



DCK (SC-70) PACKAGE
(TOP VIEW)



NC – No internal connection

***In applications with high electromagnetic interference (for example, when placed near transformers or other electromagnetic sources) or significant high-frequency switching noise, TI recommends connecting this pin to the anode.** In applications where high electromagnetic interference (for example, when placed near transformers or other electromagnetic sources) or significant high-frequency switching noise is not present, you can consider leaving this pin floating.

5 Specifications

5.1 Absolute Maximum Ratings (1)

over free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_Z	Continuous cathode current	–10	20	mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) (2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) The human-body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. All pins are rated at 2kV for human-body model, but the feedback pin which is rated at 1kV.
(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
I_Z	Cathode current		(1)	15	mA
T_A	Free-air temperature	I temperature	–40	85	°C
		Q temperature	–40	125	

(1) See parametric tables

5.4 Thermal Information

THERMAL METRIC[1]		TL4050-Q1		UNIT
		DBZ	DCK	
		3 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[1]	331.1	289.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[1]	107.5	56.4	°C/W
θ_{JB}	Junction-to-board thermal resistance[1]	63.4	93	°C/W
ψ_{JT}	Junction-to-top characterization parameter[1]	4.9	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter[1]	61.7	91.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[1]	N/A	N/A	°C/W

5.5 TL4050x20-Q1 Electrical Characteristics

at extended temperature range, full range T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TL4050A20-Q1			TL4050B20-Q1			TL4050C20-Q1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse breakdown voltage	I_Z = 100µA	25°C		2.048			2.048			2.048		V
ΔV_Z	Reverse breakdown voltage tolerance	I_Z = 100µA	25°C	–2.048		2.048	–4.096		4.096	–10.24		10.24	mV
			Full range	–12.288		12.288	–14.7456		14.7456	–17.2032		17.2032	
$I_{Z,min}$	Minimum cathode current		25°C		41	60		41	60		41	60	µA
			Full range			65			65			65	
α_{VZ}	Average temperature coefficient of reverse breakdown voltage	I_Z = 10mA	25°C		±20			±20			±20		ppm/°C
		I_Z = 1mA	25°C		±15			±15			±15		
		I_Z = 100µA	25°C		±15			±15			±15		
			Full range			±50			±50			±50	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,min} < I_Z < 1$mA	25°C		0.3	0.8		0.3	0.8		0.3	0.8	mV
			Full range			1.2			1.2			1.2	
		1mA < I_Z < 15mA	25°C		2.3	6		2.3	6		2.3	6	
			Full range			8			8			8	
Z_Z	Reverse dynamic impedance	I_Z = 1mA, f = 120Hz, I_{AC} = 0.1 I_Z	25°C		0.3			0.3			0.3		Ω
e_N	Wideband noise	I_Z = 100µA, 10Hz ≤ f ≤ 10kHz	25°C		34			34			34		μV_{RMS}
	Long-term stability of reverse breakdown voltage	t = 1000h, T_A = 25°C ± 0.1°C, I_Z = 100µA			120			120			120		ppm
V_{HYST}	Thermal hysteresis(1)	ΔT_A = –40°C to 125°C			0.7			0.7			0.7		mV

(1) Thermal hysteresis is defined as $V_{Z,25°C}$ (after cycling to –40°C) – $V_{Z,25°C}$ (after cycling to 125°C).

5.6 TL4050x25-Q1 Electrical Characteristics

at extended temperature range, full range T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TL4050B25-Q1			UNIT
				MIN	TYP	MAX	
V_Z	Reverse breakdown voltage	I_Z = 100µA	25°C		2.5		V
ΔV_Z	Reverse breakdown voltage tolerance	I_Z = 100µA	25°C	–5		5	mV
			Full range	–18		18	
$I_{Z,min}$	Minimum cathode current		25°C		41	60	µA
			Full range			65	
α_{VZ}	Average temperature coefficient of reverse breakdown voltage	I_Z = 10mA	25°C		±20		ppm/°C
		I_Z = 1mA	25°C		±15		
		I_Z = 100µA	25°C		±15		
			Full range			±50	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,min} < I_Z < 1$mA	25°C		0.3	0.8	mV
			Full range			1.2	
		1mA < I_Z < 15mA	25°C		2.3	6	
			Full range			8	
Z_Z	Reverse dynamic impedance	I_Z = 1mA, f = 120Hz, I_{AC} = 0.1 I_Z	25°C		0.3		Ω
e_N	Wideband noise	I_Z = 100µA, 10Hz ≤ f ≤ 10kHz	25°C		41		μV_{RMS}
	Long-term stability of reverse breakdown voltage	t = 1000h, T_A = 25°C ± 0.1°C, I_Z = 100µA			120		ppm
V_{HYST}	Thermal hysteresis(1)	ΔT_A = –40°C to 125°C			0.7		mV

(1) Thermal hysteresis is defined as $V_{Z,25°C}$ (after cycling to –40°C) – $V_{Z,25°C}$ (after cycling to 125°C).

5.7 TL4050x41-Q1 Electrical Characteristics

at extended temperature range, full range T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TL4050B41-Q1			UNIT
				MIN	TYP	MAX	
V_Z	Reverse breakdown voltage	I_Z = 100µA	25°C		4.096		V
ΔV_Z	Reverse breakdown voltage tolerance	I_Z = 100µA	25°C	–8.2		8.2	mV
			Full range	–29		29	
$I_{Z,min}$	Minimum cathode current		25°C		52	68	µA
			Full range			78	
α_{VZ}	Average temperature coefficient of reverse breakdown voltage	I_Z = 10mA	25°C		±30		ppm/°C
		I_Z = 1mA	25°C		±20		
		I_Z = 100µA	25°C		±20		
			Full range			±50	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,min} < I_Z < 1$mA	25°C		0.2	0.9	mV
			Full range			1.2	
		1mA < I_Z < 15mA	25°C		2	7	
			Full range			10	
Z_Z	Reverse dynamic impedance	I_Z = 1mA, f = 120Hz, I_{AC} = 0.1 I_Z	25°C		0.5		Ω
e_N	Wideband noise	I_Z = 100µA, 10Hz ≤ f ≤ 10kHz	25°C		93		μV_{RMS}
	Long-term stability of reverse breakdown voltage	t = 1000h, T_A = 25°C ± 0.1°C, I_Z = 100µA			120		ppm
V_{HYST}	Thermal hysteresis(1)	ΔT_A = –40°C to 125°C			1.148		mV

(1) Thermal hysteresis is defined as $V_{Z,25°C}$ (after cycling to –40°C) – $V_{Z,25°C}$ (after cycling to 125°C).

5.8 TL4050x50-Q1 Electrical Characteristics

at extended temperature range, full range T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TL4050A50-Q1			TL4050B50-Q1			TL4050C50-Q1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse breakdown voltage	I_Z = 100µA	25°C		5			5			5		V
ΔV_Z	Reverse breakdown voltage tolerance	I_Z = 100µA	25°C	–5		5	–10		10	–25		25	mV
			Full range	–30		30	–35		35	–50		50	
$I_{Z,min}$	Minimum cathode current		25°C		56	74		56	74		56	74	µA
			Full range			90			90			90	
α_{VZ}	Average temperature coefficient of reverse breakdown voltage	I_Z = 10mA	25°C		±30			±30			±30		ppm/°C
		I_Z = 1mA	25°C		±20			±20			±20		
		I_Z = 100µA	25°C		±20			±20			±20		
			Full range			±50			±50			±50	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,min} < I_Z < 1$mA	25°C		0.2	1		0.2	1		0.2	1	mV
			Full range			1.4			1.4			1.4	
		1mA < I_Z < 15mA	25°C		2	8		2	8		2	8	
			Full range			12			12			12	
Z_Z	Reverse dynamic impedance	I_Z = 1mA, f = 120Hz, I_{AC} = 0.1 I_Z	25°C		0.5			0.5			0.5		Ω
e_N	Wideband noise	I_Z = 100µA, 10Hz ≤ f ≤ 10kHz	25°C		93			93			93		μV_{RMS}
	Long-term stability of reverse breakdown voltage	t = 1000h, T_A = 25°C ± 0.1°C, I_Z = 100µA			120			120			120		ppm
V_{HYST}	Thermal hysteresis(1)	ΔT_A = –40°C to 125°C			1.4			1.4			1.4		mV

(1) Thermal hysteresis is defined as $V_{Z,25°C}$ (after cycling to –40°C) – $V_{Z,25°C}$ (after cycling to 125°C).

5.9 Typical Characteristics

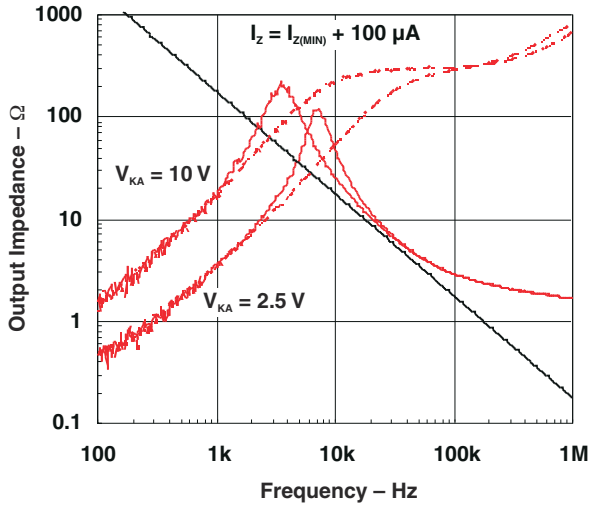


Figure 5-1. Output Impedance versus Frequency

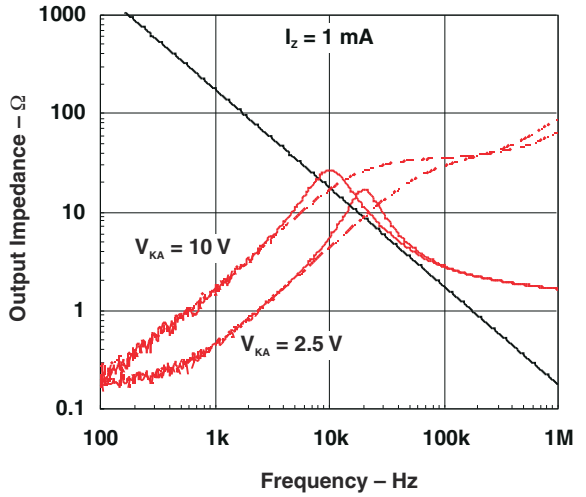


Figure 5-2. Output Impedance versus Frequency

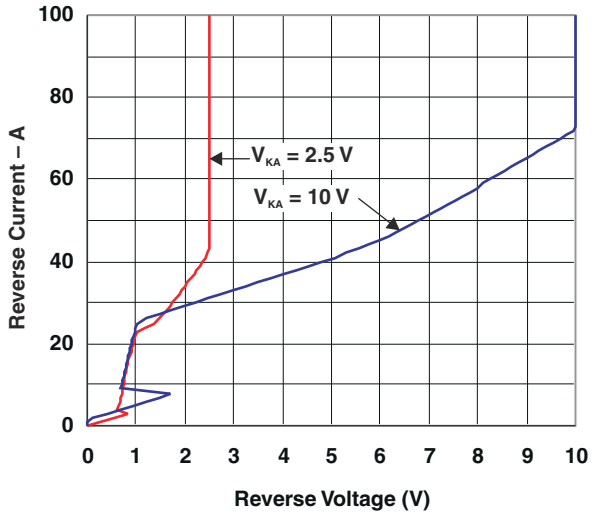


Figure 5-3. Reverse Characteristics And Minimum Operating Current

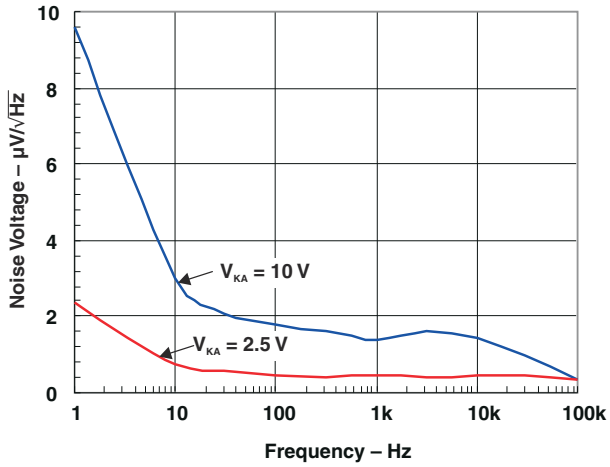


Figure 5-4. Noise Voltage versus Frequency

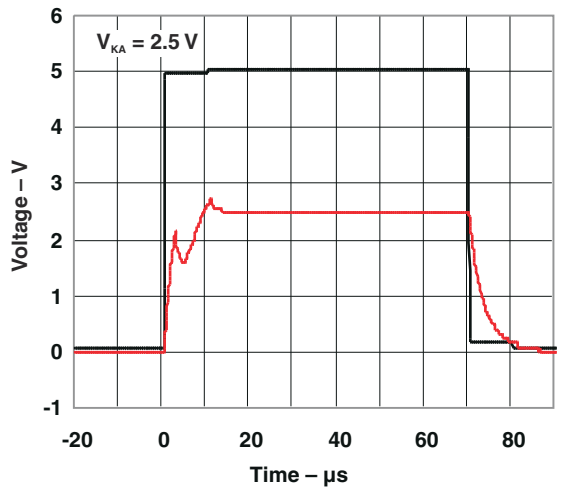


Figure 5-5. Large Signal Pulse Response

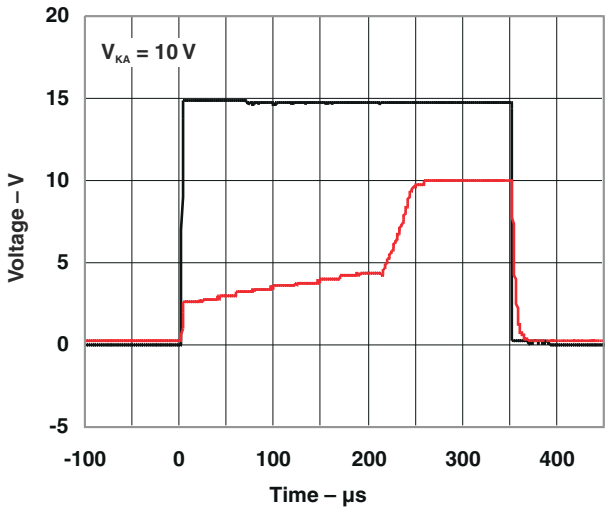


Figure 5-6. Large Signal Pulse Response

6 Detailed Description

6.1 Functional Block Diagram

For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

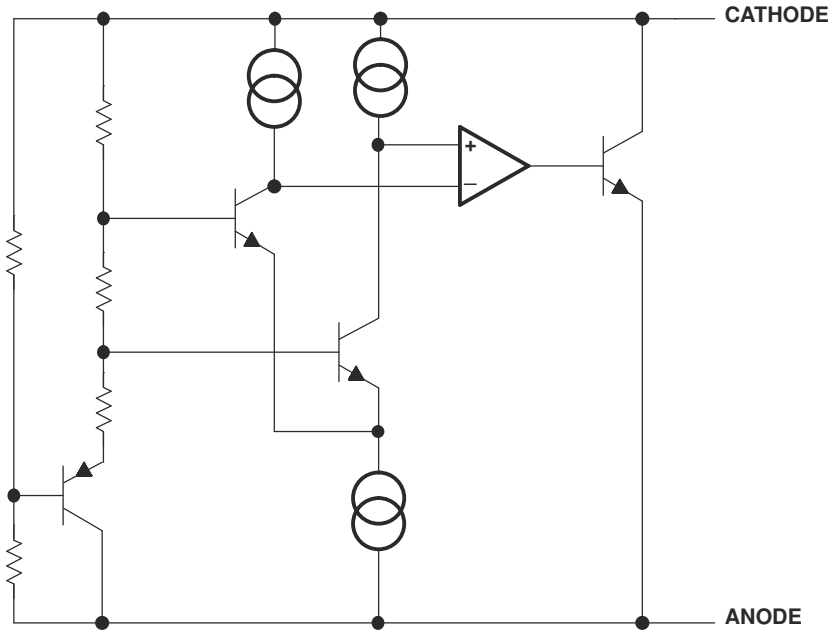


Figure 6-1. Functional Block Diagram

7 Application Information

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

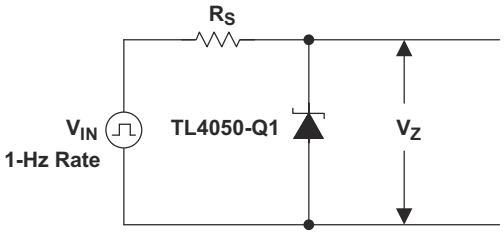


Figure 7-1. Start-Up Test Circuit

7.1 Output Capacitor

The TL4050-Q1 does not require an output capacitor across cathode and anode for stability. However, in an application using an output bypass capacitor, the TL4050-Q1 is stable with all capacitive loads.

7.2 SOT-23-3 Pin Connections

There is a parasitic Schottky diode connected between pins 2 and 3 of the SOT-23-3 packaged device. Thus, pin 3 of the SOT-23-3 package must be left floating or connected to pin 2. In applications with high electromagnetic interference (for example, when placed near transformers or other electromagnetic sources) or significant high-frequency switching noise, TI recommends connecting this pin to the anode.

7.3 Use With ADCs or DACs

The design of the TL4050x41-Q1 is as a cost-effective voltage reference, as required in 12-bit data-acquisition systems. For 12-bit systems operating from 5V supplies, such as the ADS7842 (see Figure 7-2), the TL4050x41-Q1 (4.096V) permits operation with an LSB of 1mV.

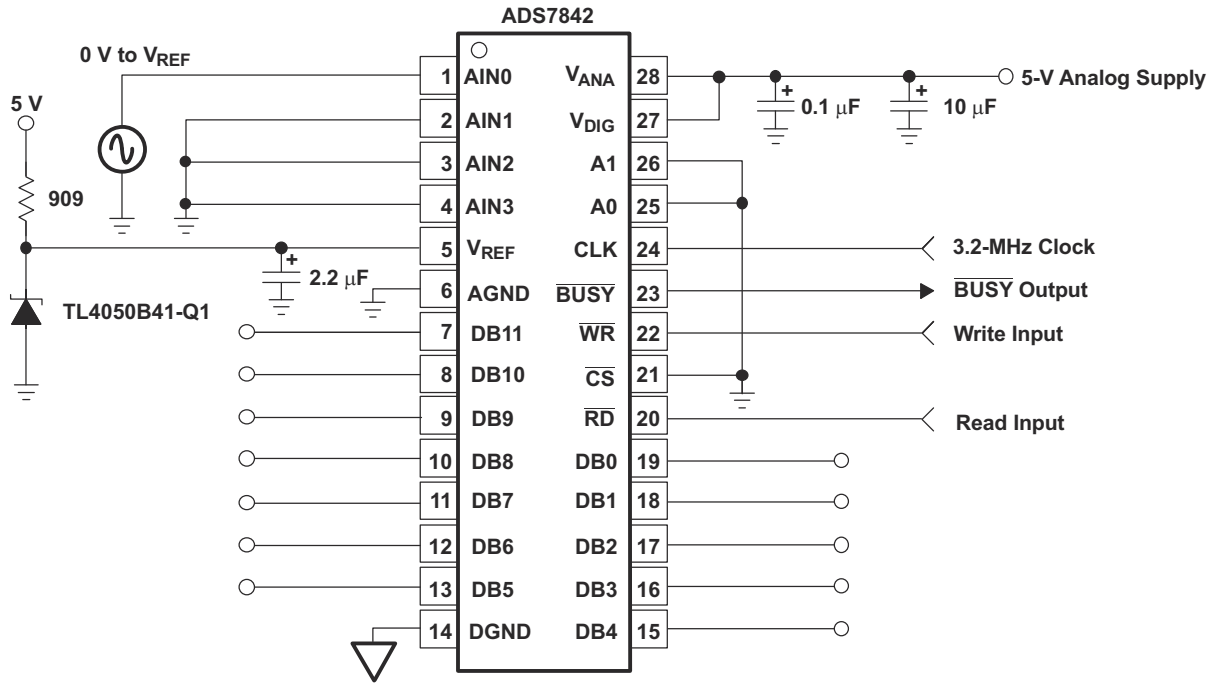


Figure 7-2. Data-Acquisition Circuit With TL4050x41-Q1

7.4 Cathode and Load Currents

In a typical shunt-regulator configuration (see Figure 7-3), an external resistor, R_S, connects between the supply and the cathode of the TL4050-Q1. Proper choice of R_S is essential, as R_S sets the total current available to supply the load (I_L) and bias the TL4050-Q1 (I_Z). In all cases, I_Z must stay within a specified range for proper operation of the reference. Taking into consideration one extreme in the variation of the load and supply voltage (maximum I_L and minimum V_S), R_S must be small enough to supply the minimum I_Z required for operation of the regulator, as given by data-sheet parameters. At the other extreme, maximum V_S and minimum I_L, R_S must be large enough to limit I_Z to less than the maximum-rated value of 15mA.

Equation 1 calculates R_S:

$$R_S = \frac{(V_S - V_Z)}{(I_L + I_Z)} \quad (1)$$

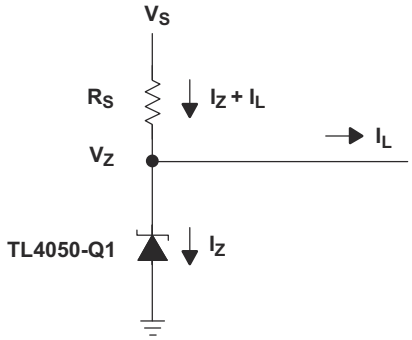


Figure 7-3. Shunt Regulator

8 Device and Documentation Support

8.1 Documentation Support

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2013) to Revision G (May 2025)	Page
• Added information about AEC-Q100 qualifications	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated pinout diagrams with device functionality information in high EMI or high switching environments.	1
• Added device functionality information in high EMI or high switching environments	3
• Added ESD ratings	4
• Added device functionality information in high EMI or high switching environments	13

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL4050A50QDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLGU
TL4050A50QDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLGU
TL4050A50QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	7GU
TL4050A50QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	7GU
TL4050B25QDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLHU
TL4050B25QDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLHU
TL4050B25QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	7HU
TL4050B25QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	7HU
TL4050B41QDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMXU
TL4050B41QDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMXU
TL4050B50QDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLJU
TL4050B50QDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLJU
TL4050B50QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	7JU
TL4050B50QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	7JU
TL4050C20QDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TMYU
TL4050C20QDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TMYU
TL4050C50QDBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TKZU
TL4050C50QDBZRQ1.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TKZU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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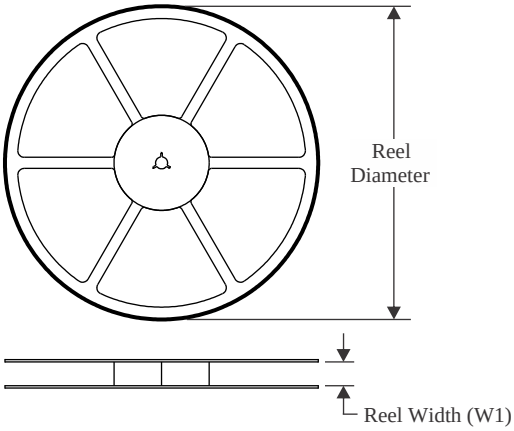
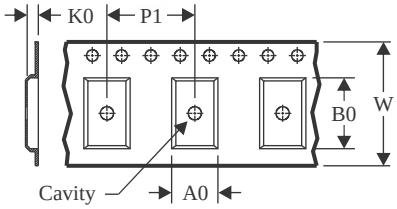
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

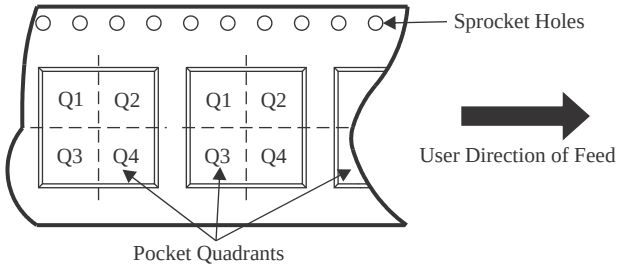


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

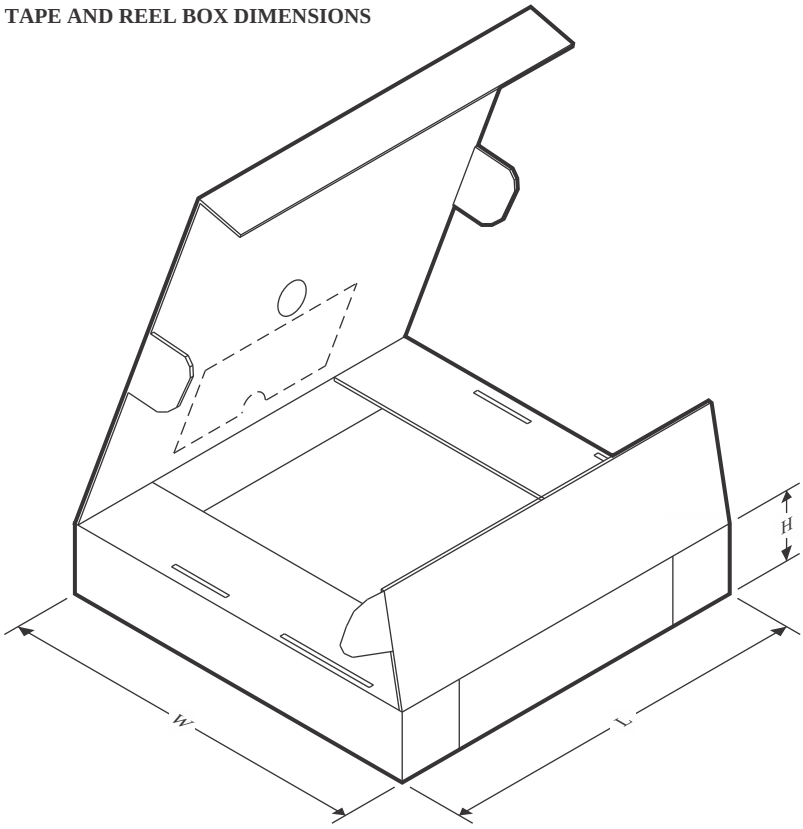
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL4050A50QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050A50QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TL4050A50QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL4050B25QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050B25QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TL4050B25QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL4050B41QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050B50QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050B50QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL4050B50QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TL4050C20QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050C20QDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
TL4050C50QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050C50QDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

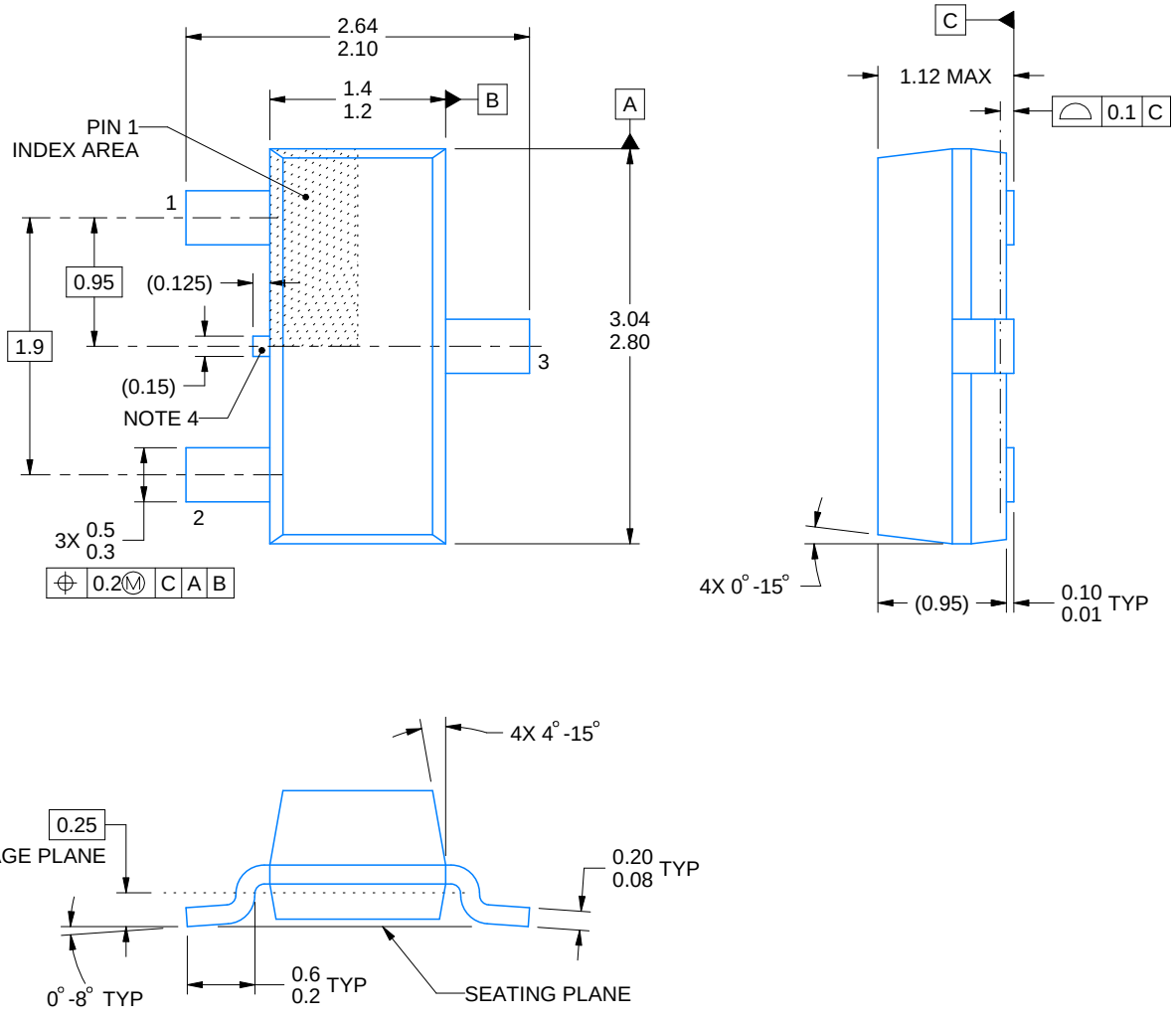
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL4050A50QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050A50QDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
TL4050A50QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
TL4050B25QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050B25QDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
TL4050B25QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
TL4050B41QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050B50QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050B50QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
TL4050B50QDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
TL4050C20QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050C20QDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TL4050C50QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050C50QDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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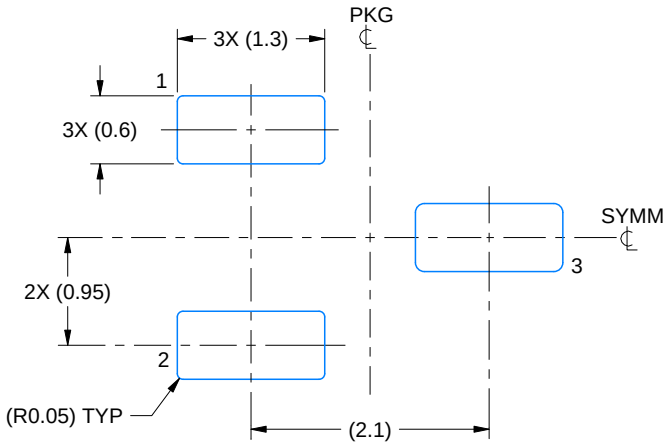
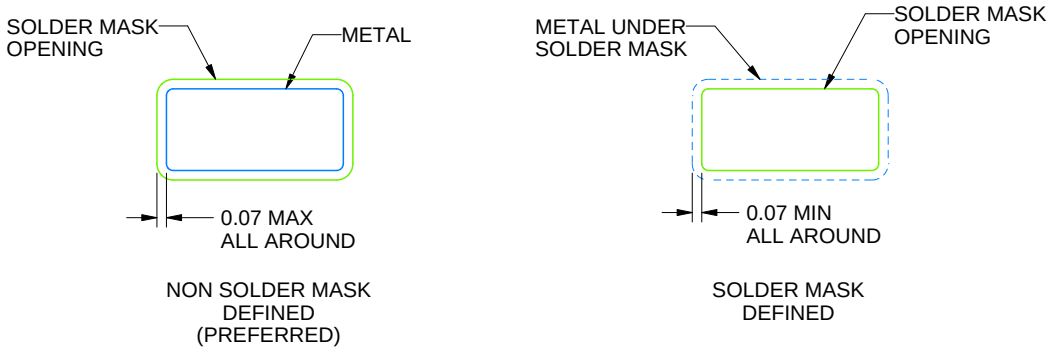
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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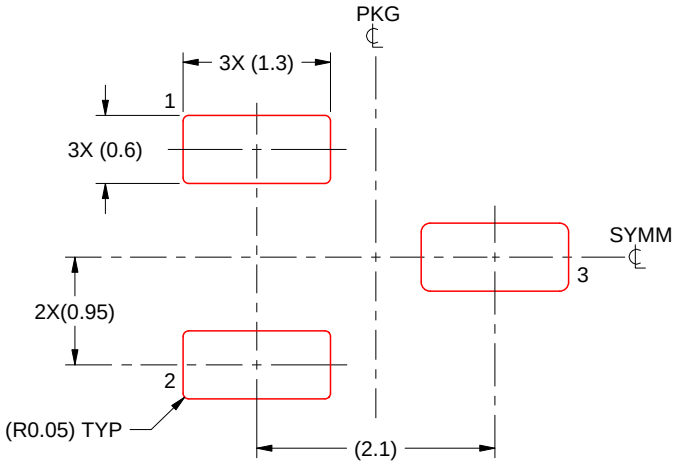
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

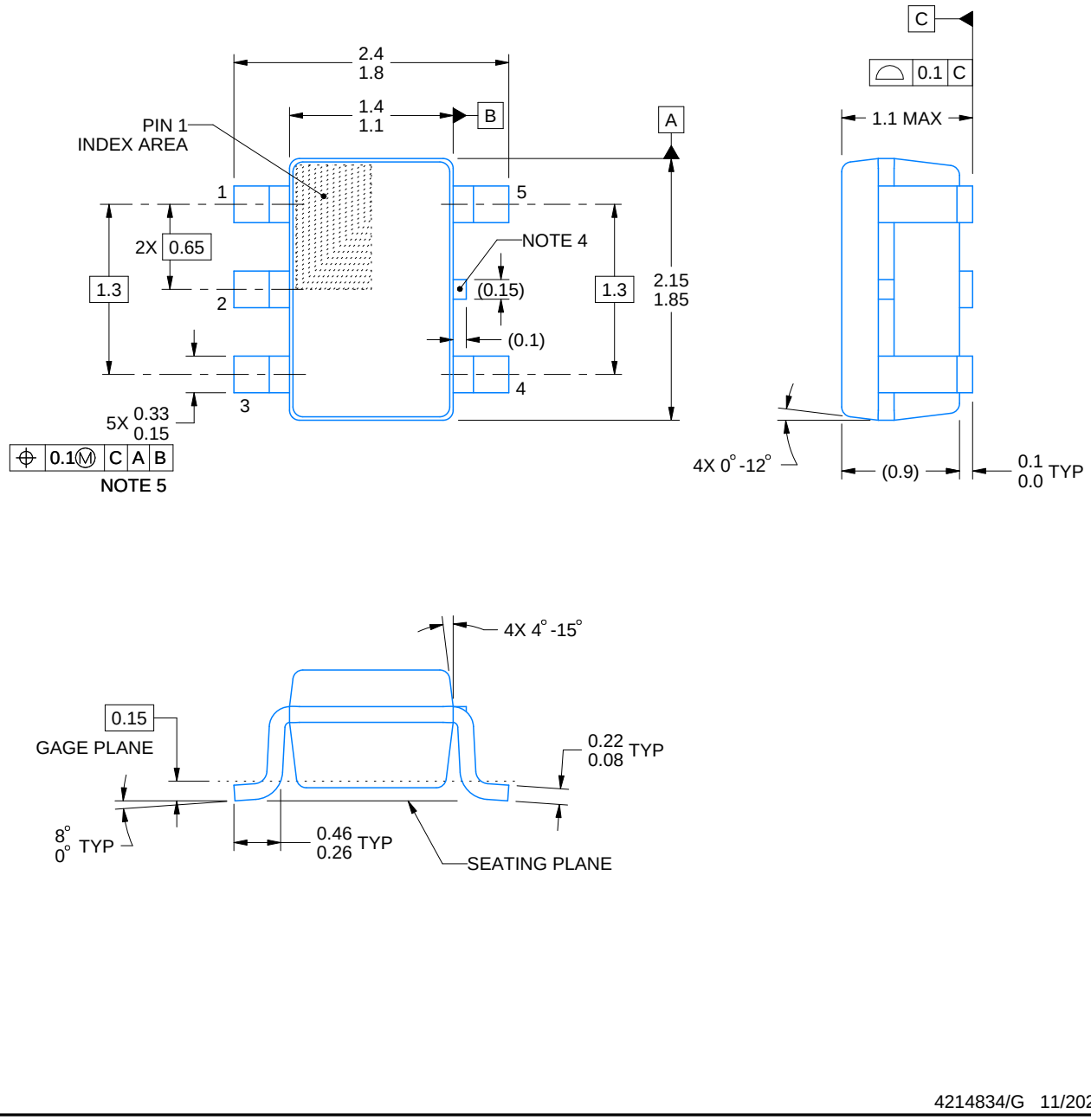
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

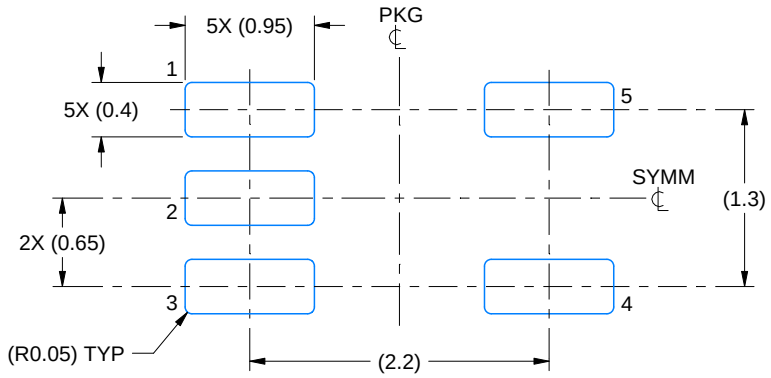
SMALL OUTLINE TRANSISTOR



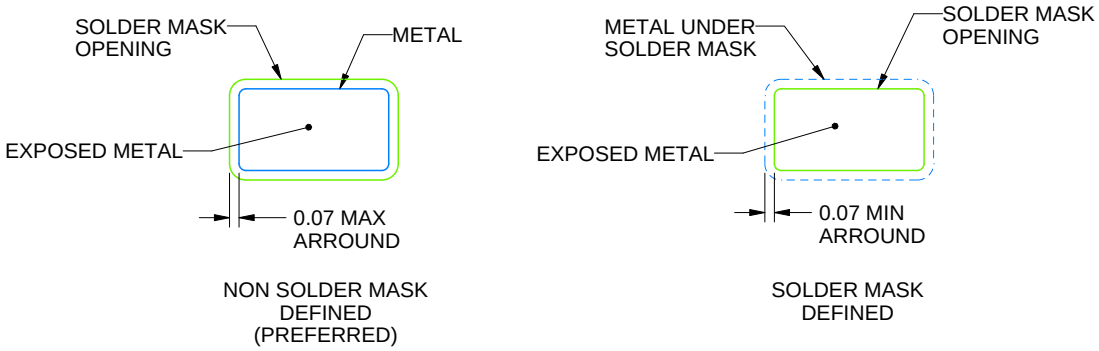
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

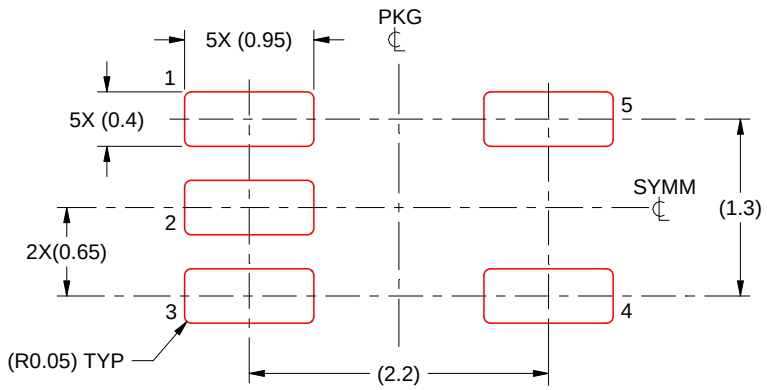


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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