# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

10UT [

v<sub>cc+</sub> []

20UT [

2IN+ [] 5

2IN- [] 6

1IN- | 2 1IN+ | 3

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14 🛮 40UT

13 4IN−

12 4IN+

10 3IN+

9 3IN-

8**∏** 30UT

11 V<sub>CC</sub>/GND

D, N, OR PW PACKAGE (TOP VIEW)

- Low Offset . . . 3 mV (Max) for A-Grade
- Wide Gain-Bandwidth Product . . . 4 MHz
- High Slew Rate . . . 13 V/μs
- Fast Settling Time . . . 1.1 μs to 0.1%
- Wide-Range Single-Supply Operation ... 4 V to 36 V
- Wide Input Common-Mode Range Includes Ground (V<sub>CC</sub>)
- Low Total Harmonic Distortion . . . 0.02%
- Large-Capacitance Drive Capability
   ... 10,000 pF
- Output Short-Circuit Protection
- Alternative to MC33074/A and MC34074/A

# description/ordering information

#### **ORDERING INFORMATION**

TA	V <sub>IO</sub> max AT 25°C	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
		PDIP (N)	Tube of 25	TL3474ACN	TL3474ACN	
		0010 (D)	Tube of 50	TL3474ACD	TI 0.47.4.A	
	A-grade: 3 mV	SOIC (D)	Reel of 2500	TL3474ACDR	TL3474A	
	01117	Tube of 90 TL3474ACPW		T0.47.4.4		
0°C to 70°C		TSSOP (PW)	Reel of 2000	TL3474ACPWR	T3474A	
	Standard grade:	PDIP (N)	Tube of 25	TL3474CN	TL3474CN	
		0010 (D)	Tube of 50	TL3474CD	TI 2474C	
		SOIC (D)	Reel of 2500	TL3474CDR	TL3474C TL3474	
	10 1117	TSSOP (PW)	Tube of 90	TL3474CPW	TI 0.47.4	
			Reel of 2000	TL3474CPWR	1L3474	
		PDIP (N)	Tube of 25	TL3474AIN	Z3474A	
		Tube of 50 TL3474AID		TL3474AID		
	A-grade: 3 mV	SOIC (D)	Reel of 2500	TL3474AIDR	Z3474A TL3474AI	
	01117	T000D (DIA))	Tube of 90	TL3474AIPW	70.47.4.4	
400C to 4050C		TSSOP (PW)	Reel of 2000	TL3474AIPWR	Z3474A	
–40°C to 105°C		PDIP (N)	Tube of 25	TL3474IN	TL3474IN	
		0010 (D)	Tube of 50	TL3474ID	TI 0.47.41	
	Standard grade: 10 mV	SOIC (D)	Reel of 2500	TL3474IDR	TL3474I	
	101111	T000D (DIA))	Tube of 90	TL3474IPW	70.47.4	
		TSSOP (PW)	Reel of 2000	TL3474IPWR	Z3474	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

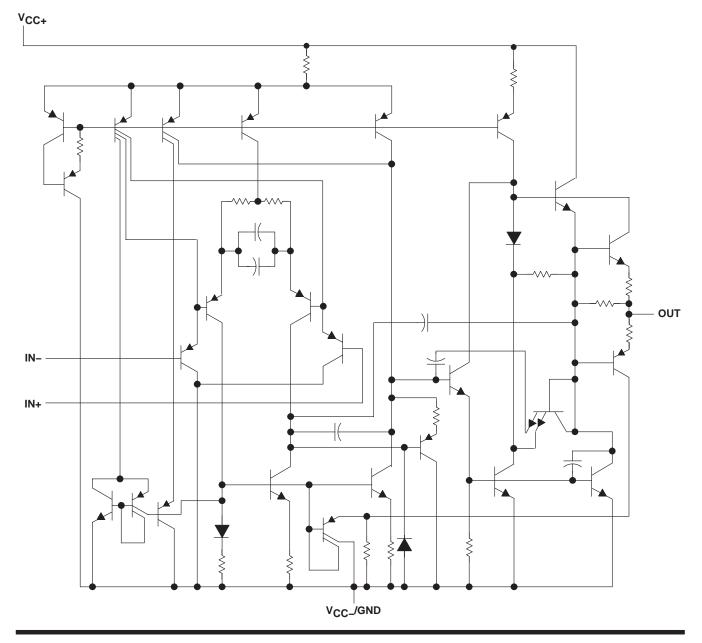


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## description/ordering information (continued)

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3474, TL3474A operational amplifiers. These devices offer 4 MHz of gain-bandwidth product,  $13\text{-V}/\mu\text{s}$  slew rate, and fast settling time without the use of JFET device technology. Although the TL3474 and TL3474A can be operated from split supplies, they are particularly suited for single-supply operation because the common-mode input voltage range includes ground potential ( $V_{\text{CC}}$ ). With a Darlington transistor input stage, these devices exhibit high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. These low-cost amplifiers are an alternative to the MC34074/A and MC33074/A operational amplifiers.

#### schematic (each amplifier)





# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V <sub>CC+</sub> (see Note 1)	18 V
V <sub>CC</sub>	
Differential input voltage, V <sub>ID</sub> (see Note 2)	±36 V
Input voltage, V <sub>I</sub> (any input)	V <sub>CC±</sub>
Input current, I <sub>I</sub> (each input)	±1 mA
Output current, IO	
Total current into V <sub>CC+</sub>	
Total current out of V <sub>CC</sub>	
Duration of short-circuit current at (or below) 25°C (see Note 3)	
Package thermal impedance, θ <sub>JA</sub> (see Notes 4 and 5): D package	86°C/W
N package	80°C/W
PW package	113°C/W
Operating virtual junction temperature, T <sub>J</sub>	
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC</sub>\_GND.
  - 2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than V<sub>CC</sub> 0.3 V.
  - 3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
  - 4. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  - 5. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions

			MIN	MAX	UNIT
VCC±	Supply voltage		4	36	V
.,	V <sub>CC</sub> = 5 V		0	2.8	V
VIC	Common-mode input voltage	$V_{CC\pm} = \pm 15 \text{ V}$	-15	12.8	V
т.	One wating tree air termograture	TL3474C, TL3474AC	0	70	°C
1A	Operating free-air temperature	TL3474I, TL3474AI	-40	105	

# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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# electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = $\pm 15$ V (unless otherwise noted)

	ARAMETER	TEST COND	ITIONS	Τ.		TL3474		٦	ΓL3474A	١	UNIT	
P	ARAMETER	TEST COND	IIIONS	TA	MIN	TYP†	MAX	MIN	TYP†	MAX	UNII	
	land offers		$V_{CC} = 5 V$	25°C		1.5	10		1.5	3		
VIO	Input offset voltage		V00 - +15 V	25°C		1.0	10		1.0	3	mV	
	Tenage		$V_{CC} = \pm 15 \text{ V}$	Full range‡			12			5		
αVΙΟ	Temperature coefficient of input offset voltage	V <sub>IC</sub> = 0, V <sub>O</sub> = 0,	V <sub>CC</sub> = ±15 V	Full range‡		10			10		μV/°C	
1	Input offset	$R_S = 50 \Omega$	V 145 V	25°C		6	75		6	75	A	
IIO	current		$V_{CC} = \pm 15 \text{ V}$	Full range <sup>‡</sup>			300			300	nA	
	land black coment		V 145 V	25°C		100	500		100	500	A	
IB	Input bias current		$V_{CC} = \pm 15 \text{ V}$	Full range‡			700			700	nA	
V <sub>ICR</sub>	Common-mode input voltage	R <sub>S</sub> = 50 Ω	,			–15 to 12.8			–15 to 12.8		V	
TION	range		Full range‡		–15 to 12.8			–15 to 12.8		v		
	High-level	$V_{CC+} = 5 \text{ V}, V_{CC-} = R_L = 2 \text{ k}\Omega$	25°C	3.7	4		3.7	4		.,		
Vон	VOH output voltage	R <sub>L</sub> = 10 kΩ	25°C	13.6	14		13.6	14		V		
		$R_L = 2 k\Omega$		Full range‡	13.4			13.4				
	Low-level	$V_{CC+} = 5 \text{ V}, V_{CC-} = R_L = 2 \text{ k}\Omega$	= 0,	25°C		0.1	0.3		0.1	0.3		
VOL	output voltage	$R_L = 10 \text{ k}\Omega$		25°C		-14.7	-14.3		-14.7	-14.3	V	
		$R_L = 2 k\Omega$		Full range‡			-13.5			-13.5		
A	Large-signal differential	V- 140 V B: 01		25°C	25	100		25	100		V/mV	
AVD	voltage amplification	$V_O = \pm 10 \text{ V, R}_L = 2 \text{ H}$	<b>47</b> 2	Full range‡	20			20			V/IIIV	
	Short-circuit	Source: V <sub>ID</sub> = 1 V,	VO = 0	25°C	-10	-34		-10	-34		A	
los	output current	Sink: $V_{ID} = -1 V$ ,	VO = 0	25°C	20	27		20	27		mA	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(min),$	$R_S = 50 \Omega$	25°C	65	97		80	97		dB	
ksvr	Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	$V_{CC\pm} = \pm 13.5 \text{ V to } \pm 100 \Omega$	16.5 V,	25°C	70	97		70	97		dB	
		\/- 0	No load	25°C		3.5	4.5		3.5	4.5		
Icc	Supply current	$V_{O} = 0,$	INO IOAG	Full range‡		4.5	5.5		4.5	5.5	mA	
100	(per channel)	$V_{CC+} = 5 \text{ V}, V_{O} = 2.$ $V_{CC-} = 0, \text{ No load}$	.5 V,	25°C		3.5	4.5		3.5	4.5	ША	



<sup>†</sup> All typical values are at T<sub>A</sub> = 25°C. ‡ Full range is 0°C to 70°C for the TL3474C, TL3474AC devices and -40°C to 105°C for the TL3474I, TL3474AI devices.

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# operating characteristics, $V_{CC\pm}$ = $\pm 15$ V, $T_A$ = $25^{\circ}C$

<b>UNIT</b> V/μs  μs
μδ
nV/√ <del>Hz</del>
pA/√ <del>Hz</del>
%
MHz
kHz
deg
-ID
dB
ΜΩ
pF
dB
Ω

## TYPICAL CHARACTERISTICS ( $T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)

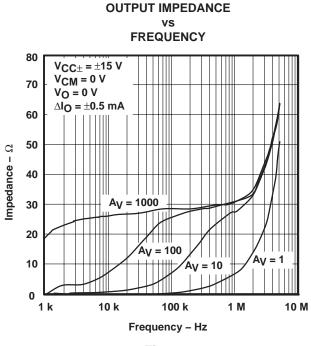


Figure 1

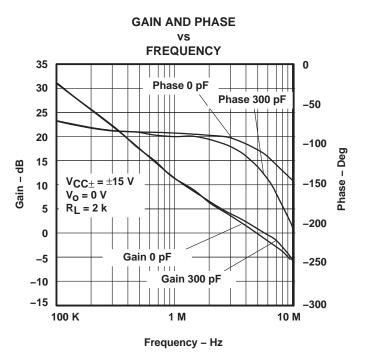


Figure 3

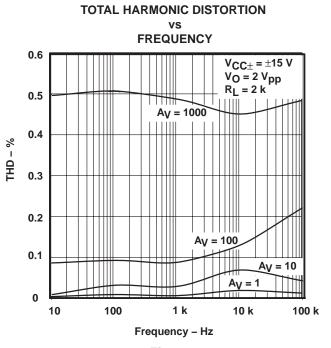


Figure 2

# **NORMALIZED INPUT BIAS CURRENT**

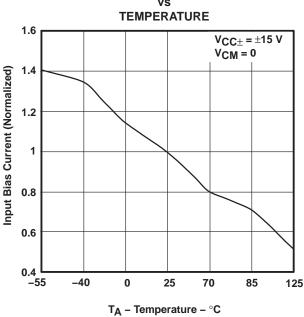


Figure 4



## TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)

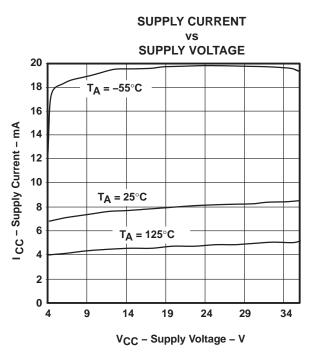


Figure 5

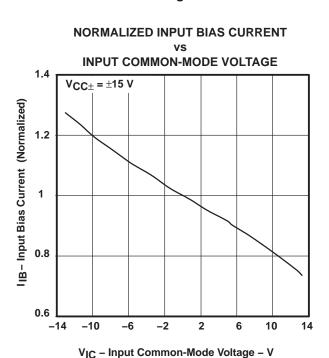


Figure 7

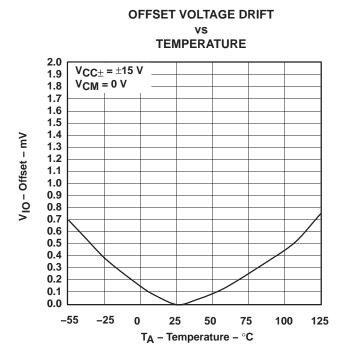


Figure 6

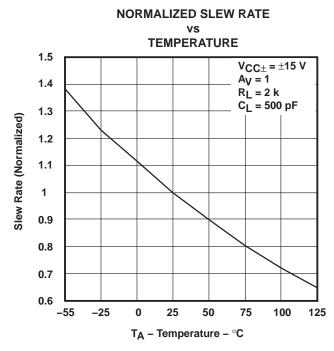


Figure 8

# TYPICAL CHARACTERISTICS ( $T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)

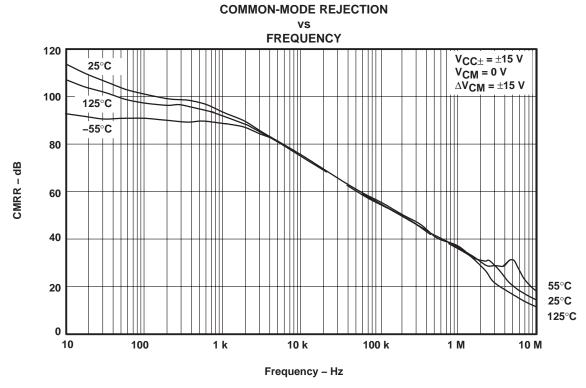


Figure 9

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## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TL3474ACDR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474A
TL3474ACDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474A
TL3474ACN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474ACN
TL3474ACN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474ACN
TL3474ACPWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T3474A
TL3474ACPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T3474A
TL3474AID	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 105	TL3474AI
TL3474AIDR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI
TL3474AIDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI
TL3474AIDR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	-	Call TI	Call TI	-40 to 105	
TL3474AIDRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI
TL3474AIDRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI
TL3474AIN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474AIN
TL3474AIN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474AIN
TL3474AIPWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474A
TL3474AIPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474A
TL3474CD	Obsolete	Production	SOIC (D)   14	-	=	Call TI	Call TI	0 to 70	TL3474C
TL3474CDR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474C
TL3474CDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474C
TL3474CN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474CN
TL3474CN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474CN
TL3474CPWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	T3474
TL3474CPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T3474
TL3474ID	Obsolete	Production	SOIC (D)   14	-	=	Call TI	Call TI	-40 to 105	TL3474I
TL3474IDR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474I
TL3474IDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474I
TL3474IDR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	=	Call TI	Call TI	-40 to 105	
TL3474IN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474IN
TL3474IN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474IN



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Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TL3474IPWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 105	Z3474
TL3474IPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3474ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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\*All dimensions are nominal

All difficultions are norminal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3474ACDR	SOIC	D	14	2500	340.5	336.1	32.0
TL3474ACPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL3474ACPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL3474AIDR	SOIC	D	14	2500	353.0	353.0	32.0
TL3474AIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TL3474AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL3474AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL3474CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL3474CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474IDR	SOIC	D	14	2500	353.0	353.0	32.0
TL3474IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

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### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL3474ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL3474AIN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474AIN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL3474CN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL3474IN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474IN.A	N	PDIP	14	25	506	13.97	11230	4.32

# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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