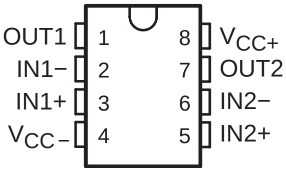
TL3414A
DUAL HIGH-OUTPUT-CURRENT OPERATIONAL AMPLIFIER

SLOS453A − DECEMBER 2004 − REVISED JANUARY 2005

- **Single/Dual Power-Supply Operation**
- **High Output Current . . . 70 mA, V_{CC+} = 5 V**
- **Wide Operating Voltage . . . 3 V to 15 V (Single Supply)**
- **Ideal for Headphone Drivers**

D (SOIC), P (PDIP), OR PW (TSSOP) PACKAGE
(TOP VIEW)



description/ordering information

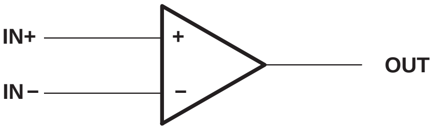
The TL3414A device is a dual operational amplifier that can be operated with single or dual power supplies. In addition to high gain and high output voltage swing, it is capable of driving a 70-mA load, making it ideally suited for simple, low-cost audio-amplifier applications, such as headphone amplifiers in DVD and CDRW applications.

ORDERING INFORMATION

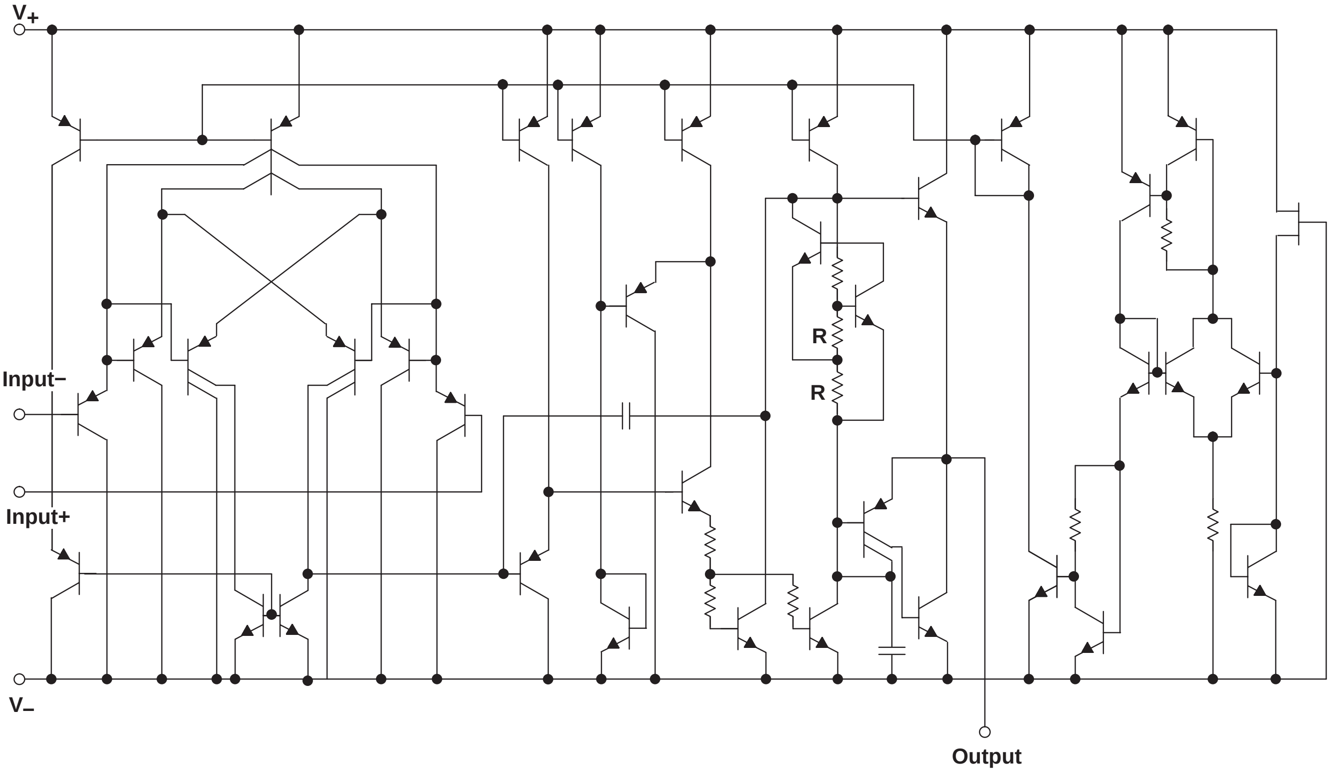
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP (P)	Tube of 50	TL3414AIP	TL3414AIP
	SOIC (D)	Tube of 75	TL3414AID	Z3414A
		Reel of 2500	TL3414AIDR	
	TSSOP (PW)	Tube of 150	TL3414AIPW	Z3414A
		Reel of 2000	TL3414AIPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol (each amplifier)



simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (single supply)		15 V
Supply voltage, V_{CC-} (single supply)		0 V
Supply voltage, V_{CC+} (dual supply)		7.5 V
Supply voltage, V_{CC-} (dual supply)		−7.5 V
Supply voltage, (V_{CC-} to V_{CC+})		15 V
Input voltage, either input (see Note 1)		V_{CC-} or V_{CC+}
Input current (see Note 2)		±10 mA
Duration of output short circuit (see Note 3)		Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5):	D package	97°C/W
	P package	85°C/W
	PW package	149°C/W
Operating virtual junction temperature, T_J		150°C
Storage temperature range, T_{stg}		−40°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
2. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
3. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
4. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage (single supply)	3	15	V
V_{CC+}	Supply voltage (dual supply)	1.5	7.5	V
V_{CC-}	Supply voltage (dual supply)	−1.5	−7.5	V
V_{ID}	Differential input voltage		15	V
V_I	Input voltage	−0.3	15	V
T_A	Operating free-air temperature range	−40	85	°C

DC electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S = 0\ \Omega$		2	5	mV
I_{IO}	Input offset current			15	100	nA
I_{IB}	Input bias current			300	600	nA
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$	77	100		dB
V_{ICR}	Common-mode input voltage range		$V_{CC+} - 2V$			V
V_{OM}	Output voltage swing	$R_L > 2\ k\Omega$, $V_{CC+} = 5$ V	3.5			V
		$I_O = 70$ mA, $V_{CC+} = 5$ V	3.2			
CMRR	Common-mode rejection ratio		70	79		dB
k_{SVR}†	Supply-voltage rejection ratio		80	90		dB
I_{CC}	Supply current (all amplifiers)	R_L = open circuit (full temperature range)	3	4	6	mA

† Measured with $V_{CC\pm}$ differentially and simultaneously varied from 5 V to 8.6 V

AC electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain		0.83	V/μs
GBW	Gain bandwidth product		1.1	MHz
V_n	Equivalent input noise voltage	f = 1 kHz	18	$nV/\sqrt{Hz}$

DC electrical characteristics, V_{CC+} = 8.6 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S = 0\ \Omega$		2	5	mV
I_{IO}	Input offset current			15	100	nA
I_{IB}	Input bias current			300	600	nA
A_{VD}	Large-signal differential voltage amplification	$R_L = 2\ k\Omega$	88	105		dB
V_{ICR}	Common-mode input voltage range		$V_{CC+} - 2V$			V
V_{OM}	Output voltage swing	$R_L > 2\ k\Omega$, $V_{CC+} = 8.6$ V	7			V
		$I_O = 70$ mA, $V_{CC+} = 8.6$ V	6.7			
CMRR	Common-mode rejection ratio		80	90		dB
k_{SVR}†	Supply-voltage rejection ratio		80	90		dB
I_{CC}	Supply current (all amplifiers)	R_L = open circuit (full temperature range)	3	4	6	mA

† Measured with $V_{CC\pm}$ differentially and simultaneously varied from 5 V to 8.6 V

AC electrical characteristics, V_{CC+} = 8.6 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain		1.3	V/μs
GBW	Gain bandwidth product		2	MHz
V_n	Equivalent input noise voltage	f = 1 kHz	18	$nV/\sqrt{Hz}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL3414AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A
TL3414AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A
TL3414AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A
TL3414AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A
TL3414AIPW	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A
TL3414AIPW.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A
TL3414AIPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A
TL3414AIPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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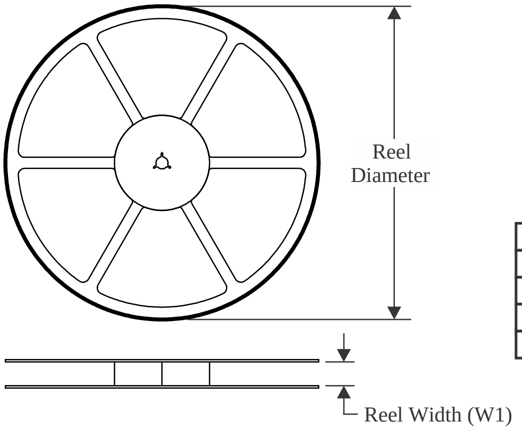
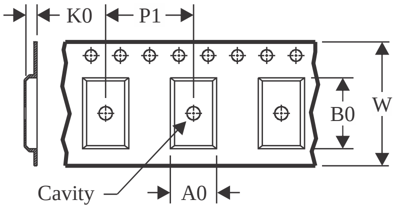
TAPE AND REEL INFORMATION

REEL DIMENSIONS

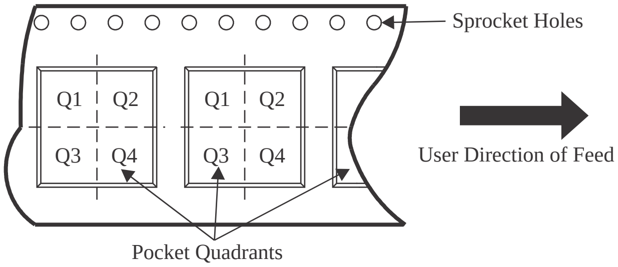


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

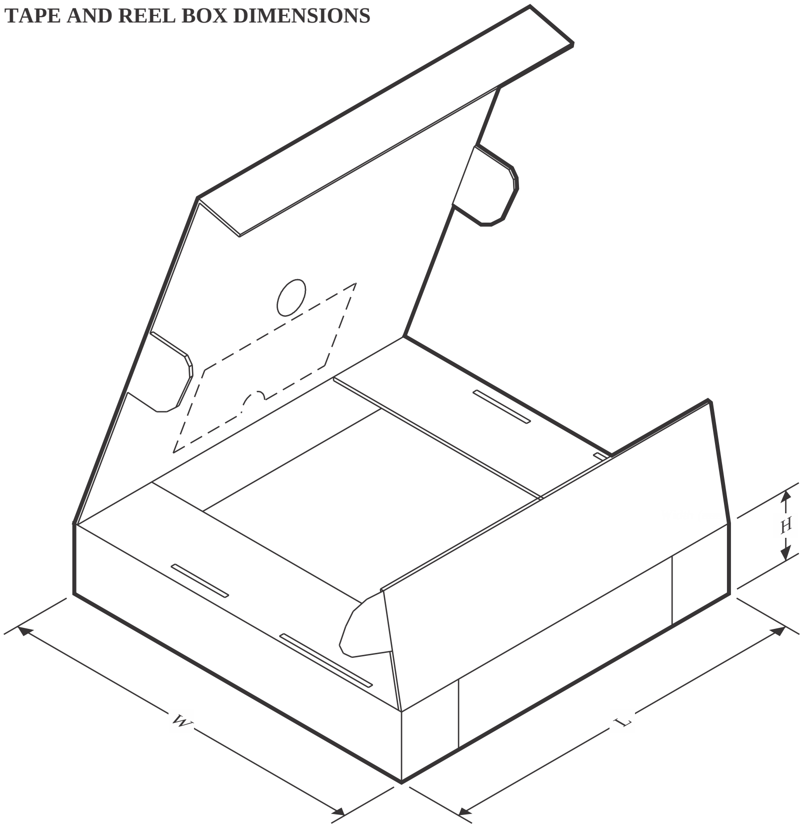
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3414AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3414AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

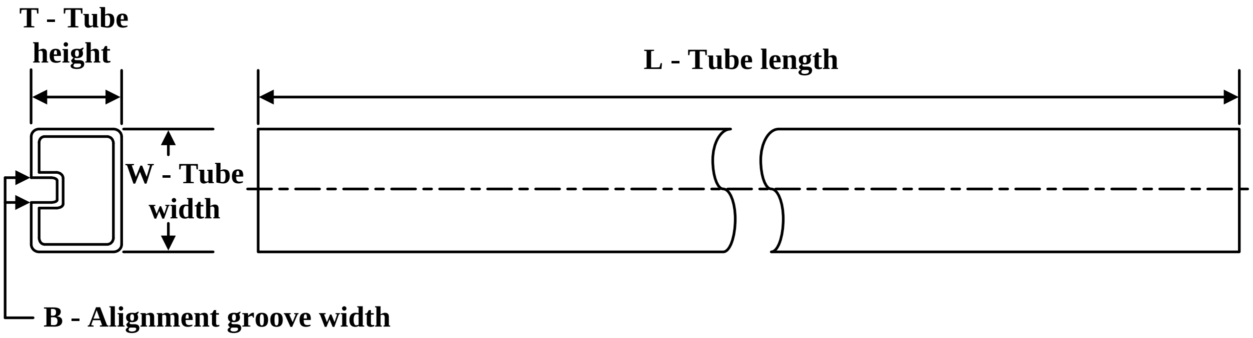
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3414AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL3414AIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

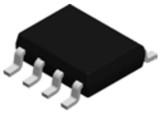
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL3414AID	D	SOIC	8	75	507	8	3940	4.32
TL3414AID.A	D	SOIC	8	75	507	8	3940	4.32
TL3414AIPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TL3414AIPW.A	PW	TSSOP	8	150	530	10.2	3600	3.5

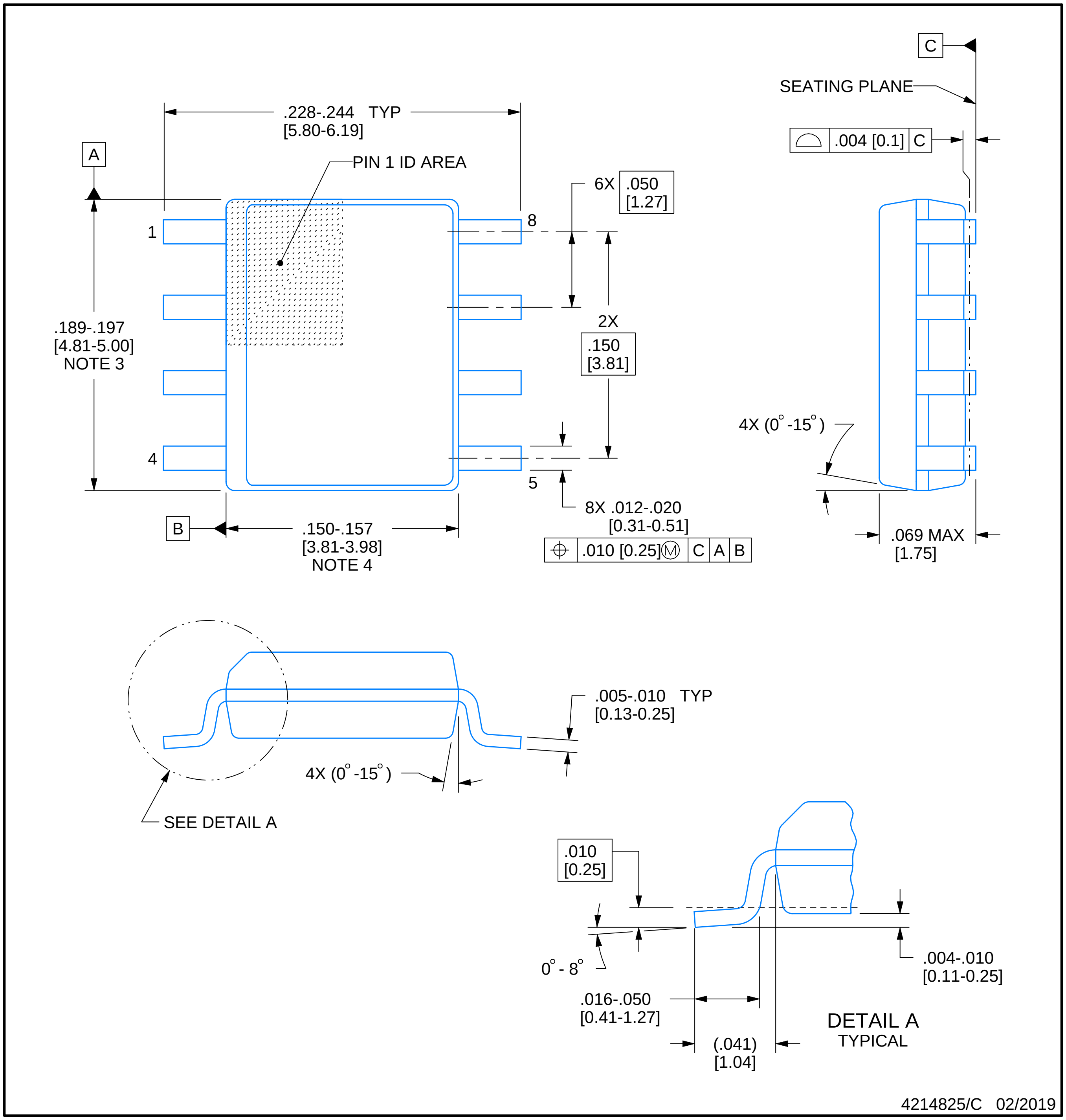
PACKAGE OUTLINE



D0008A

SOIC - 1.75 mm max height

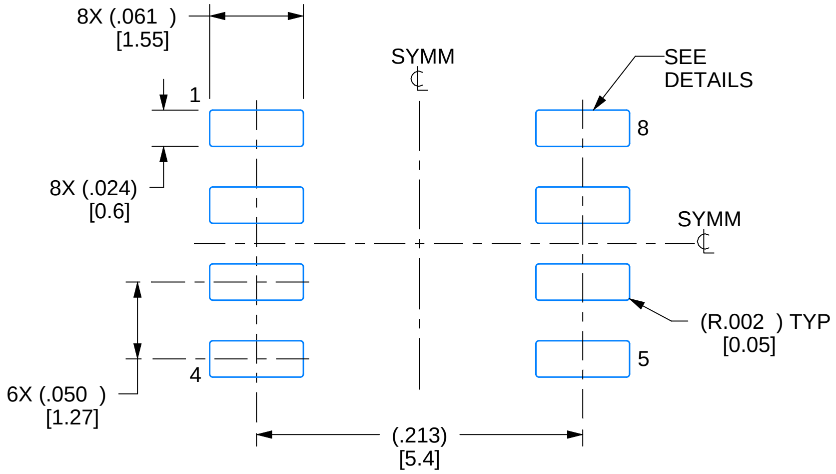
SMALL OUTLINE INTEGRATED CIRCUIT



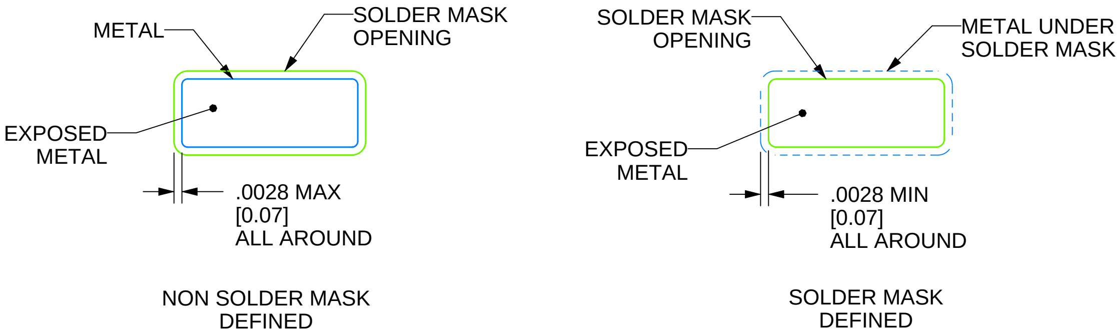
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



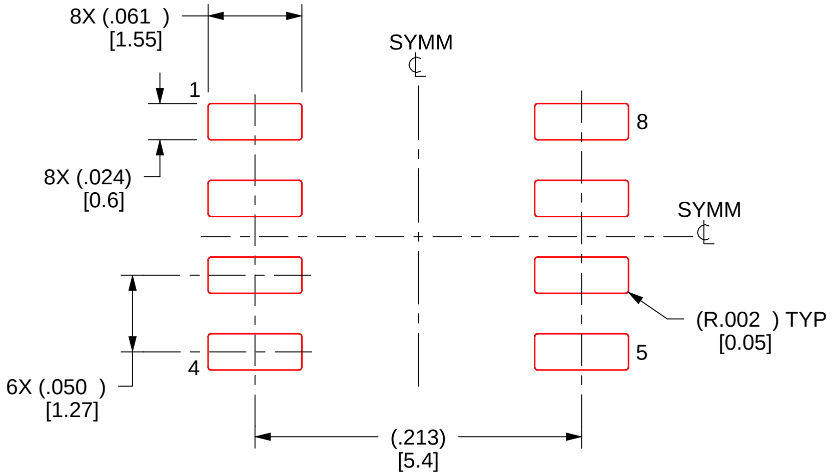
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

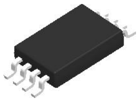
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

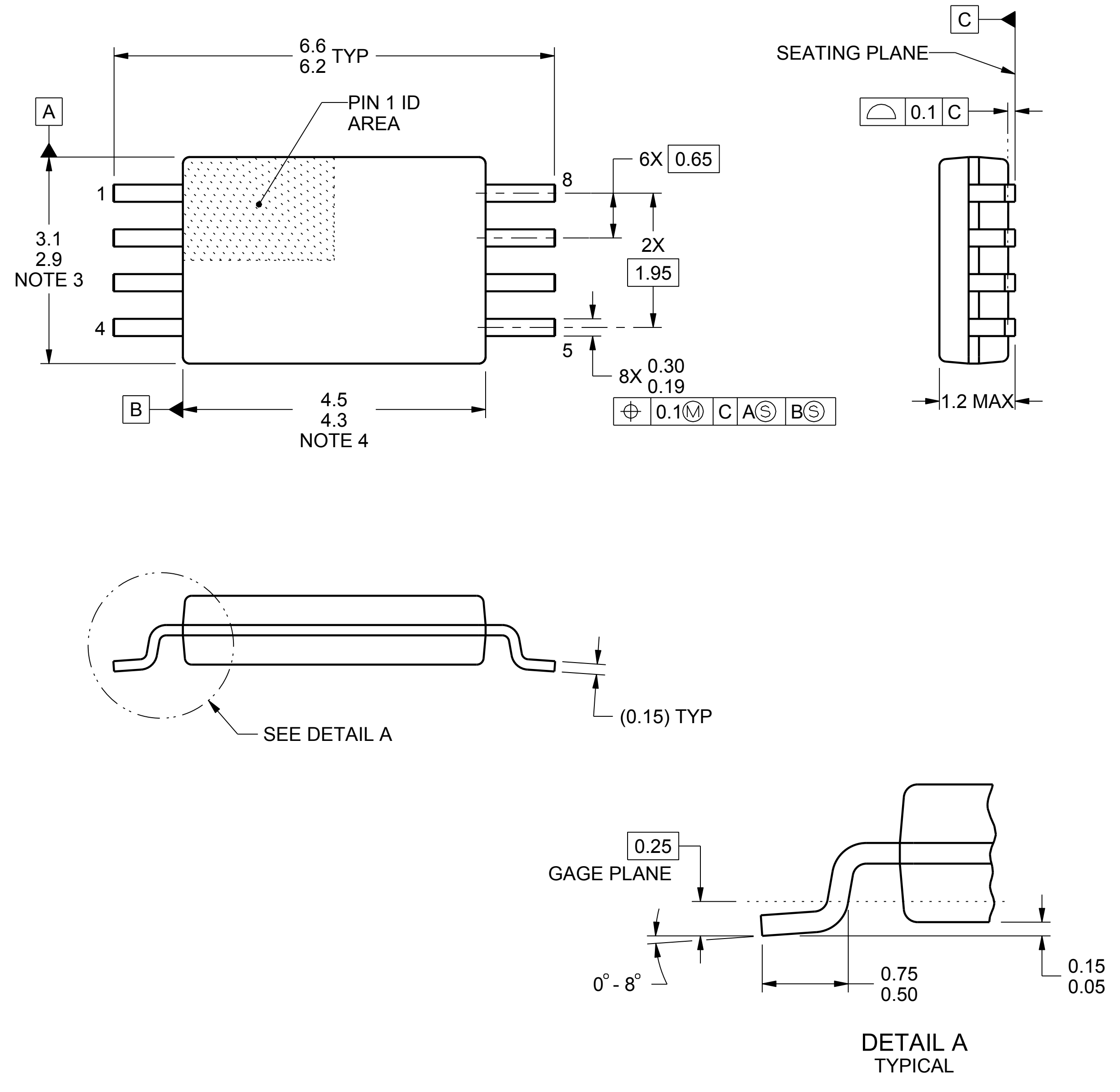
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

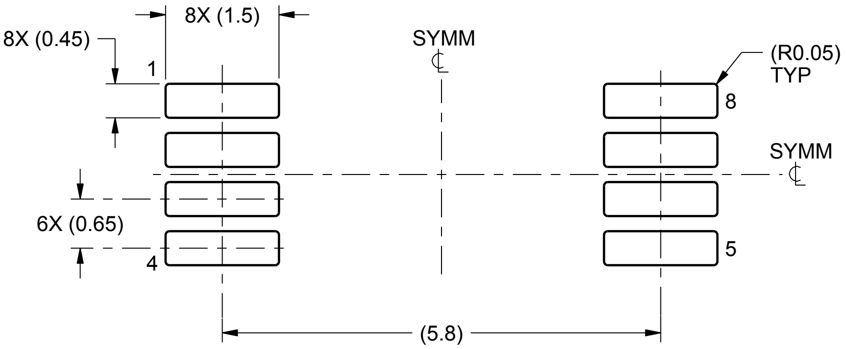
SMALL OUTLINE PACKAGE



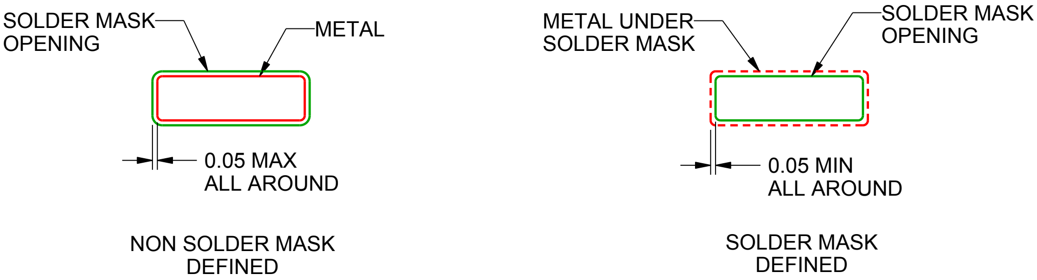
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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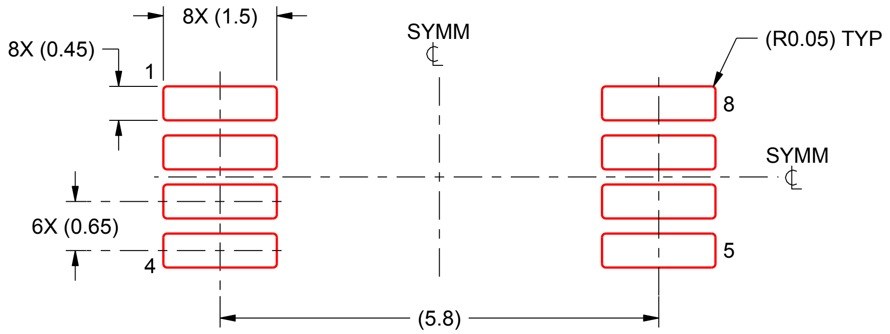
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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