TL07xx Low-Noise, FET-Input Operational Amplifiers

1 Features

- High slew rate: 20V/µs (TL07xH, typ)
- Low offset voltage: 1mV (TL07xH, typ)
- Low offset voltage drift: 2µV/°C
- Low power consumption: 940µA/ch (TL07xH, typ)
- Wide common-mode and differential voltage ranges
  - Common-mode input voltage range includes V_{CC+}
- Low input bias and offset currents
- Low noise:
  - $V_n = 37nV/\sqrt{Hz}$ (typ) at f = 1kHz
- Output short-circuit protection
- Low total harmonic distortion: 0.003% (typ)
- Wide supply voltage:
  - ±2.25V to ±20V, 4.5V to 40V

2 Applications

- Solar energy: string and central inverter
- Motor drives: ac and servo drive control and power-stage modules
- Single-phase online UPS
- Three-phase UPS
- Pro audio mixers
- Battery test equipment

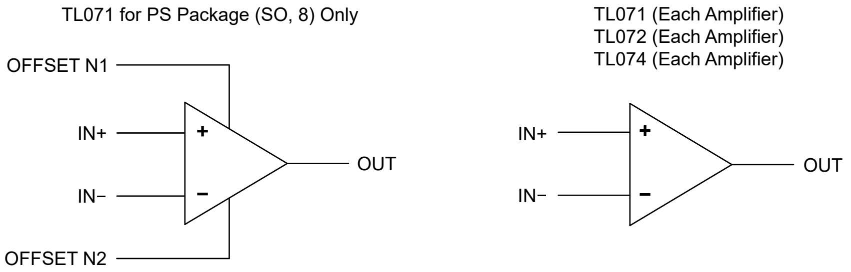
3 Description

The TL071H, TL072H, and TL074H (TL07xH) family of devices are next-generation versions of the industry-standard TL071, TL072, and TL074 (TL07x) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1mV, typical), high slew rate (20V/µs), and common-mode input to the positive supply. High ESD (1.5kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to +125°C range enable the TL07xH devices for use in the most rugged and demanding applications.

Device Information

PART NUMBER(1)	CHANNEL COUNT	PACKAGE
TL071x	Single	D (SOIC, 8)
		DBV (SOT-23, 5)
		DCK (SC70, 5)
		P (PDIP, 8)
		PS (SO, 8)
TL072x	Dual	D (SOIC, 8)
		DDF (SOT-23-THIN, 8)
		P (PDIP, 8)
		PS (SO, 8)
		PW (TSSOP, 8)
TL072M(2)	Dual	FK (LCCC, 20)
		JG (CDIP, 8)
		U (CFP, 10)
TL074x	Quad	D (SOIC, 14)
		DB (SSOP, 14)
		DYY (SOT-23-THIN, 14)
		N (PDIP, 14)
		NS (SOP, 14)
		PW (TSSOP, 14)
TL074M(2)	Quad	FK (LCCC, 20)
		J (CDIP, 14)
		W (CFP, 14)

(1) For more information, see Section 11.
(2) Devices with M suffix have an extended temperature range of –55°C to +125°C.



Logic Symbols

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4 Pin Configuration and Functions

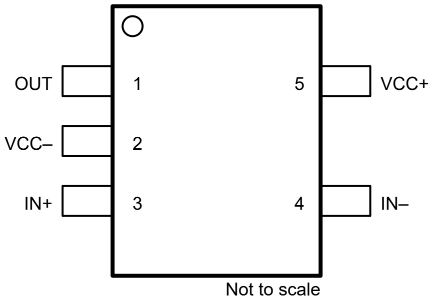


Figure 4-1. TL071H DBV Package, 5-Pin SOT-23 (Top View)

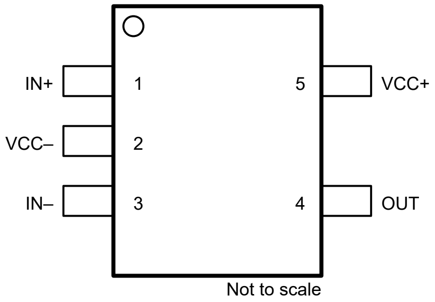


Figure 4-2. TL071H DCK Package, 5-Pin SC70 (Top View)

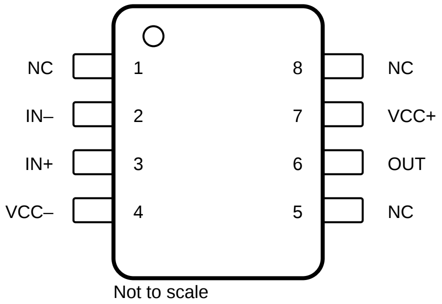
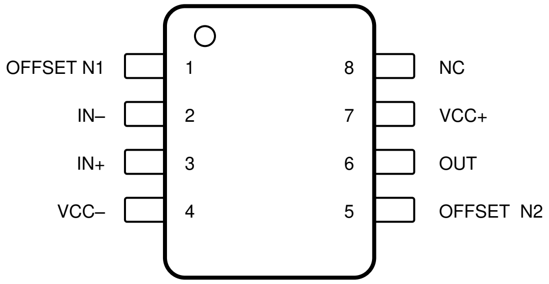


Figure 4-3. TL071x D Package, 8-Pin SOIC and P Package, 8-pin PDIP (Top View)

Table 4-1. Pin Functions: TL071x

PIN					TYPE	DESCRIPTION
NAME	NO.					
	DBV (SOT-23)	DCK (SC70)	D (SOIC)	P (PDIP)		
IN–	4	3	2	2	Input	Inverting input
IN+	3	1	3	3	Input	Noninverting input
NC	—	—	8	8	—	Do not connect
NC	—	—	1	1	—	Do not connect
NC	—	—	5	5	—	Do not connect
OUT	1	4	6	6	Output	Output
VCC–	2	2	4	4	—	Power supply
VCC+	5	5	7	7	—	Power supply

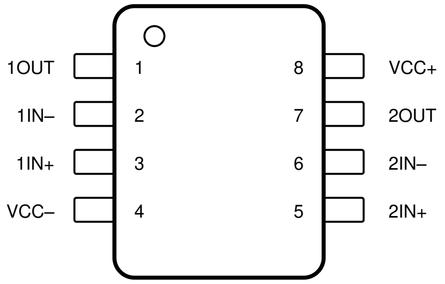


Not to scale

Figure 4-4. TL071C PS Package, 8-Pin SO (Top View)

Table 4-2. Pin Functions: TL071C

PIN		TYPE	DESCRIPTION
NAME	**NO.**		
IN–	2	Input	Inverting input
IN+	3	Input	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	Output	Output
VCC–	4	—	Power supply
VCC+	7	—	Power supply

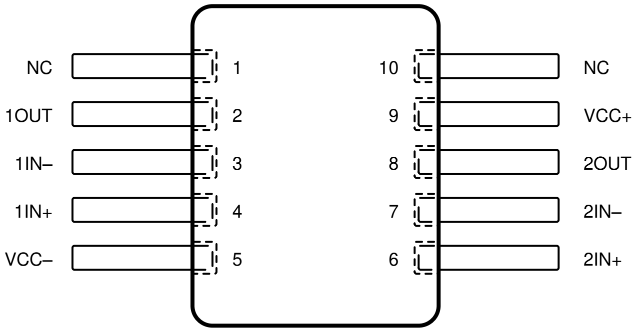


Not to scale

Figure 4-5. TL072x D, DDF, JG, P, PS, and PW Packages, 8-Pin SOIC, SOT-23-THIN, CDIP, PDIP, SO, and TSSOP (Top View)

Table 4-3. Pin Functions: TL072x

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	2	Input	Inverting input
1IN+	3	Input	Noninverting input
1OUT	1	Output	Output
2IN–	6	Input	Inverting input
2IN+	5	Input	Noninverting input
2OUT	7	Output	Output
VCC–	4	—	Power supply
VCC+	8	—	Power supply



Not to scale

Figure 4-6. TL072M U Package, 10-Pin CFP (Top View)

Table 4-4. Pin Functions: TL072M

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	3	Input	Inverting input
1IN+	4	Input	Noninverting input
1OUT	2	Output	Output
2IN–	7	Input	Inverting input
2IN+	6	Input	Noninverting input
2OUT	8	Output	Output
NC	1, 10	—	Do not connect
VCC–	5	—	Power supply
VCC+	9	—	Power supply

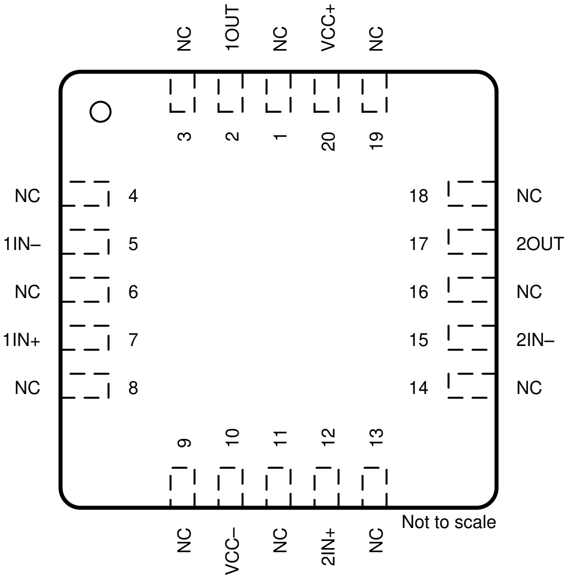


Figure 4-7. TL072M FK Package, 20-Pin LCCC (Top View)

Table 4-5. Pin Functions: TL072M

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	5	Input	Inverting input
1IN+	7	Input	Noninverting input
1OUT	2	Output	Output
2IN–	15	Input	Inverting input
2IN+	12	Input	Noninverting input
2OUT	17	Output	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC–	10	—	Power supply
VCC+	20	—	Power supply

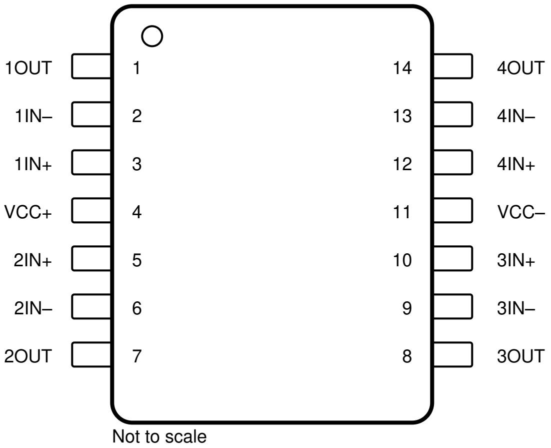


Figure 4-8. TL074x D, DYY, J, N, NS, PW and W Packages, 14-Pin SOIC, SOT-23-THIN, CDIP, PDIP, SOP, TSSOP, and CFP (Top View)

Table 4-6. Pin Functions: TL074x

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	2	Input	Inverting input
1IN+	3	Input	Noninverting input
1OUT	1	Output	Output
2IN–	6	Input	Inverting input
2IN+	5	Input	Noninverting input
2OUT	7	Output	Output
3IN–	9	Input	Inverting input
3IN+	10	Input	Noninverting input
3OUT	8	Output	Output
4IN–	13	Input	Inverting input
4IN+	12	Input	Noninverting input
4OUT	14	Output	Output
VCC–	11	—	Power supply
VCC+	4	—	Power supply

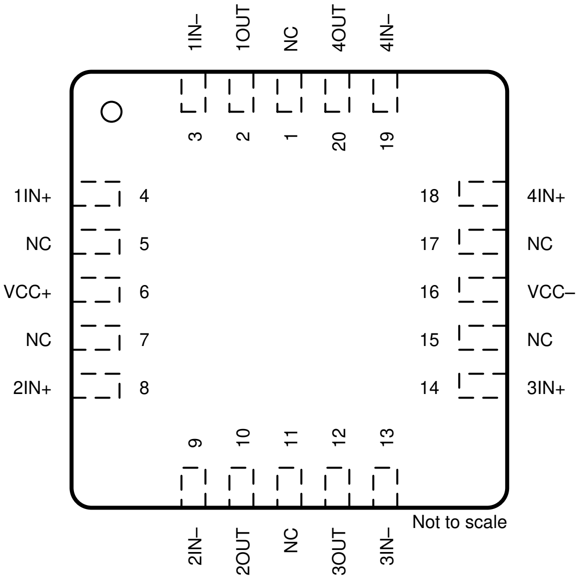


Figure 4-9. TL074M FK Package, 20-Pin LCCC
(Top View)

Table 4-7. Pin Functions: TL074M

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	3	Input	Inverting input
1IN+	4	Input	Noninverting input
1OUT	2	Output	Output
2IN–	9	Input	Inverting input
2IN+	8	Input	Noninverting input
2OUT	10	Output	Output
3IN–	13	Input	Inverting input
3IN+	14	Input	Noninverting input
3OUT	12	Output	Output
4IN–	19	Input	Inverting input
4IN+	18	Input	Noninverting input
4OUT	20	Output	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC–	16	—	Power supply
VCC+	6	—	Power supply

5 Specifications

Note

The TLV07xx series has transitioned new die fabrication into a modern process.
This new die is available with an H suffix.
A die with a different suffix is either older or newer; see also Section 9.1.1.

Section 5.7 and Section 5.10 describe the performance of the new die.

Section 5.8, Section 5.9, and Section 5.11 describe the performance of the old die.

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		All NS and PS packages; All TL07xM devices	–0.3	36	V
		All other devices	0	42	
Signal input pins	Common-mode voltage(2)	All NS and PS packages; All TL07xM devices	$(V_{CC-}) - 0.3$	$(V_{CC-}) + 36$	V
		All other devices	$(V_{CC-}) - 0.5$	$(V_{CC+}) + 0.5$	
	Differential voltage(2)	All NS and PS packages; All TL07xM devices(3)	$(V_{CC-}) - 0.3$	$(V_{CC-}) + 36$	V
		All other devices		$V_S + 0.2$	
	Current(2)	All NS and PS packages; All TL07xM devices		50	mA
		All other devices	–10	10	
Output short-circuit(4)			Continuous		
Operating ambient temperature, T_A			–55	150	°C
Junction temperature, T_J				150	°C
Case temperature for 60 seconds - FK package				260	°C
Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds				300	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to both power-supply rails on all new die. Current limit input signals that swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Differential voltage only limited by input voltage.
(4) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage, $(V_{CC+}) – (V_{CC–})$	All NS and PS packages; All TL07xM devices(1)	10	30	V
		All other devices	4.5	40	
V_I	Input voltage	All NS and PS packages; All TL07xM devices	$(V_{CC–}) + 2$	$(V_{CC+}) + 0.1$	V
		All other devices	$(V_{CC–}) + 4$	$(V_{CC+}) + 0.1$	
T_A	Specified temperature(2)	TL07xM	–55	125	°C
		TL07xH	–40	125	
		TL07xI	–40	85	
		TL07xC	0	70	

(1) V_{CC+} and $V_{CC–}$ are not required to be of equal magnitude, provided that the total V_S $((V_{CC+}) – (V_{CC–}))$ is between 10 V and 30 V.
(2) See also Section 9.1.1.

5.4 Thermal Information for Single Channel

THERMAL METRIC(1)		TL071xx					UNIT
		D (SOIC)	DCK (SC70)	DBV (SOT-23)	P (PDIP)	PS (SO)	
		8 PINS	5 PINS	5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.8	217.5	212.2	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.6	113.1	111.1	–	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.3	63.8	79.4	–	–	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.8	34.8	51.8	–	–	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	101.5	63.5	79.0	–	–	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information for Dual Channel

THERMAL METRIC(1)		TL072xx								UNIT
		D (SOIC)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SO)	PW (TSSOP)	U (CFP)	
		8 PINS	8 PINS	20 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.8	181.5	–	–	85	95	200.3	169.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.2	112.5	5.61	15.05	–	–	89.4	62.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.4	98.2	–	–	–	–	131.0	176.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	36.8	17.2	–	–	–	–	22.2	48.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90.6	97.6	–	–	–	–	129.3	144.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	N/A	5.4	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Thermal Information for Quad Channel

THERMAL METRIC(1)		**TL074xx**								**UNIT**
		D (SOIC)	**DYY (SOT-23)**	**FK (TSSOP)**	**J (TSSOP)**	**N (TSSOP)**	**NS (TSSOP)**	**PW (TSSOP)**	**W (TSSOP)**	
		14 PINS	**14 PINS**	**20 PINS**	**14 PINS**	**14 PINS**	**14 PINS**	**14 PINS**	**14 PINS**	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.2	153.2	–	–	80	76	–	128.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	88.7	5.61	14.5	–	–	14.5	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.2	65.4	–	–	–	–	–	127.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.8	9.5	–	–	–	–	–	29	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.8	65.0	–	–	–	–	–	106.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	–	–	–	–	0.5	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.7 Electrical Characteristics for TL07xH

at $V_S = (V_{CC+}) - (V_{CC-})$ = 4.5 V to 40 V (±2.25 V to ±20 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, $V_{CM} = V_S$ / 2, and $V_{OUT} = V_S$ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±4	mV
			T_A = –40°C to +125°C			±5	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to +125°C		±2		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 5 V to 40 V, $V_{CM} = V_S$ / 2	T_A = –40°C to +125°C		±1	±10	µV/V
	Channel separation	f = 0 Hz			10		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±120	pA
			DCK and DBV packages		±1	±300	pA
			T_A = –40°C to +125°C(1)			±5	nA
I_{OS}	Input offset current				±0.5	±120	pA
			DCK and DBV packages		±0.5	±250	pA
			T_A = –40°C to +125°C(1)			±5	nA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			9.2		μV_{PP}
					1.4		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			37		nV/√Hz
		f = 10 kHz			21		
i_N	Input current noise	f = 1 kHz			80		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage			$(V_{CC-}) + 1.5$		(V_{CC+})	V
CMRR	Common-mode rejection ratio	V_S = 40 V, (V_{CC-}) + 2.5 V < $V_{CM} < (V_{CC+})$ – 1.5 V		100	105		dB
			T_A = –40°C to +125°C	95			dB
		V_S = 40 V, (V_{CC-}) + 2.5 V < $V_{CM} < (V_{CC+})$		90	105		dB
			T_A = –40°C to +125°C	80			dB
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 2		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S$ / 2, (V_{CC-}) + 0.3 V < $V_O < (V_{CC+})$ – 0.3 V	T_A = –40°C to +125°C	118	125		dB
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S$ / 2, R_L = 2 kΩ, (V_{CC-}) + 1.2 V < $V_O < (V_{CC+})$ – 1.2 V	T_A = –40°C to +125°C	115	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.25		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			20		V/µs
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, C_L = 20 pF			0.63		µs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, C_L = 20 pF			0.56		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, C_L = 20 pF			0.91		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, C_L = 20 pF			0.48		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20 pF			56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 6 V_{RMS}, G = +1, f = 1 kHz			0.00012		%
EMIRR	EMI rejection ratio	f = 1 GHz			53		dB

5.7 Electrical Characteristics for TL07xH (continued)

at $V_S = (V_{CC+}) – (V_{CC–})$ = 4.5 V to 40 V (±2.25 V to ±20 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, $V_{CM} = V_S$ / 2, and $V_{OUT} = V_S$ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail	Positive rail headroom	V_S = 40 V, R_L = 10 kΩ		115	210	mV
			V_S = 40 V, R_L = 2 kΩ		520	965	
		Negative rail headroom	V_S = 40 V, R_L = 10 kΩ		105	215	
			V_S = 40 V, R_L = 2 kΩ		500	1030	
I_{SC}	Short-circuit current				±26		mA
C_{LOAD}	Capacitive load drive				300		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			125		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			937.5	1125	µA
		I_O = 0 A, (TL071H)			960	1156	
		I_O = 0 A	T_A = –40°C to +125°C			1130	
		I_O = 0 A, (TL072H)				1143	
		I_O = 0 A, (TL071H)				1160	
	Turn-on time	At T_A = 25°C, V_S = 40 V, V_S ramp rate > 0.3 V/µs			60		µs

---

(1) Maximum I_B and I_{OS} data are specified based on characterization results.

5.8 Electrical Characteristics (DC) for TL07xC, TL07xAC, TL07xBC, TL07xI, TL07xM

at $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15$ V and $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1] [2]			MIN	TYP	MAX	UNIT
DC								
V_{OS}	Input offset voltage	$V_O = 0$ V $R_S = 50\ \Omega$	TL07xC			3	10	mV
				T_A = Full range			13	
			TL07xAC			3	6	
				T_A = Full range			7.5	
			TL07xBC			2	3	
				T_A = Full range			5	
			TL07xI			3	6	
				T_A = Full range			8	
			TL071M, TL072M			3	6	
				T_A = Full range			9	
			TL074M			3	9	
				T_A = Full range			15	
dV_{OS}/dT	Input offset voltage drift	$V_O = 0$ V, $R_S = 50\ \Omega$	T_A = Full range			±18		µV/°C
I_{OS}	Input offset current	$V_O = 0$ V	TL07xC			5	100	pA
				T_A = Full range			10	nA
			TL07xAC, TL07xBC, TL07xI			5	100	pA
				T_A = Full range			2	nA
			TL07xM			5	100	pA
				T_A = Full range			20	nA
I_B	Input bias current	$V_O = 0$ V	TL07xC, TL07xAC, TL07xBC, TL07xI			65	200	pA
				T_A = Full range			7	nA
			TL071M, TL072M			65	200	pA
				T_A = Full range			50	nA
			TL074M			65	200	pA
				T_A = Full range			20	nA
V_{CM}	Common-mode voltage				±11	–12 to 15		V
VOM	Maximum peak output voltage swing	$R_L = 10\ k\Omega$			±12	±13.5		V
		$R_L \geq 10\ k\Omega$	T_A = Full range		±12			
		$R_L \geq 2\ k\Omega$			±10			
A_{OL}	Open-loop voltage gain	$V_O = 0$ V	TL07xC		25	200		V/mV
				T_A = Full range	15			
			TL07xAC, TL07xBC, TL07xI		50	200		
				T_A = Full range	25			
			TL07xM		35	200		
				T_A = Full range	15			
GBW	Gain-bandwidth product	All NS and PS packages; All TL07xM devices				3		MHz
		All other devices				5.25		
R_{ID}	Common-mode input resistance					1		TΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$ $V_O = 0$ V $R_S = 50\ \Omega$	TL07xC		70	100		dB
			TL07xAC, TL07xBC, TL07xI		75	100		
			TL07xM		80	86		
PSRR	Input offset voltage versus power supply	$V_S = \pm 9$ V to ± 18 V $V_O = 0$ V $R_S = 50\ \Omega$	TL07xC		70	100		dB
			TL07xAC, TL07xBC, TL07xI		80	100		
			TL07xM		80	86		

5.8 Electrical Characteristics (DC) for TL07xC, TL07xAC, TL07xBC, TL07xI, TL07xM (continued)

at $V_S = (V_{CC+}) – (V_{CC–})$ = ±15 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1) (2)	MIN	TYP	MAX	UNIT
I_Q	Quiescent current per amplifier	V_O = 0 V, no load		1.4	2.5	mA
	Channel separation	f = 0 Hz		1		µV/V

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is T_A = 0°C to 70°C for the TL07xC, TL07xAC, and TL07xBC; T_A = –40°C to +85°C for the TL07xI; and T_A = –55°C to +125°C for the TL07xM.

5.9 Electrical Characteristics (AC) for TL07xC, TL07xAC, TL07xBC, TL07xI, TL07xM

at $V_S = (V_{CC+}) – (V_{CC–})$ = ±15 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC							
SR	Slew rate	V_I = 10 V, C_L = 100 pF, R_L = 2 kΩ	TL07xM	5	20		V/µs
			TL07xC, TL07xAC, TL07xBC, TL07xI	8	20		V/µs
t_S	Settling time	V_I = 20 V, C_L = 100 pF, R_L = 2 kΩ			0.1		µs
					20%		
e_N	Input voltage noise density	All PS and NS packages, all TL07xM devices	R_S = 20 Ω, f = 1 kHz		18		nV/√Hz
		All other devices	f = 1 kHz		37		nV/√Hz
			f = 10 kHz		21		
E_N	Input voltage noise	All PS and NS packages, all TL07xM devices	R_S = 20 Ω, f = 10 Hz to 10 kHz		4		$µV_{RMS}$
		All other devices	f = 0.1 Hz to 10 Hz		1.4		$µV_{RMS}$
i_N	Input current noise	R_S = 20 Ω, f = 1 kHz			10		fA/√Hz
	Phase margin	TL07xC, TL07xAC, TL07xBC, TL07xI	G = +1, R_L = 10kΩ, C_L = 20 pF		56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns
THD+N	Total harmonic distortion + noise	All PS and NS packages, all TL07xM devices	V_O = 6 V_{RMS}, R_L ≥ 2 kΩ, f = 1 kHz, G = +1, R_S ≤ 1 kΩ		0.003		%
		All other devices	V_S = 40 V, V_O = 6 V_{RMS}, G = +1, f = 1 kHz		0.00012		%
EMIRR	EMI rejection ratio	TL07xC, TL07xAC, TL07xBC, TL07xI	f = 1 GHz		53		dB
Z_O	Open-loop output impedance	TL07xC, TL07xAC, TL07xBC, TL07xI	f = 1 MHz, I_O = 0 A		125		Ω

5.10 Typical Characteristics: TL07xH

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

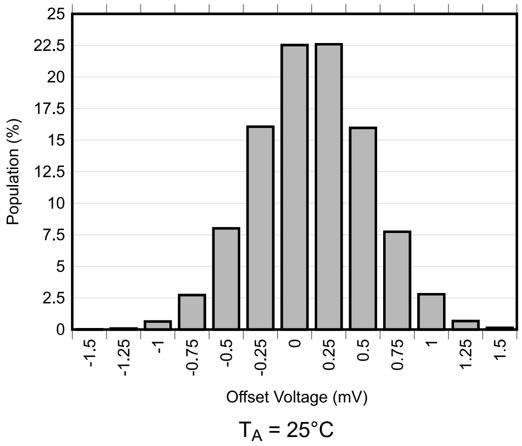


Figure 5-1. Offset Voltage Production Distribution

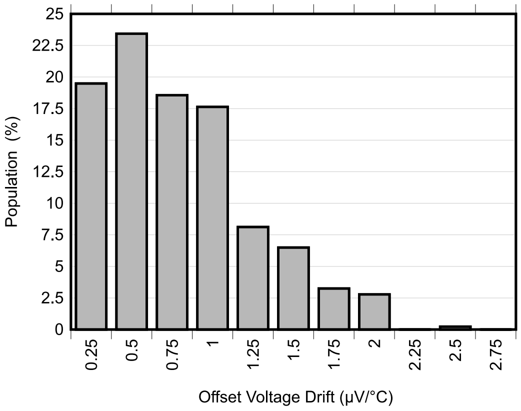


Figure 5-2. Offset Voltage Drift Distribution

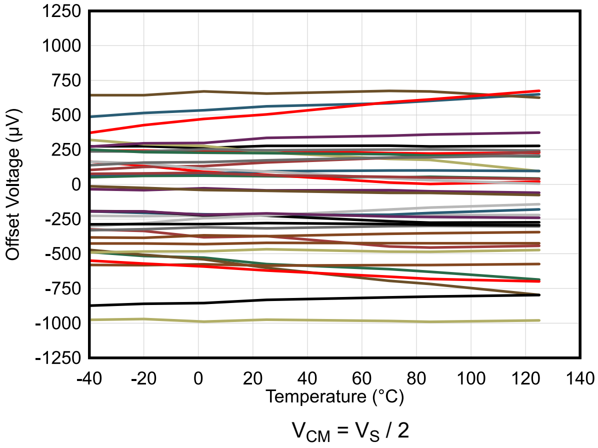


Figure 5-3. Offset Voltage vs Temperature

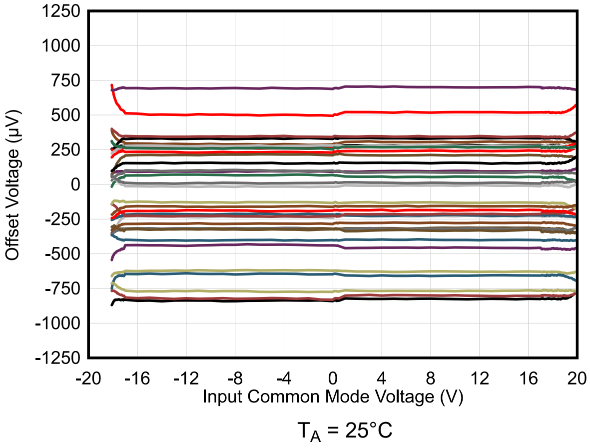


Figure 5-4. Offset Voltage vs Common-Mode Voltage

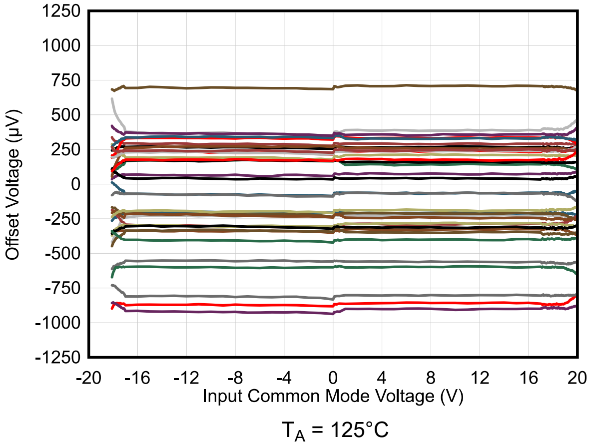


Figure 5-5. Offset Voltage vs Common-Mode Voltage

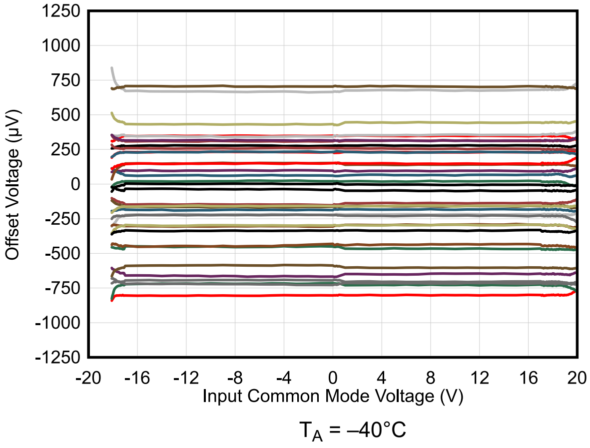


Figure 5-6. Offset Voltage vs Common-Mode Voltage

5.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

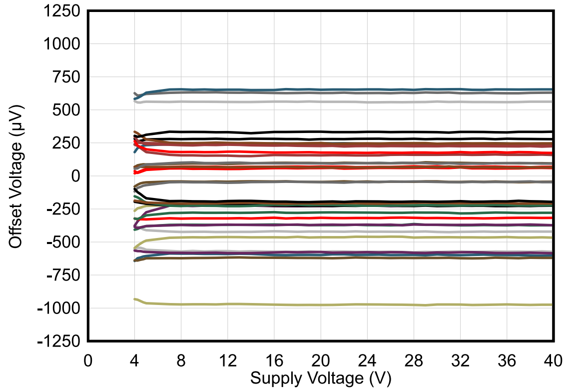


Figure 5-7. Offset Voltage vs Power Supply

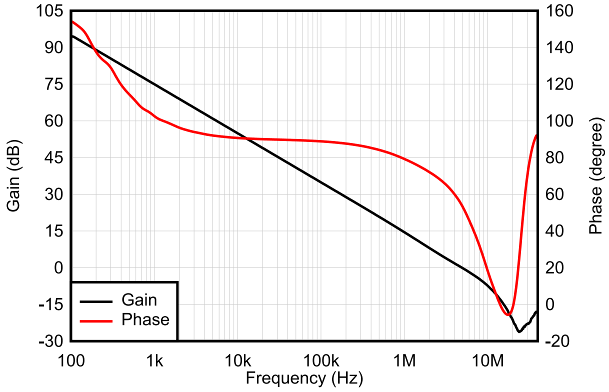


Figure 5-8. Open-Loop Gain and Phase vs Frequency

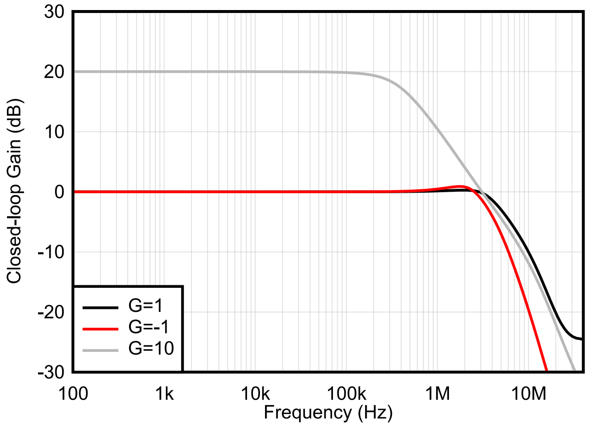


Figure 5-9. Closed-Loop Gain vs Frequency

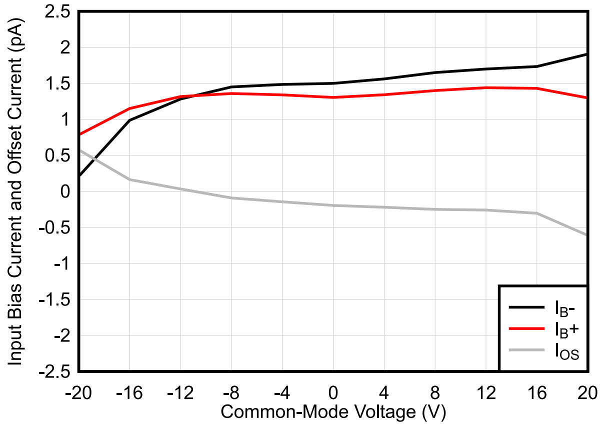


Figure 5-10. Input Bias Current vs Common-Mode Voltage

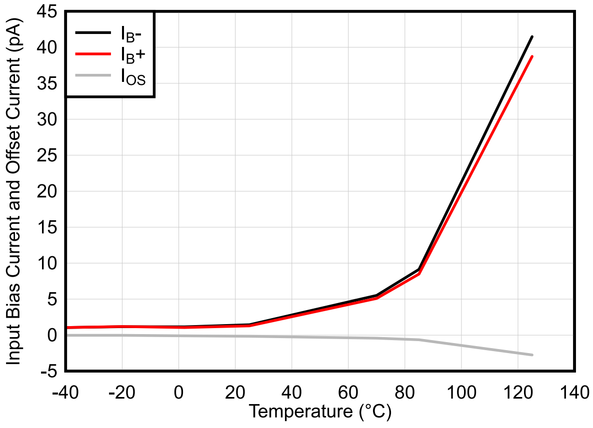


Figure 5-11. Input Bias Current vs Temperature

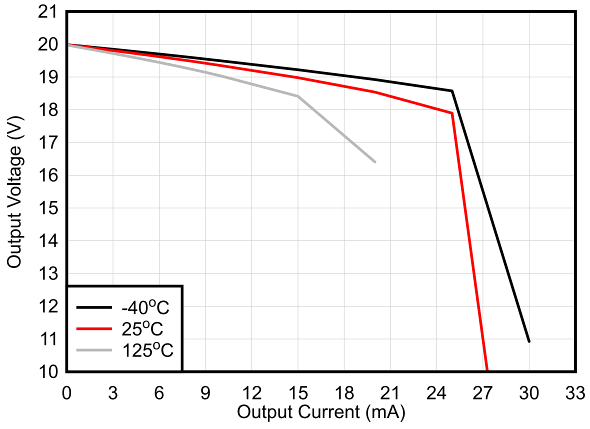


Figure 5-12. Output Voltage Swing vs Output Current (Sourcing)

5.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

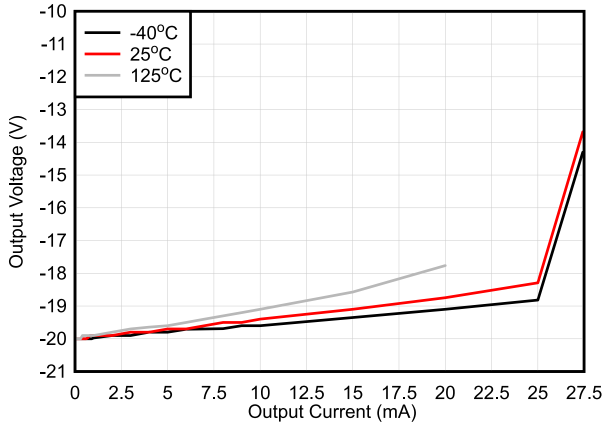


Figure 5-13. Output Voltage Swing vs Output Current (Sinking)

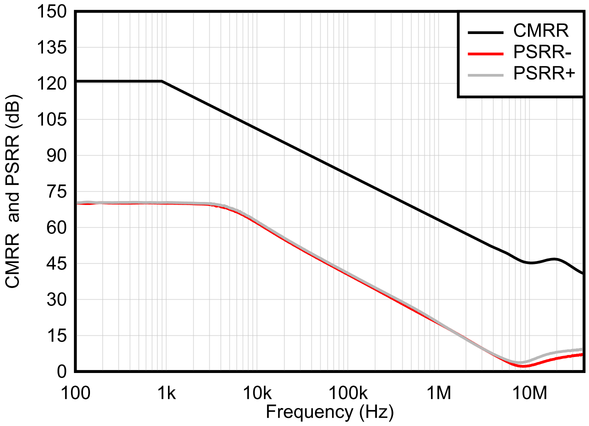
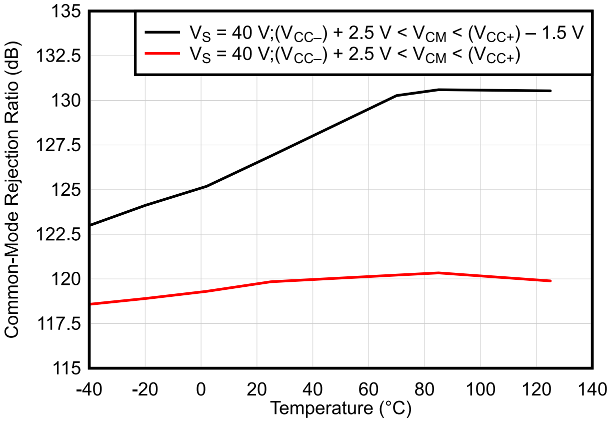
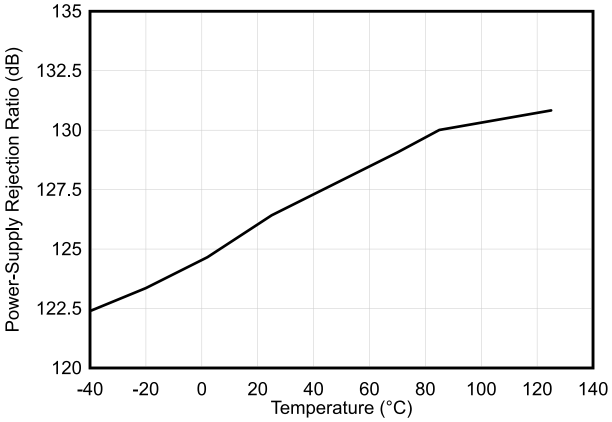


Figure 5-14. CMRR and PSRR vs Frequency



f = 0 Hz

Figure 5-15. CMRR vs Temperature (dB)



f = 0 Hz

Figure 5-16. PSRR vs Temperature (dB)

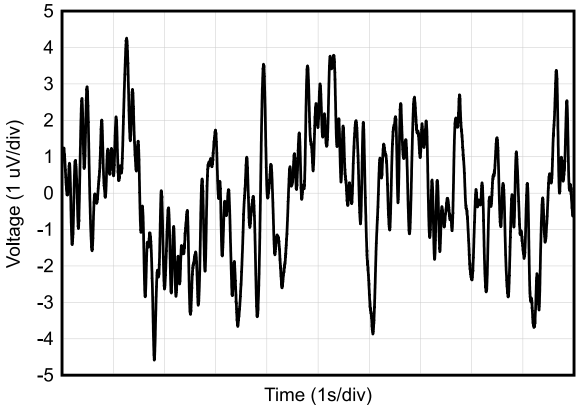


Figure 5-17. 0.1-Hz to 10-Hz Noise

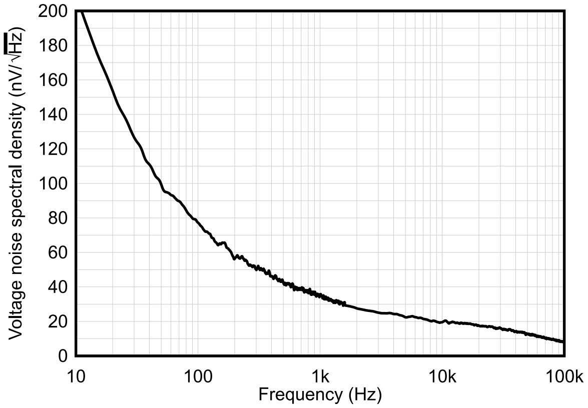
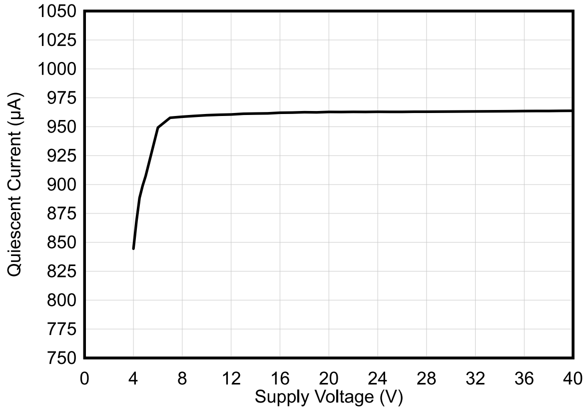


Figure 5-18. Input Voltage Noise Spectral Density vs Frequency

5.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



V_{CM} = V_S / 2

Figure 5-19. Quiescent Current vs Supply Voltage

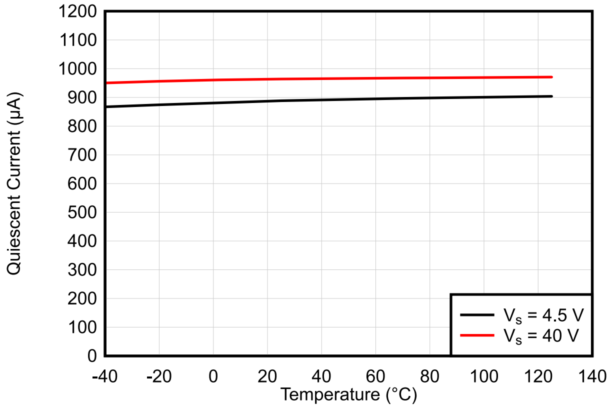


Figure 5-20. Quiescent Current vs Temperature

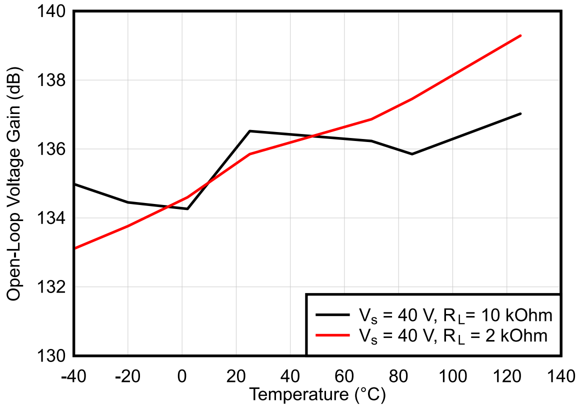


Figure 5-21. Open-Loop Voltage Gain vs Temperature

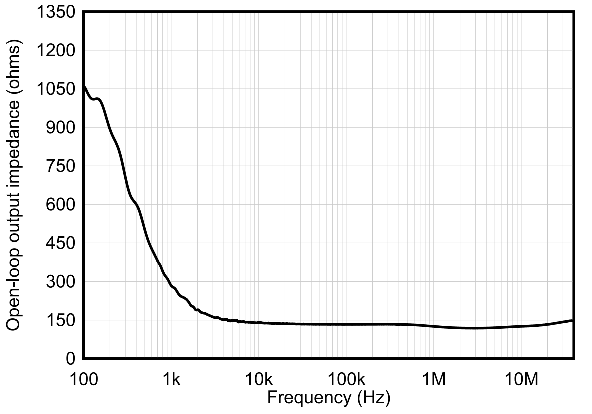
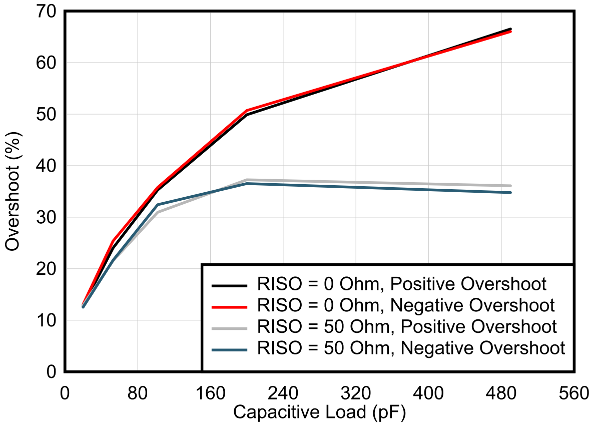
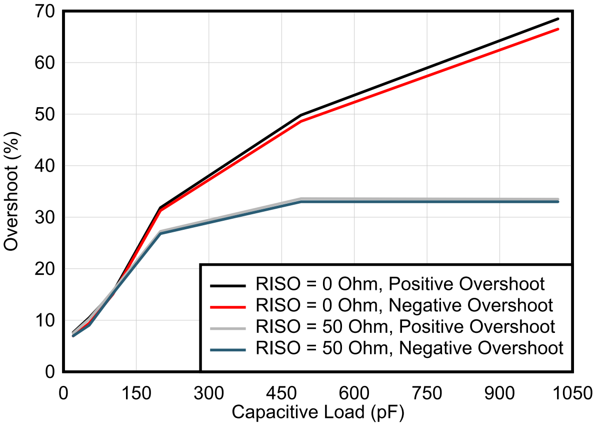


Figure 5-22. Open-Loop Output Impedance vs Frequency



G = –1, 25-mV output step

Figure 5-23. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

Figure 5-24. Small-Signal Overshoot vs Capacitive Load

5.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

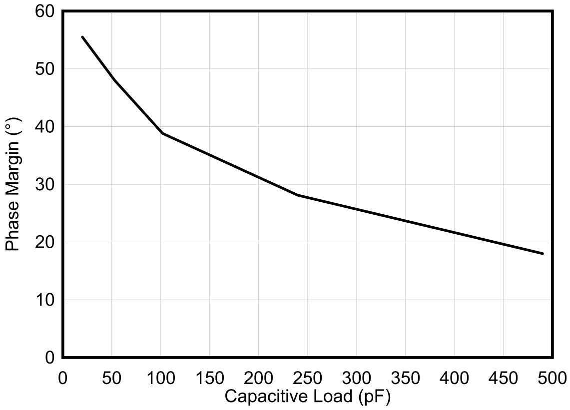
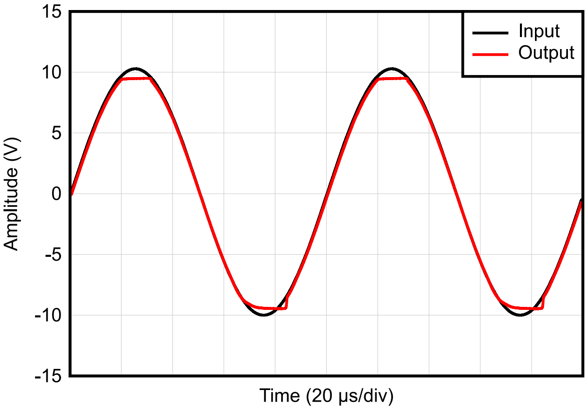
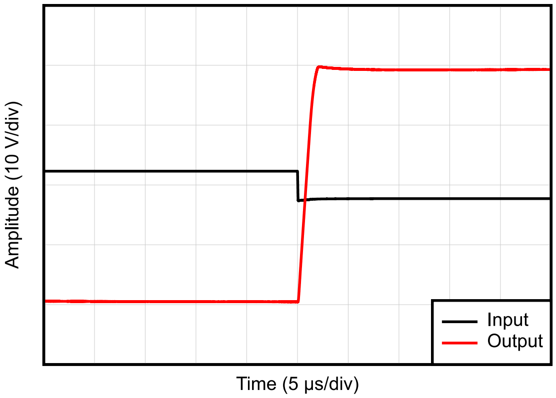


Figure 5-25. Phase Margin vs Capacitive Load



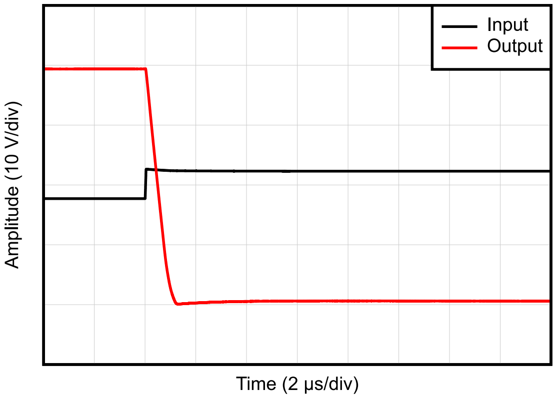
V_S = ±10 V, V_{IN} = V_{OUT}

Figure 5-26. No Phase Reversal



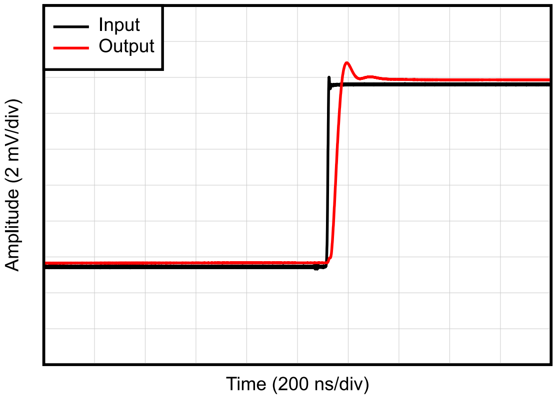
G = –10

Figure 5-27. Positive Overload Recovery



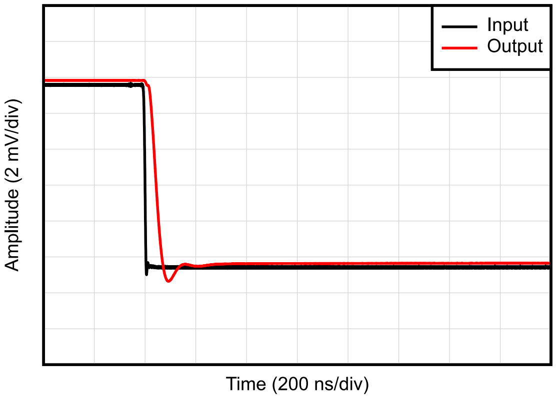
G = –10

Figure 5-28. Negative Overload Recovery



C_L = 20 pF, G = 1, 10-mV step response

Figure 5-29. Small-Signal Step Response, Rising

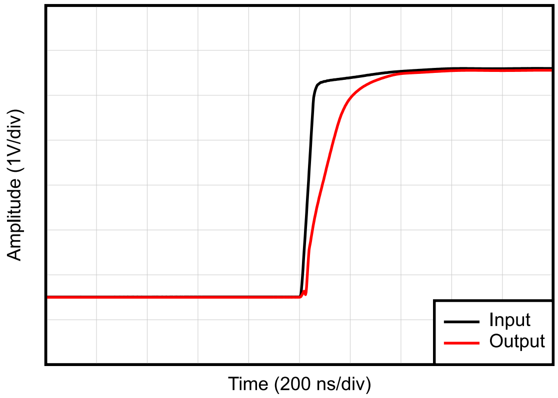


C_L = 20 pF, G = 1, 10-mV step response

Figure 5-30. Small-Signal Step Response, Falling

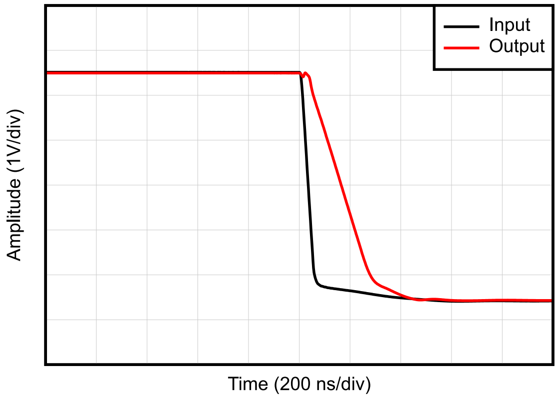
5.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



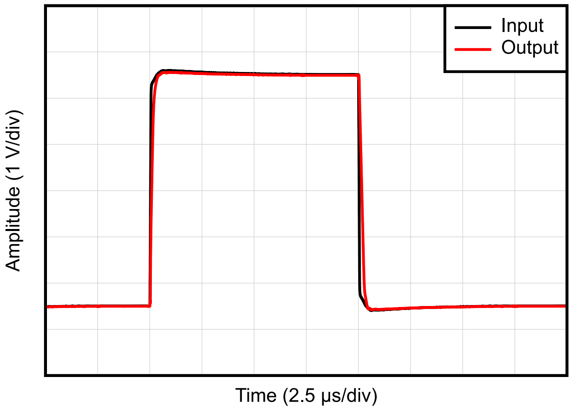
C_L = 20 pF, G = 1

Figure 5-31. Large-Signal Step Response (Rising)



C_L = 20 pF, G = 1

Figure 5-32. Large-Signal Step Response (Falling)



C_L = 20 pF, G = 1

Figure 5-33. Large-Signal Step Response

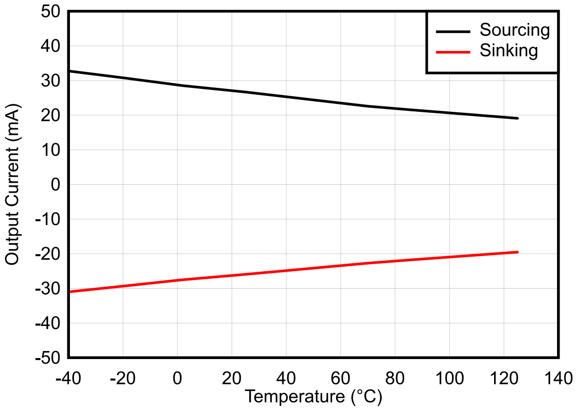


Figure 5-34. Short-Circuit Current vs Temperature

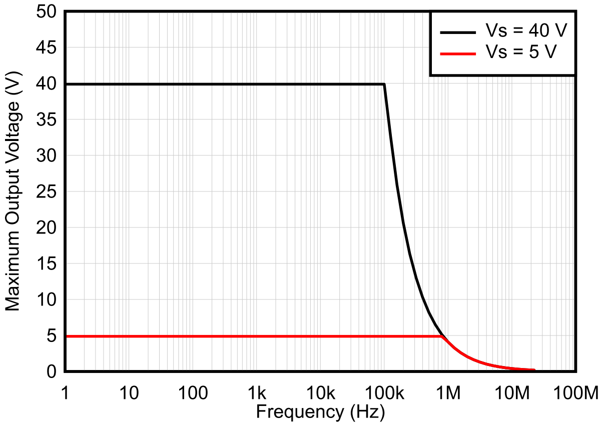


Figure 5-35. Maximum Output Voltage vs Frequency

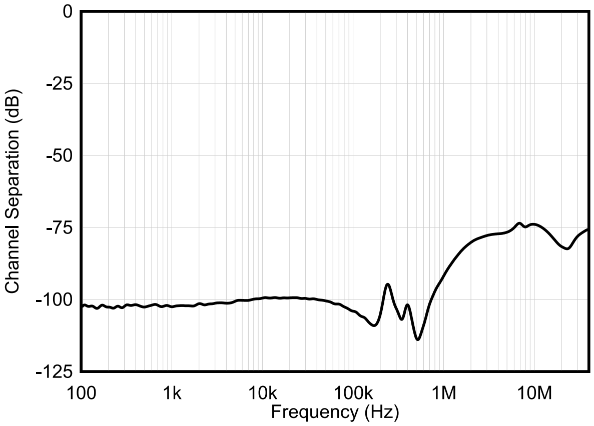


Figure 5-36. Channel Separation vs Frequency

5.10 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

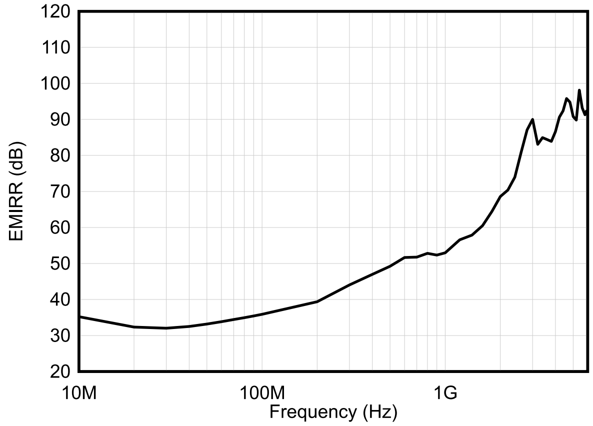


Figure 5-37. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

5.11 Typical Characteristics: All Devices Except TL07xH

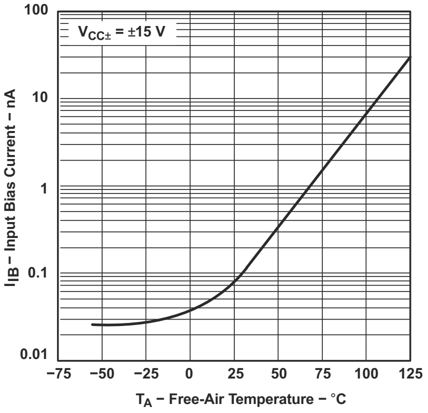


Figure 5-38. Input Bias Current vs Free-Air Temperature

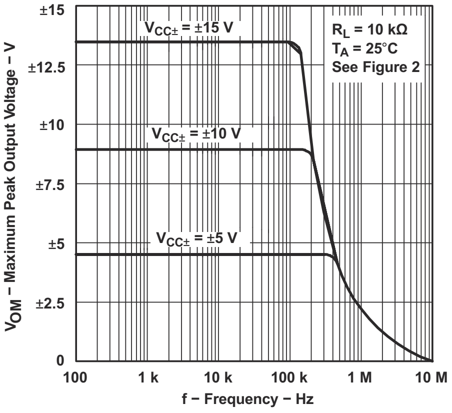


Figure 5-39. Maximum Peak Output Voltage vs Frequency

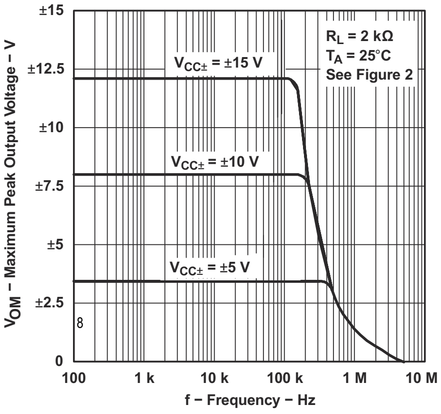


Figure 5-40. Maximum Peak Output Voltage vs Frequency

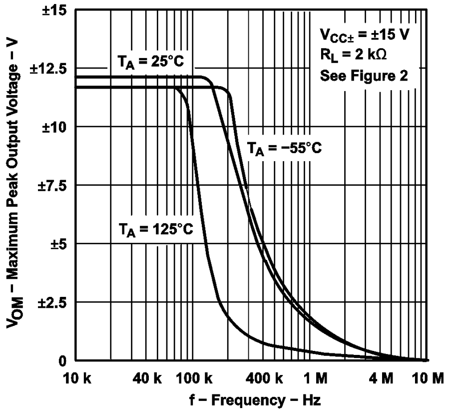


Figure 5-41. Maximum Peak Output Voltage vs Frequency

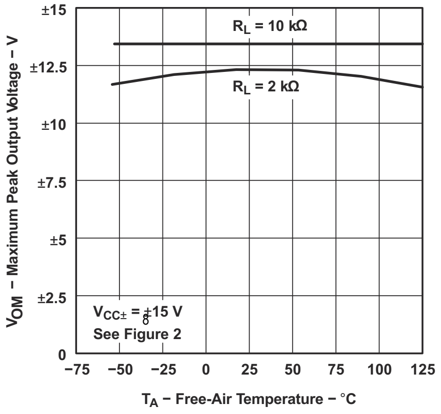


Figure 5-42. Maximum Peak Output Voltage vs Free-Air Temperature

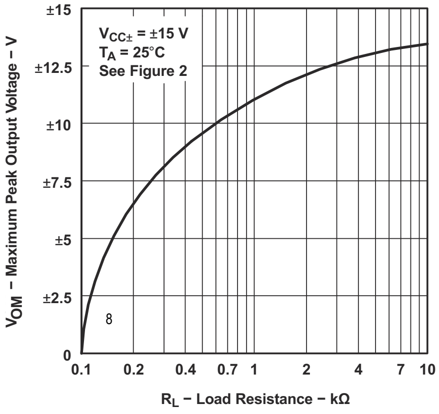


Figure 5-43. Maximum Peak Output Voltage vs Load Resistance

5.11 Typical Characteristics: All Devices Except TL07xH (continued)

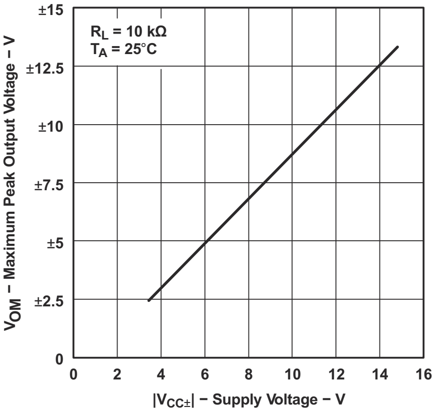


Figure 5-44. Maximum Peak Output Voltage vs Supply Voltage

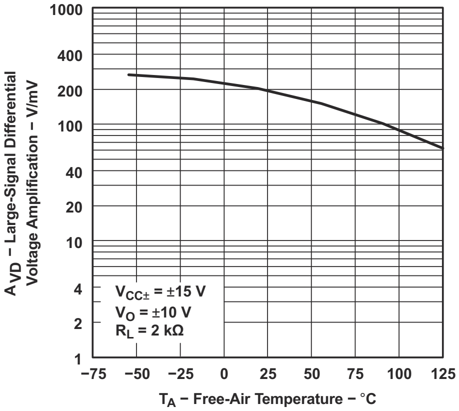


Figure 5-45. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

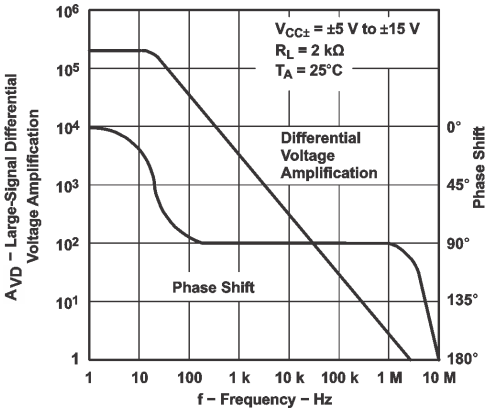


Figure 5-46. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

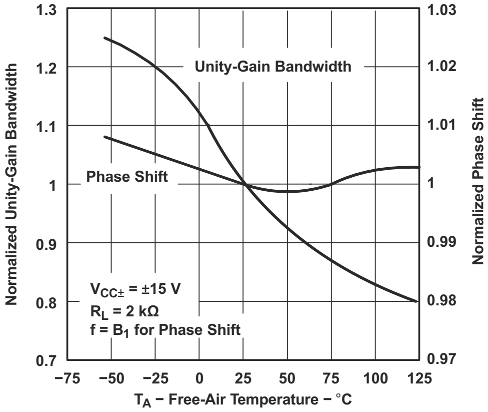


Figure 5-47. Normalized Unity-Gain Bandwidth and Phase Shift vs Free-Air Temperature

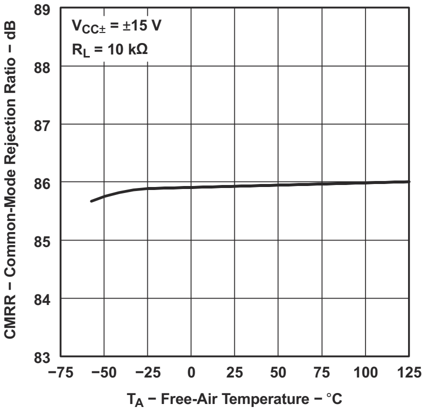


Figure 5-48. Common-Mode Rejection Ratio vs Free-Air Temperature

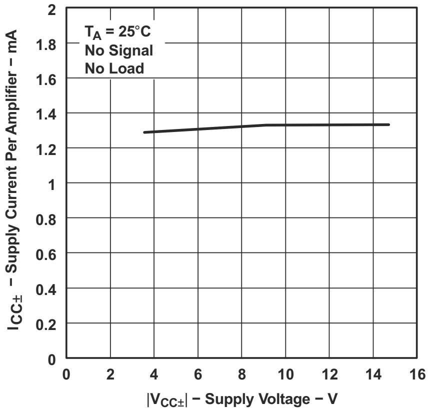


Figure 5-49. Supply Current Per Amplifier vs Supply Voltage

5.11 Typical Characteristics: All Devices Except TL07xH (continued)

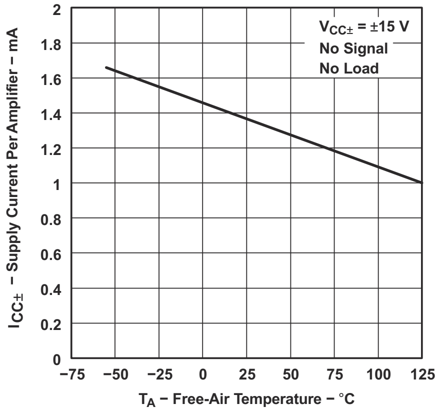


Figure 5-50. Supply Current Per Amplifier vs Free-Air Temperature

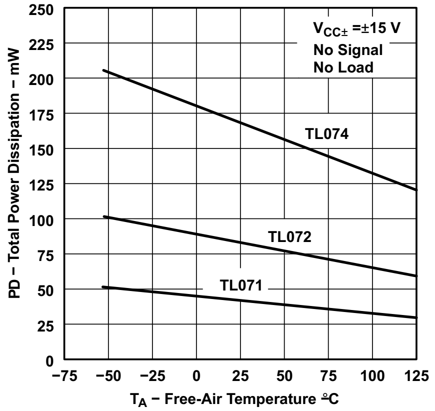


Figure 5-51. Total Power Dissipation vs Free-Air Temperature

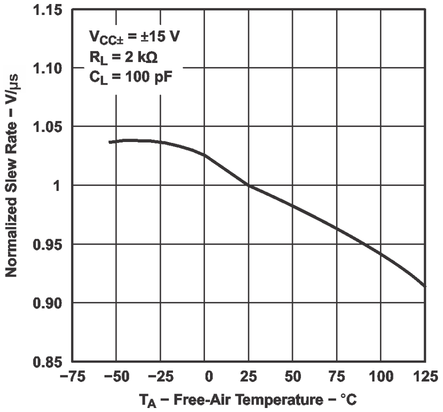


Figure 5-52. Normalized Slew Rate vs Free-Air Temperature

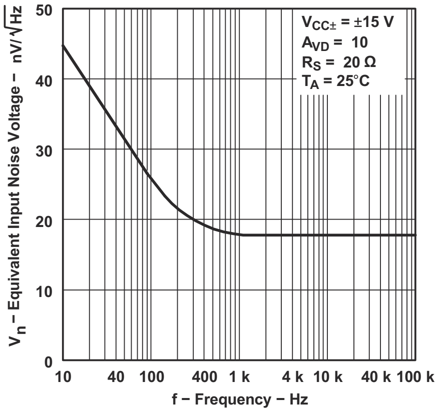


Figure 5-53. Equivalent Input Noise Voltage vs Frequency

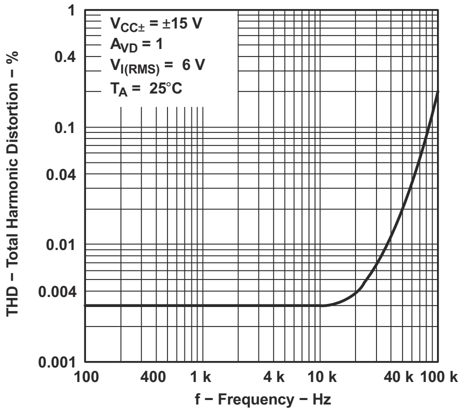


Figure 5-54. Total Harmonic Distortion vs Frequency

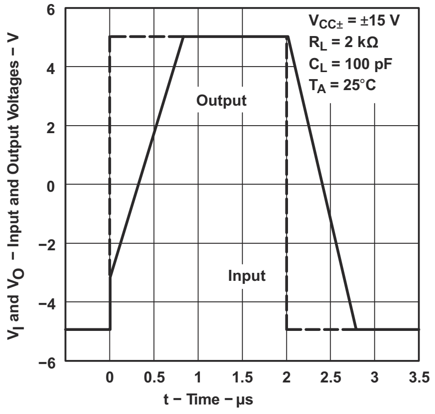


Figure 5-55. Voltage-Follower Large-Signal Pulse Response

5.11 Typical Characteristics: All Devices Except TL07xH (continued)

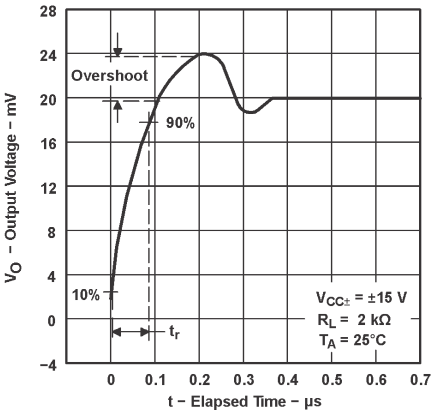


Figure 5-56. Output Voltage vs Elapsed Time

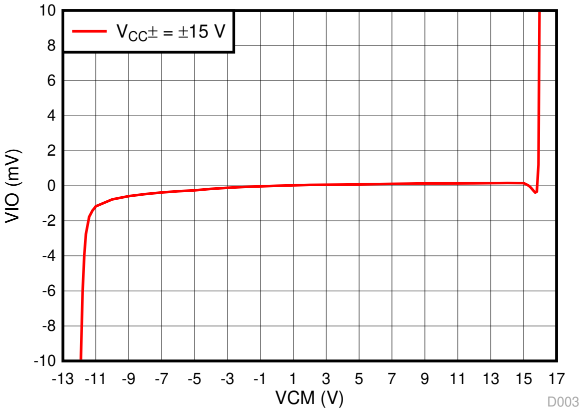


Figure 5-57. V_{IO} vs V_{CM}

6 Parameter Measurement Information

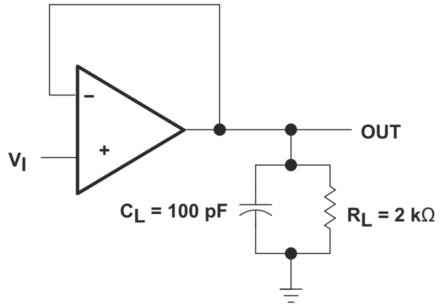


Figure 6-1. Unity-Gain Amplifier

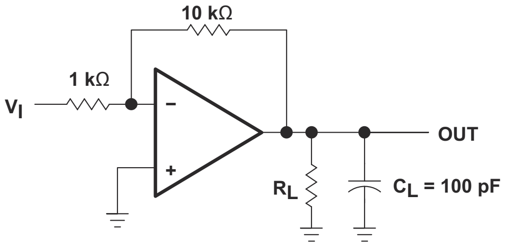


Figure 6-2. Gain-of-10 Inverting Amplifier

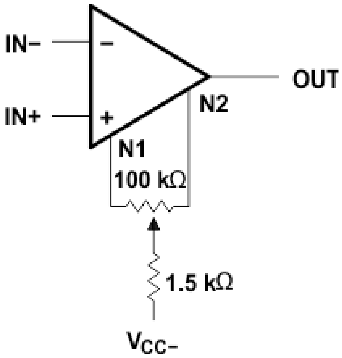


Figure 6-3. Input Offset-Voltage Null Circuit
for PS Package (SO, 8) Only

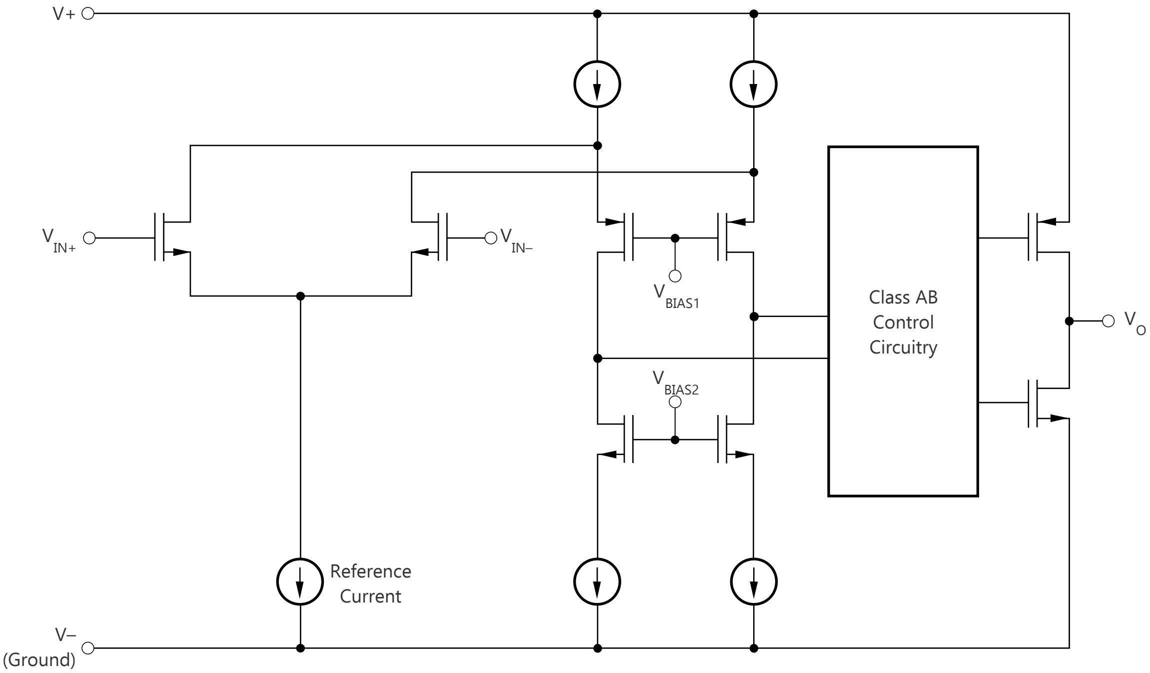
7 Detailed Description

7.1 Overview

The TL07xH (TL071H, TL072H, and TL074H) family of devices are the next-generation versions of the industry-standard TL07x (TL071, TL072, and TL074) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1 mV, typical), high slew rate (20 V/µs, typical), and common-mode input to the positive supply. High ESD (2 kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to 125°C enable the TL07xH devices to be used in the most rugged and demanding applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to +85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

The TL07xH family of devices improve many specifications as compared to the industry-standard TL07x family. Several comparisons of key specifications between these families are included in the following sections to show the advantages of the TL07xH family.

7.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL07x device adds little harmonic distortion when used in audio signal applications.

7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. These devices have a 20-V/µs slew rate.

7.4 Device Functional Modes

These devices are powered on when the supply is connected. These devices can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes the voltage a negative voltage. In the same manner, the amplifier makes negative voltages positive.

8.2 Typical Applications

8.2.1 Inverting Amplifier

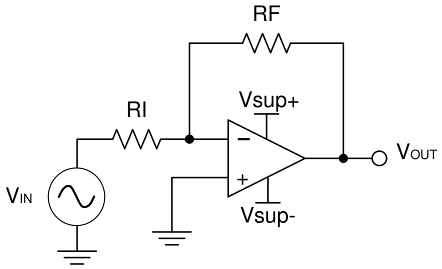


Figure 8-1. Inverting Amplifier

8.2.1.1 Design Requirements

The supply voltage must be selected so the supply voltage is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

8.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

After the desired gain is determined, select a value for RI or RF. Selecting a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamp range. This example uses 10 kΩ for RI, which means 36 kΩ is used for RF. The gain is determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

8.2.1.3 Application Curve

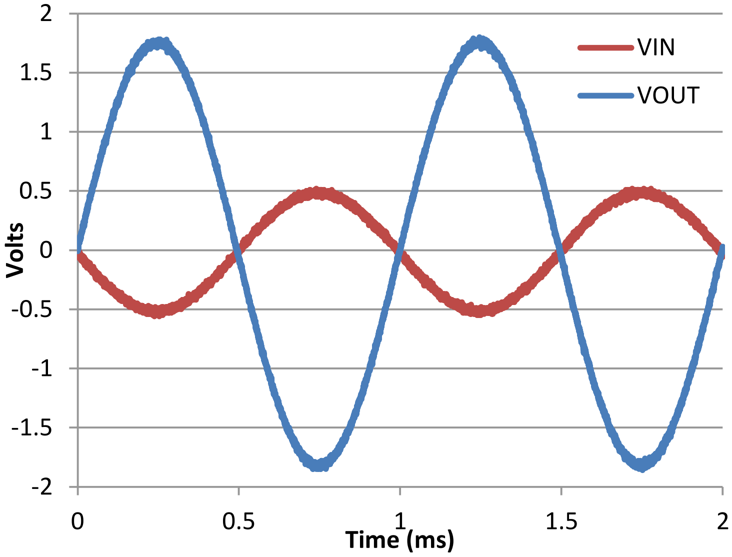


Figure 8-2. Input and Output Voltages of the Inverting Amplifier

8.3 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see Section 5.1).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Section 8.4.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_{CC+} to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If not possible, then better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance; see also Section 8.4.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Example

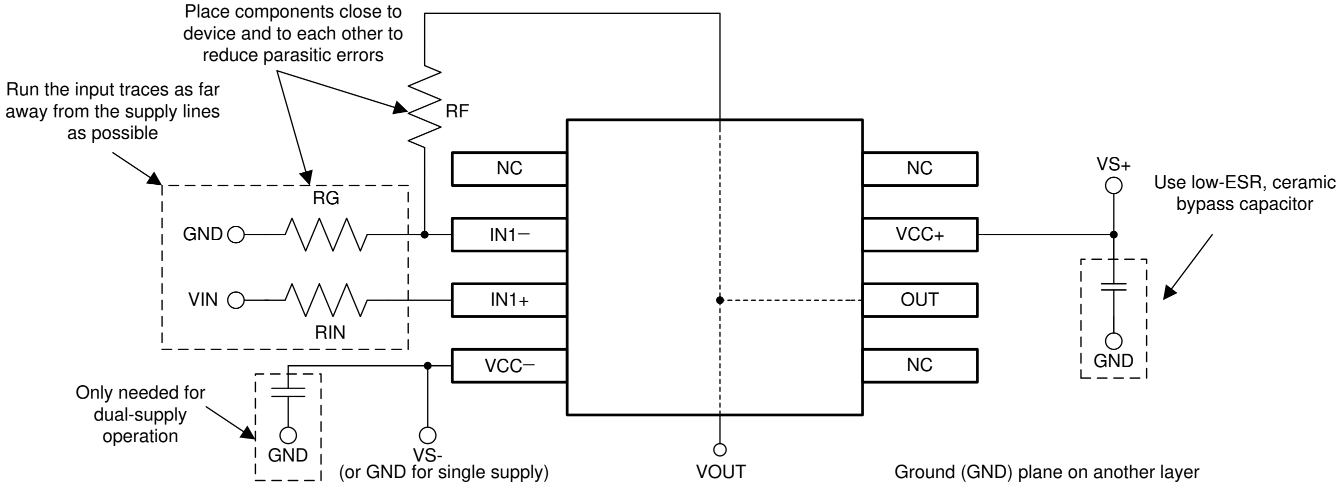


Figure 8-3. Operational Amplifier Board Layout for Noninverting Configuration

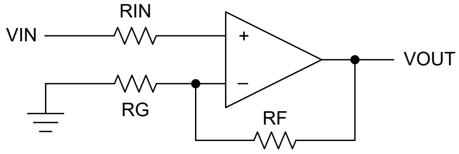


Figure 8-4. Operational Amplifier Schematic for Noninverting Configuration

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Device Nomenclature

PART NUMBER	DEFINITION
TL07*xyzzzzzz*	*x* is the channel count
	If *y* = H, the die is manufactured on the latest flow (CSO: RFB). Section 5.7 and Section 5.10 describe the performance of the new die.
	If *y* ≠ H and *y* ≠ M, the die is manufactured on the legacy flow (CSO: SFAB) or the latest flow (CSO: RFB). Section 5.8, Section 5.9, and Section 5.11 describe the performance of the original die. Section 5.7 and Section 5.10 describe the performance of the new die.
	If *y* = M, the device is specified for the extended temperature range of –55°C to +125°C. The die is manufactured on the legacy flow (CSO:SFAB). The letters and numbers represented by *z* are grade-out and package options described in Section 5.8 and the *Package Option Addendum* at the end of this data sheet.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision V (April 2023) to Revision W (July 2025) **Page**

- Deleted references to trim function from all packages except PS (SO, 8) package..1
- Changed V_n from 18nV/$\sqrt{\text{Hz}}$ to 37nV/$\sqrt{\text{Hz}}$ in *Features* 1
- Updated *Device Information* table to match *Package Option Addendum* 1
- Updated front page image to show which device uses the PS package only.. 1
- Updated *Pin Configuration and Functions* to show that only PS package (PDIP, 8) has trim function...............3

- Added note regarding old and new dies..10
- Deleted Figure 5-19, *THD+N Ratio vs Frequency* and Figure 5-20, *THD+N vs Output Amplitude* 17
- Added "for PS Package (SO, 8) Only" to Figure 7-3 caption...28
- Deleted *Unity Gain Buffer* and *System Examples* sections...30
- Deleted Equation 1 from *Detailed Design Procedure* 30
- Deleted "This ensures the part does not draw too much current." from *Detailed Design Procedure* 30
- Added *Device Nomenclature* table...34

Changes from Revision U (December 2022) to Revision V (April 2023) **Page**

- Updated *Overview*, *Functional Block Diagram*, and *Feature Description* sections 29

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
81023052A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023052A TL072MFKB
8102305HA	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305HA TL072M
8102305PA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305PA TL072M
81023062A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023062A TL074MFKB
8102306CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306CA TL074MJB
8102306DA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306DA TL074MWB
JM38510/11905BPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510 /11905BPA
JM38510/11905BPA.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510 /11905BPA
M38510/11905BPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510 /11905BPA
TL071ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC
TL071ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC
TL071ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071ACP
TL071ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071ACP
TL071BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC
TL071BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC
TL071BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071BCP
TL071BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071BCP
TL071CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C
TL071CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C
TL071CDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL071CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL071CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071CP

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL071CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL071CP
TL071CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TL071CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T071
TL071CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T071
TL071HIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T71V
TL071HIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T71V
TL071HIDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T71V
TL071HIDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T71V
TL071HIDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T71V
TL071HIDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IO
TL071HIDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IO
TL071HIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL071D
TL071HIDR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL071D
TL071IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDR1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDR1G4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I
TL071IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL071IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL071IP
TL071IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL071IP
TL072ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC
TL072ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072ACP
TL072ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072ACP
TL072ACPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TL072ACPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072A
TL072ACPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072A
TL072BCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	072BC
TL072BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL072BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC
TL072BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072BCP
TL072BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072BCP
TL072CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
TL072CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C
TL072CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072CP
TL072CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL072CP
TL072CPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPSRG4	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072
TL072CPWRE4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL072CPWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL072HIDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O72F
TL072HIDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O72F
TL072HIDDFR.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O72F
TL072HIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL072D
TL072HIDR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL072D
TL072HIPWR	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	072HPW
TL072HIPWR.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	072HPW
TL072IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I
TL072IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I
TL072IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL072IP
TL072IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL072IP
TL072IPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	-40 to 85	
TL072MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023052A TL072MFKB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL072MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023052A TL072MFKB
TL072MJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL072MJG
TL072MJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL072MJG
TL072MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305PA TL072M
TL072MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305PA TL072M
TL072MUB	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305HA TL072M
TL072MUB.A	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102305HA TL072M
TL074ACDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC
TL074ACDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC
TL074ACN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074ACN
TL074ACN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074ACN
TL074ACNSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A
TL074ACNSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A
TL074BCD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL074BC
TL074BCDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC
TL074BCN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074BCN
TL074BCN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074BCN
TL074CD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL074C
TL074CDBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CDBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL074CDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C
TL074CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074CN
TL074CN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL074CN
TL074CNSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074
TL074CNSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074
TL074CPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	T074
TL074CPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CPWRE4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074CPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074
TL074HIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID
TL074HIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID
TL074HIDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID
TL074HIDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID
TL074HIDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID
TL074HIDYYR	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T074HDYY
TL074HIDYYR.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T074HDYY
TL074HIDYYR.B	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T074HDYY
TL074HIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074PW
TL074HIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074PW
TL074ID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	TL074I
TL074IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I
TL074IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL074IN

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL074IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL074IN
TL074ING4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL074IN
TL074ING4.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL074IN
TL074MFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL074MFK
TL074MFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL074MFK
TL074MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023062A TL074MFKB
TL074MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	81023062A TL074MFKB
TL074MJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL074MJ
TL074MJ.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL074MJ
TL074MJB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306CA TL074MJB
TL074MJB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306CA TL074MJB
TL074MWB	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306DA TL074MWB
TL074MWB.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102306DA TL074MWB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :

- Catalog : TL072, TL074

- Enhanced Product : TL072-EP, TL072-EP, TL074-EP, TL074-EP

- Military : TL072M, TL074M

NOTE: Qualified Version Definitions:

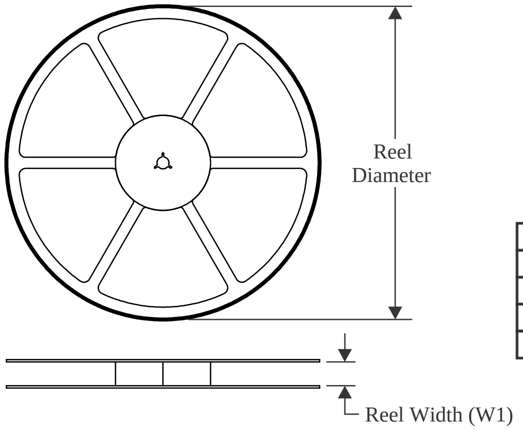
- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

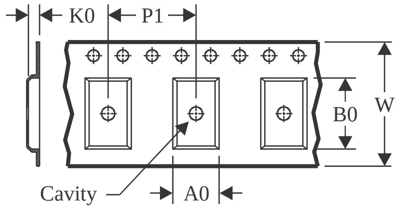
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

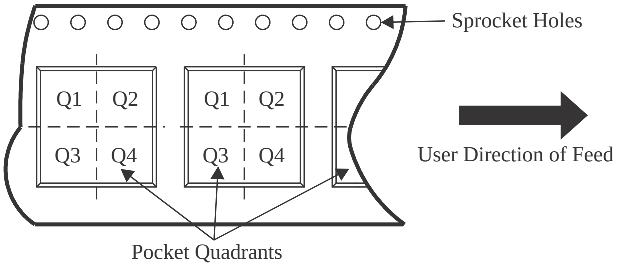


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

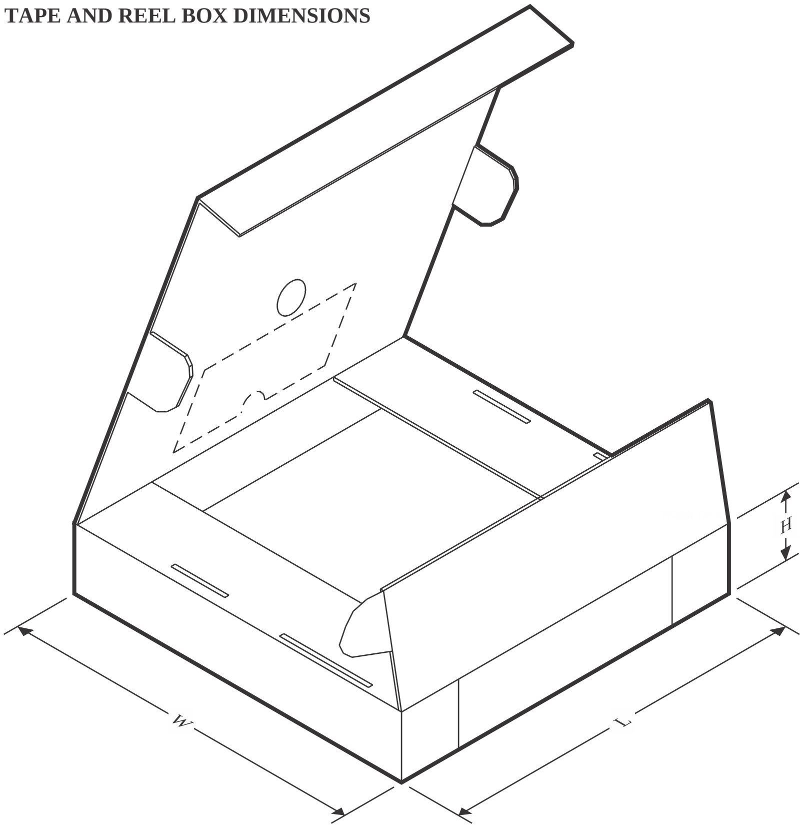


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL071HIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL071HIDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL071HIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TL071HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL072HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072HIPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CNSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074HIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL074HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

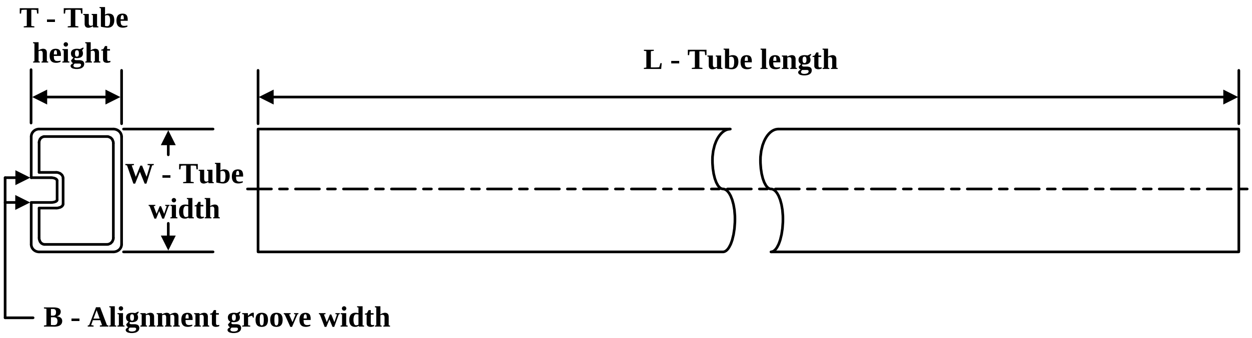


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	353.0	353.0	32.0
TL071BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL071CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL071CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL071HIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL071HIDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL071HIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TL071HIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL071IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL071IDR1G4	SOIC	D	8	2500	353.0	353.0	32.0
TL072ACDR	SOIC	D	8	2500	353.0	353.0	32.0
TL072BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL072CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL072CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL072CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TL072HIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL072HIPWR	TSSOP	PW	8	3000	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL072IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL074ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074ACNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL074BCDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074BCDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074CDBR	SSOP	DB	14	2000	353.0	353.0	32.0
TL074CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074CDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TL074CNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL074CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL074CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL074HIDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074HIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL074HIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL074IDR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
81023052A	FK	LCCC	20	55	506.98	12.06	2030	NA
8102305HA	U	CFP	10	25	506.98	26.16	6220	NA
81023062A	FK	LCCC	20	55	506.98	12.06	2030	NA
8102306DA	W	CFP	14	25	506.98	26.16	6220	NA
TL071ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL071ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL071BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL071BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL071CP	P	PDIP	8	50	506	13.97	11230	4.32
TL071CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL071IP	P	PDIP	8	50	506	13.97	11230	4.32
TL071IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACPS	PS	SOP	8	80	530	10.5	4000	4.1
TL072ACPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TL072BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL072BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072CP	P	PDIP	8	50	506	13.97	11230	4.32
TL072CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072CPS	PS	SOP	8	80	530	10.5	4000	4.1
TL072CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TL072IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL072MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL072MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL072MUB	U	CFP	10	25	506.98	26.16	6220	NA
TL072MUB.A	U	CFP	10	25	506.98	26.16	6220	NA
TL074ACN	N	PDIP	14	25	506	13.97	11230	4.32

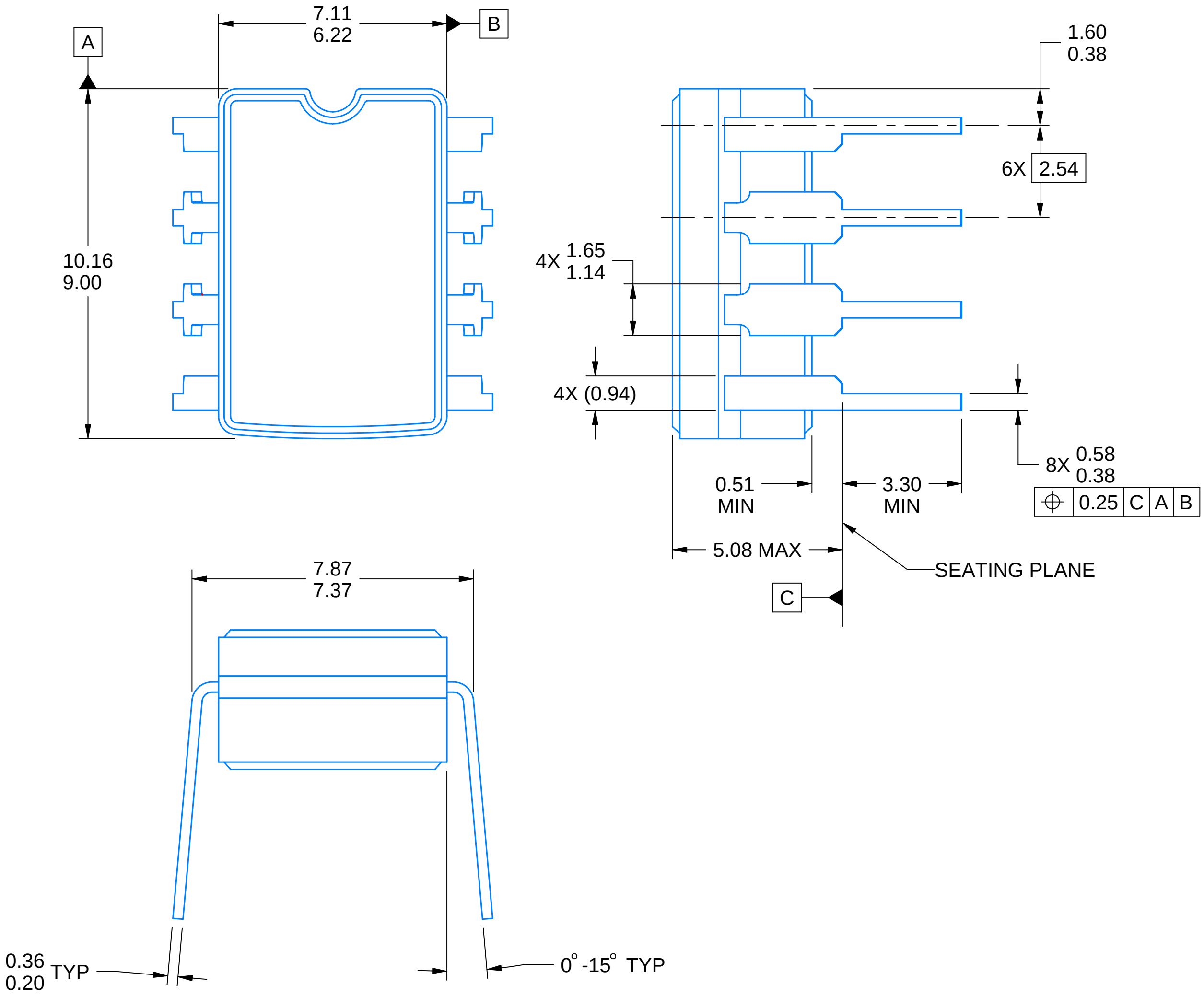
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL074ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL074ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074IN	N	PDIP	14	25	506	13.97	11230	4.32
TL074IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074ING4	N	PDIP	14	25	506	13.97	11230	4.32
TL074ING4.A	N	PDIP	14	25	506	13.97	11230	4.32
TL074MFK	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MWB	W	CFP	14	25	506.98	26.16	6220	NA
TL074MWB.A	W	CFP	14	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

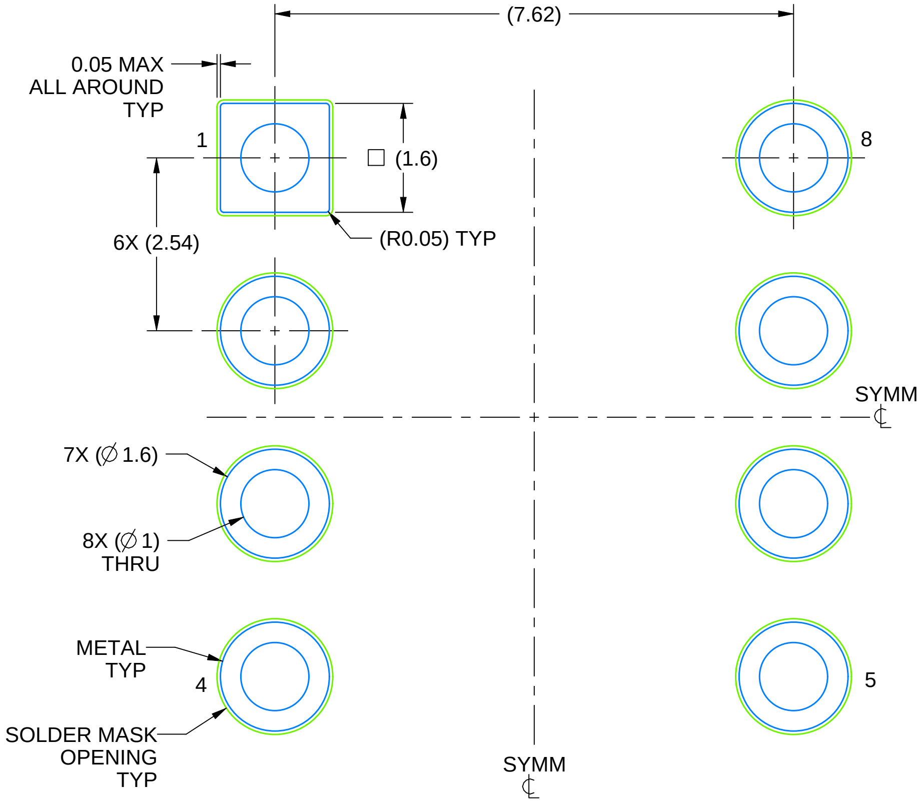
CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

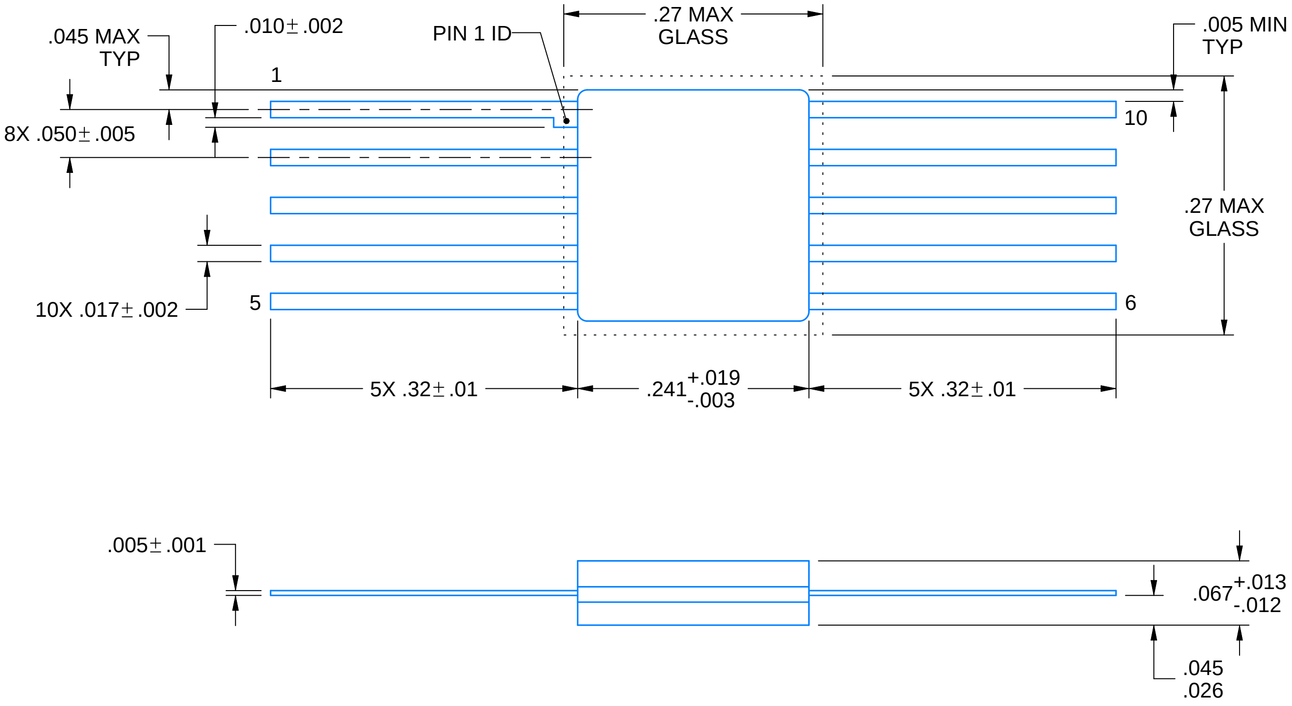
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023



4225582/A 01/2020

NOTES:

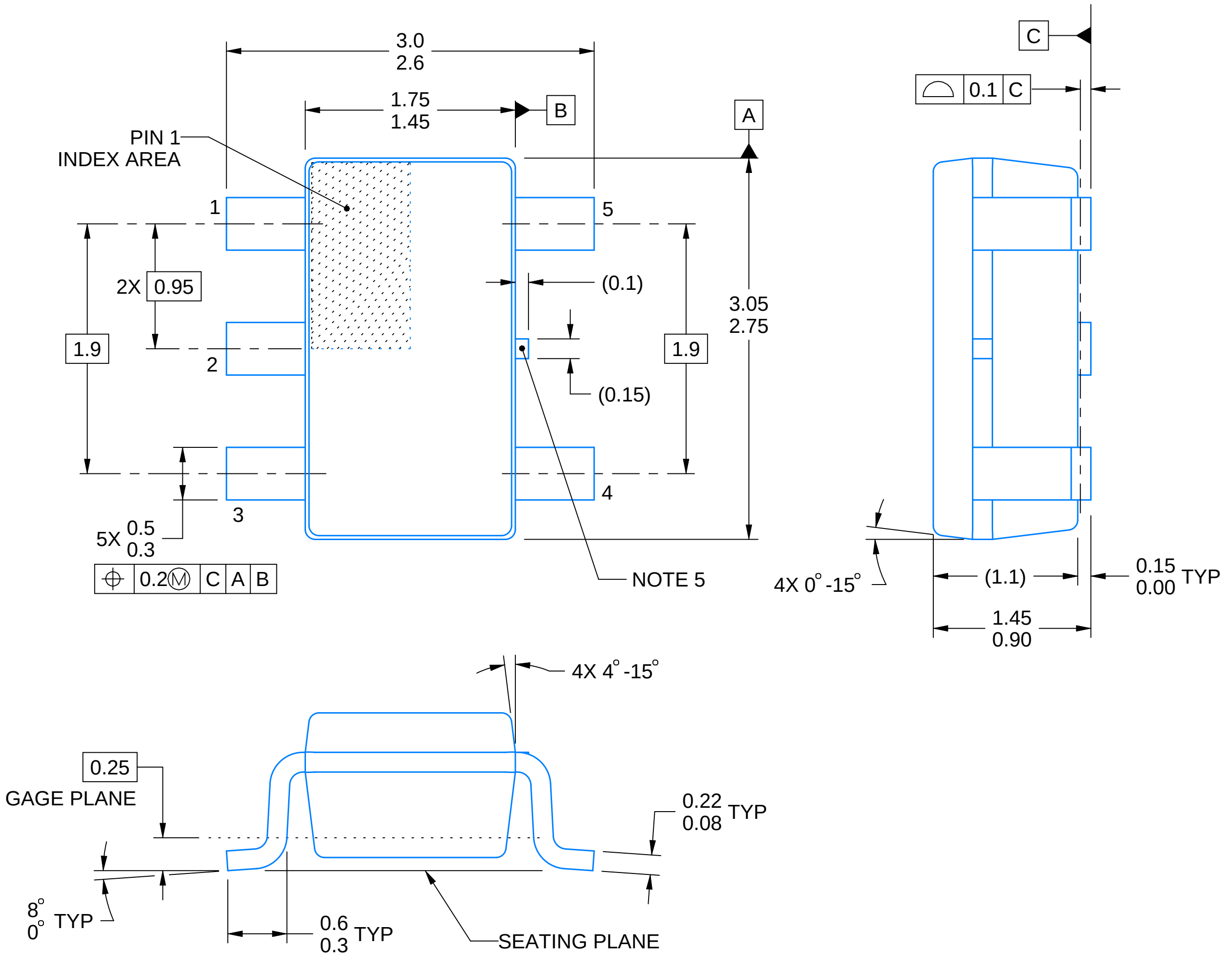
1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

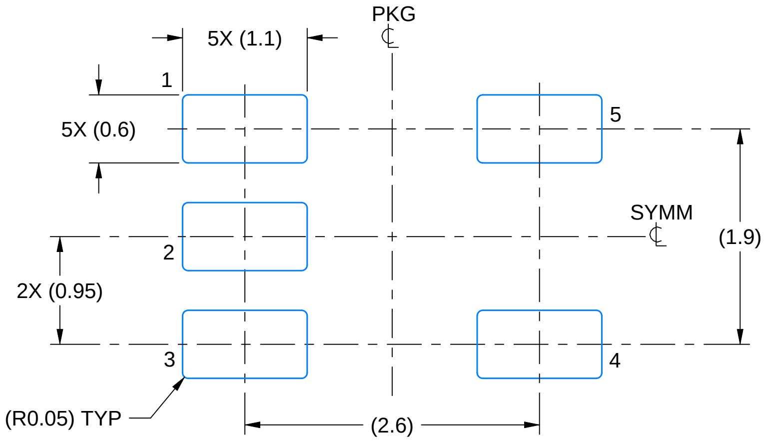
SMALL OUTLINE TRANSISTOR



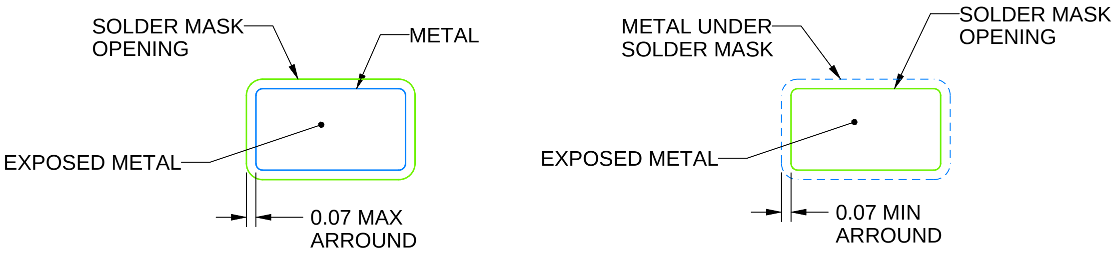
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



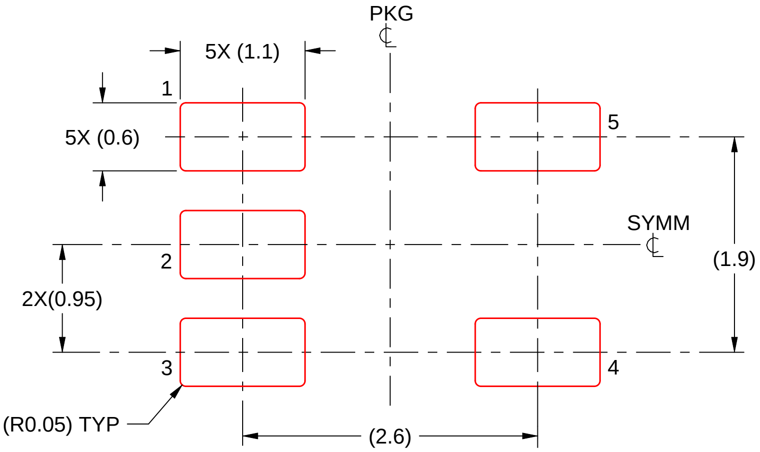
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

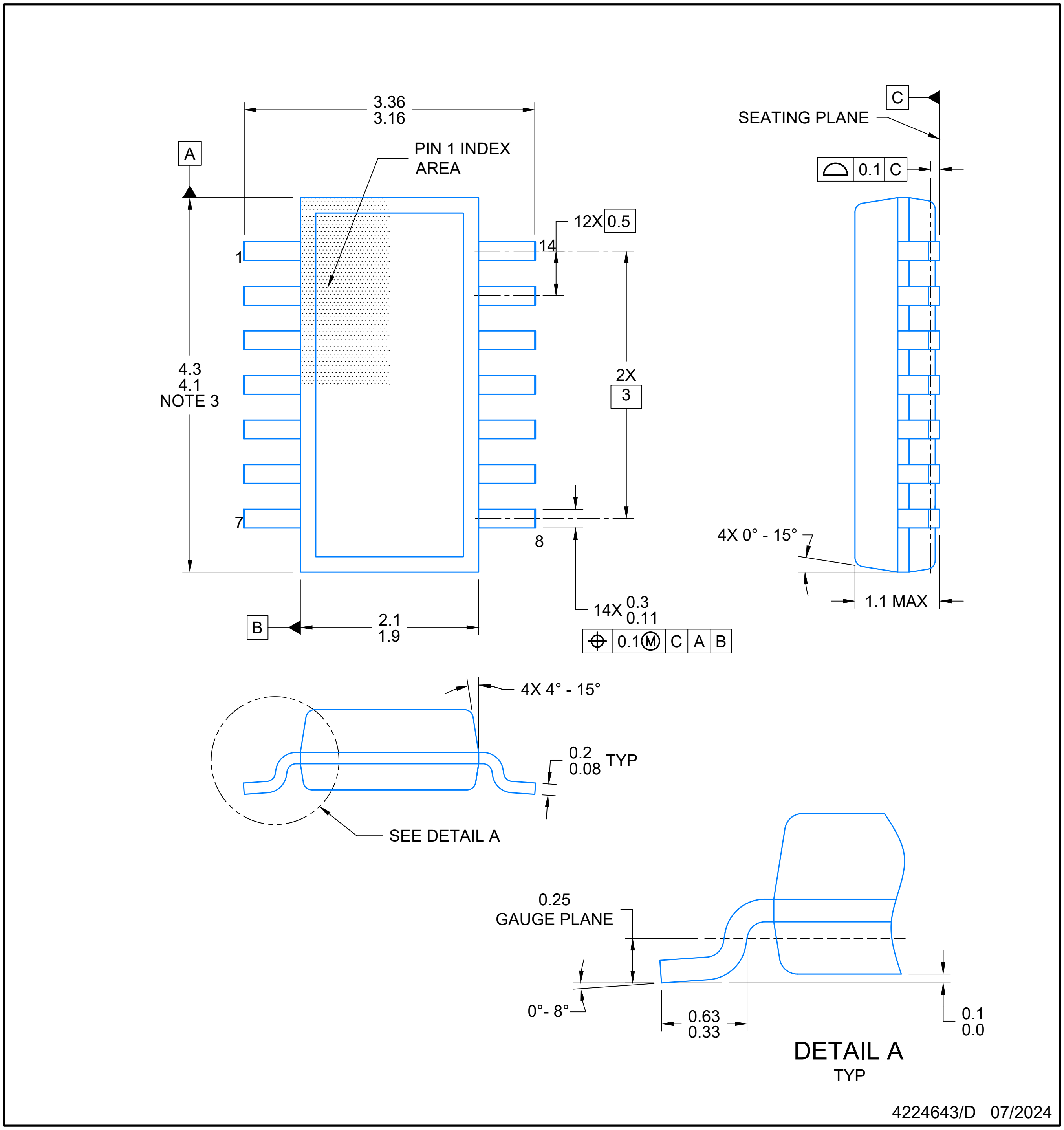
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

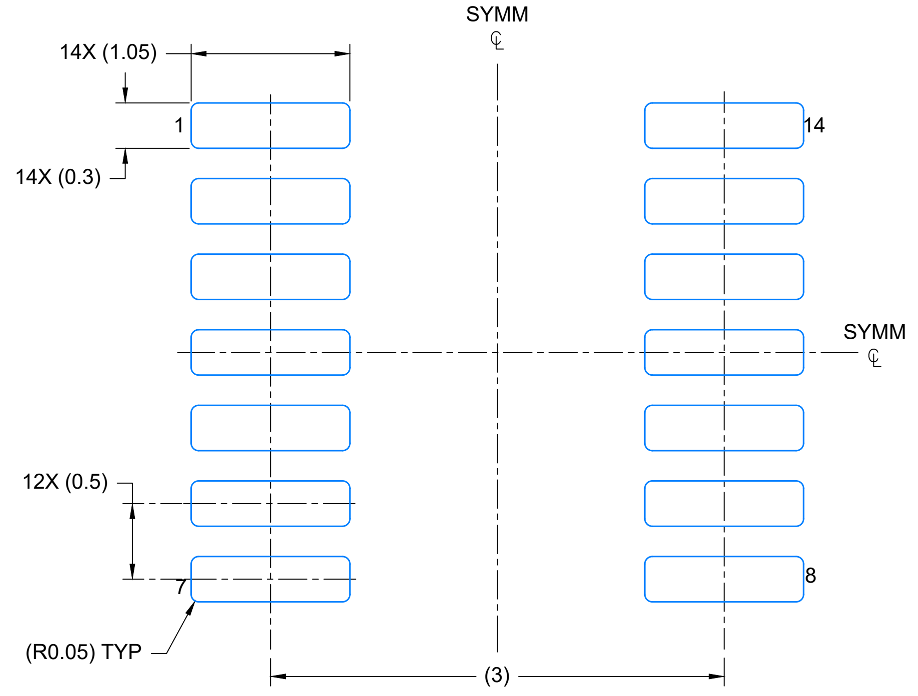
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

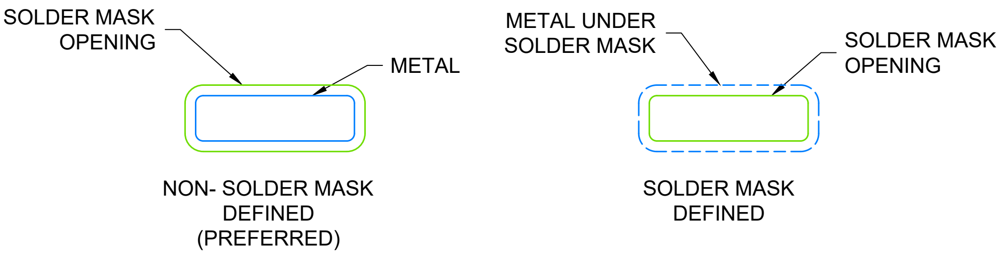


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

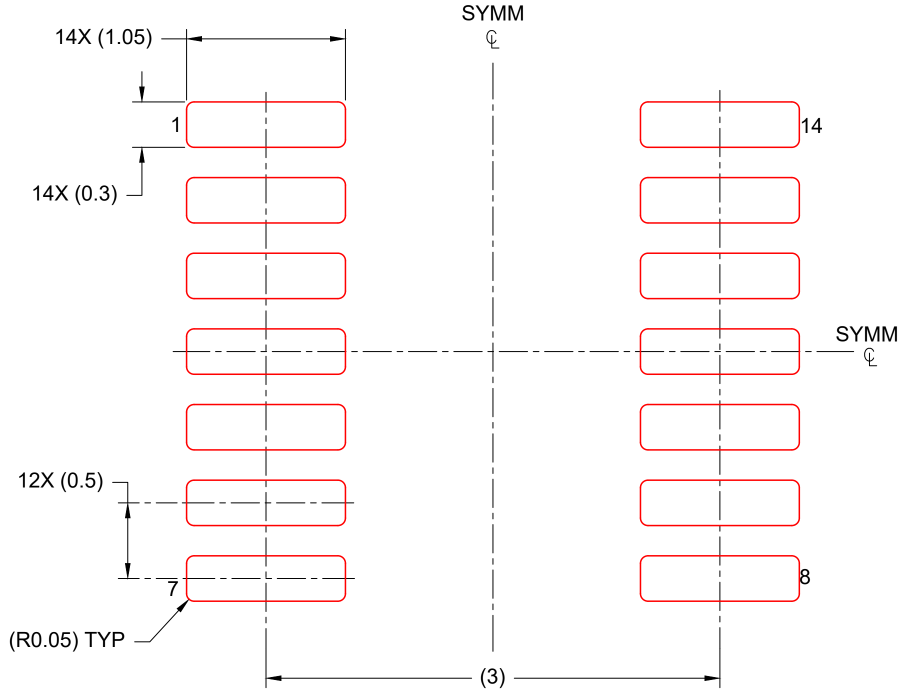


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

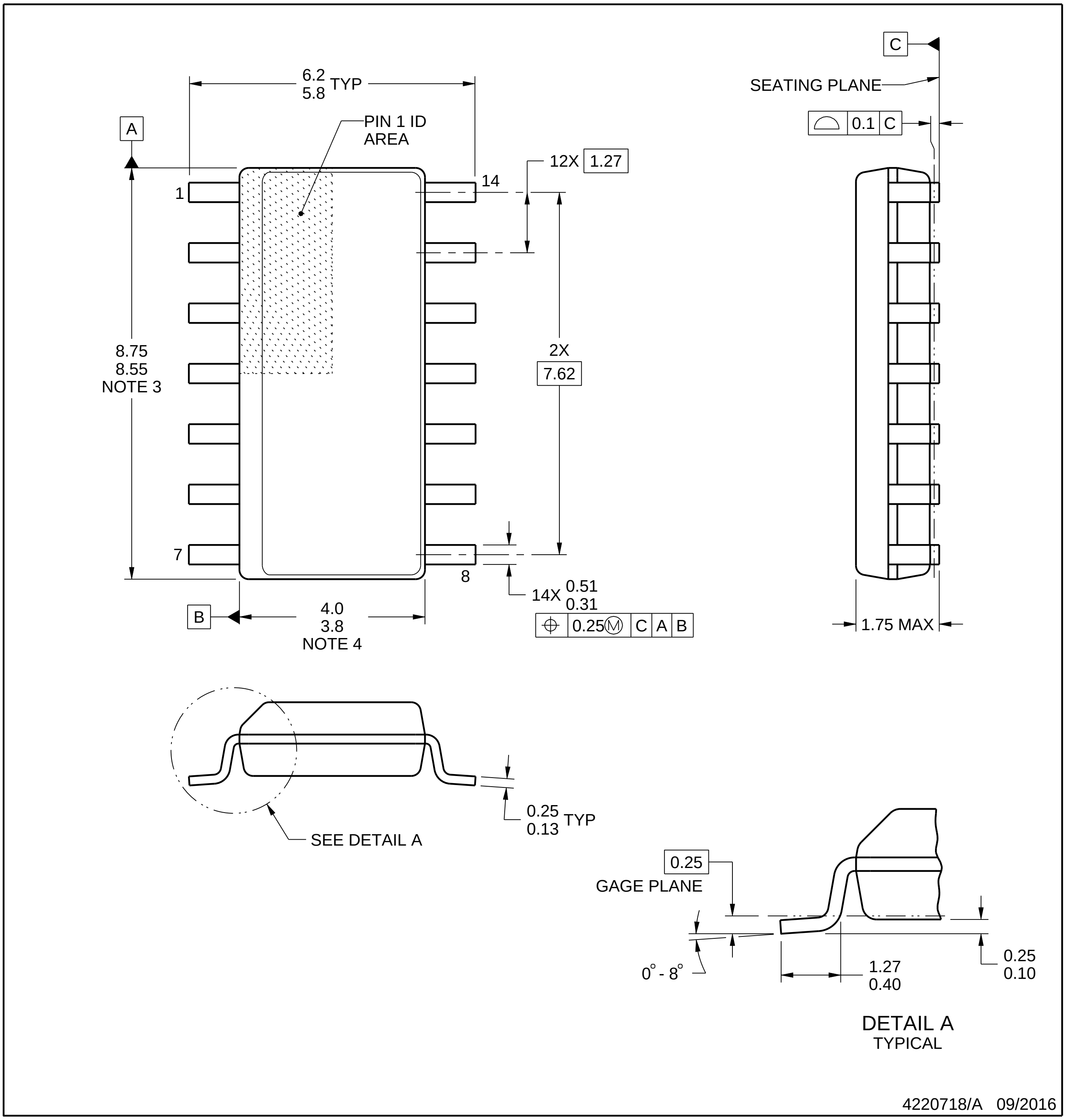
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

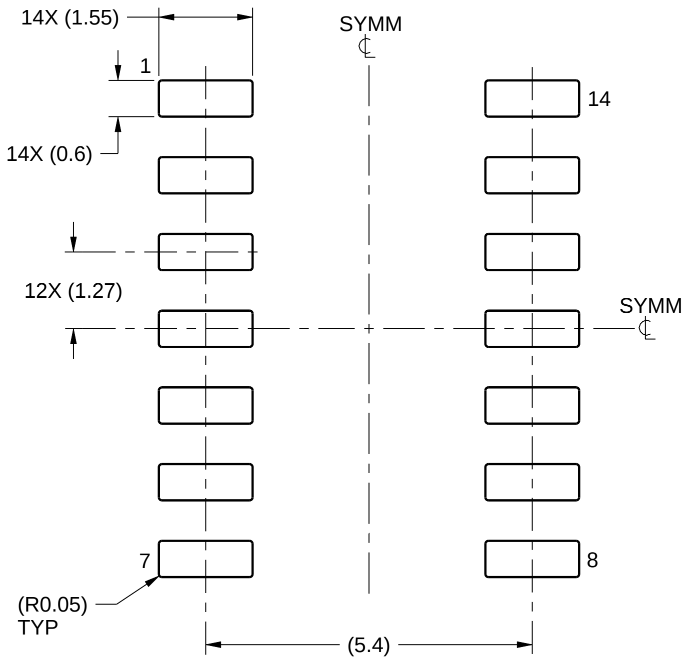
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

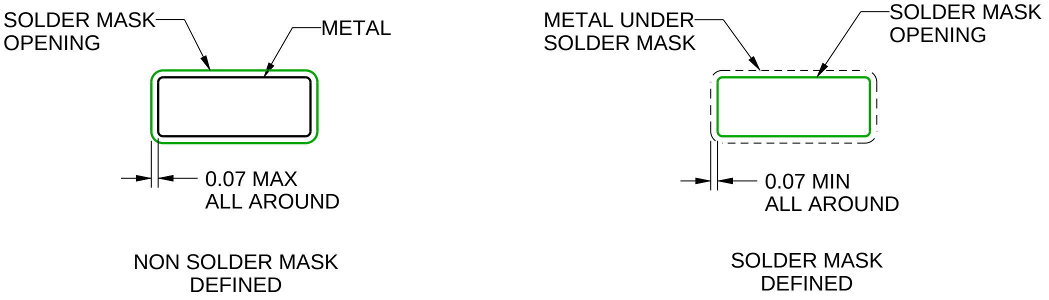


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

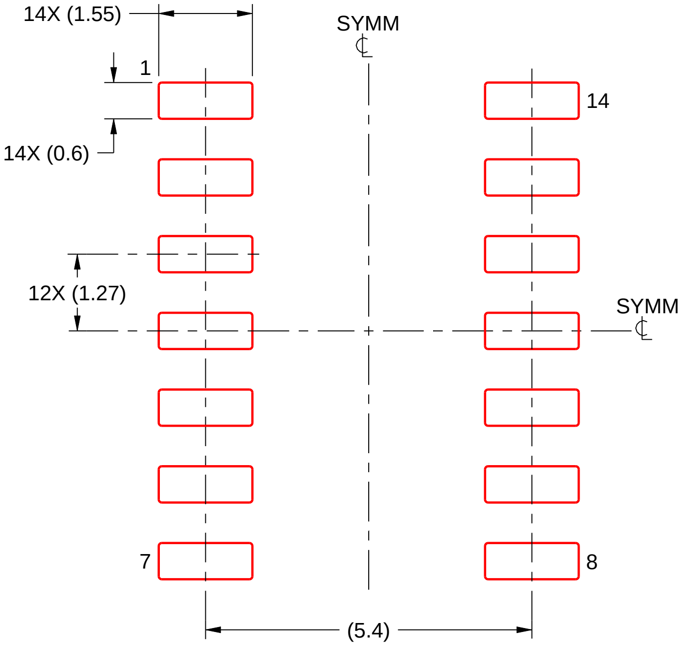
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

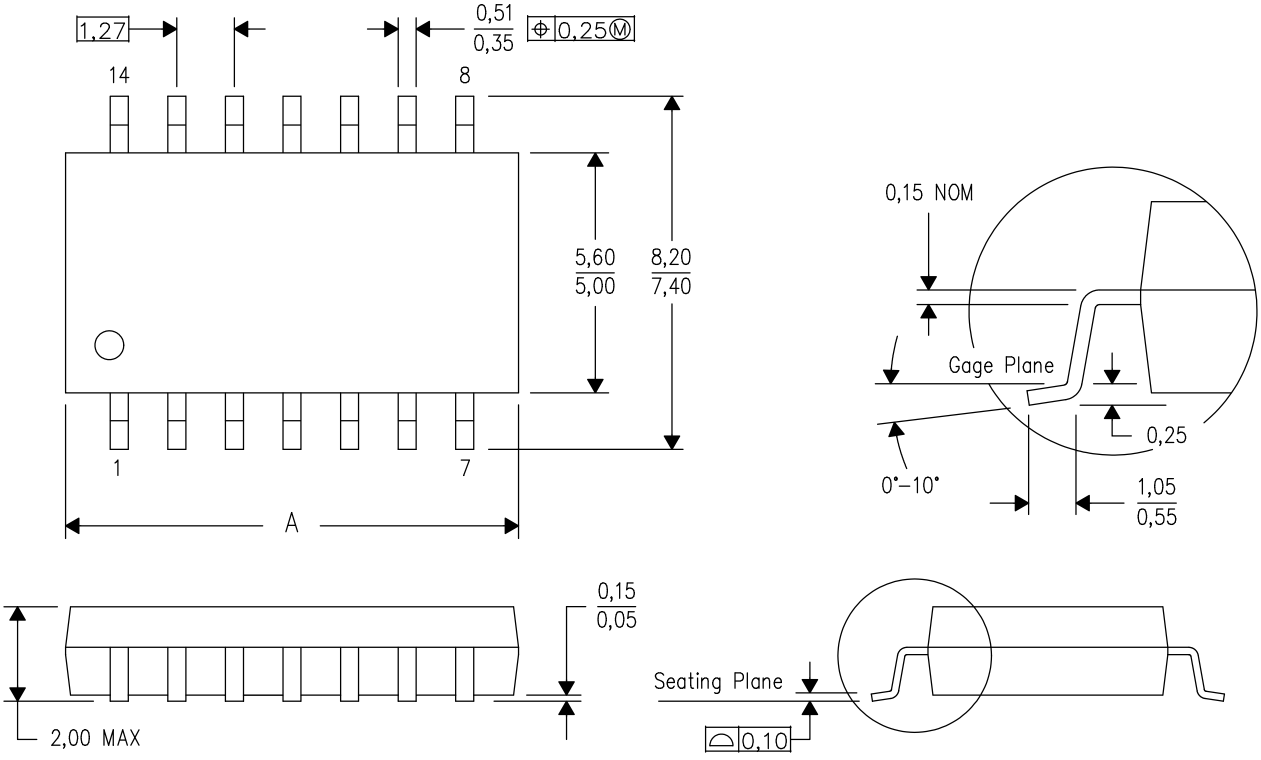
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

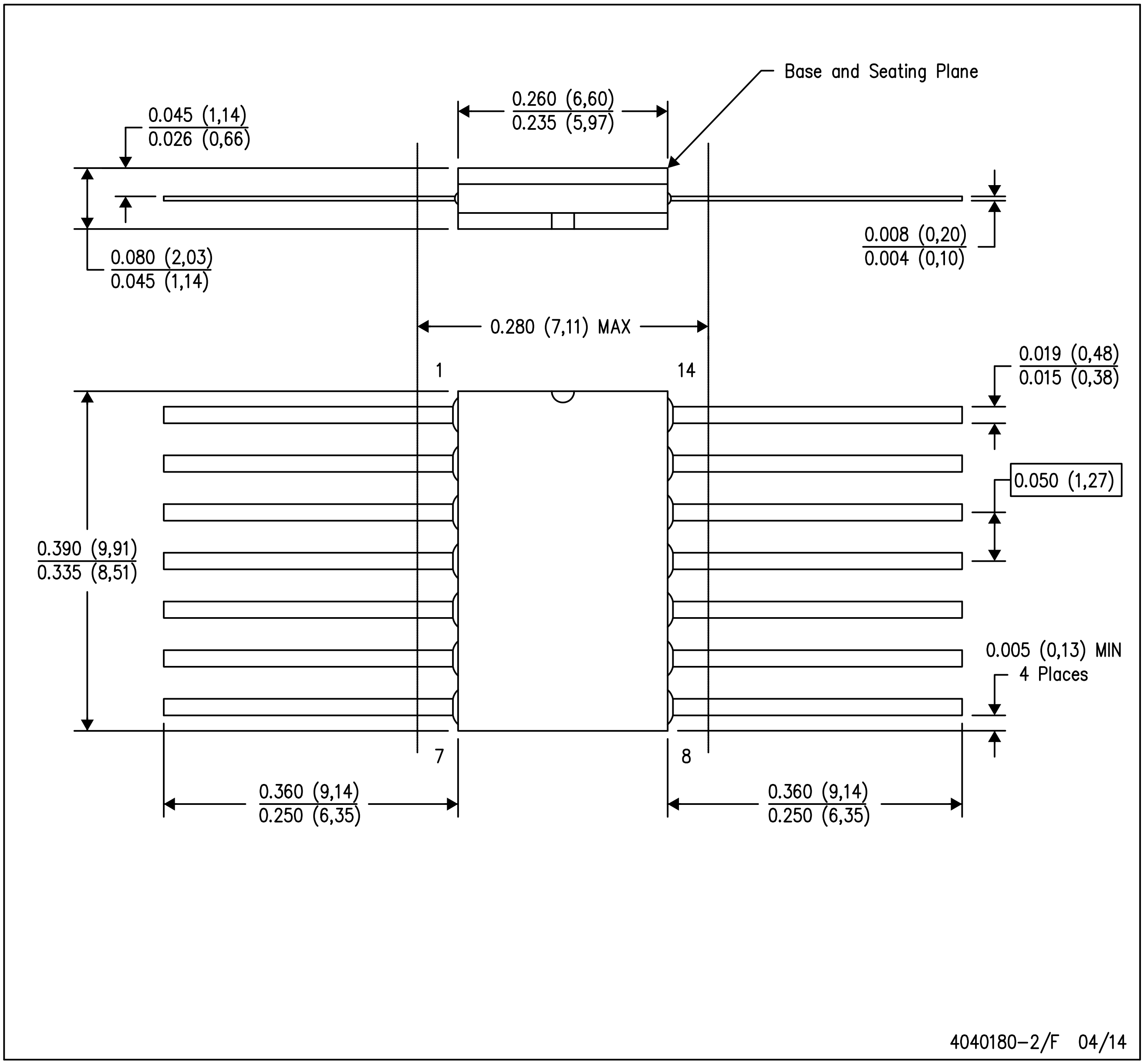


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

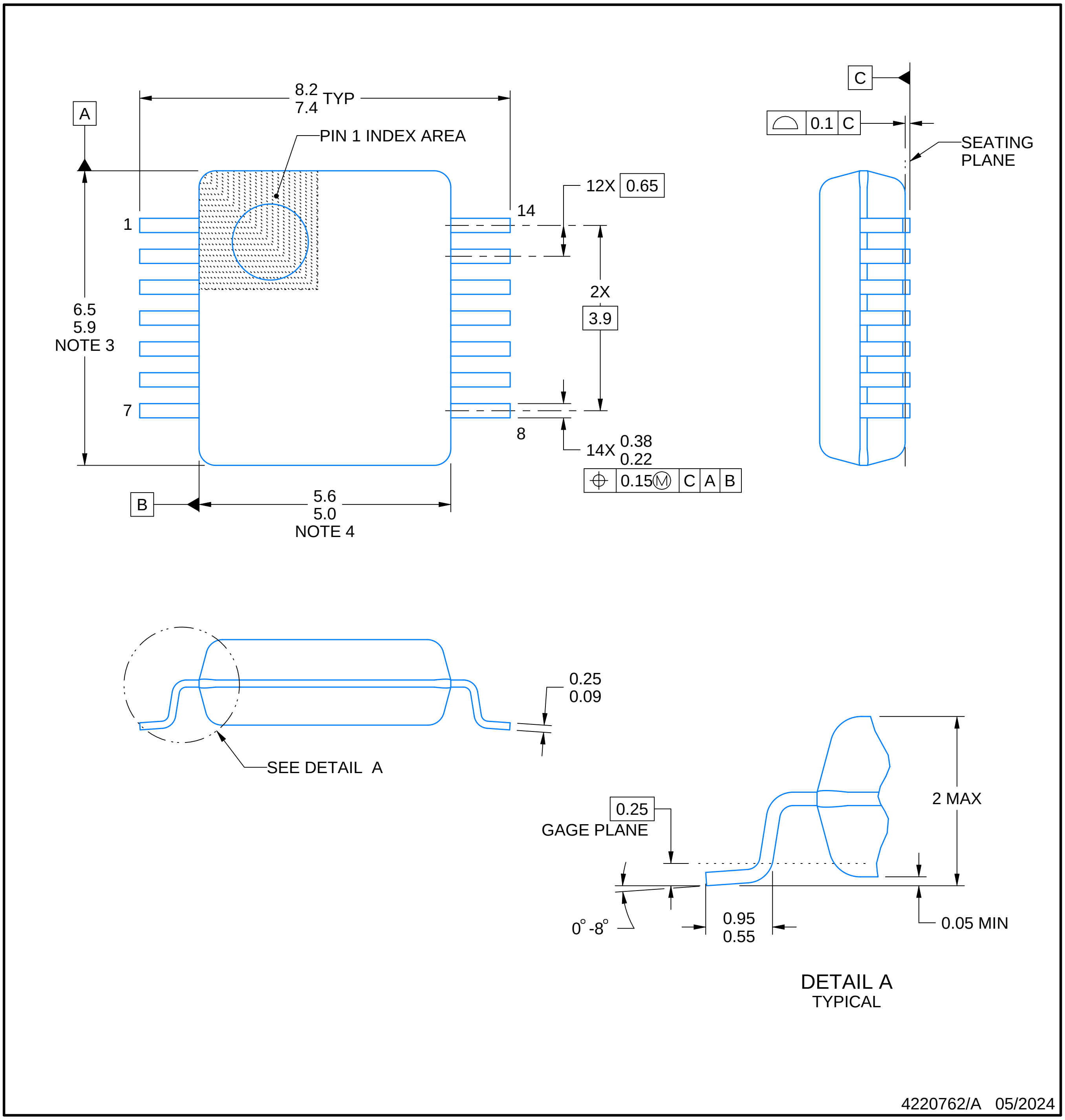
4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

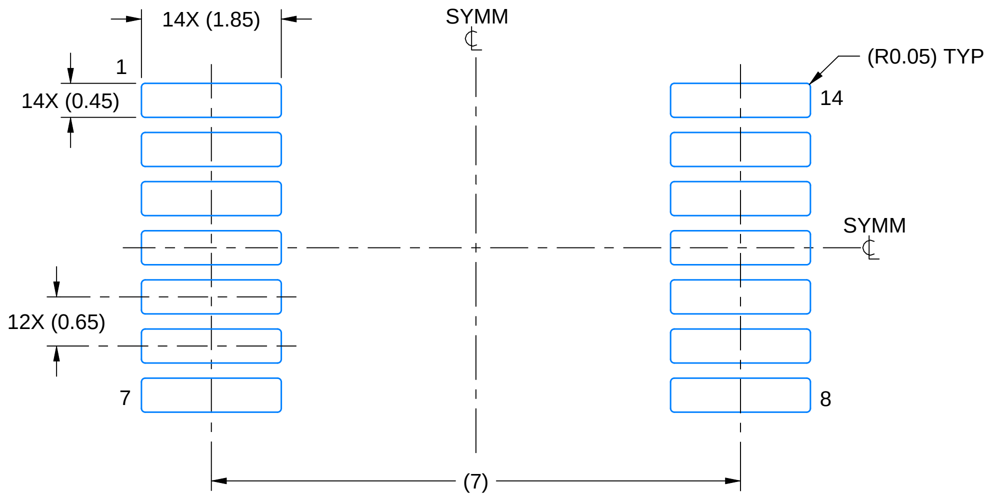


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F14

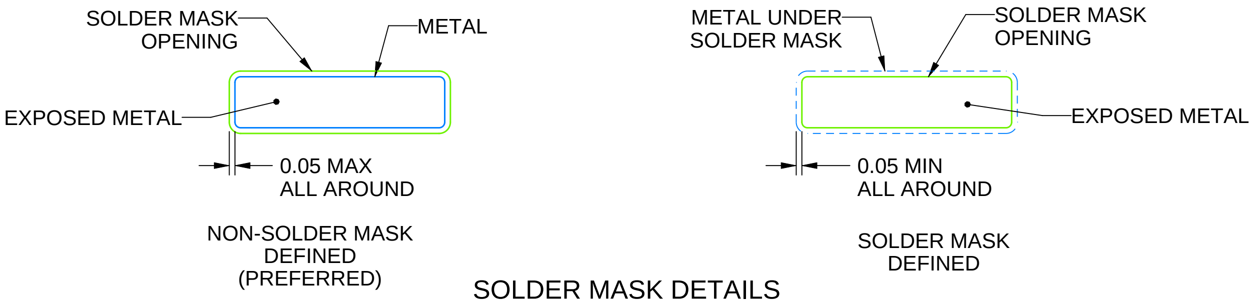


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

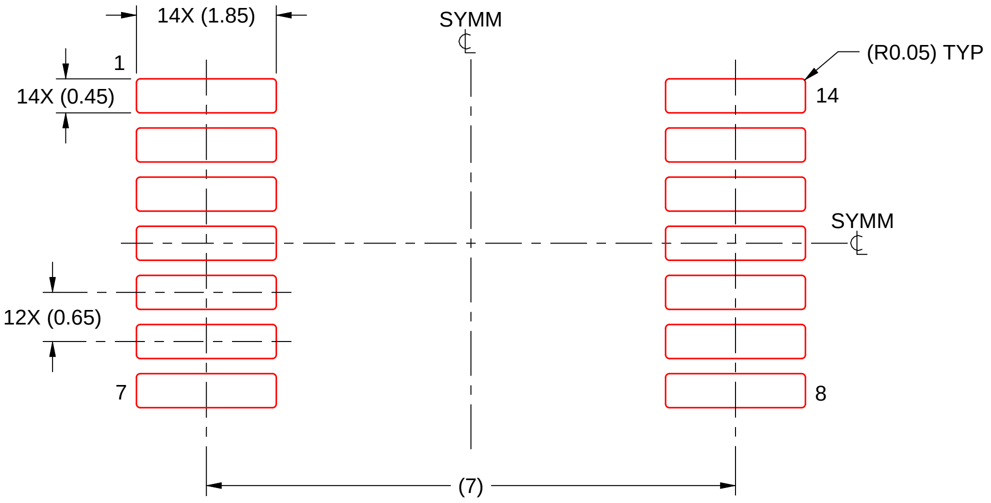


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

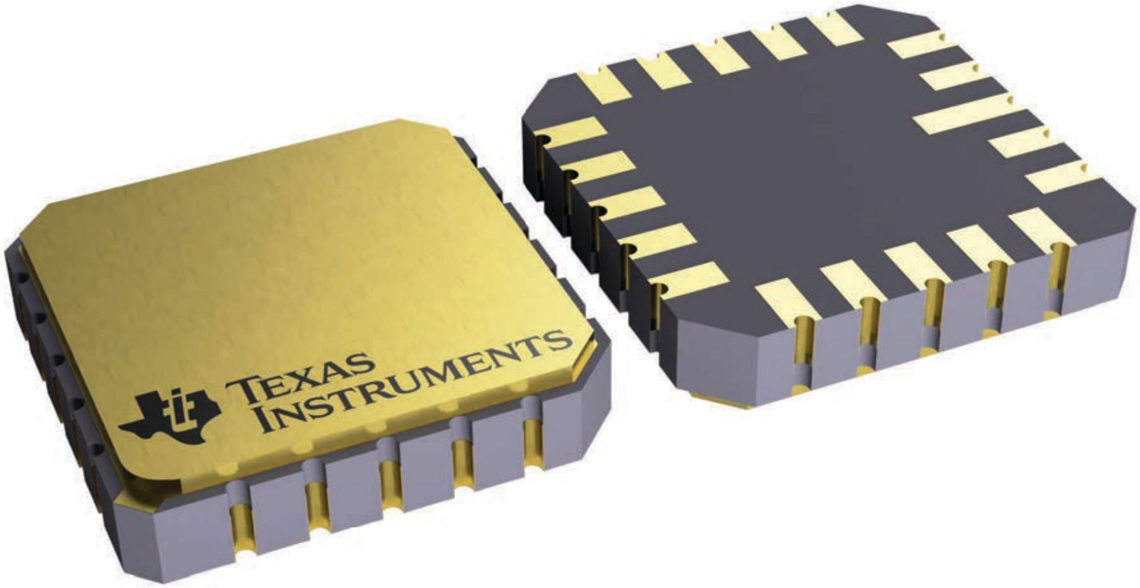
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

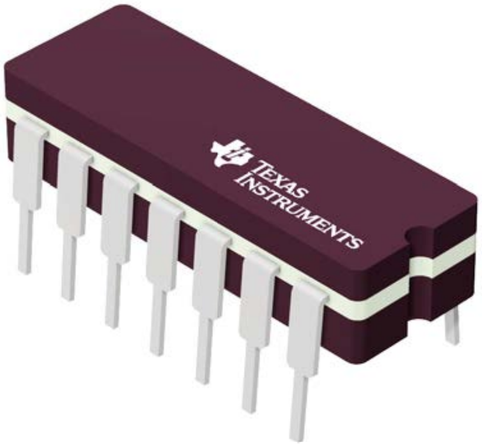


GENERIC PACKAGE VIEW

J 14

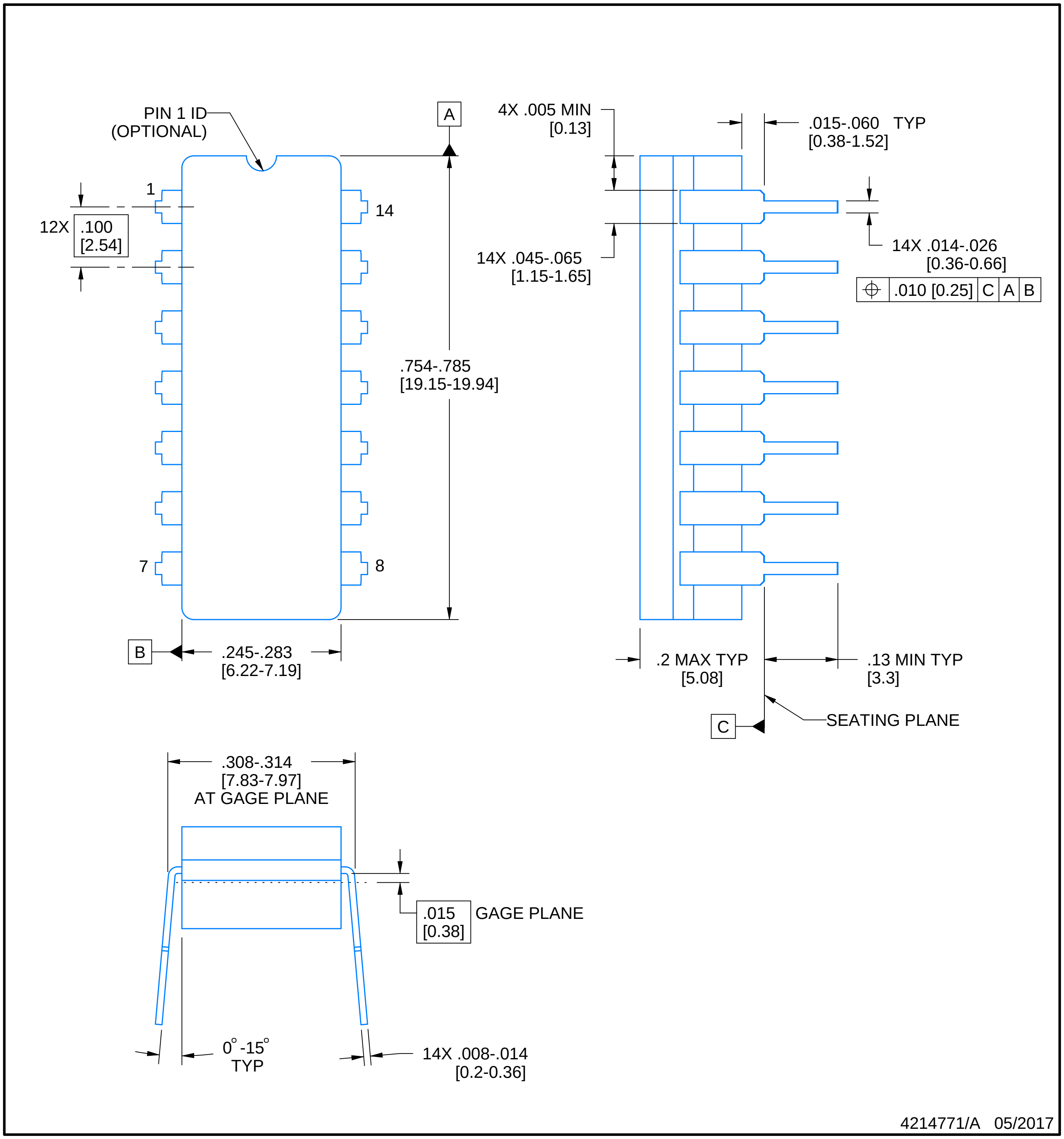
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



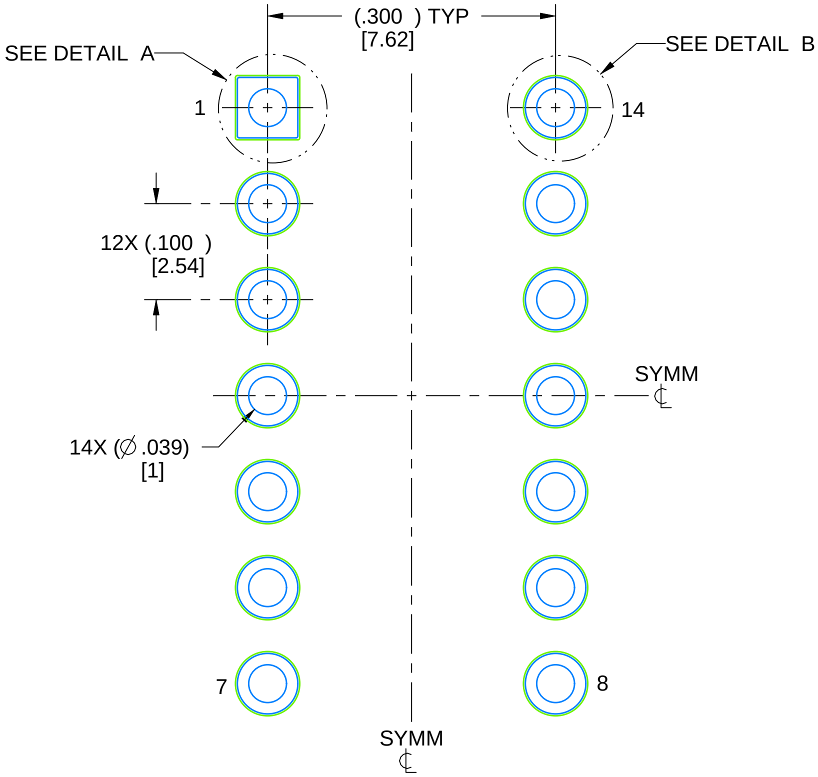
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

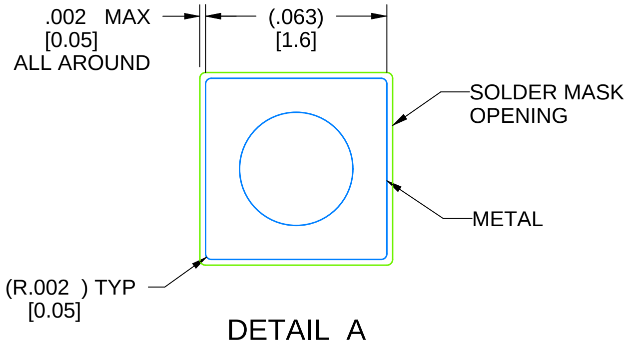


NOTES:

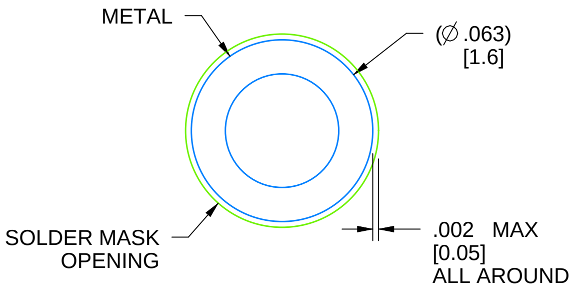
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



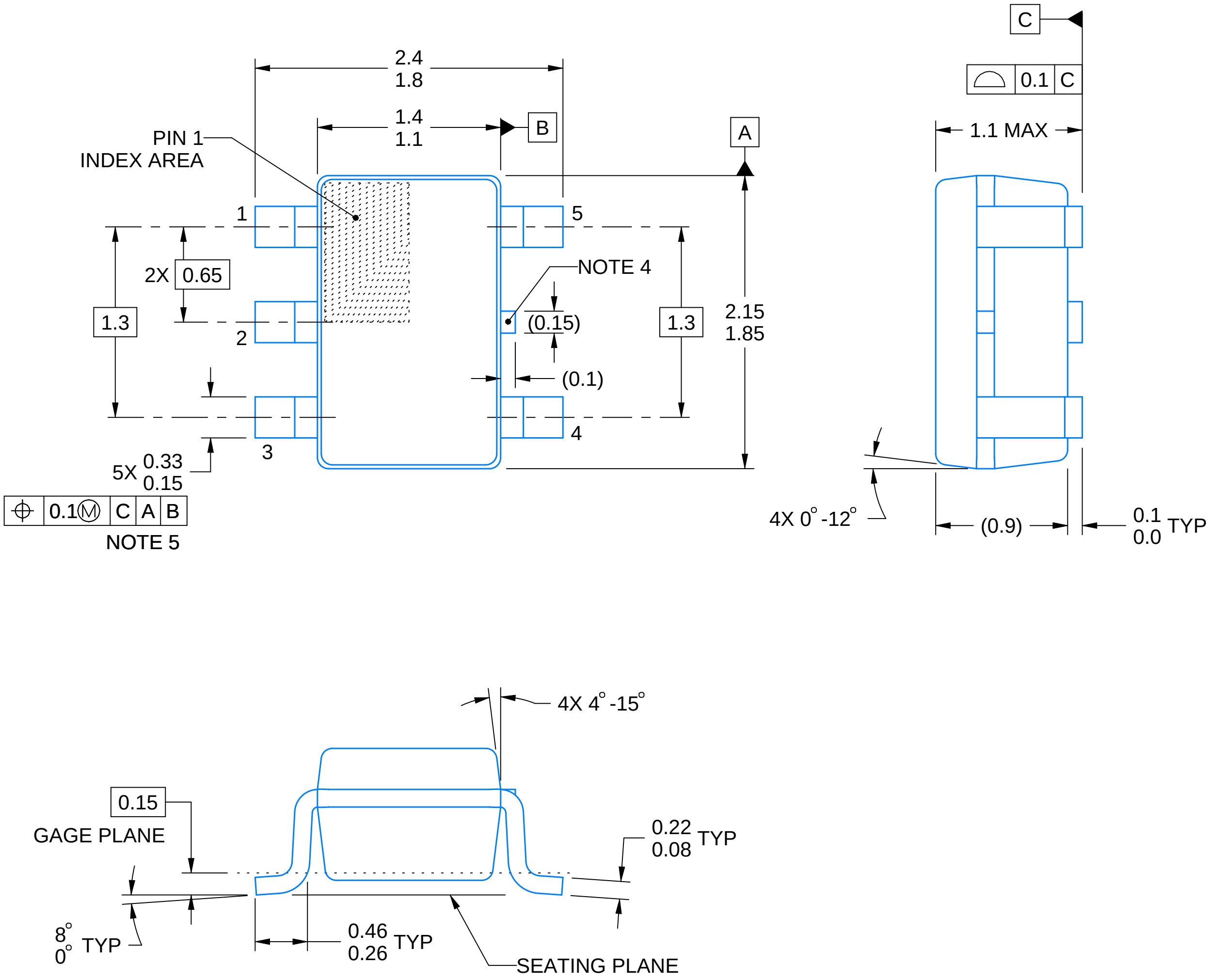
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



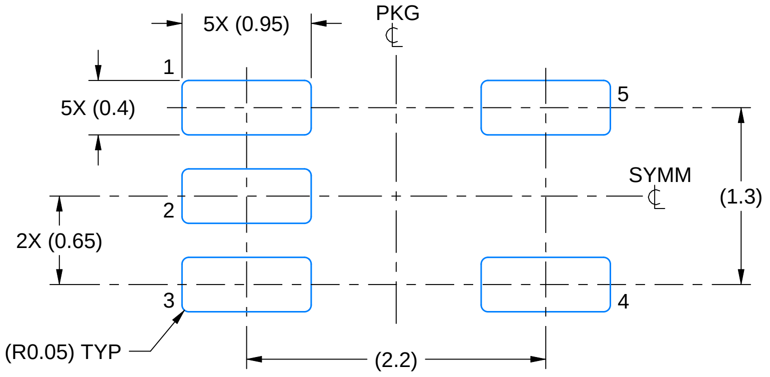
DETAIL B
13X, SCALE: 15X



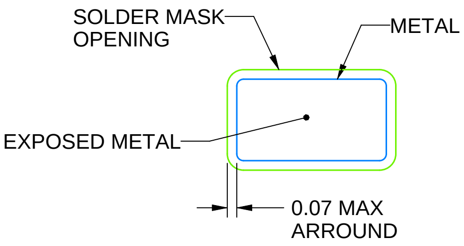
4214834/G 11/2024

NOTES:

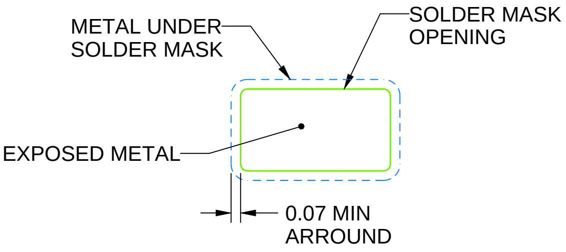
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

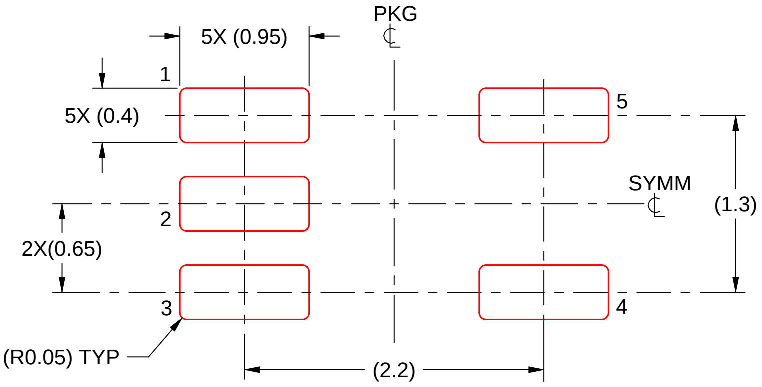


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

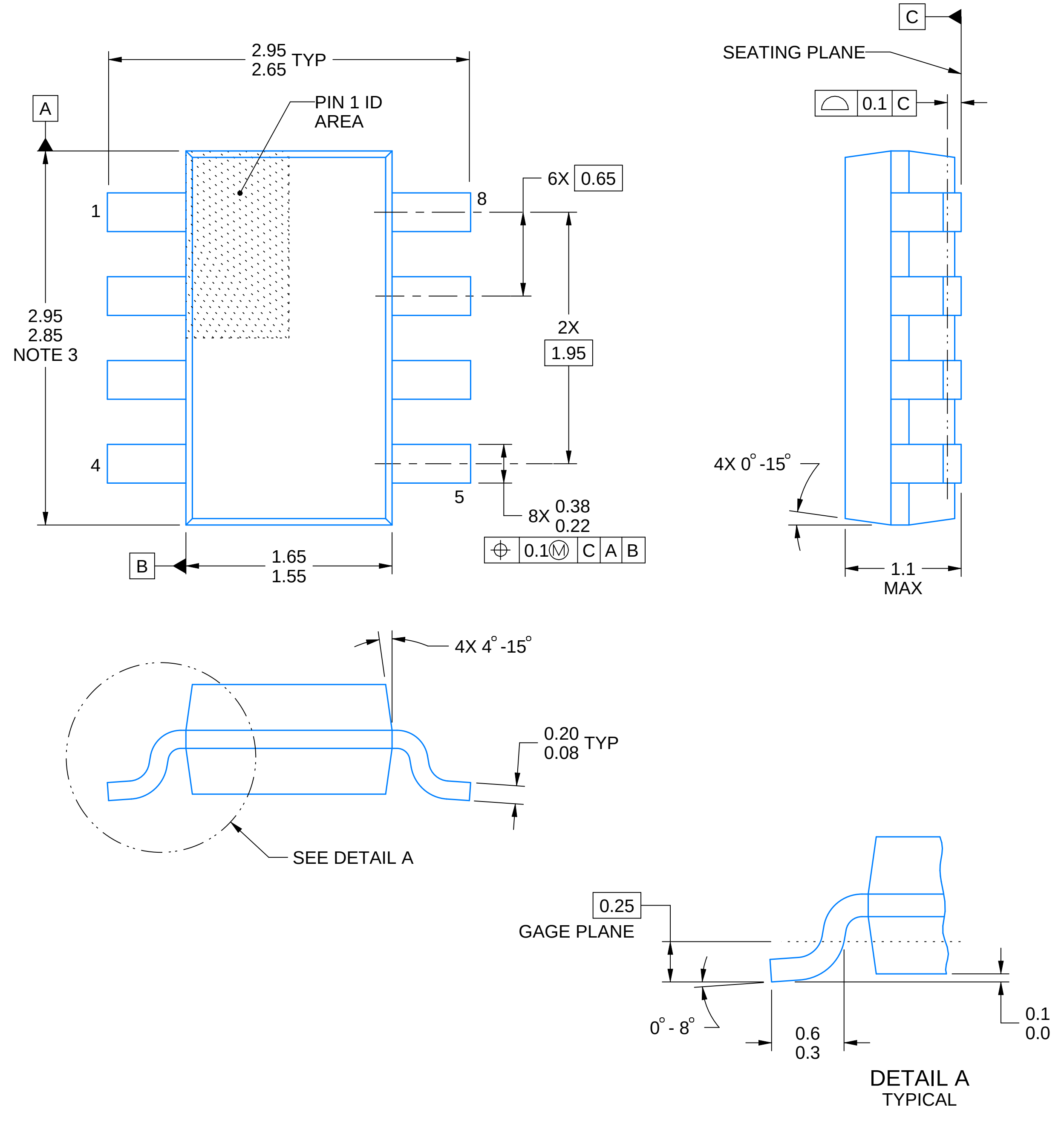
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

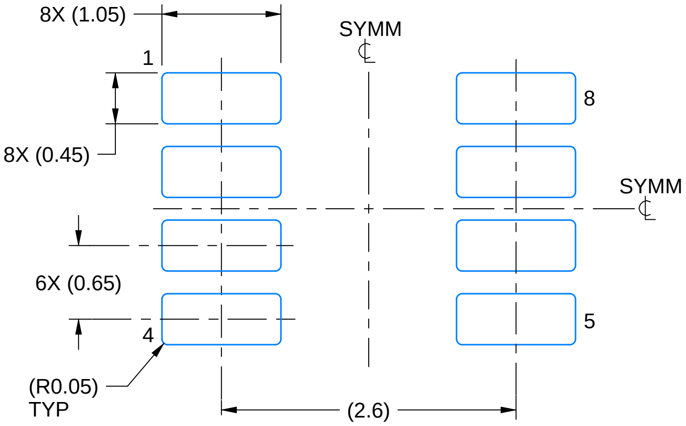


4222047/E 07/2024

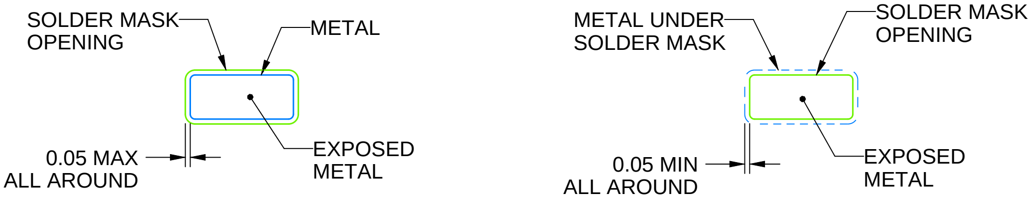
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



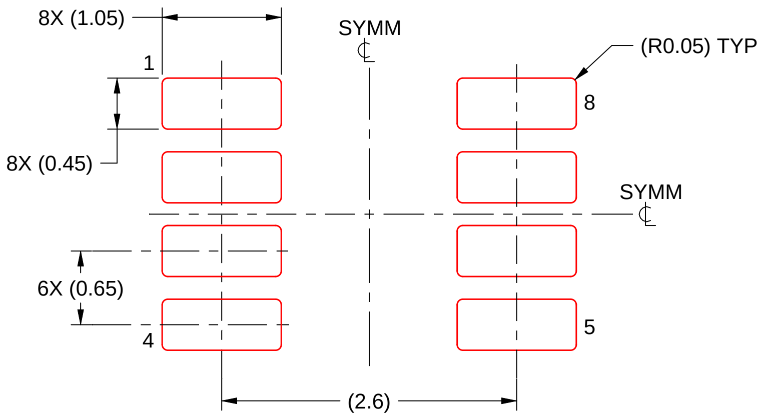
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

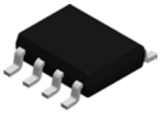


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

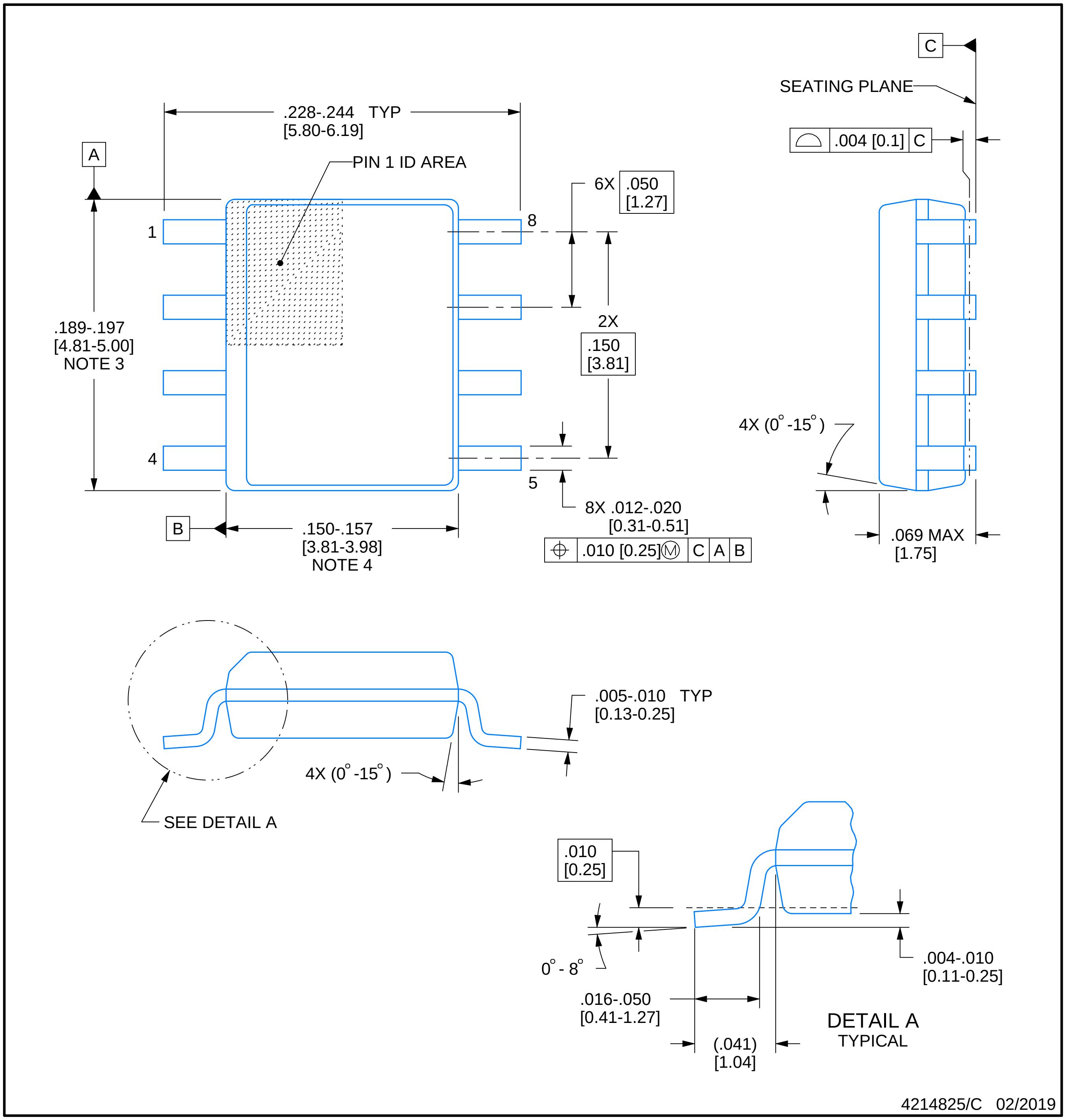


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

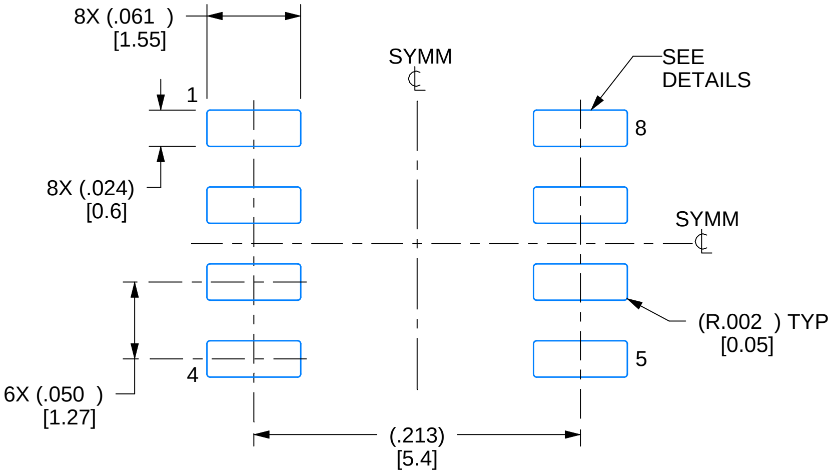
SMALL OUTLINE INTEGRATED CIRCUIT



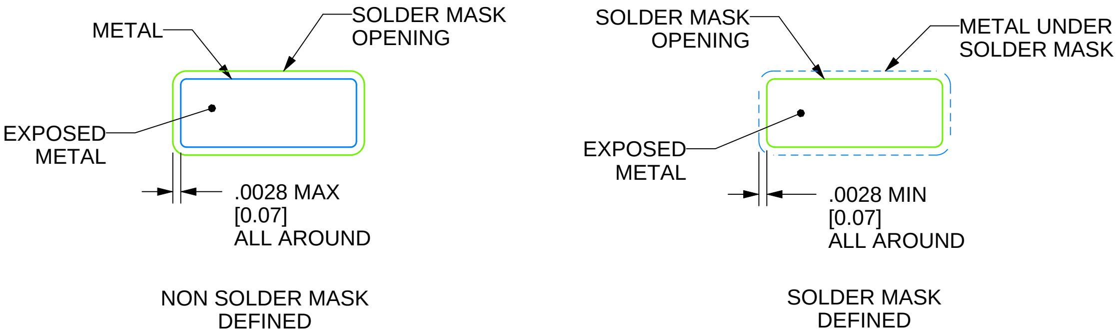
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



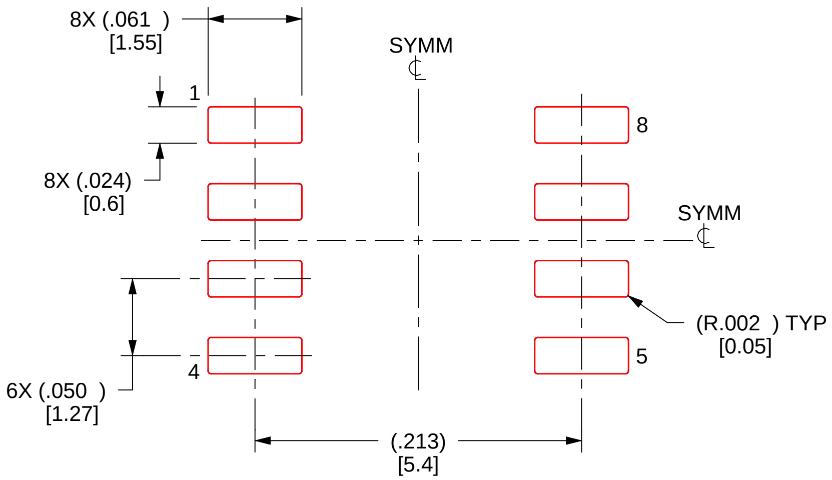
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



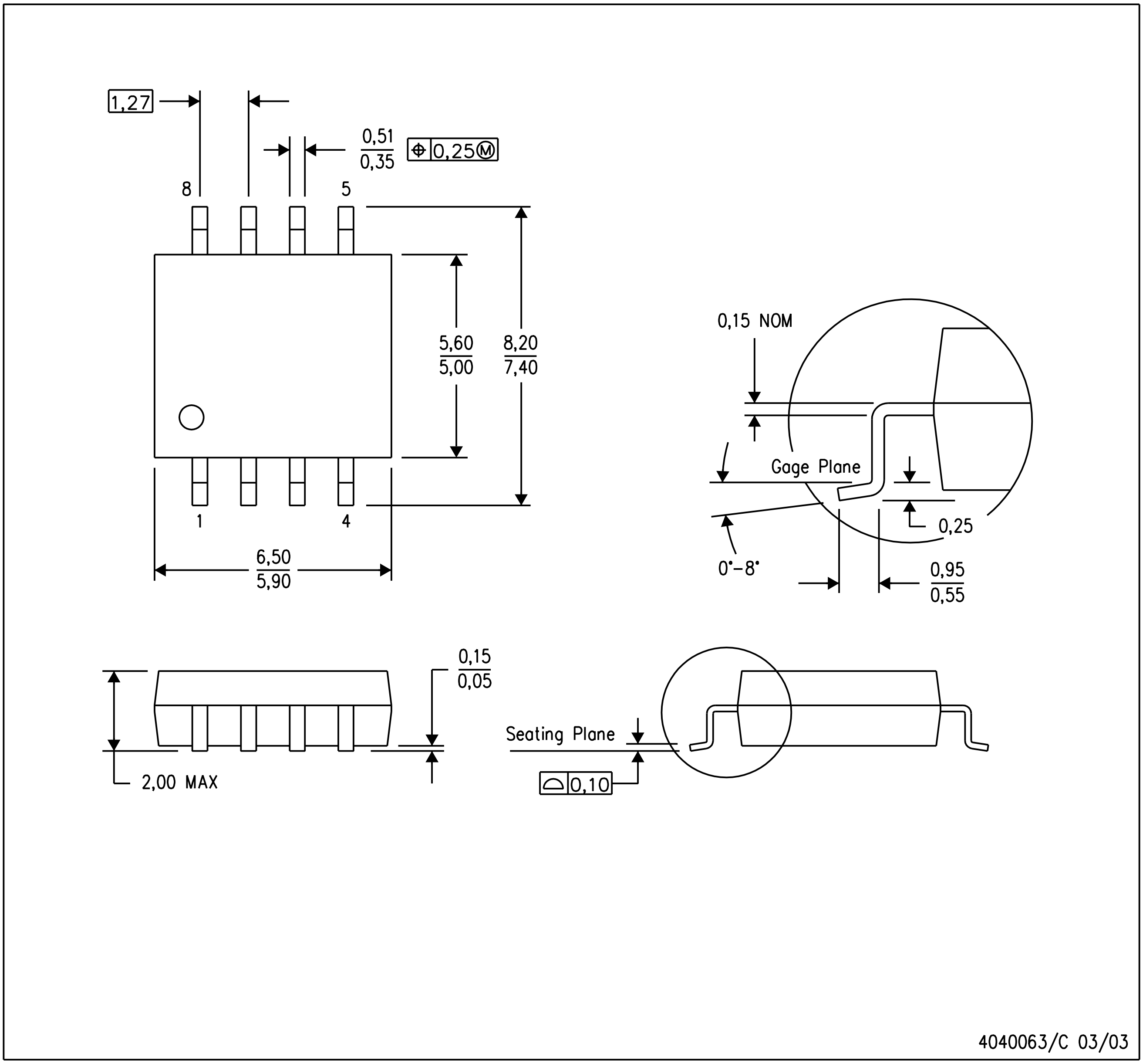
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

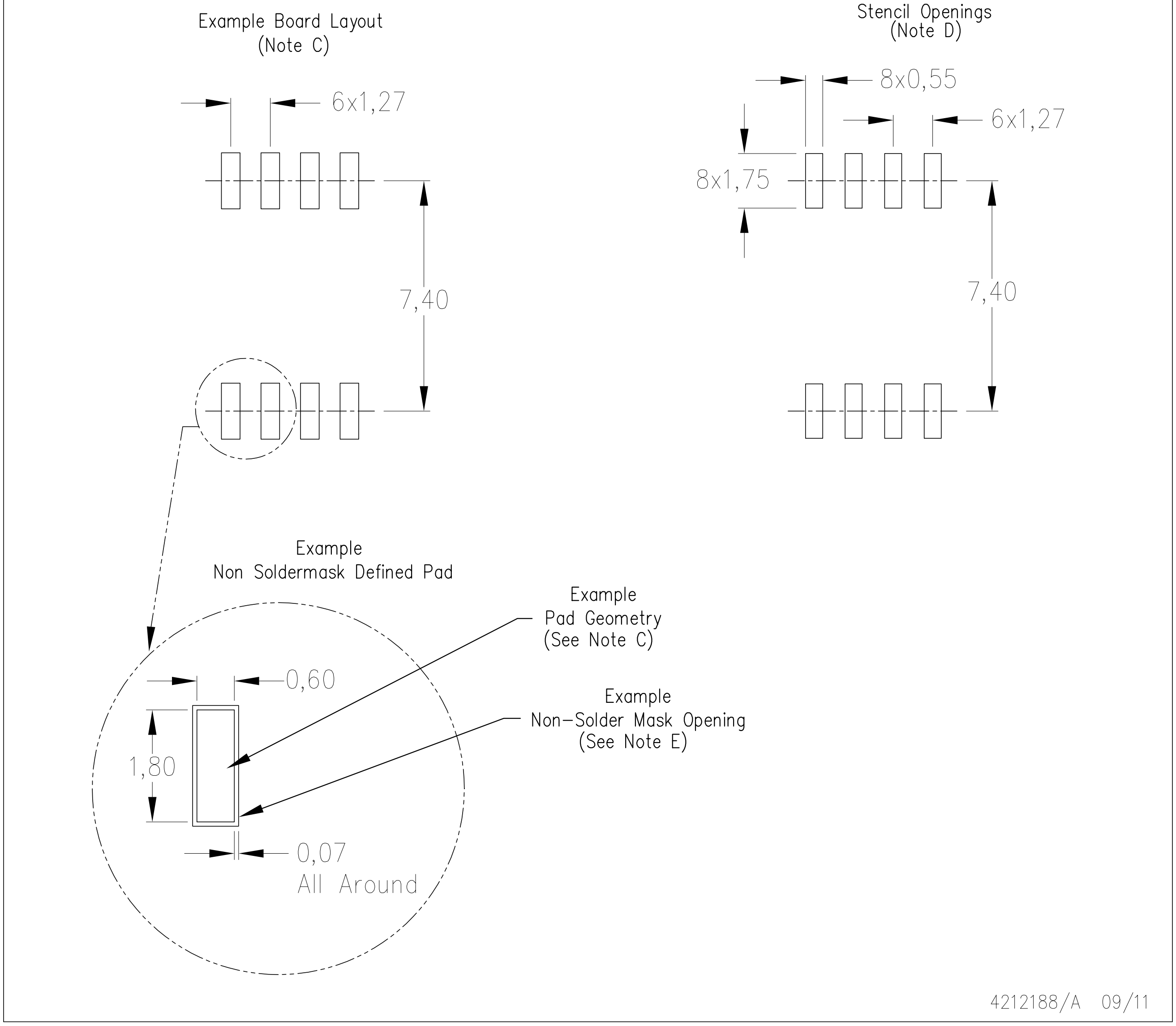
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

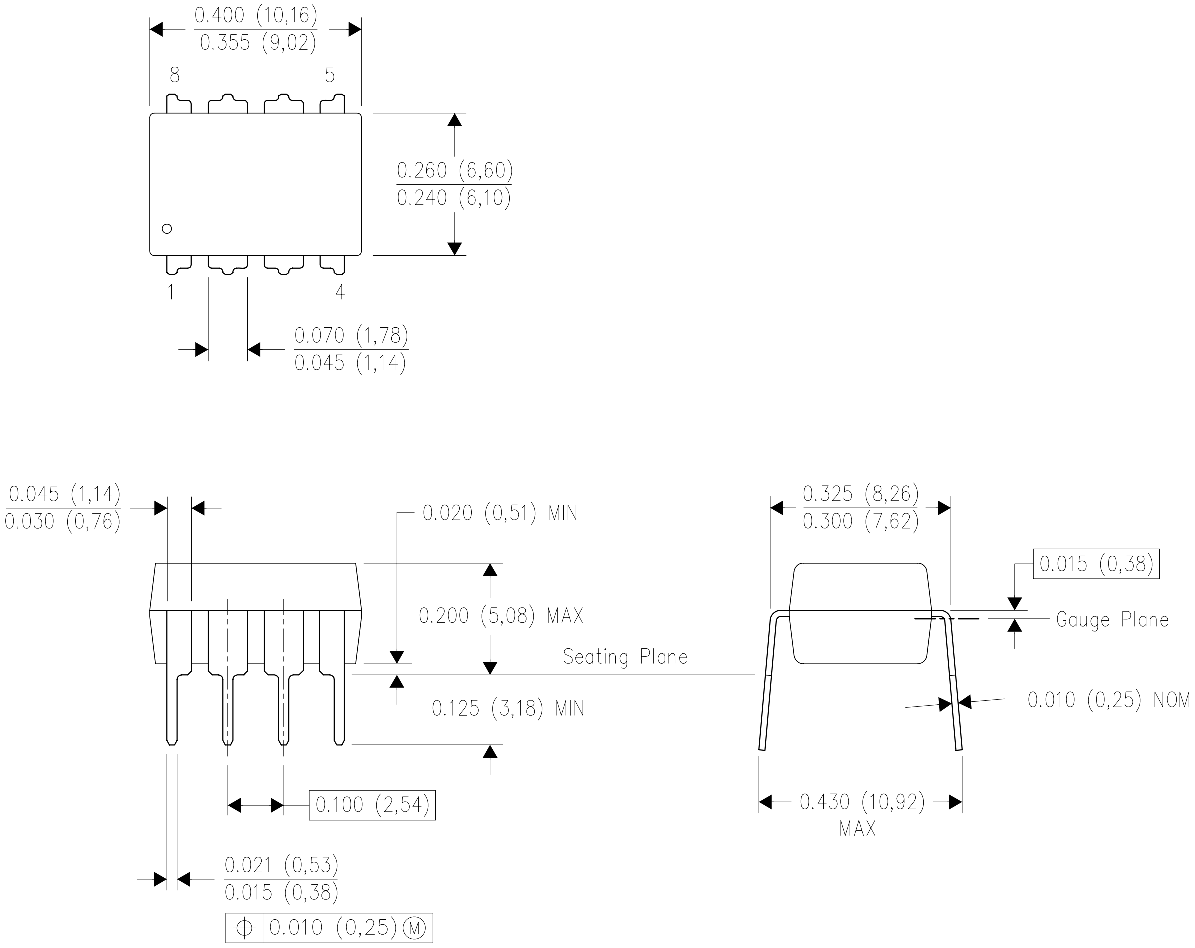
PS (R-PDSO-G8) PLASTIC SMALL OUTLINE



4212188/A 09/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

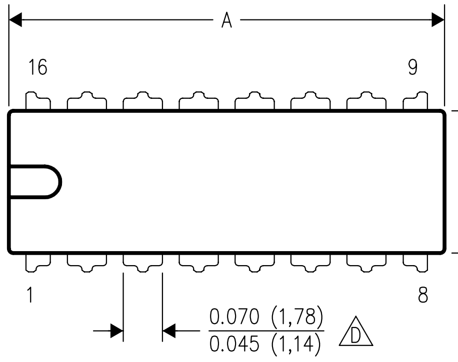


4040082/E 04/2010

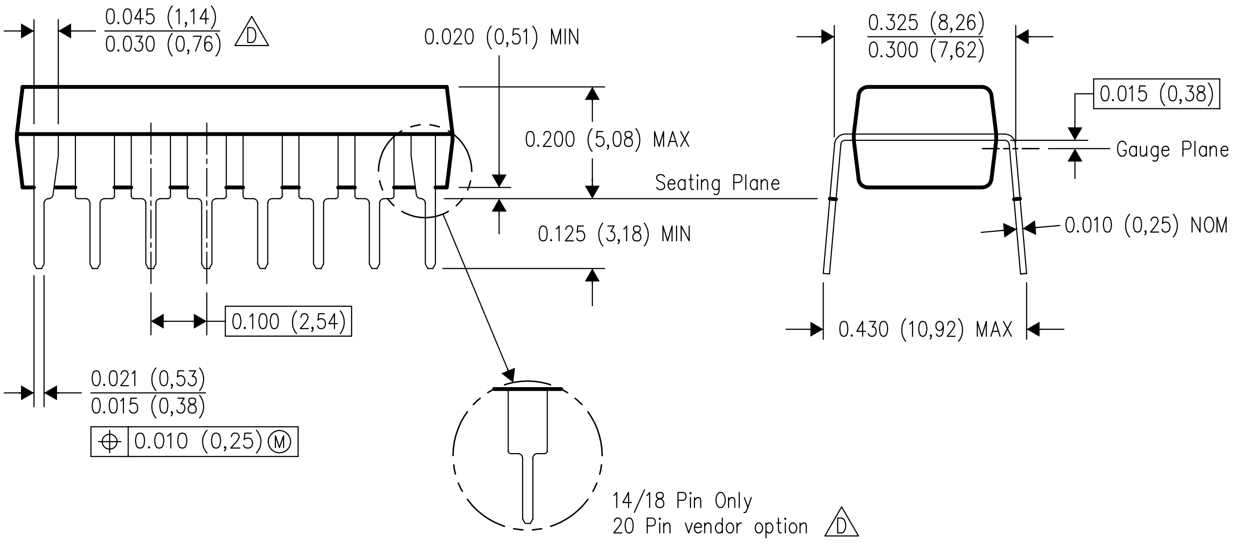
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



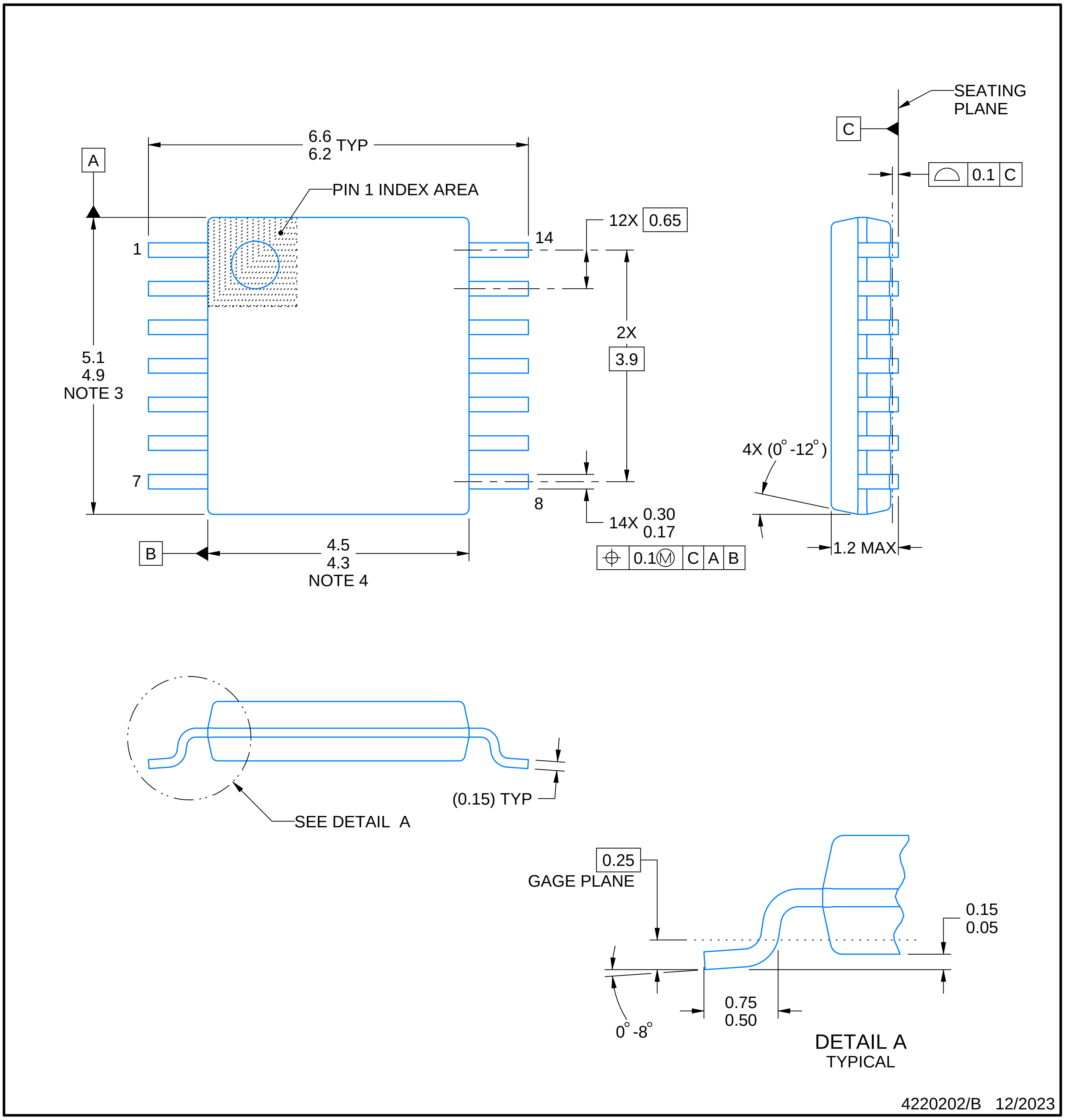
4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

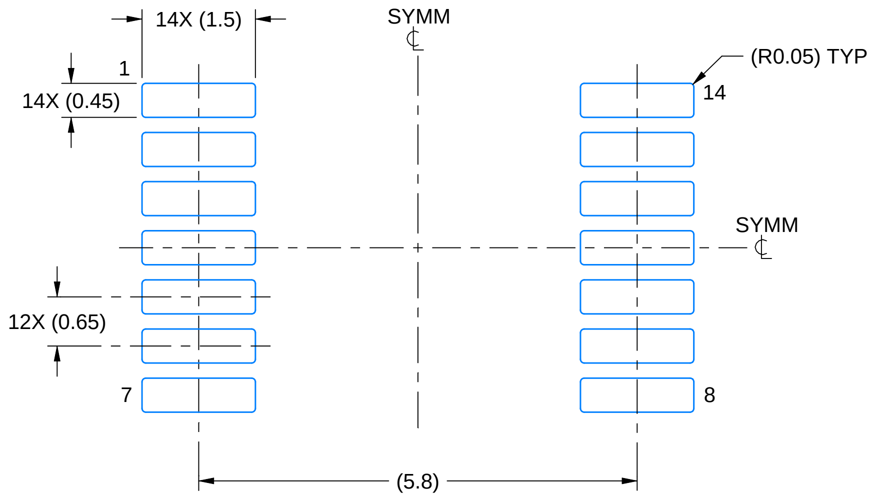
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

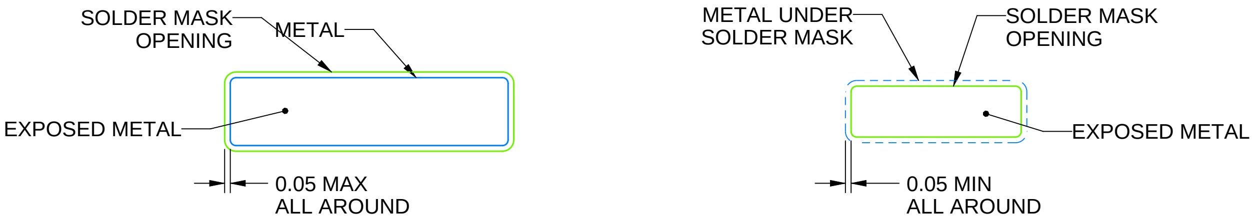


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



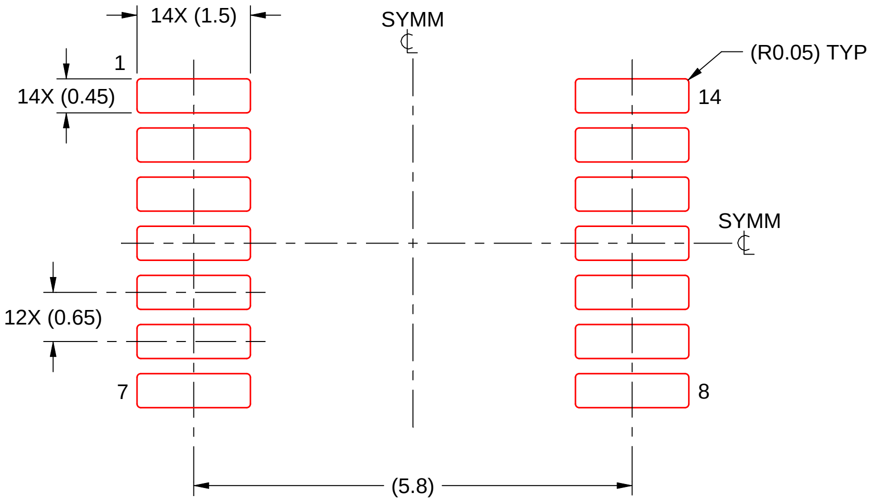
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

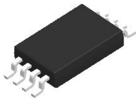
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

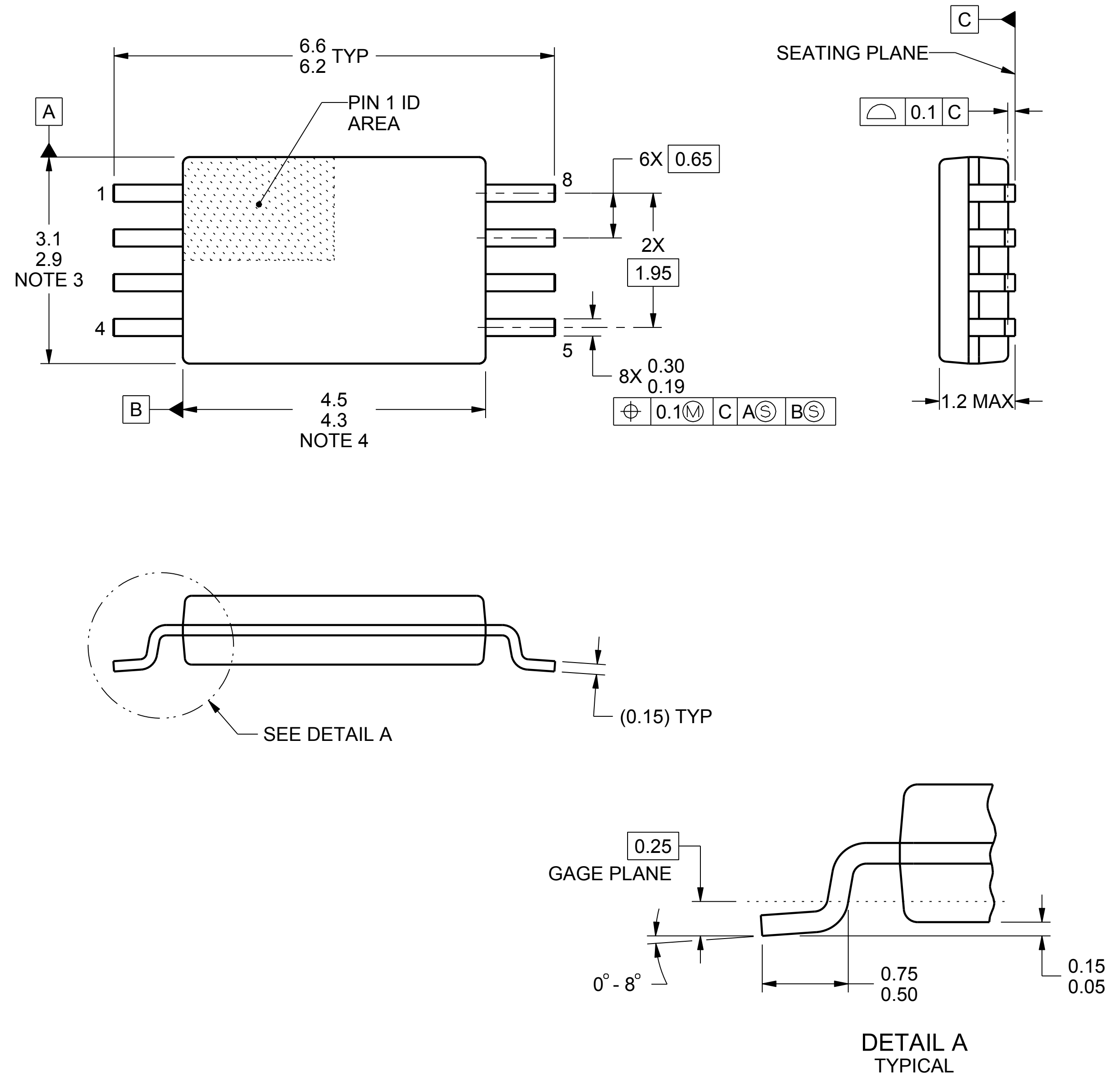


PACKAGE OUTLINE

PW0008A

TSSOP - 1.2 mm max height

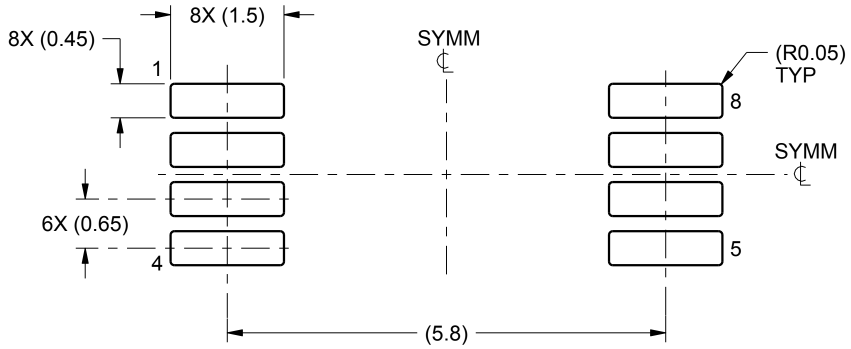
SMALL OUTLINE PACKAGE



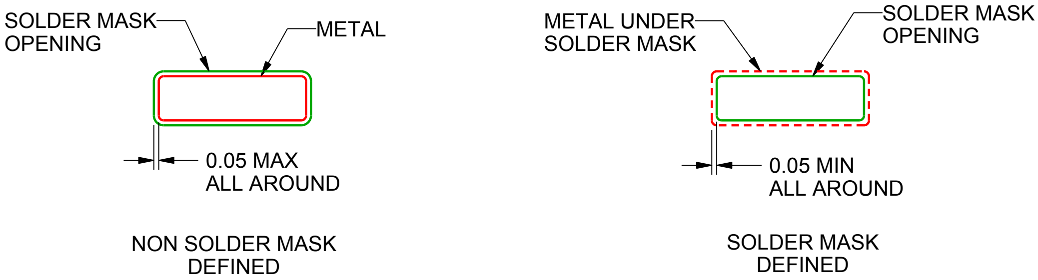
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

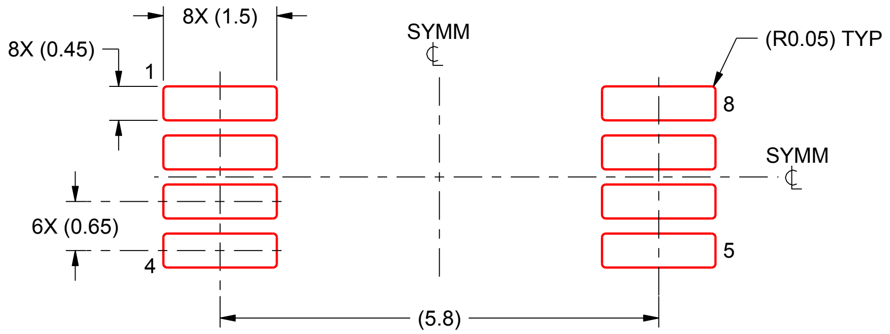


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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