TIOL221 Dual Channel IO-Link Device PHY with Integrated LDO and SPI Interface

1 Features

- 7V to 36V supply voltage
- IO-link configurable CQ output with auxiliary digital output (DO) and digital input (DI) channels
- Configurable via pin-control or SPI interface
- Both CQ and DO channels configurable for use in IO-link master modules
- PNP, NPN or IO-Link configurable CQ output
  - IEC 61131-9 COM1, COM2 and COM3 Data Rate Support
- Output drivers with low power dissipation and high configurability
  - Low R_{DSON} 2.5Ω (typical)
  - Active driver current limiting capability
  - Configurable driver overcurrent limit: 50mA to 500mA
  - Active reverse polarity protection of up to 65V on LP, CQ, DO and DI
  - Safe and fast demagnetization of inductive loads
- Integrated protection features for robust systems
  - Fault indicator for overcurrent, overtemperature and UVLO faults
  - Extended ambient temperature operation: –40°C to 125°C
  - ±8kV IEC 61000-4-2 ESD contact discharge
  - ±4kV IEC 61000-4-4 electrical fast transient
  - ±1.2kV, 500Ω IEC 61000-4-5 surge
- Large capacitive and inductive load driving capability
- Integrated LDO provides up to 20mA current
- Optional external regulator input (5V) to reduce internal power dissipation in the LDO
- Small space-saving package options
  - 4mm x 4mm VQFN package
  - 2.7mm x 2.7mm DSBGA package

2 Applications

- Field Transmitters and actuators
- Factory automation
- Process automation
- IO-link PHY in remote IO

3 Description

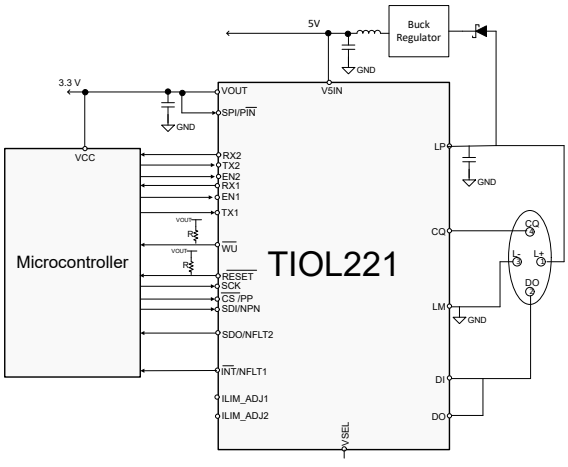
The TIOL221 transceiver integrates dual low-power output drivers with active reverse polarity protection. When the device is connected to an IO-Link controller through a three-wire interface, the controller can initiate communication, and exchange data with the remote node while the TIOL221 acts as a complete physical layer for the communication. The device also integrates an auxiliary DI channel.

The device is capable of withstanding up to 1.2kV (500Ω) of IEC 61000-4-5 surge and features integrated reverse polarity protection. In addition to the SPI interface for configurability and expanded diagnostic capability, a simple pin-programmable interface allows easy interfacing with the controller circuits. The output current limit can be configured using either an external resistor or per-configured limits via SPI interface. TIOL221 can be configured to generate wake-up pulse, and be used in IO-link controller applications. Fault reporting and internal protection functions are provided for undervoltage, overcurrent and overtemperature conditions.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TIOL221	VQFN (24)	4mm x 4mm
	DSBGA (25) (3)	2.7mm x 2.7mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product Preview



Typical Application Diagram

Table of Contents

4 Pin Configuration and Functions

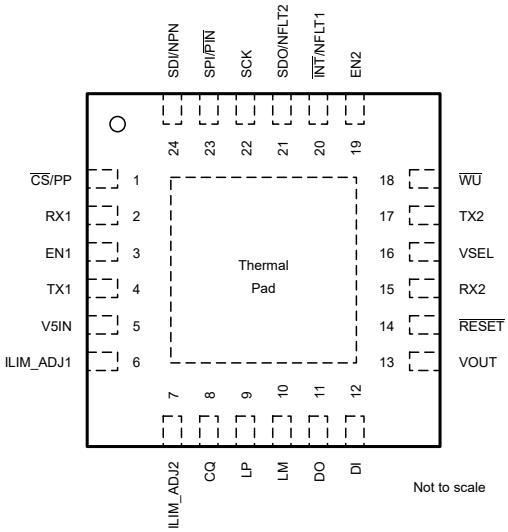


Figure 4-1. RGE (VQFN), 24-Pin (Top View)

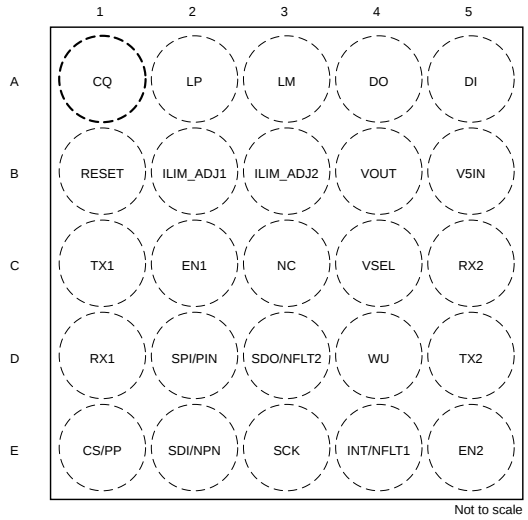


Figure 4-2. YAH (DSBGA), 25-Pin (Top View, Bumps Down)

Table 4-1. Pin Functions

PIN NAME	PIN NUMBER		I/O	TYPE	DESCRIPTION
	VQFN	DSBGA			
CQ	8	A1	I/O	High Voltage	IO-link signal data pin.
$\overline{CS}$/PP	1	E1	I	Digital	Chip select input pin in the SPI-mode. Push-pull mode selection input in pin-mode
DI	12	A5	I	High Voltage	DI receiver Input. DI receiver output can be monitored at the RX2 pin.
DO	11	A4	O	High Voltage	DO driver output. DO is the inverse logic level of the input at the TX2 pin.
EN1	3	C2	I	Low voltage Digital	CQ driver enable input signal from the local controller. Logic low sets the CQ output at Hi-Z. Weak internal pull-down.
EN2	19	E5	I	Low voltage Digital	DO driver enable input signal from the local controller. Logic low sets the DO output at Hi-Z. Weak internal pull-down.
ILIM_ADJ1	6	B2	I	Low voltage Analog	Input for the current limit adjustment for the CQ driver. Connect resistor RSET1 between ILIM_ADJ1 and LM.
ILIM_ADJ2	7	B3	I	Low voltage Analog	Input for the current limit adjustment for the DO driver. Connect resistor RSET2 between ILIM_ADJ2 and LM.
$\overline{INT}$/NFLT1	20	E4	O	Low voltage Digital	Interrupt output, push-pull (SPI-mode) or fault indicator for CQ channel, open-drain (pin-mode)
LM	10	A3	G	Ground	Ground.
LP	9	A2	PI	High Voltage	Power supply input (24V typical) to the device. Connect 1µF capacitor to LM (ground) as close to the device as possible.
NC	--	C3	NC	No Connect	Not connected internally.
RX1	2	D1	O	Low voltage Digital	C/Q Receiver Logic Output. RX2 is the inverse logic level of the signal on the CQ input.
RX2	15	C5	O	Low voltage Digital	DI Receiver Logic Output. RX2 is the inverse logic level of the signal on the DI input.
SCK	22	E3	I	Low voltage Digital	SPI clock input
SDI/NPN	24	E2	I	Low voltage Digital	SPI serial data input (SPI-mode) Or NPN mode selector (pin-mode)
SDO/NFLT2	21	D3	O	Low voltage Digital	SPI serial data output, push-pull (SPI-mode) or fault inductor for DO channel, open-drain (pin-mode)

Table 4-1. Pin Functions (continued)

PIN NAME	PIN NUMBER		I/O	TYPE	DESCRIPTION
	VQFN	DSBGA			
SPI/$\overline{\text{PIN}}$	23	D2	I	Low voltage Digital	SPI or pin-mode selection input. Drive this pin low for pin-mode operation. Drive this pin high for SPI-mode control.
TX1	4	C1	I	Low voltage Digital	CQ driver input data from local microcontroller. Weak internal pull-up.
TX2	17	D5	I	Low voltage Digital	DO driver input data from local microcontroller. Weak internal pull-up.
VOUT	13	B4	PO	Low voltage	LDO regulator output. Output level determined by VSEL pin
VSEL	16	C4	I	Low voltage	• Connect to GND for 3.3V LDO output with LP as the LDO input supply • Connect to VOUT for 5V LDO output with LP as the LDO input supply • Leave the pin floating for 3.3V LDO output with V5IN as the LDO input supply
$\overline{\text{RESET}}$	14	B1	O	Low voltage	Reset output pin, open-drain, active low. The pin behaves as a reset pin to indicate UV on LP or VOUT.
V5IN	5	B5	PI	Low voltage	(Optional) Connect this pin 5V supply input from external regulator to reduce the power dissipation from the internal regulator. Leave the pin floating if unused.
$\overline{\text{WU}}$	18	D4	O	Low voltage Digital	Wake-up indicator to the local microcontroller. Open-drain output, connect this pin via pull-up resistor to VOUT.
Thermal Pad	Thermal Pad	N/A	G	Ground	Connect the exposed thermal pad to ground (LM) for optimal thermal and electrical performance

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
LP, CQ, DO, DI	Steady state voltage for LP, CQ, DO and DI	–65	65	V
	Transient pulse width < 100 µs for LP, CQ, DO and DI	–70	70	V
$\lvert V_{(LP)} - V_{(CQ)}\rvert$, $\lvert V_{(LP)} - V_{(DO)}\rvert$, $\lvert V_{(LP)} - V_{(DI)}\rvert$, $\lvert V_{(CQ)} - V_{(DO)}\rvert$, $\lvert V_{(CQ)} - V_{(DI)}\rvert$, $\lvert V_{(DO)} - V_{(DI)}\rvert$	Voltage drop between bus pins		65	V
V_{OUT}	Regulator output voltage	–0.3	6	V
TX1, TX2, EN1, EN2, VSEL, RX1, RX2, $\overline{CS}$/PP, SDI/NPN, SDO/NFLT2, SCK, $\overline{INT}$/NFLT1, $\overline{WU}$, ILIM_ADJ1, ILIM_ADJ2, SPI/$\overline{PIN}$	Logic pin voltage	–0.3	min(V_{OUT}+0.3, 6)	V
Output current	RX1, RX2, $\overline{WU}$, $\overline{INT}$/NFLT1, SDO/NFLT2,	–5	5	mA
Storage temperature, T_{stg}		-55	170	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute maximum ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime. All voltages are with reference to the L- pin, unless otherwise specified.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±4000	V
$V_{(ESD)}$	Electrostatic discharge	Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	All pins	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), LP, CQ, DO, DI and LM (1) (2)	±8,000	V
	Electrostatic discharge	IEC 61000-4-5, 1.2 µs/50 µs Surge with 500 Ω in series, LP, CQ, DO, DI and LM (1)	±1,200	
	Electrostatic discharge	IEC 61000-4-4 EFT (Fast transient or burst), LP, CQ, DO, DI and LM (1)	±4,000	

(1) Minimum 100-nF capacitor is required between LP and LM. Minimum 1-µF capacitor is required between VOUT and LM.
(2) Device requires a minimum 1nF capacitor between the CQ/DO driver output and LM to pass ±8000 V. Passing level is ±4000 V without the minimum 1nF capacitor

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(LP)}$	24V Input Supply Voltage		7	24	36	V
$V_{(V5IN)}$	5V Input Supply Voltage	5V Input Supply Voltage	4.5	5	5.5	V
$V_{(I)}$	Logic level input voltage at TX1, TX2, EN1, EN2,$\overline{CS}$/PP, SDI/NPN, SCK, SPI/$\overline{PIN}$	3.3 V configuration	3	3.3	3.6	
		5 V configuration	4.5	5	5.5	V
$1/t_{BIT}$	Data rate (Communication mode)				250	kbps
$I_{(VOUT)}$	LDO output current				20	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Junction temperature		-40		150	°C

5.5 Thermal Information

THERMAL METRIC(1)		TIOL221		UNIT
		RGE (24 Pins)	YAH (25 Pins)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	58.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.2	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.4	14.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.4	14.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at LP = 24 V, V_{VOUT} = 3.3 V and T_A = 25 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (LP)							
$I_{(LP-SHDN)}$	Supply quiescent current in shutdown mode	CQ TX and RX, DO and DI are disabled. No load on VOUT. SPI mode only			1.2	2.1	mA
$I_{(LP-RX-ONLY)}$	Supply current when only inputs are enabled	CQ and DO are disabled. CQ RX and DI are enabled. No load on VOUT. R_{SETx} >= 10kΩ (current limit < 500mA) , EN1=EN2=L	CQ and DO are disabled. CQ RX and DI are enabled. No load on VOUT		1.4	2.5	mA
$I_{(LP-CQ-DO)}$	Quiescent supply current when both CQ and DO are enabled. V5IN supplied externally	R_{SETx} >= 10kΩ. TX1=TX2=H, No load on CQ or DO, Push-pull or NPN mode only			4.5	5.5	mA
$I_{(LP-CQ-DO)}$		R_{SETx} >= 10kΩ. TX1=TX2=L, No load on CQ or DO			3.6	4.5	mA
$V_{(LP-UVLO)}$	LP under voltage lockout	LP falling; UVLO indicated by $\overline{RESET}$ pin going low		6	6.3		V
$V_{(LP-UVLO)}$	LP under voltage lockout	LP rising; UVLO recovery indicated on $\overline{RESET}$ pin going high			6.5	6.8	V
$V_{(LP-UVLO,HYS)}$	LP under voltage hysteresis	Rising to falling threshold		150	250		mV
$V_{(LPW)}$	LP undervoltage warning	LP falling		14	16	18	V
$V_{(LPW-HYS)}$	LP undervoltage warning hysteresis				530		mV
V5IN							
V5IN(UVLO, F)	Falling UVLO level for V5IN	V5IN Falling		3.4	3.5	3.6	V
V5IN(UVLO, R)	Rising UVLO level for V5IN	V5IN Rising		3.7	3.8	4.0	V
V5IN(UVLO, HYS)	V5IN UVLO hysteresis				0.3		V
I5_IN	Input supply current at 5VIN	CQ and DO disabled, No load on VOUT			0.15	1	mA
LINEAR REGULATOR (VOUT)							
$V_{(VOUT)}$	Voltage regulator output	VOUT set to 5 V		4.75	5	5.25	V
		VOUT set to 3.3 V		3.13	3.3	3.46	V
$LINEREG_{VOUT}$	Line regulation ($dV_{(VOUT)}/dV(LP)$)	$I_{(VCC\_OUT)}$ = 1 mA $V_{(LP)}$ = 7 V to 36 V (VOUT = 5 V) $V_{(LP)}$ = 7 V to 36 V OR V5IN = 4.5 to 5.5 V (VOUT = 3.3 V)				1.7	mV/V
$LOADREG_{VOUT}$	Load regulation ($dV_{(VOUT)}/V_{(OUT)}$)	$V_{(LP)}$ = 24 V for VOUT=5V $V_{(LP)}$ = 24 V or V5IN= 5V for VOUT=3.3 V $I_{(VCC\_OUT)}$ = 100 µA to 20 mA				1	%
UV_{VOUT5F}	Falling UV threshold on VOUT (5V setting)	VSEL connected to VOUT, VOUT falling		3.4	3.6	3.8	V
UV_{VOUT5R}	Rising UV threshold on VOUT (5V setting)	VSEL connected to VOUT, VOUT rising		3.6	3.8	4.0	V

5.6 Electrical Characteristics (continued)

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at LP = 24 V, V_{VOUT} = 3.3 V and T_A = 25 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
UV_{VOUT3F}	Falling UV threshold on VOUT (3.3V setting)	VSEL connected to GND or Floating(V5IN supplied), VOUT falling		2.5	2.7	2.9	V
UV_{VOUT3R}	Rising UV threshold on VOUT (3.3V setting)	VSEL connected to GND or Floating(V5IN supplied), VOUT rising		2.6	2.8	3.0	V
PSSR	Power Supply Rejection Ratio	100 kHz, $I_{(VCC\_OUT)}$ = 20 mA			40		dB
DRIVER OUTPUT (CQ, DO)							
$R_{DSON-HS}$	High-side driver on-resistance	I_{LOAD} = 200 mA, Current Limit = 300 mA			2.5	4.5	Ω
$R_{DSON-LS}$	Low-side driver on-resistance	I_{LOAD} = 200 mA, Current Limit = 300 mA			2.5	4.5	Ω
$I_{O(LIM)}$	Driver output current limit	SPI/$\overline{PIN}$ = LOW $V_{(DRIVER)}$= (V_{LP} - 3) V or 3V,	R_{SETx} = 110 kΩ	35	55	70	mA
			R_{SETx} = 10 kΩ	300	350	400	mA
			R_{SETx} = 0 to 5 kΩ	500			mA
			R_{SETx} = OPEN	260	330	415	mA
$I_{O(LIM)}$	Driver output current limit	SPI/$\overline{PIN}$ = HIGH, $V_{(DRIVER)}$= (V_{LP} - 3) V or 3V,	3h[7:6]= 0h	35	60	75	mA
			3h[7:6]= 1h	50	75	95	mA
			3h[7:6]= 2h	100	140	175	mA
			3h[7:6]= 3h	150	190	260	mA
			3h[7:6]= 4h	200	230	330	mA
			3h[7:6] = 5h	250	290	410	mA
			3h[7:6] = 6h	300	350	485	mA
			3h[7:6]= 7h	500	700		mA
$I_{OZ(CQ)}$	CQ leakage	EN1 = LOW, 0 ≤ $V_{(CQ)}$ ≤ ($V_{(LP)}$ - 0.1 V)		–2		2	µA
$I_{LLM(CQ)}$	CQ load discharge current	EN1 = LOW, R_{SET1} = 0 to 5 kΩ (1), $V_{(CQ)}$ >= 5 V		5	8.5	15	mA
$I_{LLM(DO)}$	DO load discharge current	EN2 = LOW, R_{SET2} = 0 to 5 kΩ; $V_{(DO)}$ >= 5 V		5	8.5	15	mA
I_{PU-DO}	DO driver weak pull-up current	SPI/$\overline{PIN}$=HIGH, EN2=LOW, TX2=HIGH, RSET2: 10 kΩ to 110 kΩ AND Weak pull-up enabled (SPI mode only)	0 ≤ V(DO) ≤ (V(LP) - 2 V)	40	50	80	µA
I_{PD-DO}	DO driver weak pull-down current	(SPI/$\overline{PIN}$=HIGH, EN2=LOW, TX2=LOW, RSET2: 10 kΩ to 110 kΩ AND Weak pull-up enabled (SPI mode only)	2 ≤ V(DO) ≤ V(LP)	40	50	80	µA
I_{PU-CQ}	CQ driver weak pull-up current	Driver disabled, Weak pull-up enabled (SPI mode)	0 ≤ V(CQ) ≤ (V(LP) - 2 V)	40	50	80	µA
I_{PD-CQ}	CQ driver weak pull-down current	Driver disabled, Weak pull-down enabled (SPI mode)	2 ≤ V(CQ) ≤ V(LP)	40	50	80	µA
RECEIVER INPUT (CQ, DI)							
$V_{(THH)}$	Input threshold “H”	$V_{(LP)}$ > 18 V, EN= LOW		10.5		13	V
$V_{(THL)}$	Input threshold “L"			8		11.5	V
$V_{(HYS)}$	Receiver Hysteresis ($V_{(THH)}$ - $V_{(THL)}$)				0.75		V
$V_{(THH)}$	Input threshold “H”	$V_{(LP)}$ < 18 V, EN= LOW		See Note (2)		See Note (3)	V
$V_{(THL)}$	Input threshold “L"	$V_{(LP)}$ < 18 V, EN= LOW		See Note (4)		See Note (5)	V
$V_{(HYS)}$	Receiver Hysteresis ($V_{(THH)}$ - $V_{(THL)}$)				0.75		V
C_{IN-CQ}	CQ input capacitance	CQ driver disabled, weak pull-up/ pull-down disabled, f =100kHz			150		pF
C_{IN-DI}	DI input capacitance	f =100kHz			100		pF

5.6 Electrical Characteristics (continued)

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at LP = 24 V, V_{VOUT} = 3.3 V and T_A = 25 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{PU-DI}	DI weak pull-up current	SPI Mode, Weak pull-up enabled on DI pin	0 ≤ V(DI) ≤ (V(LP) - 2 V)	40	50	80	µA
I_{PD-DI}	DI weak pull-down current	SPI Mode, Weak pull-down enabled on DI pin	2 ≤ V(DI) ≤ V(LP)	40	50	80	µA
LOGIC-LEVEL INPUTS ($\overline{CS}$/PP, SCK, SDI/NPN, SPI/$\overline{PIN}$, EN1, EN2, TX1, TX2, VSEL)							
V_{IL}	Input logic low voltage					0.3*VOUT	V
V_{IH}	Input logic high voltage			0.7*VOUT			V
R_{PD}	Pull-down resistance at EN1, EN2, SDI/NPN, SCK				100		kΩ
R_{PU}	Pull-up resistance at TX1, TX2, , $\overline{CS}$/PP, SPI/$\overline{PIN}$				100		kΩ
R_{PU}	Pull-up resistance at VSEL				500		kΩ
LOGIC-LEVEL OUTPUTS ($\overline{WU}$, SDO/NFLT2, $\overline{INT}$/NFLT1, RX1, RX2, $\overline{RESET}$)							
V_{OH}	Output logic high voltage RX1, RX2, SDO, $\overline{INT}$	I_O = 4 mA	I_O = 4 mA	VOUT-0.5			V
V_{OL}	Output logic low voltage	I_O = 4 mA				0.4	V
I_{OZ}	Output high impedance leakage at NFLT1, NFLT2, $\overline{WU}$, $\overline{RESET}$	Output in Hi-Z, V_O = 0 V or VCC_IN/OUT		–1		1	µA
PROTECTION CIRCUITS							
$T_{(WRN)}$	Thermal warning	Die temperature T_J		125			°C
$T_{(SDN)}$	Thermal shutdown			150	160		°C
$T_{(HYS)}$	Thermal hysteresis for shutdown				14		°C
$T_{(WRN)}$	Thermal hysteresis for warning	Die temperature T_J	Die temperature T_J		14		°C
I_{REV}	CQ, DO, DI Leakage current in reverse polarity (Drivers disabled)	EN1/2=LOW, TX1/2=x; LP= 24 V $V_{(CQ/ DO/ DI)}$ = ($V_{(LP)}$ -36V) OR $V_{(CQ/ DO/ DI)}$ = ($V_{(LP)}$ +36V)				60	µA
		EN1/2=LOW, TX1/2=x; LP= 24 V $V_{(CQ/ DO/DI)}$ = ($V_{(LP)}$ -65V) OR $V_{(CQ/ DO/ DI)}$ = 65V				110	µA
	CQ, DO (Drivers enabled)	EN1/2 = HIGH, TX1/2 = LOW; $V_{(CQ/DO\ to\ LP)}$ = 3 V, R_{SET} >= 10 kΩ				650	µA
		EN1/2 = HIGH, TX1/2 = HIGH; $V_{(CQ/DO\ to\ LM)}$ = -3 V				10	µA

(1) Current fault indication and current fault auto recovery will be de-activated.
(2) V_{THH} (min) = 5 V + (11/18) [$V_{(LP)}$ - 8 V]
(3) V_{THH} (max) = 6.5 V + (13/18) [$V_{(LP)}$ - 8 V]
(4) V_{THL} (min) = 4 V + (8/18) [$V_{(LP)}$ -8 V]
(5) V_{THL} (max) = 6 V + (11/18) [$V_{(LP)}$ -8 V]

5.7 Switching Characteristics

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at LP = 24 V, V_{VOUT} = 3.3 V and T_A = 25 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CQ, DO DRIVER								
t_{PLH}	Driver propagation delay, low-to-high transition	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R_L = 2 kΩ C_L = 5 nF Push-pull and PNP configuration R_{SET} = 10 kΩ				600	1200	ns
t_{PHL}	Driver propagation delay, high-to-low transition	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R_L = 2 kΩ C_L = 5 nF Push-pull and NPN configuration R_{SET} = 10 kΩ				600	1200	ns
$t_{P(skew)}$	Driver propagation delay skew. $\lvert t_{PLH} - t_{PHL} \rvert$	See Test Circuit for Driver Output Measurements See Driver Output Switching Waveforms R_L = 2 kΩ C_L = 5 nF Push-pull configuration R_{SET} = 10 kΩ				120		ns
t_{PZH}	Driver enable delay high	See Test Circuit for Driver Output Measurements and Driver Enable/Disable Timing Diagrams R_L = 2 kΩ C_L = 5 nF Push-pull and PNP configuration only R_{SET} = 10 kΩ					4	µs
t_{PZL}	Driver enable delay low	See Test Circuit for Driver Output Measurements and Driver Enable/Disable Timing Diagrams R_L = 2 kΩ C_L = 5 nF Push-pull and NPN configuration only R_{SET} = 10 kΩ					4	µs
t_{PHZ}	Driver disable delay high	See Test Circuit for Driver Output Measurements and Driver Enable/Disable Timing Diagrams R_L = 2 kΩ C_L = 5 nF Push-pull and PNP configuration only R_{SET} = 10 kΩ					4	µs
t_{PLZ}	Driver disable delay low	See Test Circuit for Driver Output Measurements and Driver Enable/Disable Timing Diagrams R_L = 2 kΩ C_L = 5 nF Push-pull and NPN configuration only R_{SET} = 10 kΩ					4	µs
t_r	Driver output rise time	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R_L = 2 kΩ C_L = 5 nF Push-pull and PNP configuration R_{SET} = 10 kΩ			200	530	900	ns
t_f	Driver output fall time	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R_L = 2 kΩ C_L = 5 nF Push-pull and NPN configuration R_{SET} = 10 kΩ			200	480	900	ns

5.7 Switching Characteristics (continued)

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at LP = 24 V, V_{VOUT} = 3.3 V and T_A = 25 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert t_r - t_f \rvert$	Difference in rise and fall time	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R_L = 2 kΩ C_L = 5 nF Push-pull configuration only R_{SET} = 10 kΩ				60		ns
t_{WU1}	Wake-up recognition begin	See Wake-up recognition timing diagram			45	60	75	µs
t_{WU2}	Wake-up recognition end				85	100	145	µs
t_{pWAKE}	Wake-up output delay						150	µs
t_{WUL}	Wake output pulse duration on wake detection				175	225	285	µs
t_{SC}	Current fault blanking time	See Wake-up recognition timing diagram	(SPI/$\overline{PIN}$ = low and 10 kΩ <= RSETx <= 110 kΩ) OR SPI/$\overline{PIN}$=high and CQ_BL_TIME[1:0]=00b (CQ) OR DO_BL_TIME[1:0]=00b (DO)		0.175	0.2		ms
			SPI/$\overline{PIN}$=high and CQ_BL_TIME[1:0]=01b (CQ) OR DO_BL_TIME[1:0]=01b (DO)		0.25	0.5		ms
			SPI/$\overline{PIN}$=high and CQ_BL_TIME[1:0]=10b (CQ) OR DO_BL_TIME[1:0]=10b (DO)			5		ms
			(SPI/$\overline{PIN}$ = low and ILIM_ADJ floating) OR SPI/$\overline{PIN}$=high and CQ_BL_TIME[1:0]=11b (CQ) OR DO_BL_TIME[1:0]=11b (DO)		0.5	2	4	µs
t_{AR}	Auto retry time after current fault	Auto retry time after current fault	SPI/$\overline{PIN}$ = L OR SPI/$\overline{PIN}$=H and CQ_RETRY_TIME=00b			50		ms
			SPI/$\overline{PIN}$=H and CQ_RETRY_TIME=01b			100		ms
			SPI/$\overline{PIN}$=H and CQ_RETRY_TIME=10b			200		ms
			SPI/$\overline{PIN}$=H and CQ_RETRY_TIME=11b			500		ms
$t_{(UVLO)}$	CQ and DO re-enable delay after LP UVLO (1)	CQ and DO re-enable delay after UVLO (1)	SPI/$\overline{PIN}$ = L OR SPI/$\overline{PIN}$=H and T_UVLO=1b0		0.05	0.25	0.5	ms
$t_{(UVLO)}$	CQ and DO re-enable delay after LP UVLO (1)	CQ and DO re-enable delay after UVLO (1)	SPI/PIN = L OR SPI/PIN=H and T_UVLO=1b1		10	30	50	ms
CQ, DI RECEIVER								
t_{PLH_CQ}, t_{PHL_CQ}	CQ Receiver propagation delay	See Receiver Test Circuit Diagram and Receiver Timing Diagram C_L=15 pF	SPI/PIN=L OR SPI/PIN=H and CQ_RX_FILTER=1b0			0.2	0.36	µs
			SPI/PIN=H and CQ_RX_FILTER=1b1			1.15	1.6	µs
t_{PLH_DI}, t_{PHL_DI}	DI Receiver propagation delay		SPI/PIN=L OR SPI/PIN=H and DI_RX_FILTER=1b0			1	1.5	µs
			SPI/PIN=H and DI_RX_FILTER=1b1			1.8	2.7	µs
SPI Timing ($\overline{CS}$, SCK, SDI, SDO/CUR_OK2)								
t_{INT_TOG}	INT pin High/low time (when toggling)	C_{OUT}= 10 pF				100		µs

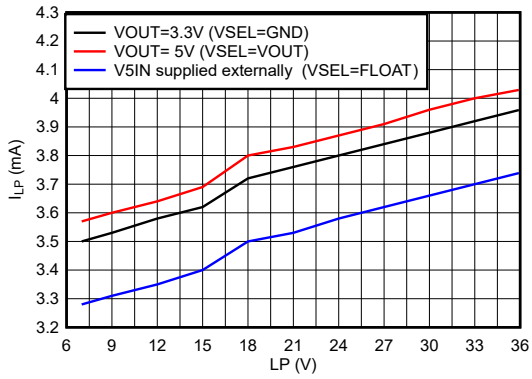
5.7 Switching Characteristics (continued)

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at LP = 24 V, V_{VOUT} = 3.3 V and T_A = 25 ℃ unless otherwise specified.

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCK_BURST}	Maximum SPI clock frequency	Burst mode					10	MHz
tSCK	SCK period				100			ns
t_{SCKH}	SCK pulse-width high				50			ns
t_{SCKL}	SCK pulse-width low				50			ns
f_{SCK}	Maximum SPI clock frequency	Non-burst mode					12.5	MHz
tSCK	SCK period				80			ns
t_{SCKH}	SCK pulse-width high				40			ns
t_{SCKL}	SCK pulse-width low				40			ns
t_{CSS}	$\overline{CS}$ falling edge to SCK rise time				20			ns
t_{CSH}	$\overline{SCK}$ rise to CS rise hold time				40			ns
t_{DH}	SDI hold time				10			ns
t_{DS}	SDI setup time						25	ns
t_{DO}	SDO data propagation delay	C_{OUT}= 10 pF					20	ns
t_{DORF}	SDO rise and fall time	C_{OUT}= 10 pF					20	ns
t_{CSPW}	Minimum $\overline{CS}$ pulse width (idle time between SPI transactions)				10			ns

(1) CQ/DO output remains Hi-Z for this time

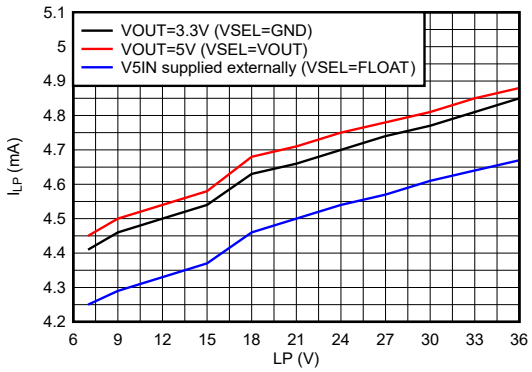
5.8 Typical Characteristics



CQ, DO enabled but no load, push-pull mode

RSETx = 10kΩ T_A = 25°C

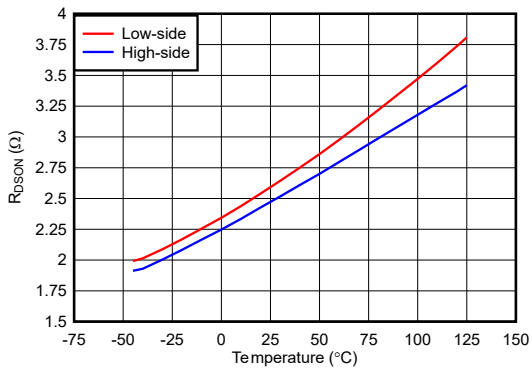
Figure 5-1. Supply Current vs Supply Voltage (TX1=TX2=GND)



CQ, DO enabled but no load, push-pull mode

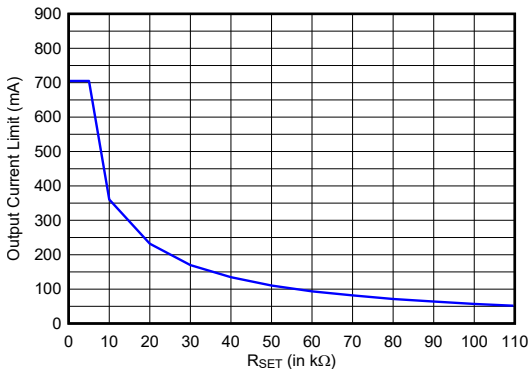
RSETx = 10kΩ T_A = 25°C

Figure 5-2. Supply Current vs Supply Voltage (TX1=TX2=VOUT)



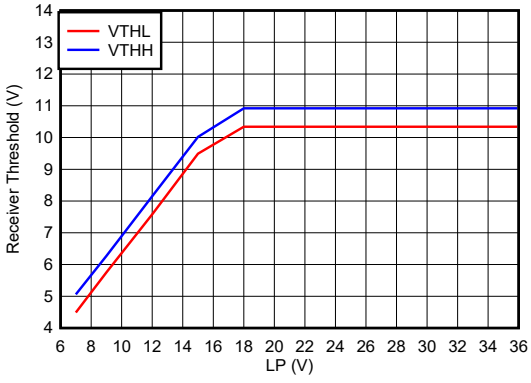
LP = 24V Load = 200mA R_{SETx} = 10kΩ

Figure 5-3. CQ, DO R_{DSON} vs. Temperature



LP = 24V T_A = 25°C

Figure 5-4. CQ, DO Current Limit vs R_{SETx} [1]



T_A = 25°C

Figure 5-5. CQ, DI Receiver Threshold Boundaries

[1] For R_{SET} in the 0-5kΩ range, TIOL221 can source/sink 500mA required for wake-up pulse generation in IO-link applications. For R_{SET} in the 0-5kΩ range, TIOL221 also activates a pull-down current source (I_{LLM}) when the driver is disabled.

6 Parameter Measurement Information

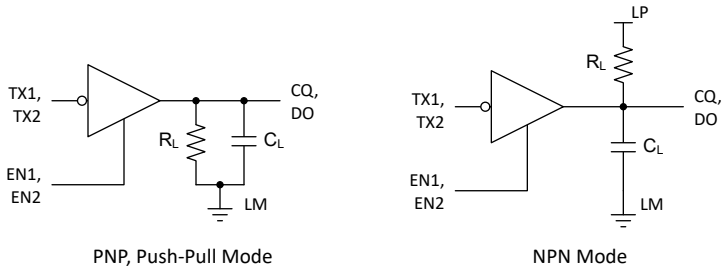


Figure 6-1. Test Circuit for Driver Switching

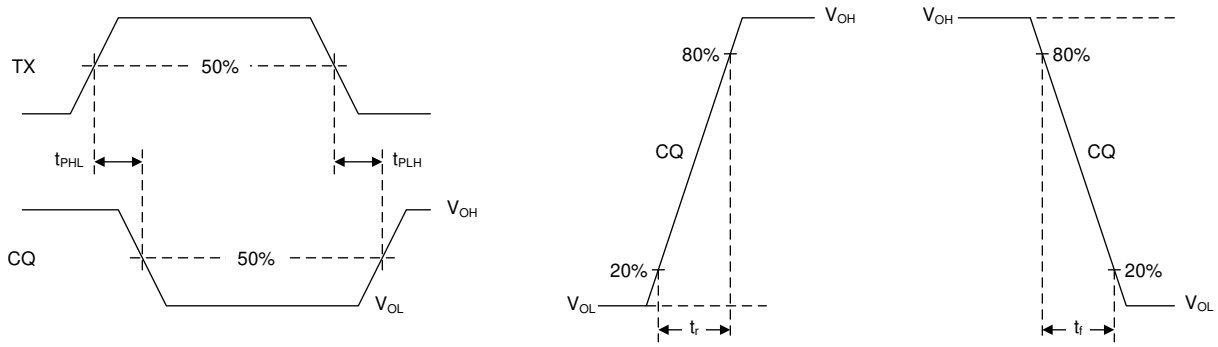


Figure 6-2. Waveforms for Driver Output Switching Measurements

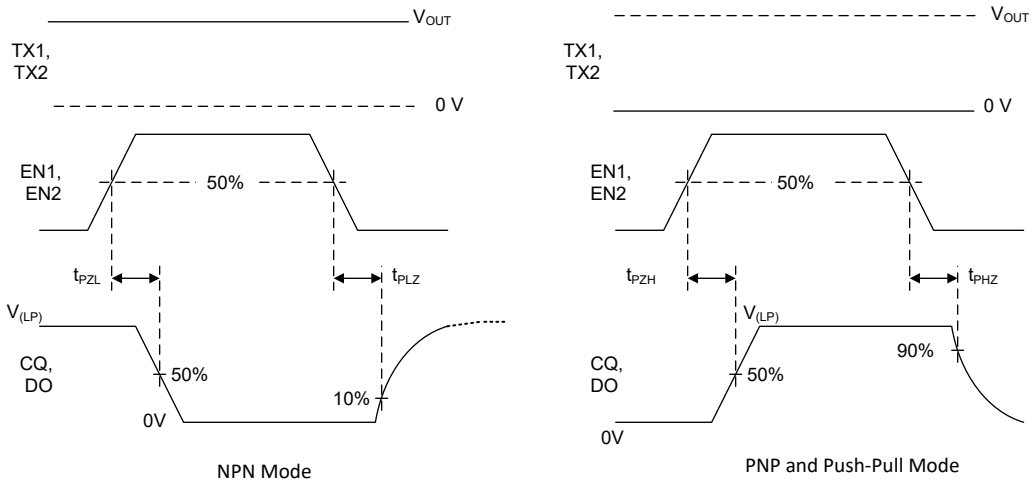


Figure 6-3. Waveforms for Driver Enable or Disable Time Measurements

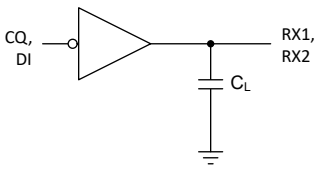


Figure 6-4. Test Circuit for Receiver Switching

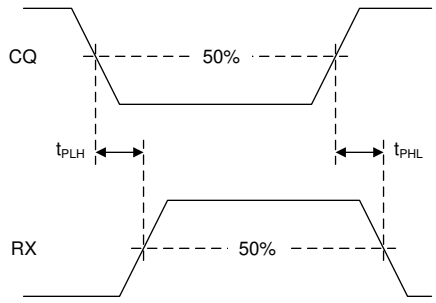
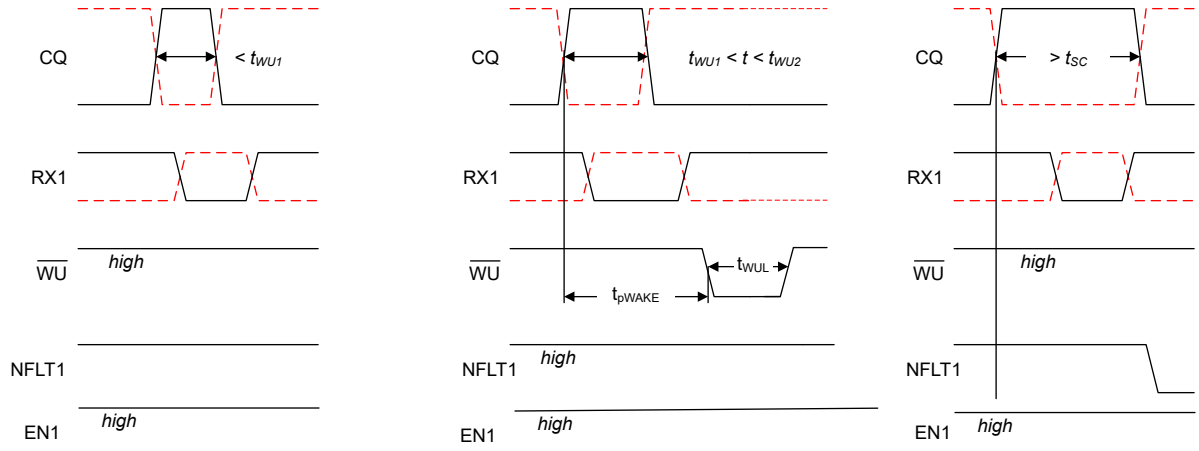
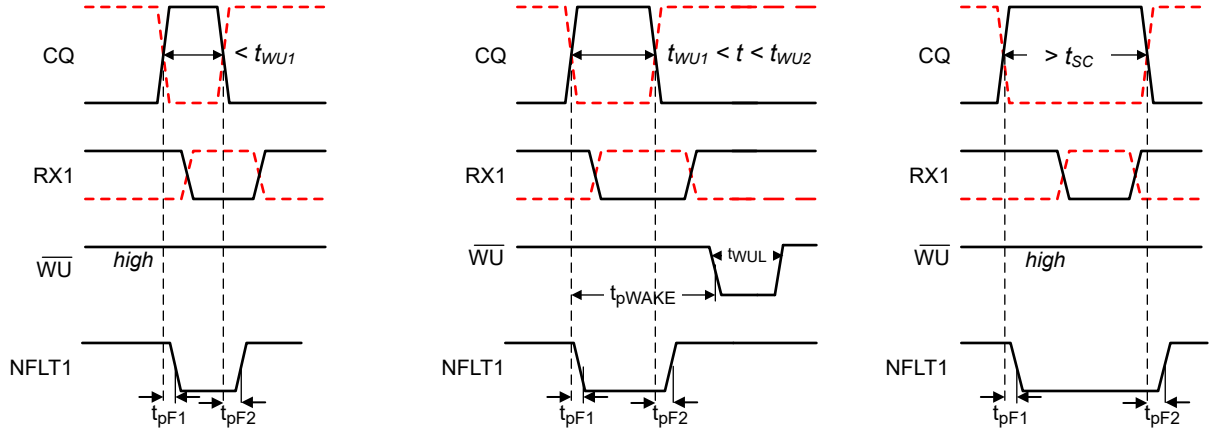


Figure 6-5. Receiver Switching Measurements



a) Over-current due to transient **b) Valid Wake-up pulse** **c) Over-current due to fault condition**

Figure 6-6. Overcurrent and Wake Conditions for EN = H and ILIM_ADJ = 10kΩ to 110kΩ, TX = H (Full Lines); and TX = L (Red Dotted Lines)



a) Over-current due to transient **b) Valid Wake-up pulse** **c) Over-current due to fault condition**

Figure 6-7. Overcurrent and Wake Conditions for EN = H and ILIM_ADJ is floating, TX = H (Full Lines); and TX = L (Red Dotted Lines)

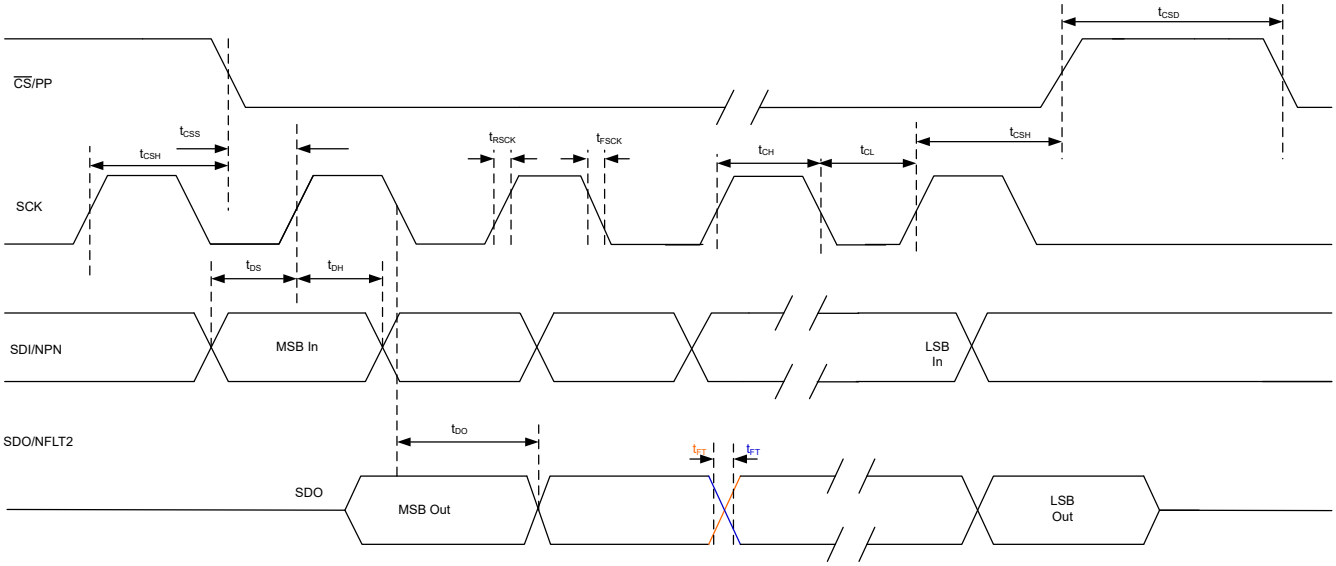


Figure 6-8. SPI Read/Write Timing Characteristics

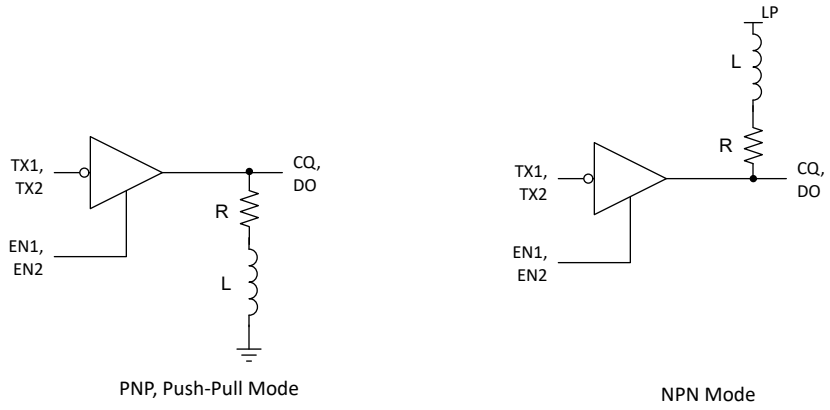


Figure 6-9. Driving the Inductive Load

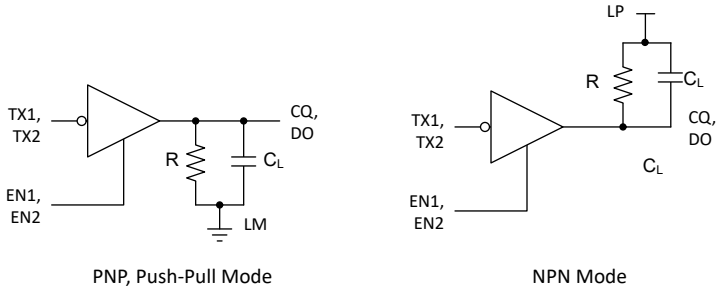


Figure 6-10. Driving the Capacitive Load

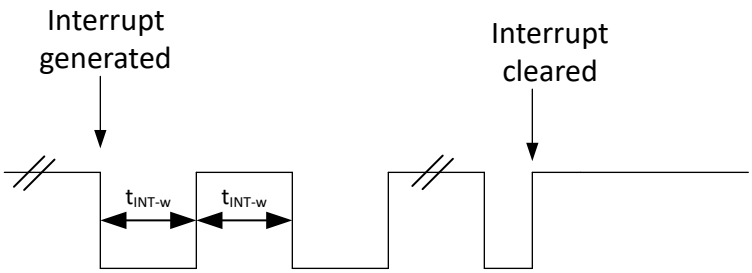


Figure 6-11. Interrupt Pin Toggling Behavior (SPI Mode; INT_TOG = 1b)

7 Detailed Description

7.1 Overview

Figure 7-1 shows the functional block diagram of TIOL221. The device has an IO-link compatible channel (CQ), a digital output driver (DO) and a digital input (DI) interface. The drivers at CQ and DO can be used in either push-pull, high-side driver (PNP), or low-side driver (NPN) configuration using the $\overline{CS}$/PP and SDI/NPN pins in the pin-mode or via the serial peripheral interface (SPI). The internal receiver on the CQ line converts the 24V signal to standard logic levels on the receiver data output pin, RX1. Similarly, internal receiver on the DI line converts the 24V signal to standard logic levels on the receiver data output pin, RX2. A simple parallel interface is used to receive/transmit data and status information between the device and the local controller.

The device can be configured by using the pins via pin mode (when SPI/$\overline{PIN}$ is tied low) or using the SPI interface (when SPI/$\overline{PIN}$ is tied high). By using the SPI interface, the micro controller can read additional diagnostics and status information as well as configure the device.

The device has integrated IEC 61000-4-4/5 EFT and surge protection. In addition, tolerance to ±70V transients enables flexibility to choose from a wider range of TVS diodes if an application requires higher levels of protection. These integrated robustness features simplify the system level design by reducing external protection circuitry.

TIOL221 transceiver implements protection features for overcurrent, overvoltage and over-temperature conditions. The devices also provide a current-limit setting of the driver output current using an external resistor.

The devices derive the low-voltage supply from the IO-Link LP voltage (24V nominal) via an internal linear regulator to provide power to the local controller and sensor circuitry.

7.2 Functional Block Diagrams

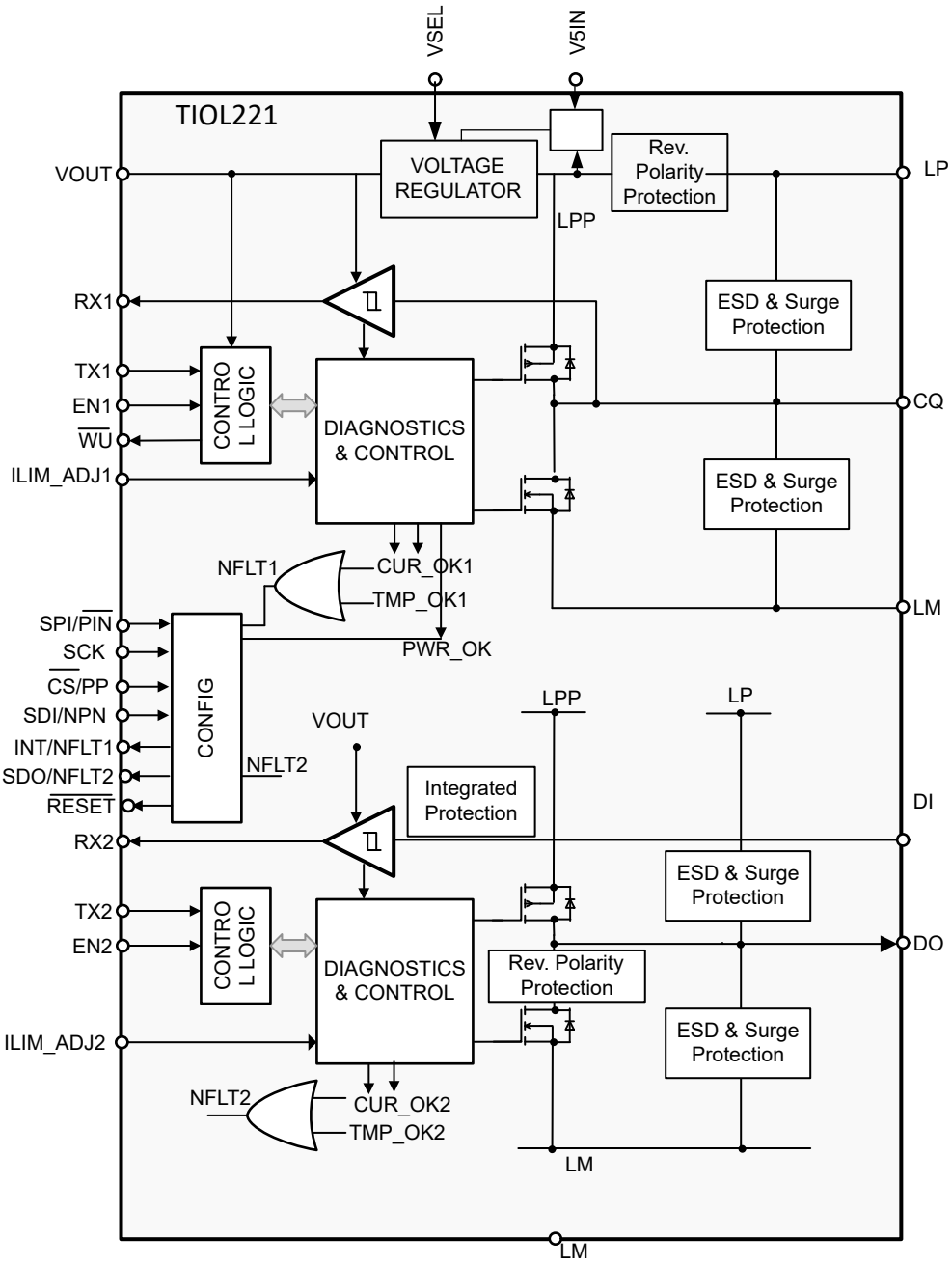


Figure 7-1. Block Diagram

7.3 Feature Description

7.3.1 Wake-Up Detection

The CQ channel of TIOL221 may be operated in IO-Link mode or Standard Input / Output (SIO) mode. If the CQ channel is in SIO mode, and the IO-link controller node wants to initiate communication with the device node, the controller drives the CQ line to the opposite of the present state. The device either sinks or sources the current (≥ 500mA) for the wake-up duration (typically 80µs) depending on the CQ logic level as per the IO-Link specification. The TIOL221 detects a wake-up condition and communicates to the local microcontroller

by asserting the $\overline{WU}$ pin low for the duration of t_{WUL}. The IO-Link communication specification requires the device node to switch to receive mode within 500µs after receiving the wake-up signal.

Table 7-1. Wake-Up Function (t_{WU1} < t < t_{WU2})

EN1	TX1	CQ CURRENT	WAKE	COMMENT
L / Open	X	X	Asserts low for t_{WUL}	Device asserts low for t_{WUL} if RX output changes high-to-low or low-to-high for t_{WU1} < t < t_{WU2}
H	H / Open	$\lvert I_{(CQ)} \rvert \geq I_{O(LIM)}$ mA	Asserts low for t_{WUL}	Device receives high-level wake-up request over the IO-Link bus
H	L	$\lvert I_{(CQ)} \rvert \geq I_{O(LIM)}$ mA	Asserts low for t_{WUL}	Device receives low-level wake-up request over the IO-Link bus

For overcurrent conditions shorter or longer than a valid wake-up pulse, the WAKE pin remains in a high-impedance (inactive) state. This is illustrated in Figure 6-6.

In the SPI-mode, in addition to the $\overline{WU}$ asserted low, WU_INT bit is set. Wake-up signaling can be disabled in the SPI-mode by setting the WU_DIS bit to 1b in the DEVICE_CONFIG register. Wake-up detection cannot be disabled in the pin-mode.

The DO channel of TIOL221 does not recognize wake-up pulses. The DO pin does provide overcurrent limiting and detection.

7.3.2 Current Limit Configuration

The output current of CQ and DO pins can be configured independently in the pin-mode as well as SPI-mode.

7.3.2.1 Current Limit Configuration in Pin-Mode

In the pin-mode, the current limit of CQ and DO can be configured with an external resistor on the ILIM_ADJ1 and ILIM_ADJ2 pins respectively. The highest current limit setting with an external resistor of 10kΩ provides a minimum of 300mA over the operating temperature and voltage range. Refer to Table 7-2 for the pin-mode configuration of the CQ and DO drivers.

Output disable due to current fault and current fault auto recovery features can be disabled by floating ILIM_ADJ1/2 pins. However, the current fault indication is still active in this configuration. This feature is useful when driving large capacitance.

When ILIM_ADJ1/2 pins are shorted to ground, the CQ and the DO drivers can configured to be in the IO-link controller mode. In this mode, the drivers can source or sink minimum of 500mA to generate a wake-up request. In addition, drivers enable a small current sink of 5mA (minimum) at the driver output pins. The current fault indication, output disable, and auto recovery features are disabled in this mode.

Table 7-2. Current Limit Configuration in Pin-mode

ILIM_ADJ1/2 Pin Condition	CQ/DO Current Limit (Min.)	NFLT1/2 Indication Due to Current Fault	Current Fault Blanking Time (t_{SC})	Output Disable and Auto Recovery
R_{SET} resistor to L- (10kΩ to 110kΩ)	Variable (35mA to 300mA)	Yes	200µs (typical)	Yes
Connected to L- (R_{SET} 0 to 5kΩ)	500mA	No	N/A	No
OPEN	260mA	Yes	None (immediate fault indication)	No

7.3.2.2 Current Limit Configuration in SPI mode

In the SPI mode, CQ and DO driver current limit can be configured via SPI. CQ driver can be configured via CQ_CURLIM Register. CQ_CURLIM[7:5] register can be used to configure the current limits.

Similarly, DO_CURLIM[7:5] register can be used to configure the current limits for the DO driver.

7.3.3 CQ Current Fault Detection, Indication and Auto Recovery

If the output current at CQ exceeds the internally-set current limit $I_{O(LIM)}$ for a duration longer than the current blanking time, t_{SC}, the device detects the condition as an overcurrent fault.

In pin-mode, the $\overline{INT}$/NFLT1 pin is driven logic low to indicate a fault condition. The output can be set to either turn off (auto-recovery mode) or continue to supply the current until the device enters thermal shutdown. The behavior depends on how the ILIM_ADJ1 pin is connected. See Table 7-2. In the auto-recovery mode, the driver periodically retries to check if the output is still in the over current condition. In this mode, the output is switched on for t_{SC} in t_{AR} intervals. Current fault auto retry mode can be disabled by setting ILIM_ADJ1 = OPEN or GND. Current fault blanking time is zero when ILIM_ADJ1=OPEN. See current limit indicator function ($t > t_{SC}$) for details.

In SPI-mode, CQ_CURLIM register settings can be used to configure the CQ driver behavior. CQ_CUR_LIM bits set the current limit whereas the CQ_BL_TIME and CQ_RETRY_TIME set the current fault blanking time and auto-recovery time respectively. CQ_AUTO_RETRY_EN controls the auto-recovery behavior.

When the driver is disabled, the current limit indicator is inactive.

7.3.4 DO Current Fault Detection, Indication and Auto Recovery

If the output current at DO exceeds the internally-set current limit $I_{O(LIM)}$ for a duration longer than the current blanking time, t_{SC}, the device detects the condition as an overcurrent fault.

In pin-mode, the SDO/NFLT2 pin is driven logic low to indicate a fault condition. The output can be set to either turn off (auto-recovery mode) or continue to supply the current until the device enters thermal shutdown. The behavior depends on how the ILIM_ADJ2 pin is connected. See Table 7-2 In the auto-recovery mode, the driver periodically retries to check if the output is still in the over current condition. In this mode, the output is switched on for t_{SC} in t_{AR} intervals. Current fault auto retry mode can be disabled by setting ILIM_ADJ2 = OPEN or GND. Current fault blanking time is zero when ILIM_ADJ2=OPEN.

In SPI-mode, DO_CURLIM register settings can be used to configure the DO driver behavior. DO_CUR_LIM bits set the current limit whereas the DO_BL_TIME and DO_RETRY_TIME set the current fault blanking time and auto-recovery time respectively. DO_RETRY_EN controls the auto-recovery behavior.

When the driver is disabled, the current limit indicator is inactive.

7.3.5 CQ and DI Receivers

RX1 is the output of the CQ receiver. The receiver output is the inverse logic of the CQ input and the receiver function is summarized in Table 7-3. In pin-mode, the CQ receiver is always on. In SPI mode, in addition to the RX1 output, the CQ_RX_LEVEL bit in the STATUS register reflects the logic level of CQ bus input level. In SPI mode, the receiver can be disabled by setting the RX_DIS bit in the CQ_CONFIG register. When the receiver is disabled, RX1 output is in high-impedance and CQ_RX_LEVEL bit in the status register is invalid.

Table 7-3. CQ Receiver Function

SPI/$\overline{\text{PIN}}$	CQ VOLTAGE	RX1	CQ_RX_LEVEL bit	COMMENT
L or (H && RX_DIS =0)	$V_{(CQ)} < V_{(THL)}$	H	L	Normal receive mode, input low
	$V_{(THL)} < V_{(CQ)} < V_{(THH)}$	?	?	Indeterminate output, can be either high or low
	$V_{(THH)} < V_{(CQ)}$	L	H	Normal receive mode, input high
	Open	?	?	Indeterminate output, can be either high or low
H && RX_DIS =1	X	Z	Z	Output is in high-Z

RX2 is the output of the DI receiver. The receiver output is the inverse logic of the DI input and the receiver function is summarized in Table 7-3. In pin-mode, the DI receiver is always on. In SPI mode, in addition to the RX2 output, the DI_LEVEL bit in the STATUS register reflects the logic level of DI input. In SPI mode, the receiver can be disabled by setting the DI_DIS bit in the DI_CONFIG register. When the receiver is disabled, RX2 output is in high-impedance and DI_LEVEL bit in the status register is invalid.

Table 7-4. DI Receiver Function

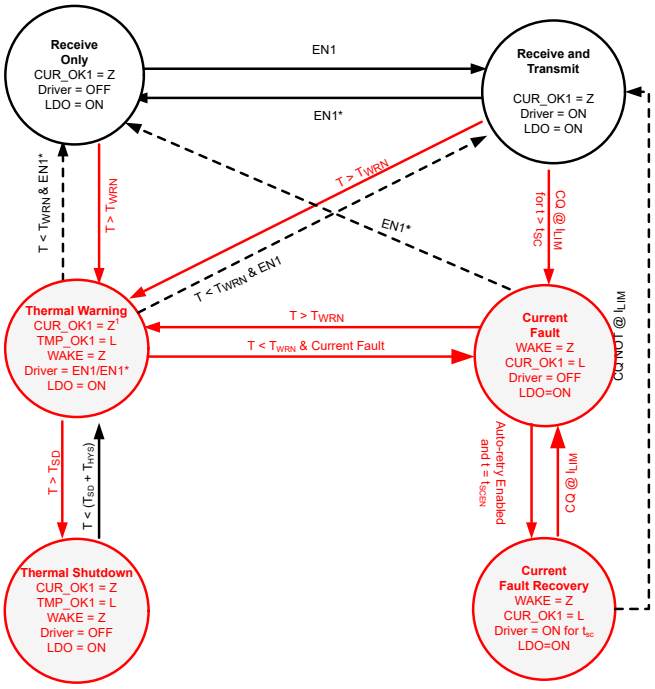
DI VOLTAGE	RX2	DI_LEVEL bit	COMMENT
$V_{(DI)} < V_{(THL)}$	H	L	Normal receive mode, input low
$V_{(THL)} < V_{(DI)} < V_{(THH)}$	?	?	Indeterminate output, can be either high or low
$V_{(THH)} < V_{(DI)}$	L	H	Normal receive mode, input high
Open	?	?	Indeterminate output, can be either high or low

7.3.6 Fault Reporting

In the pin mode, NFLT1 pin is driven low if the CQ driver enters overcurrent condition, or if the CQ driver temperature sensor has exceeded $T_{(WRN)}$. NFLT1 returns to high-impedance as soon as both the fault conditions clear.

Similarly, NFLT2 pin is driven low if the DO driver enters overcurrent condition, or if the DO driver temperature sensor has exceeded $T_{(WRN)}$. NFLT2 returns to high-impedance as soon as both the fault conditions clear.

If the LP supply or the VOUT supply fall below their UVLO thresholds, $\overline{\text{RESET}}$ pin goes low. $\overline{\text{RESET}}$ pin goes high after both LP and VOUT rise above their UVLO thresholds.



Note: NFLT1 = [CUR_OK1 && TMP_OK1]. The LDO has a thermal sensor. The LDO can turn off if the sensor temperature reaches $T_{(SDN)}$, and turn-off both the CQ and DO drivers.

Figure 7-2. CQ Driver State Diagram

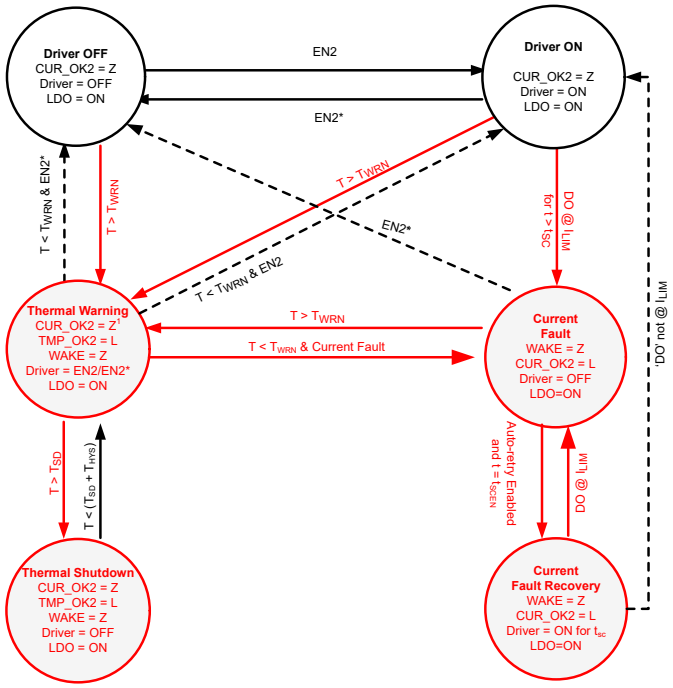


Figure 7-3. DO Driver State Diagram

Note

Note: NFLT2 = [CUR_OK2 && TMP_OK2]. The LDO has a thermal sensor. The LDO can turn off if the sensor temperature reaches $T_{(SDN)}$, and turn-off both the CQ and DO drivers.

7.3.6.1 Thermal Warning, Thermal Shutdown

The TIOL221 has three separate thermal sensors: one for each of the driver and another one for the LDO.

If the die temperature around the CQ driver exceeds $T_{(WRN)}$, the NFLT1 flag is held low indicating a potential over temperature problem. When the T_J exceeds $T_{(SDN)}$, the CQ driver is disabled. The LDO and DO driver remain operational as long as the respective thermal sensors do not exceed $T_{(SDN)}$. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal circuit re-enables the driver, subject to the state of the EN1 and TX1 pins.

If the die temperature around the DO driver exceeds $T_{(WRN)}$, the NFLT2 flag is held low indicating a potential over temperature problem. When the T_J exceeds $T_{(SDN)}$, the DO driver is disabled. The LDO and CQ driver remain operational as long as the respective thermal sensors do not exceed $T_{(SDN)}$. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal circuit re-enables the driver, subject to the state of the EN2 and TX2 pins.

The thermal sensor near the LDO detects the temperature exceeding the $T_{(SDN)}$. The LDO and both the drivers are turned off and $\overline{\text{RESET}}$ is held low. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal circuit re-enables the LDO and the drivers and $\overline{\text{RESET}}$ is released after the VOUT is above the UVLO threshold.

7.3.7 The Integrated Voltage Regulator (LDO)

The TIOL221 has an integrated linear voltage regulator (LDO) which can supply power to external components. The LDO is capable of delivering up to 20mA. LDO output level is configurable via VSEL pin. When VSEL is connected to GND, VOUT is configured to provide a 3.3V output with LP as the input supply. When VSEL is left floating, VOUT provides a 3.3V output, with V5IN as the supply input to reduce the power dissipation in the device. When VSEL is connected to VOUT, VOUT is set to 5V. The VSEL pin status is detected at power-up and VOUT output level is determined and latched until the next power-up cycle.

Table 7-5. LDO Output Configuration via VSEL pin

VSEL pin connection	VOUT
Connected to LM	3.3V (supplied from LP)
Floating	3.3V (supplied from V5IN)
Connected to VOUT	5V

When configured for 5V output, the voltage regulator works with input voltage, LP, in the range of 7V to 36V with respect to LM. When configured for 3.3V output, the regulator can work with either V5IN supply (when VSEL is floating) or LP supply (when VSEL is connected to VOUT).

Selecting V5IN as the supply input for the 3.3V output on VOUT helps reduce the on-chip power dissipation. When VSEL is set to be floating, if the V5IN supply is not present or below the V5IN_UVLO threshold, the VOUT regulator is shut-off and $\overline{\text{RESET}}$ output is active.

The LDO is designed to be stable with standard ceramic capacitors with values of 1µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1Ω. With tolerance and dc bias effects, the minimum capacitance to make sure the output stability is 1µF.

The voltage regulator has an internal 35mA current limit to protect against initial startup inrush current due to large decoupling capacitors and accidental short circuit conditions.

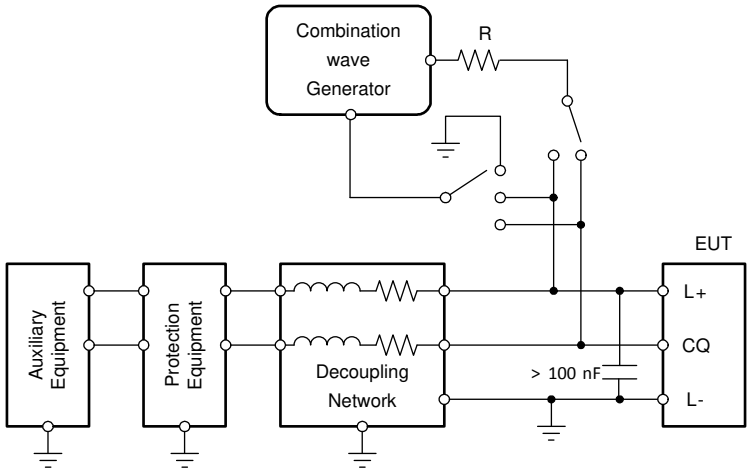
7.3.8 Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the LP, CQ, DO, DI and LM pins. Any combinations of the pins can be connected to DC voltages up to 65V (max). The maximum voltage between any of the pins may not exceed 65V DC at any time.

7.3.9 Integrated Surge Protection and Transient Waveform Tolerance

The LP, CQ, DO and DI pins of the device are capable of withstanding up to 1.2kV of 1.2/50 – 8/20µs IEC 61000-4-5 surge with a source impedance of 500Ω. The surge testing should be performed with a minimum 100nF supply decoupling capacitor between LP and LM, and 1µF between VOUT and LM.

External TVS diodes may be required for higher transient protection levels. The system designer must make sure the maximum clamping voltage of the external diodes is < 65V at the desired current level. The device is capable of withstanding up to ±70V transient pulses < 100µs.



1.2/50 – 8/20µs CWG
R = 500Ω

Figure 7-4. Surge Test Setup

7.3.10 Undervoltage Lock-Out (UVLO)

The device enters UVLO if either the LP voltage or the VOUT supply fall below their respective UVLO thresholds. As soon as the supplies falls below UVLO thresholds, $\overline{\text{RESET}}$ is pulled low, and the drivers (CQ and DO) are disabled (Hi-Z). Receiver performance is not specified in this mode.

When the supplies rise above their rising thresholds, $\overline{\text{RESET}}$ pin goes high. The driver outputs are turned on after $t_{(UVLO)}$ delay.

7.3.11 Interrupt Function

The interrupt is used to signal some of the critical events to the microcontroller via the $\overline{INT}$ pin in the SPI mode. In the SPI mode, $\overline{INT}$ pin is a push-pull output stage. When an interrupt-generating event takes place, the $\overline{INT}$ pin is pulled low.

Following events can generate interrupt and the corresponding bits are set in the interrupt register:

- Thermal Shutdown (TSD_INT)
- A valid wake-up pulse received on CQ (WU_INT)
- DO output overcurrent fault (DO_FAULT_INT)
- CQ output overcurrent fault (CQ_FAULT_INT)
- LP falls below warning threshold (LPW_INT)
- V5IN falls below UVLO threshold (UV_V5_INT)
- Temperature reached above the thermal warning threshold (TEMP_WARN)

Individual interrupt events can be masked via INT_MASK register. When an interrupt is masked, that particular event does not activate the INT pin. However, interrupt bit is set if the interrupt generating event occurs.

The interrupt bits are not cleared automatically when the interrupt generating event is no longer present. The interrupt bit needs to be cleared explicitly by the microcontroller. The INT pin goes high when all interrupt bits are cleared by the MCU (cleared on read) and the event does not persist. INT pin also goes high if all the interrupt bits are masked. If the interrupt bits are unmasked and if any of the interrupt bits are still set, the INT pin goes low again.

7.4 Device Functional Modes

The device can operate in two modes: pin mode or SPI mode. When the $\overline{\text{SPI/PIN}}$ pin is low, the device operates in pin mode. When the $\overline{\text{SPI/PIN}}$ pin is high, the device operates in SPI mode.

The CQ driver control in either of the modes is described in Table 7-6. The DO driver control is described in Table 7-7. Additionally, if using SPI mode, both CQ and DO driver can be connected together to drive higher load currents. The settings for this configuration is described in Table 7-8 and *CQ and DO Tracking mode*. The recommended is to have the drivers in disabled state before changing the driver configuration settings including the driver modes, current limits and overcurrent blanking time.

Table 7-6. CQ Control

SPI/$\overline{\text{PIN}}$	EN1	TX1	CQ_TX_MODE = 11 (CQ Disabled)	CQ_Q	NPN Mode	PNP Mode	Push-Pull Mode
L	L/Open	L	X	X	Z	Z	Z
		H	X	X	Z	Z	Z
	H	L	X	X	Z	H	H
		H	X	X	L	Z	L
H	L	L	0	0	Z	Z	Z
		H			Z	Z	Z
		L		1	Z	H	H
		H			Z	H	H
	H	L		0	Z	H	H
		H			L	Z	L
		L		1	Z	H	H
		H			Z	H	H
	X	X	1	X	Z	Z	Z

Table 7-7. DO Control

When DO and CQ are set to track (DO_CQ_TRACK set to 1b), see Table 7-8.

SPI/$\overline{\text{PIN}}$	EN2	TX2	DO_MODE=11 (DO disabled)	DO_Q	NPN Mode	PNP Mode	Push-Pull Mode
L	L/Open	L	X	X	Z	Z	Z
		H	X	X	Z	Z	Z
	H	L	X	X	Z	H	H
		H	X	X	L	Z	L
H	L	L	0	0	Z	Z	Z
		H			Z	Z	Z
		L		1	Z	H	H
		H			Z	H	H
	H	L		0	Z	H	H
		H			L	Z	L
		L		1	Z	H	H
		H			Z	H	H
	X	X	1	X	Z	Z	Z

Table 7-8. DO Control (When DO_CQ_TRACK = 1b)

When DO and CQ are set to track (DO_CQ_TRACK set to 1b), DO driver follows the CQ configuration and the DO configuration is ignored, including the driver modes, current limits and driver settings.

SPI/$\overline{PIN}$	DO_CQ_TRACK=1b	EN2/TX2/ DO_MODE/ DO_CQ	EN1	TX1	CQ_TX_MODE=11 (CQ disabled)	CQ_Q	NPN Mode (Per CQ Configuration)	PNP Mode (Per CQ Configuration)	Push-Pull Mode (Per CQ Configuration)
H	1b	X	L	L	0	0	Z	Z	Z
				H			Z	Z	Z
				L		1	Z	H	H
				H			Z	H	H
			H	L		0	Z	H	H
				H			L	Z	L
				L		1	Z	H	H
				H			Z	H	H
			X	X	1	X	Z	Z	Z

Table 7-9. NPN, PNP and Push-Pull Mode Selection in Pin-Mode

SPI/$\overline{PIN}$	$\overline{CS}$/PP	SDI/NPN	CQ and DO Driver Mode
L	L	L	PNP
	L	H	NPN
	H	X	Push-Pull
H	X	X	CQ and DO driver modes selected via SPI interface

7.4.1 CQ and DO Tracking mode

In SPI mode, CQ and DO output drivers can be set to sync with each other using only the TX1 as the input and EN1 as the enable pin using the DO_CQ_TRACK bit setting. When this bit is enabled, both the drivers take TX1 as the input and are controlled by the EN1 enable pin. The following configurations go into effect when the DO_CQ_TRACK bit is set:

- DO configuration settings are ignored and CQ configuration settings are used (overcurrent, blanking time, auto re-try and CQ_Q impact both the drivers)
- TX2 and EN2 input pins are ignored
- If one of the drivers goes into overcurrent or thermal faults, both the drivers are turned-off.
  - The interrupt and status bits of only the driver that goes into the fault condition are set

7.5 SPI Programming

When SPI/PIN is tied high, TIOL221 is in SPI mode. The SPI communication uses a standard SPI. Physically the digital interface pins are $\overline{CS}$ /PP (Chip select active-low), SDI/NPN (SPI Data In), SDO/NFLT2 (SPI Data Out) and SCK (SPI Clock). Each SPI transaction is initiated by a seven bit address with a R/W bit. The data shifted out on the SDO pin for the transaction always starts with the register 8'h01[7:0] which is the status register. This register provides the high-level status information about the device. The data byte which is the ‘response’ to the address and R/W byte are shifted out next. See Figure 7-5 and Figure 7-6 for SPI read and write frame diagrams for non-burst mode. See Figure 7-7 and Figure 7-8 for SPI read and write frame diagrams for burst mode.

The SPI controller must generate clock and data signals in SPI MODE0 (clock polarity CPOL = 0 and clock phase CPHA = 0) to communicate with TIOL221. The SPI input data on SDI is sampled on the low to high edge of SCK. The SPI output data on SDO is changed on the high to low edge of SCK.

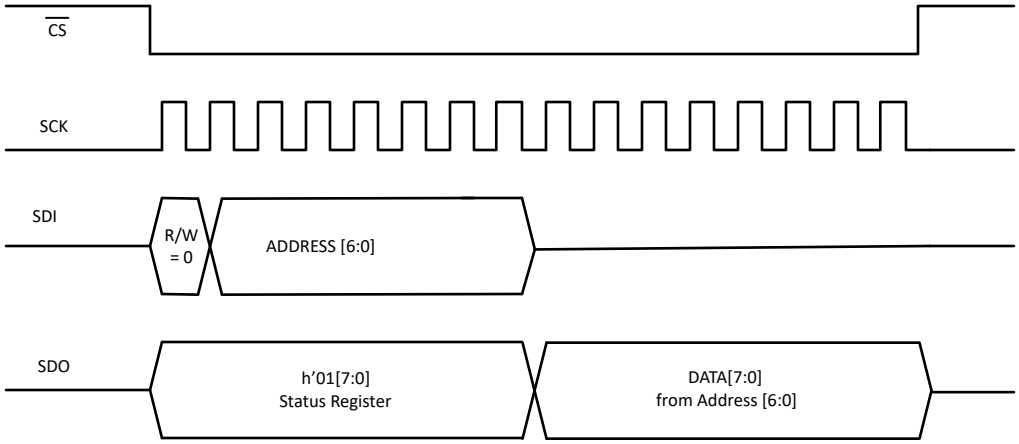


Figure 7-5. SPI Read (Single byte)

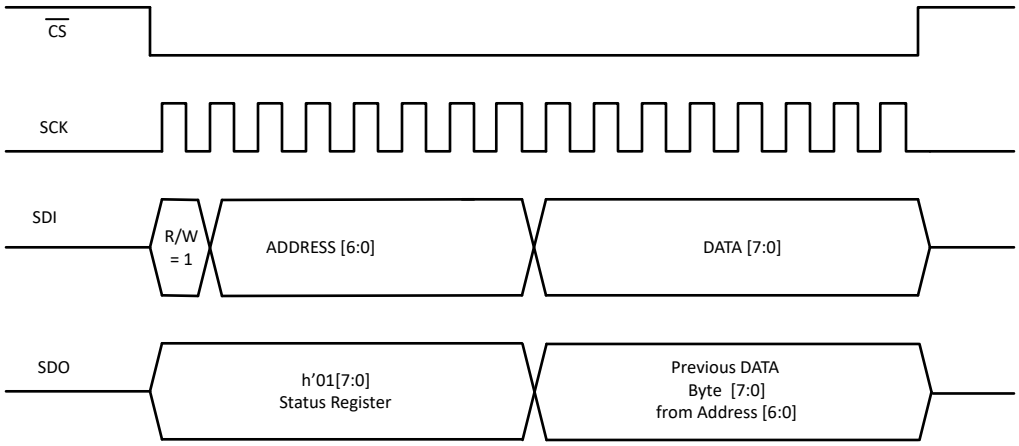


Figure 7-6. SPI Write (Single byte)

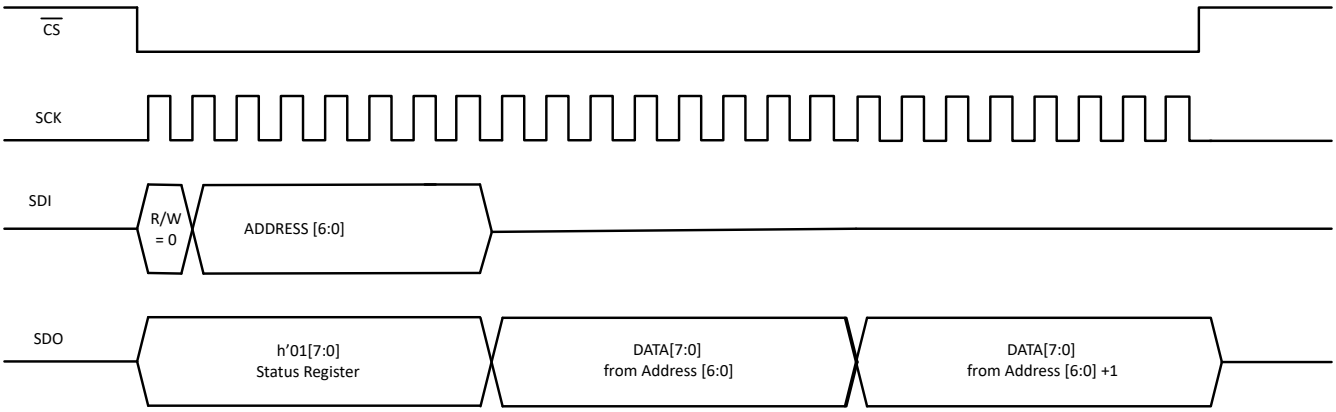


Figure 7-7. SPI Read (Burst mode)

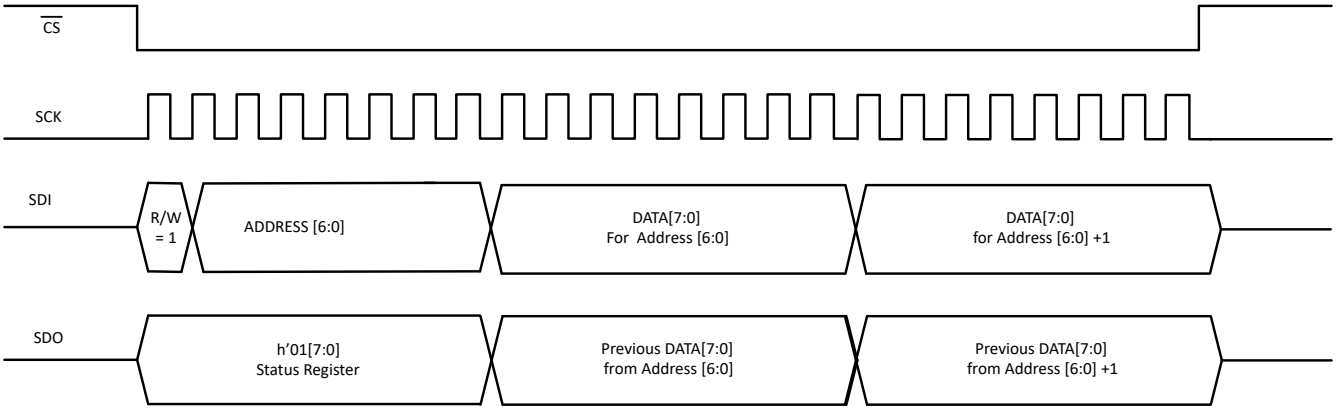


Figure 7-8. SPI Write (Burst mode)

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

When TIOL221 is connected to an IO-Link controller through a three or four wire interface (Figure 8-1), the controller can initiate communication and exchange data with a remote node with the TIOL221 IO-Link transceiver acting as a complete physical layer for the communication.

8.2 Typical Application

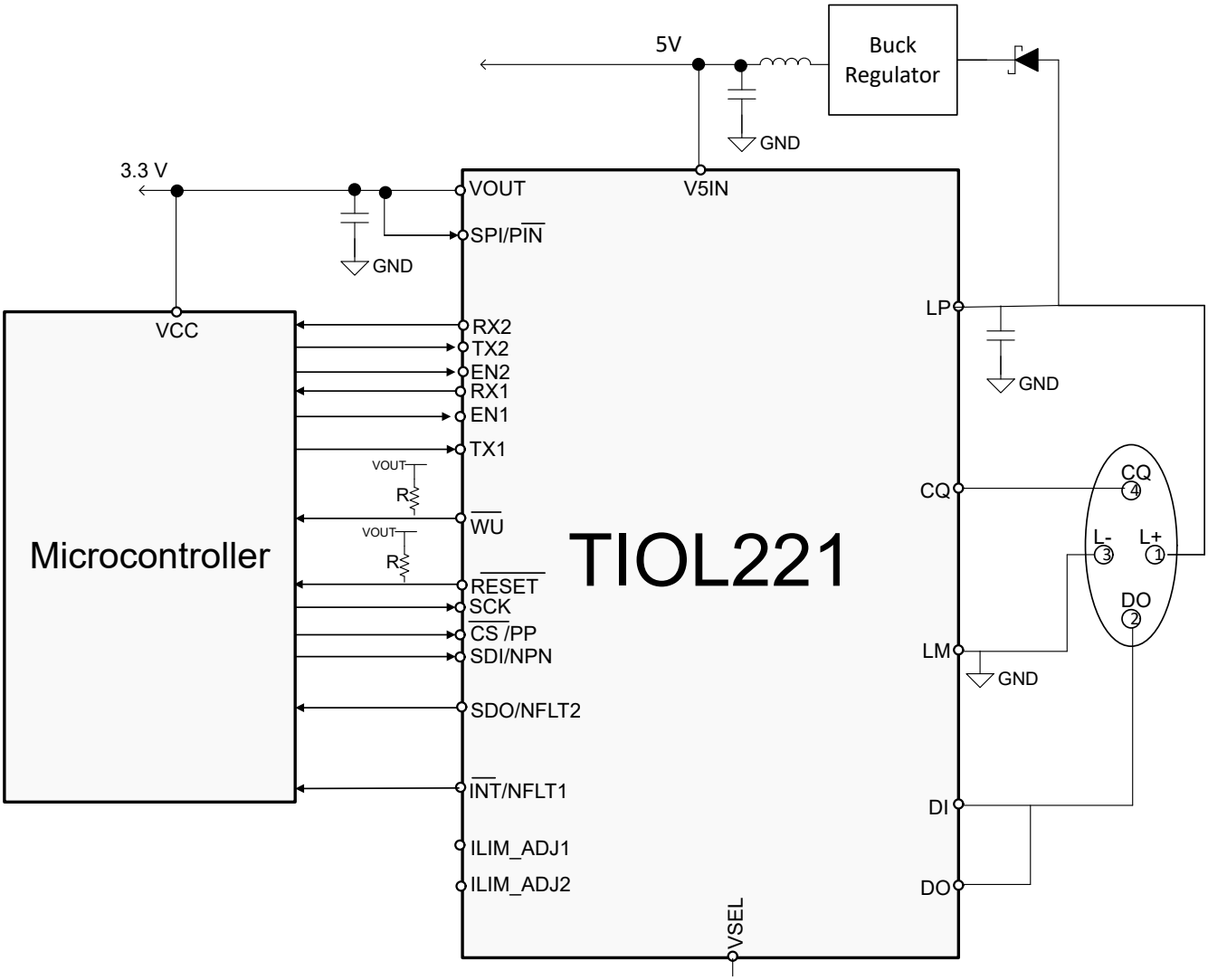


Figure 8-1. Typical Application Schematic (SPI Mode)

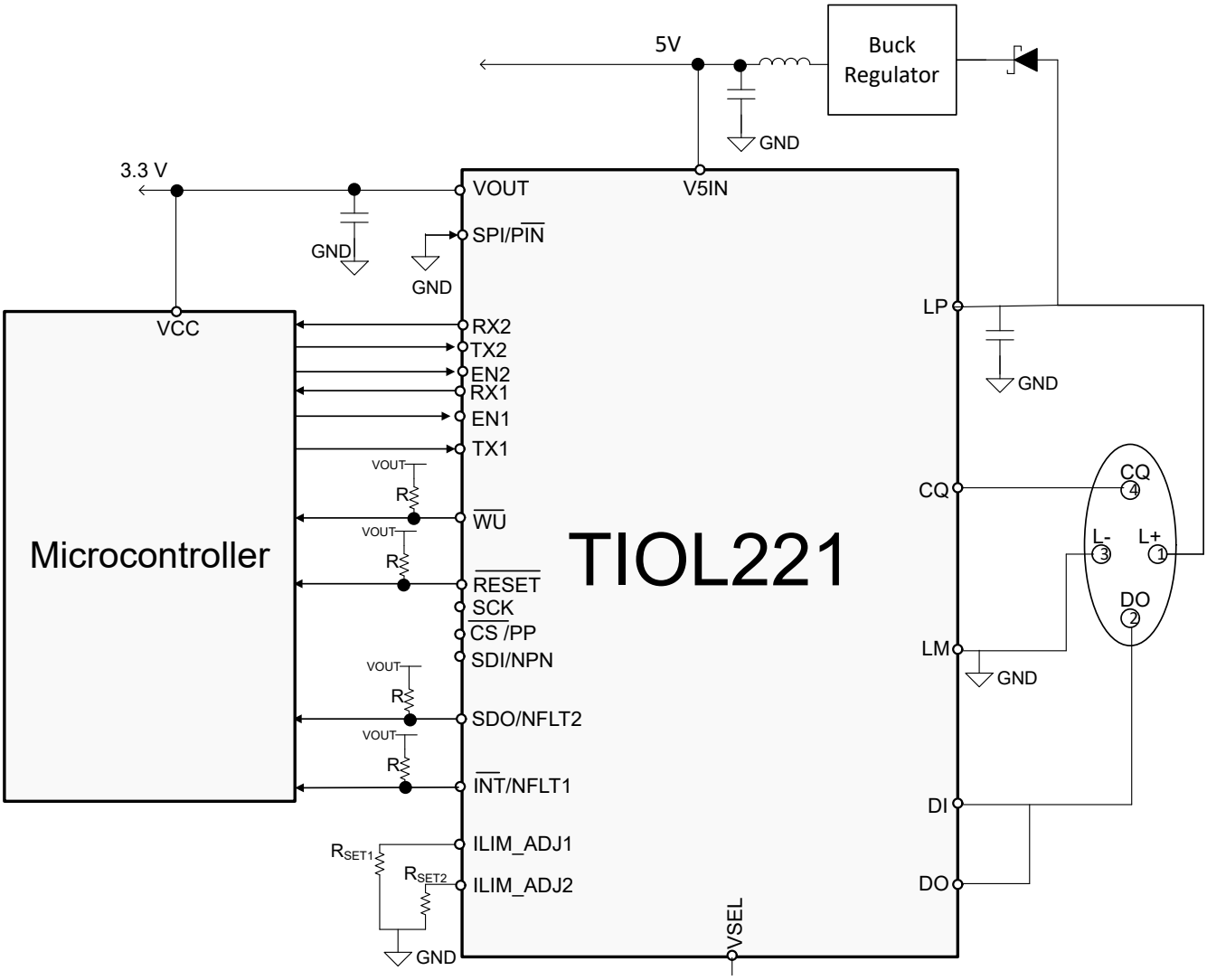


Figure 8-2. TIOL221 Application Schematic (Pin Mode)

8.2.1 Design Requirements

TIOL221 IO-Link transceiver can be used to communicate using the IO-Link protocol, or as standard digital outputs to either sense or drive a wide range of sensors and loads. Table 8-1 shows recommended components for a typical system design.

Table 8-1. Design Parameters

PARAMETERS	Design Requirement	TIOL221 Specification
Input voltage range (LP)	24V (typ), 30V (max)	7V to 36V
Output current (CQ)	200mA	Choose 250mA limit (min) with R_{SET1} = 15kΩ
LDO Output voltage	5V	VOUT = 5V By connecting VSEL=VOUT
LDO output current	5mA	$I_{(VOUT)}$: Up to 20mA
Pull-up resistors for NFLT1, NFLT2 and $\overline{WU}$	10kΩ	10kΩ
LP decoupling capacitor	0.1µF / 100V	0.1µF / 100V
VOUT output capacitor	1µF / 10V	1µF / 10V
Maximum Ambient Temperature, T_A	105°C	TIOL221 can support up to T_A of 125 °C if $T_J < T_{(SDN)}$

8.2.2 Detailed Design Procedure

8.2.2.1 Driving Capacitive Loads

These devices are capable of driving capacitive loads on the CQ and DO outputs. Assuming a pure capacitive load without series/parallel resistance, the maximum capacitance that can be charged without triggering current fault can be calculated as:

$$C_{LOAD} = \frac{[I_{O(LIM)} \times t_{SC}]}{V_{(L+)}} \quad (1)$$

To drive higher capacitive loads and avoid overcurrent condition disabling the driver, the recommendation is to leave the corresponding ILIM_ADJx pin floating. With ILIM_ADJx pin floating, TIOL221 indicates overcurrent fault without blanking time delay (t_{SC}) but does not disable the driver. Another approach is to drive high capacitive loads with a series resistor between the CQ output and the load to avoid overcurrent condition. Capacitive loads can be connected to LM or LP.

8.2.2.2 Driving Inductive Loads

The TIOL221 is capable of magnetizing and demagnetizing large inductive loads. These devices contain internal circuitry that enables fast and safe demagnetization when configured as either P-switch or N-switch mode.

In P-switch configuration, the load inductor L is magnetized when the driver (CQ or DO) output is driven high. When the PNP is turned off, there is a significant amount of negative inductive kick back at the driver output pin. This voltage is safely clamped internally at about −15V.

Similarly, in N-switch configuration, the load inductor L is magnetized when the driver output is driven low. When the NPN is turned off, there is a significant amount of positive inductive kick back at the driver output pin. This voltage is safely clamped internally at about 15V.

The equivalent protection circuits are shown in Figure 8-3 and Figure 8-4. The minimum value of the resistive load R can be calculated as:

$$R = \frac{V_{(L+)}}{I_{O(LIM)}} \quad (2)$$

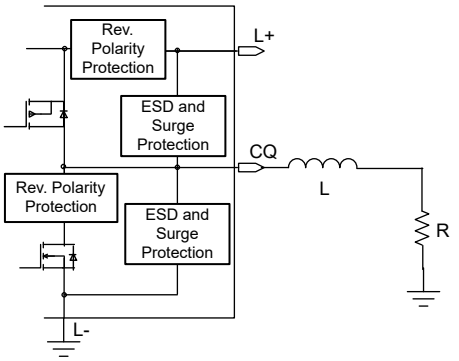


Figure 8-3. P-Switch Mode

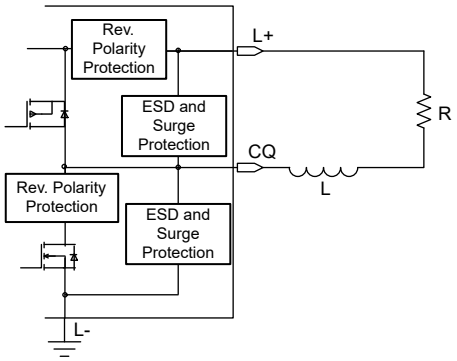
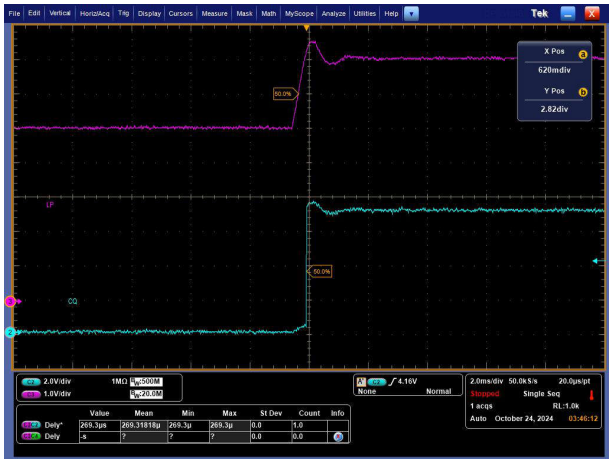


Figure 8-4. N-Switch Mode

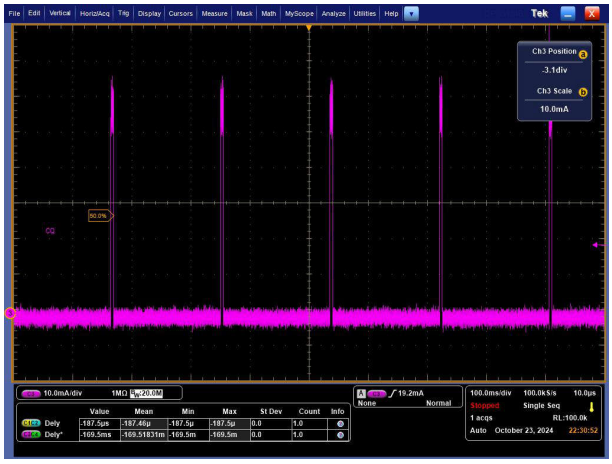
8.2.3 Application Curves



LP ramping from below the UVLO threshold to above the UVLO threshold

T_A =25°C

Figure 8-5. CQ Power Up Delay, $t_{(UVLO)}$(Pin mode or the default 00b setting in SPI mode)



t_{SC} = 5ms

t_{AR}= 200ms

$I_{O(LIM)}$ = 35mA (min)

Figure 8-6. CQ in Current Fault Auto Recovery

L = 1.5H, I_{LOAD} = 100mA

LP = 36V

TA - 25°C

Figure 8-7. Inductive Load Demagnetization (PNP mode)

8.3 Power Supply Recommendations

The TIOL221 transceiver is designed to operate from a 24V nominal supply at LP, which can vary by +12V and -17V from the nominal value to remain within the device recommended supply voltage range of 7V to 36V. This supply should be buffered with at least a 100nF/100V capacitor.

8.4 Layout

8.4.1 Layout Guidelines

- Use of a 4-layer board is recommended for good heat conduction. Use layer 1 (top layer) for control signals, layer 2 as power ground layer for LM, layer 3 for the 24V supply plane (LP), and layer 4 for the regulated output supply (VOUT).
- Connect the thermal pad to LM with maximum amount of thermal vias for best thermal performance.
- Use entire planes for LP, VOUT and LM for minimum inductance.

- The LP terminal must be decoupled to ground with a low-ESR ceramic decoupling capacitor. The recommended minimum capacitor value is 100nF. The capacitor must have a voltage rating of 50V minimum (100V depending on max sensor supply fault rating) and an X5R or X7R dielectric.
- The optimum placement of the capacitor is closest to the transceiver's LP and LM terminals to reduce supply drops during large supply current loads. See Figure 8-8 for a PCB layout example.
- Connect all open-drain control outputs via 10kΩ pull-up resistors to the VOUT plane to provide a defined voltage potential to the system controller inputs when the outputs are high-impedance.
- If using pin mode, connect the R_{SET} resistor between ILIM_ADJ1/2 and LM, as needed
- Decouple the regulated output voltage at VOUT to ground with a low-ESR, ≥ 1µF, ceramic decoupling capacitor. The capacitor should have a voltage rating of 10V minimum and an X5R or X7R dielectric.

8.4.2 Layout Example

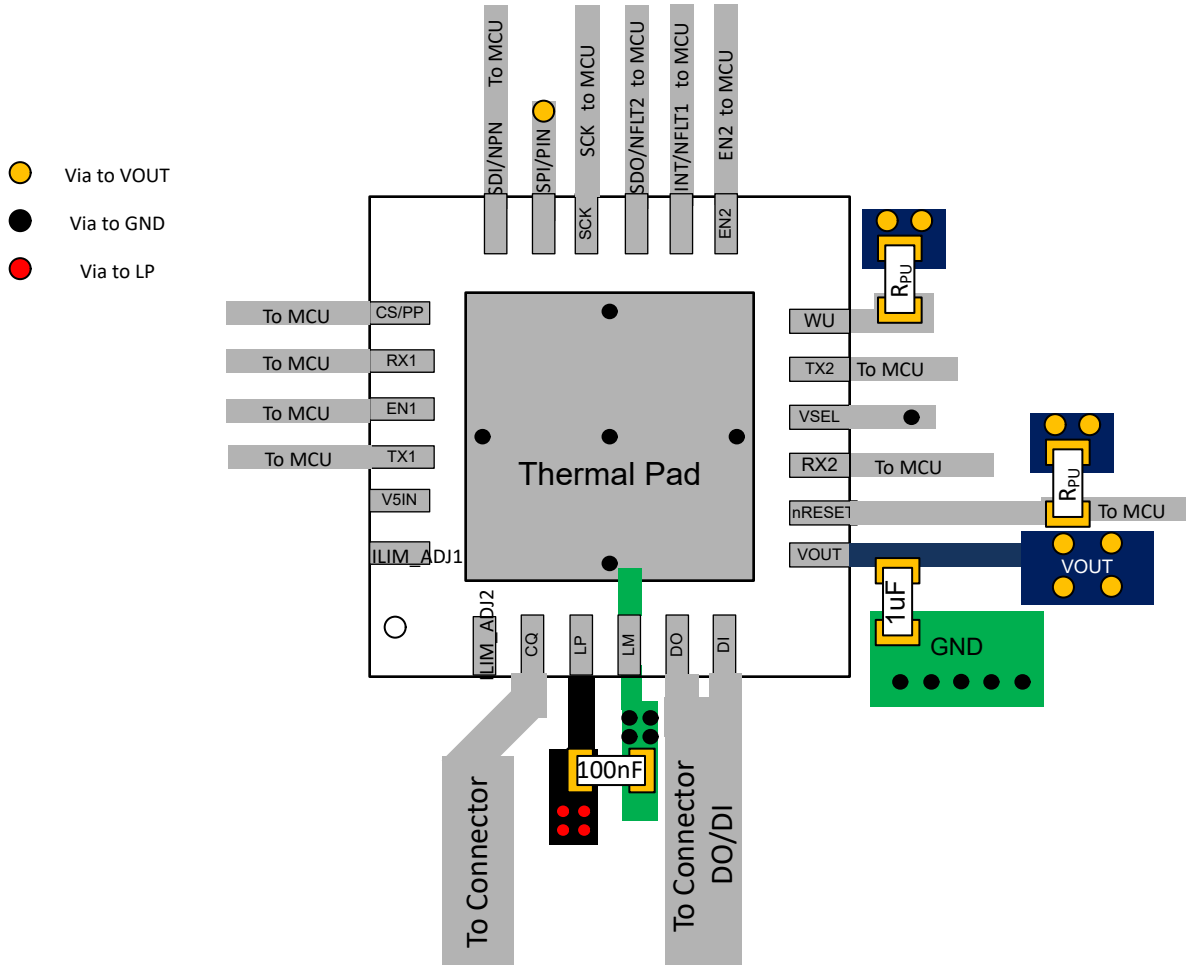


Figure 8-8. Layout Example (SPI mode shown)

9 TIOL221 Registers

Table 9-1 lists the memory-mapped registers for the TIOL221 registers. All register offset addresses not listed in Table 9-1 should be considered as reserved locations and the register contents should not be modified.

Table 9-1. TIOL221 Registers

Address	Acronym	Register Name	Section
0h	INT	Interrupt	Go
1h	STATUS	Status	Go
2h	DEVICE_CONFIG	Device Configuration	Go
3h	CQ_CURLIM	CQ Driver Current Limit	Go
4h	CQ_CONFIG	CQ Configuration	Go
5h	DIO_CONFIG	DIO Configuration	Go
6h	DO_CURLIM	DO Driver current limit	Go
7h	DEVICE_ID	Device ID	Go
8h	INT_MASK	Interrupt Mask	Go
9h	RESET_CONFIG	Reset pin configuration register	Go

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. TIOL221 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.1 INT Register (Address = 0h) [Reset = 00h]

INT is shown in Figure 9-1 and described in Table 9-3.

Return to the Summary Table.

Interrupt registers reflect current status of various fault conditions. Interrupt registers are not cleared automatically after the fault clears. They are cleared on read if the fault condition does not exist

Figure 9-1. INT Register

7	6	5	4	3	2	1	0
TSD_INT	WU_INT	DO_FAULT_INT	CQ_FAULT_INT	LPW_INT	RESERVED	UV_V5_INT	TEMP_WARN
RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	R-0b	RC-0b	RC-0b

Table 9-3. INT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSD_INT	RC	0b	Thermal shutdown interrupt bit. This bit is not cleared automatically when the fault is cleared. The bit is cleared on read if the fault does not exist anymore 0b = The device is not in thermal shutdown 1b = The device has entered thermal shutdown
6	WU_INT	RC	0b	This bit is set when an IO-link wake-up condition is detected on CQ. 0b = No wake-up detected 1b = Wake-up detected
5	DO_FAULT_INT	RC	0b	This bit is set when DO driver fault occurs (overcurrent or thermal) 0b = No fault on DO driver 1b = DO driver fault has occurred
4	CQ_FAULT_INT	RC	0b	This bit is set when CQ driver fault occurs (overcurrent or thermal) 0b = No fault on CQ driver 1b = CQ driver fault has occurred
3	LPW_INT	RC	0b	This bit is set when LP goes below the warning threshold 0b = LP is above the warning threshold 1b = LP has fallen below the warning threshold
2	RESERVED	R	0b	Reserved
1	UV_V5_INT	RC	0b	Undervoltage on the V5IN supply input (valid only if VSEL pin is floating and V5IN is the LDO input) 0b = No UV fault on V5IN 1b = UV fault on V5IN
0	TEMP_WARN	RC	0b	Thermal warning interrupt 0b = No thermal warning 1b = Thermal warning limit reached

9.2 STATUS Register (Address = 1h) [Reset = 00h]

STATUS is shown in Figure 9-2 and described in Table 9-4.

Return to the Summary Table.

Status registers reflect current status of various fault conditions. They are read-only and cleared automatically when the fault is cleared. Note: Soft reset does not reset the STATUS register bits as they reflect the current status of the faults. It is recommended to read the MSB byte when reading the STATUS register because the POR recovery bit is cleared by the time LSB byte is transferred to data output

Figure 9-2. STATUS Register

7	6	5	4	3	2	1	0
POR_RECOVERY	TSD	DI_LEVEL	DO_FAULT	CQ_FAULT	UV_V5	CQ_RX_LEVEL	TEMP_WARN
RC-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 9-4. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	POR_RECOVERY	RC	0b	The bit is set when the device recovers from POR event. The bit is cleared on read 0b = The device is operating normally 1b = The device has recovered from POR event
6	TSD	R	0b	The bit reflects the status of thermal shutdown. The bit is automatically cleared when temperature falls below thermal shutdown threshold 0b = No thermal shutdown 1b = Part in thermal shutdown
5	DI_LEVEL	R	0b	This bit is set when DI voltage is logic high and cleared when DI voltage is logic low Note: This bit is invalid if DI_DIS bit is set to 1. 0b = 0x0 1b = 0x1
4	DO_FAULT	R	0b	The bit reflects the status of DO drive fault 0b = No fault at DO pin 1b = Fault at DO pin
3	CQ_FAULT	R	0b	This bit reflects the status of the CQ driver fault 0b = No fault at CQ pin 1b = Fault at CQ pin
2	UV_V5	R	0b	This bit reflects the status of the UV condition at the V5IN pin 0b = V5IN voltage above UVLO threshold 1b = V5IN below UVLO threshold
1	CQ_RX_LEVEL	R	0b	This bit is set when CQ voltage is logic high and cleared when CQ voltage is logic low. Note: This bit is invalid if CQ_RX_DIS bit is set to 1. 0b = 0x0 1b = 0x1

Table 9-4. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TEMP_WARN	R	0b	Shows the status of the device temperature above or below the temperature warning threshold 0b = No temperature warning 1b = Device temperature is above the warning threshold

9.3 DEVICE_CONFIG Register (Address = 2h) [Reset = 00h]

DEVICE_CONFIG is shown in Figure 9-3 and described in Table 9-5.

Return to the Summary Table.

Device level configuration registers

Figure 9-3. DEVICE_CONFIG Register

7	6	5	4	3	2	1	0
SOFT_RESET	WU_DIS	DO_CQ_TRACK	IOLINK_5MA_PD	DI_RX_FILTER	CQ_RX_FILTER	T_UVLO	INT_TOG
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 9-5. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RESET	R/W	0b	Resets all registers to their defaults. Note: The status and interrupt bits may still be set depending upon the corresponding fault status. 0b = No reset 1b = Resets the device configuration
6	WU_DIS	R/W	0b	0b = CQ can recognize wake-up pulse 1b = CQ ignores the wake-up pulse
5	DO_CQ_TRACK	R/W	0b	If the bit is set, DO and CQ drivers both track together as a function of the TX input and CQ_CONFIG setting. 0b = DO and CQ drivers are independent 1b = DO and CQ drivers track as a function of the TX input
4	IOLINK_5MA_PD	R/W	0b	Enables 5mA pull-down current ILLM at both CQ and DO drivers when the respective driver is disabled. Note: CQ_CUR_LIM and DO_CUR_LIM limit needs to be set to 500mA to enable this respectively at CQ and DO. 0b = 5mA (min) pull-down current disabled 1b = 5mA (min) pull-down current enabled when the respective driver is disabled
3	DI_RX_FILTER	R/W	0b	Turns on or off the RX glitch filter on the DI line 0b = DI glitch filter disabled 1b = DI glitch filter enabled
2	CQ_RX_FILTER	R/W	0b	Turns on or off the RX glitch filter on the CQ line 0b = CQ RX glitch filter disabled 1b = CQ RX glitch filter enabled
1	T_UVLO	R/W	0b	CQ, DO re-enable delay, t(UVLO), after the recovery from LP UVLO 0b = 0.5 ms (typ) 1b = 30 ms (typ)
0	INT_TOG	R/W	0b	Enables interrupt pin toggling 0b = Interrupt pin set to active low 1b = Interrupt pin set to toggle with 200us period and 50% duty cycle

9.4 CQ_CURLIM Register (Address = 3h) [Reset = 20h]

CQ_CURLIM is shown in Figure 9-4 and described in Table 9-6.

Return to the Summary Table.

CQ Driver current limit and auto-retry configuration

Figure 9-4. CQ_CURLIM Register

7	6	5	4	3	2	1	0
CQ_CUR_LIM			CQ_BL_TIME		CQ_RETRY_TIME		CQ_AUTO_RETRY_EN
R/W-001b			R/W-00b		R/W-00b		R/W-0b

Table 9-6. CQ_CURLIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	CQ_CUR_LIM	R/W	001b	Sets current limits 000b = 35 mA (min) 001b = 50 mA (min) 010b = 100 mA (min) 011b = 150 mA (min) 100b = 200 mA (min) 101b = 250 mA (min) 110b = 300 mA (min) 111b = 500 mA (min)
4-3	CQ_BL_TIME	R/W	00b	Sets current blanking time 00b = 200 µs (typ) 01b = 500 µs (typ) 10b = 5 ms (typ) 11b = 0 s (no blanking time)
2-1	CQ_RETRY_TIME	R/W	00b	Sets auto re-try time 00b = 50 ms (typ) 01b = 100 ms (typ) 10b = 200 ms (typ) 11b = 500 ms (typ)
0	CQ_AUTO_RETRY_EN	R/W	0b	Enable auto re-try. When enabled the driver gets disabled after blanking time and re-enabled after the retry time. When auto retry is disabled, the driver stays enabled and shut off only after thermal shutdown NOTE: It is not recommended to enable auto retry when blanking time is configured to 2b11 (no blanking time) . 0b = Disabled 1b = Enabled

9.5 CQ_CONFIG Register (Address = 4h) [Reset = 0Ch]

CQ_CONFIG is shown in Figure 9-5 and described in Table 9-7.

Return to the Summary Table.

CQ configration registers for PNP/NPN modes and weak pull-up/down

Figure 9-5. CQ_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED		CQ_WEAK_PD_EN	CQ_WEAK_PU_EN	CQ_TX_MODE		CQ_Q	RX_DIS
R-0b		R/W-0b	R/W-0b	R/W-11b		R/W-0b	R/W-0b

Table 9-7. CQ_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	Reserved
5	CQ_WEAK_PD_EN	R/W	0b	Configures the weak pull-down on CQ when the driver is disabled 0b = Weak pull-down disabled 1b = Weak pull-down enabled
4	CQ_WEAK_PU_EN	R/W	0b	Configures the weak pull-up on CQ when the driver is disabled 0b = Weak pull-up disabled 1b = Weak pull-up enabled
3-2	CQ_TX_MODE	R/W	11b	Configures the driver transmission mode 00b = PNP mode 01b = Push-pull mode 10b = NPN mode 11b = Driver disabled
1	CQ_Q	R/W	0b	CQ driver output logic 0b = CQ is in high-impedance when EN1 is low (or CQ_DIS is low) 1b = CQ driver outputs logic high in push-pull or PNP mode and is turned-off in NPN mode
0	RX_DIS	R/W	0b	Configures the RX of the CQ line 0b = RX is enabled 1b = RX is disabled

9.6 DIO_CONFIG Register (Address = 5h) [Reset = 0Ch]

DIO_CONFIG is shown in Figure 9-6 and described in Table 9-8.

Return to the Summary Table.

Figure 9-6. DIO_CONFIG Register

7	6	5	4	3	2	1	0
DI_WEAK_PD_EN	DI_WEAK_PU_EN	DO_WEAK_PD_EN	DO_WEAK_PU_EN	DO_MODE		DO_Q	DI_DIS
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-11b		R/W-0b	R/W-0b

Table 9-8. DIO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DI_WEAK_PD_EN	R/W	0b	Configures the weak pull-down on DI 0b = Weak pull-down disabled 1b = Weak pull-down enabled
6	DI_WEAK_PU_EN	R/W	0b	Configures the weak pull-up on DI 0b = Weak pull-up disabled 1b = Weak pull-up enabled
5	DO_WEAK_PD_EN	R/W	0b	Configures the weak pull-down on DO when the driver is disabled 0b = Weak pull-down disabled 1b = Weak pull-down enabled
4	DO_WEAK_PU_EN	R/W	0b	Configures the weak pull-up on DO when the driver is disabled 0b = Weak pull-up disabled 1b = Weak pull-up enabled
3-2	DO_MODE	R/W	11b	Configures the DO driver transmission mode 00b = PNP mode 01b = Push-pull mode 10b = NPN mode 11b = Driver disabled
1	DO_Q	R/W	0b	DO driver output logic 0b = DO is in high-impedance when EN2 is low (or DO_DIS is low) 1b = DO driver outputs logic high in push-pull or PNP mode and is turned-off in NPN mode
0	DI_DIS	R/W	0b	Configures the DI receiver 0b = DI is enabled 1b = DI is disabled

9.7 DO_CURLIM Register (Address = 6h) [Reset = 20h]

DO_CURLIM is shown in Figure 9-7 and described in Table 9-9.

Return to the Summary Table.

DO Driver current limit and auto-retry configuration

Figure 9-7. DO_CURLIM Register

7	6	5	4	3	2	1	0
DO_CUR_LIM			DO_BL_TIME		DO_RETRY_TIME		DO_RETRY_EN
R/W-001b			R/W-00b		R/W-00b		R/W-0b

Table 9-9. DO_CURLIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	DO_CUR_LIM	R/W	001b	Sets current limits 000b = 35 mA (min) 001b = 50 mA (min) 010b = 100 mA (min) 011b = 150 mA (min) 100b = 200 mA (min) 101b = 250 mA (min) 110b = 300 mA (min) 111b = 500 mA (min)
4-3	DO_BL_TIME	R/W	00b	Sets current blanking time. NOTE: It is not recommended to configure 0b11 (no blanking time) when Auto retry is enabled. 00b = 200 µs (typ) 01b = 500 µs (typ) 10b = 5 ms (typ) 11b = 0 s (no blanking time)
2-1	DO_RETRY_TIME	R/W	00b	Sets auto re-try time NOTE: It is not recommended to enable auto retry when blanking time is configured to 2b11 (no blanking time) . 00b = 50 ms (typ) 01b = 100 ms (typ) 10b = 200 ms (typ) 11b = 500 ms (typ)
0	DO_RETRY_EN	R/W	0b	Enable auto re-try 0b = Disabled 1b = Enabled

9.8 DEVICE_ID Register (Address = 7h) [Reset = 01h]

DEVICE_ID is shown in Figure 9-8 and described in Table 9-10.

Return to the Summary Table.

Figure 9-8. DEVICE_ID Register

7	6	5	4	3	2	1	0
RESERVED					Revision ID		
R-0b					R-001b		

Table 9-10. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved
2-0	Revision ID	R	001b	Indicates the device revision number 001b = 1st revision

9.9 INT_MASK Register (Address = 8h) [Reset = 00h]

INT_MASK is shown in Figure 9-9 and described in Table 9-11.

Return to the Summary Table.

Interrupt masking registers. When an interrupt is masked, the interrupt pin does not indicate the interrupt but the interrupt register is still updated to indicate the interrupt.

Figure 9-9. INT_MASK Register

7	6	5	4	3	2	1	0
TSD_INT_MASK	WU_INT_MASK	DO_FAULT_INT_MASK	CQ_FAULT_INT_MASK	LPW_INT_MASK	RESERVED	UV_V5_INT_MASK	TEMP_WARN_MASK
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b

Table 9-11. INT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSD_INT_MASK	R/W	0b	0b = Interrupt active 1b = Interrupt masked
6	WU_INT_MASK	R/W	0b	0b = Interrupt active 1b = Interrupt masked
5	DO_FAULT_INT_MASK	R/W	0b	0b = Interrupt active 1b = Interrupt masked
4	CQ_FAULT_INT_MASK	R/W	0b	0b = Interrupt active 1b = Interrupt masked
3	LPW_INT_MASK	R/W	0b	0b = Interrupt active 1b = Interrupt masked
2	RESERVED	R	0b	Reserved
1	UV_V5_INT_MASK	R/W	0b	0b = Interrupt active 1b = Interrupt masked
0	TEMP_WARN_MASK	R/W	0b	0b = Interrupt active 1b = Interrupt masked

9.10 RESET_CONFIG Register (Address = 9h) [Reset = 00h]

RESET_CONFIG is shown in Figure 9-10 and described in Table 9-12.

Return to the Summary Table.

Configures the behavior of the RESET pin

Figure 9-10. RESET_CONFIG Register

7	6	5	4	3	2	1	0
RESET_SEL		RESET_POL	RESERVED				
R/W-00b		R-0b	R-0b				

Table 9-12. RESET_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESET_SEL	R/W	00b	Selects which events will activate the reset output 00b = Both UVLP and UVOUT 01b = UVLP 10b = UVOUT 11b = Reserved
5	RESET_POL	R	0b	Selects between active low and active high configuration for reset output 0b = Pin output low (active-low) 1b = Pin output high (active-high)
4-0	RESERVED	R	0b	Reserved

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

Changes from Revision * (September 2024) to Revision A (December 2024)	Page
• Changed the document status from Advanced Information to *Production* data	1

12 Mechanical, Packaging, and Orderable Information

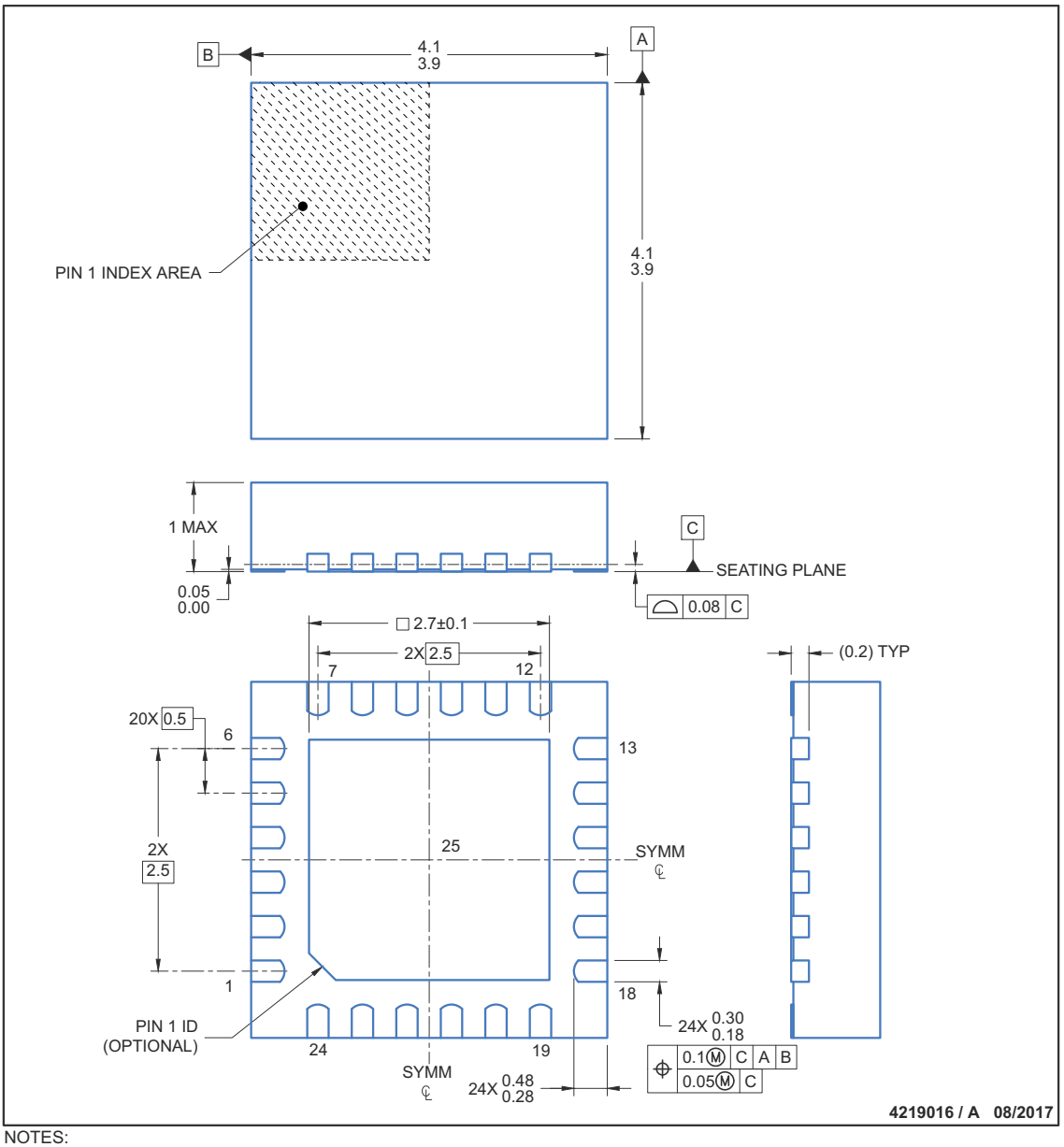
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Mechanical Data

PACKAGE OUTLINE

RGE0024H — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

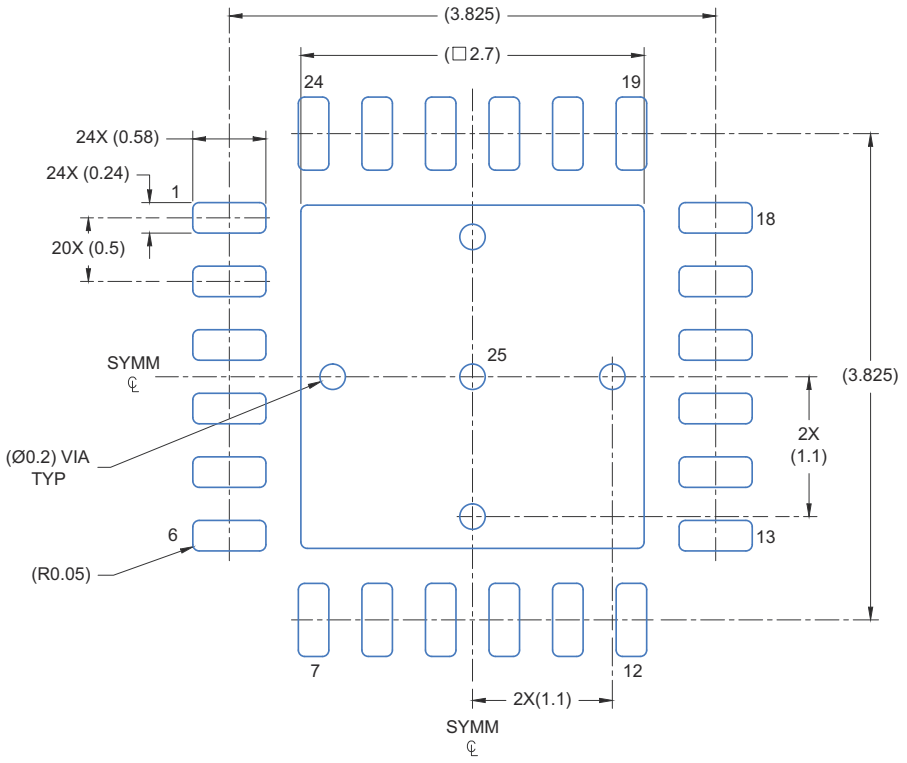
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

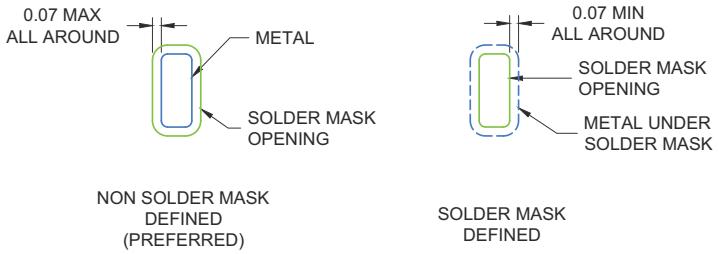
RGE0024H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

4219016 / A 08/2017

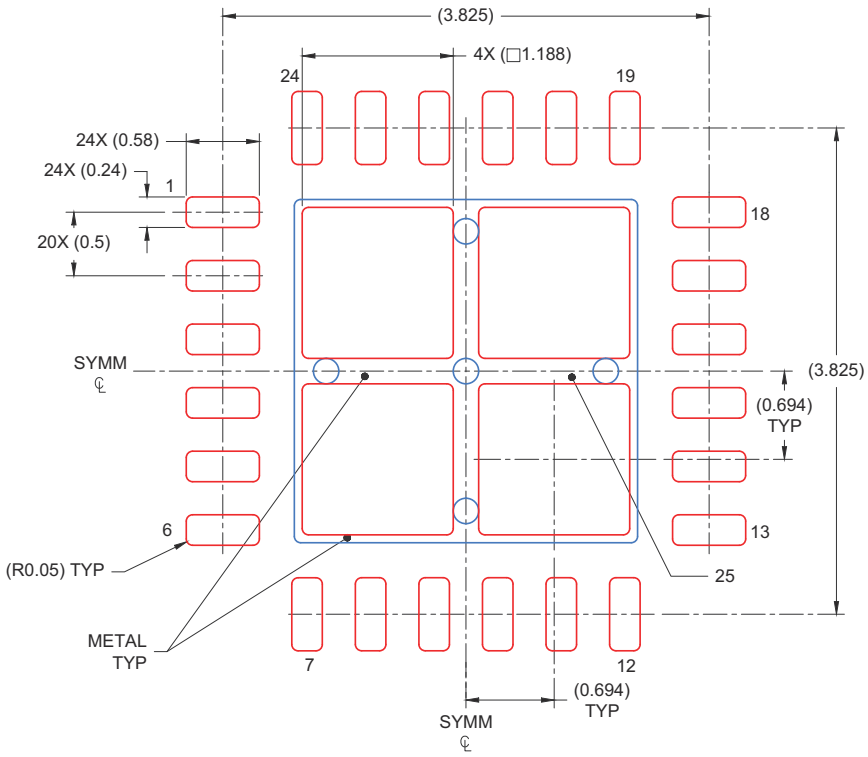
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RGE0024H — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

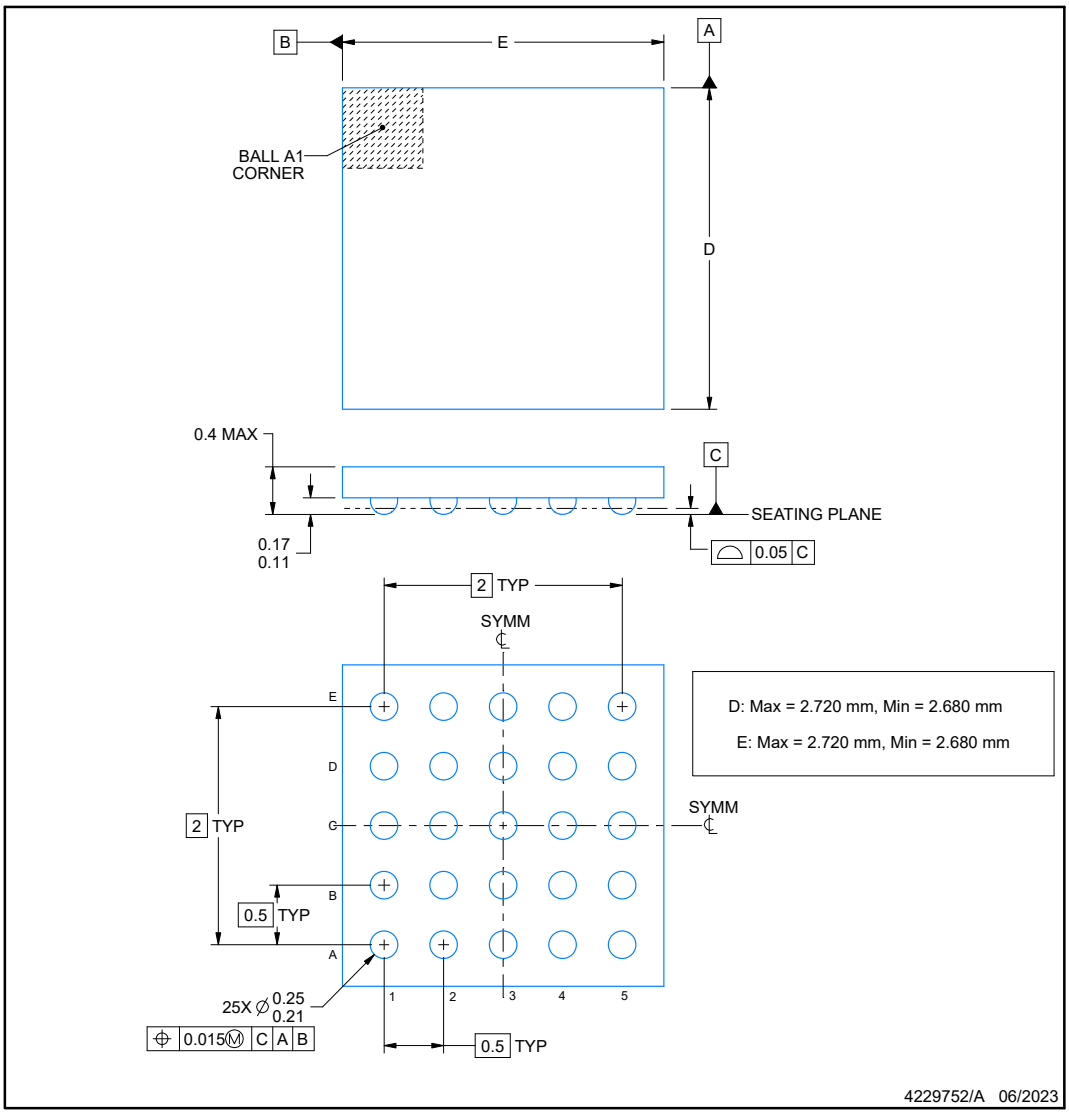
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

PACKAGE OUTLINE

YAH0025-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

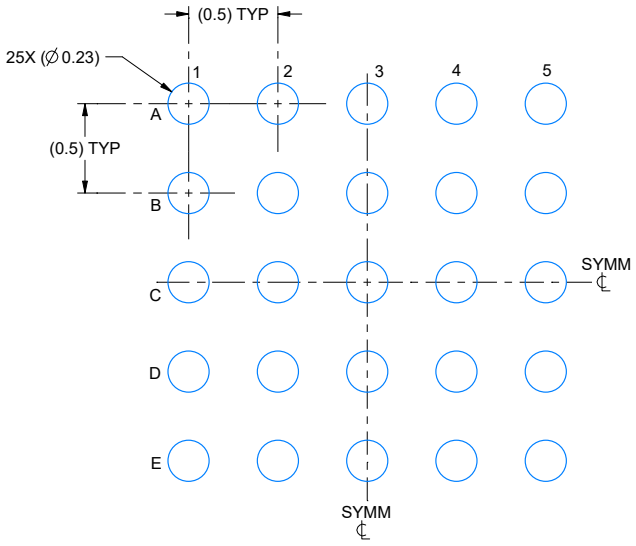
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

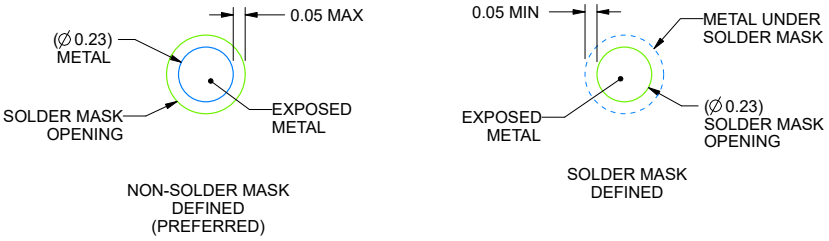
YAH0025-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

4229752/A 06/2023

NOTES: (continued)

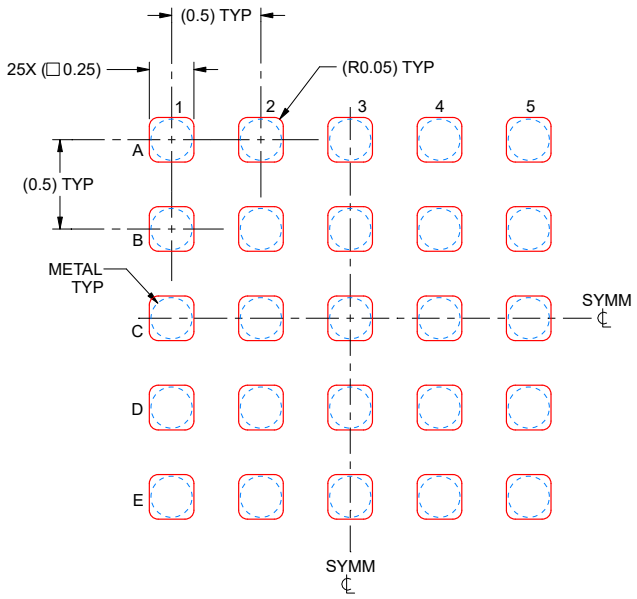
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YAH0025-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 30X

4229752/A 06/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TIOL221RGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TIOL 221
TIOL221RGER.A	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TIOL 221

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

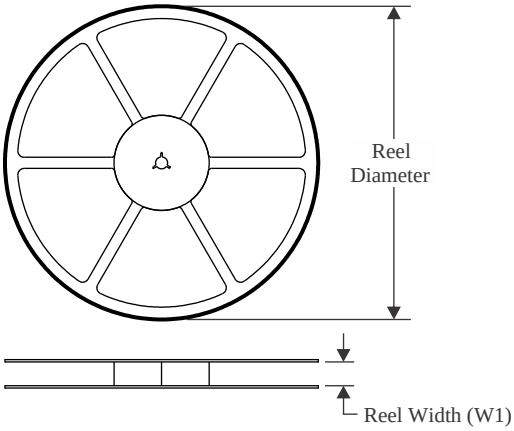
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

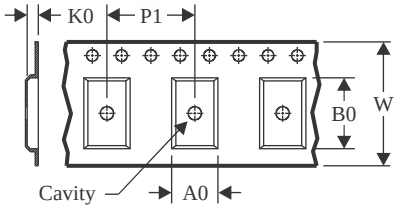
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

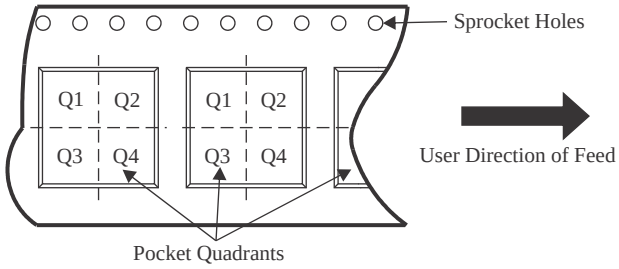


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

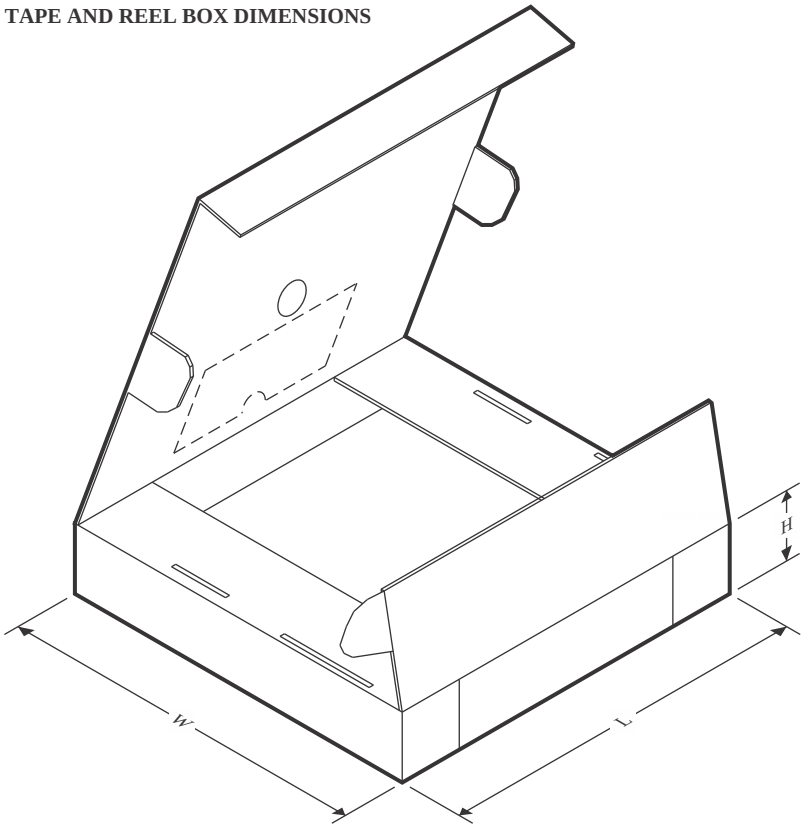
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TIOL221RGER	VQFN	RGE	24	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TIOL221RGER	VQFN	RGE	24	5000	367.0	367.0	35.0

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