# THVD24x2 ±70V Fault-Protected 3V to 5.5V Full Duplex RS-485 Transceivers With IEC ESD

## 1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A and TIA/EIA-422B standards
- 3V to 5.5V supply voltage
- Differential output exceeds 2.1V for PROFIBUS compatibility with 5V supply
- Bus I/O protection
  - ±70V DC bus fault
  - ±16kV HBM ESD
  - ±8kV IEC 61000-4-2 contact discharge
  - ±8kV IEC 61000-4-2 air-gap discharge
  - ±4kV IEC 61000-4-4 fast transient burst
- Full-duplex devices available in two speed grades
  - THVD2412: 250kbps
  - THVD2442: 20Mbps
- Extended ambient temperature range: -40°C to 125°C
- Extended operational common-mode range: ±25V
- Enhanced receiver hysteresis for noise immunity
- Low power consumption
  - Low shutdown supply current: < 10μA
  - Current during operation: < 5.6mA
- Glitch-free power-up/down for hot plug-in capability
- Open, short, and idle bus failsafe
- Thermal shutdown
- 1/8 unit load (up to 256 bus nodes) in - 7V to 12V common mode range
- Small 3mm x 3mm VSON package to save board space

## 2 Applications

- Motor drives
- Factory automation and control
- HVAC systems
- Building automation
- Grid infrastructure
- Electricity meters
- Process analytics
- Video surveillance

## 3 Description

THVD2412 and THVD2442 are ±70V fault-protected, full-duplex, RS-422/RS-485 transceivers operating on a single 3V to 5.5V supply. Bus interface pins are protected against overvoltage conditions during all modes of operation ensuring robust communication in rugged industrial environments.

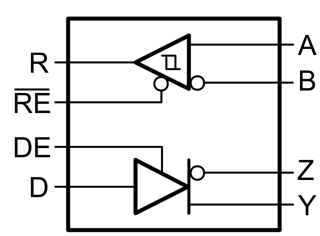
These devices feature integrated IEC ESD protection, eliminating the need for external system-level protection components. Extended ±25V input common-mode range ensures reliable data communication over longer cable run lengths and/or in the presence of large ground loop voltages. Enhanced 250mV receiver hysteresis provides high noise rejection. In addition, the receiver fail-safe feature provides a logic high when the bus inputs are open or shorted together.

THVD24x2 devices are available in small and thermally efficient VSON packages for space-constrained applications. These devices are characterized over ambient temperature from –40°C to 125°C.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| THVD2412<br>THVD2442 | VSON (10) | 3mm × 3mm |

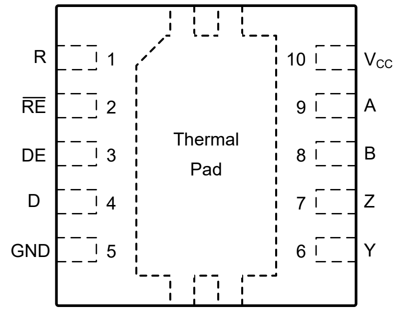
(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**THVD2412 and THVD2442 Simplified Schematic**

# Table of Contents

# 4 Pin Configuration and Functions




Not to scale

**Figure 4-1. DRC (VSON), 10-Pin Package, Top View**

**Table 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | DRC | | |
| R | 1 | Digital output | Receive data output |
| $\overline{RE}$ | 2 | Digital input | Receiver enable input; integrated weak pull-up (~2 MΩ) |
| DE | 3 | Digital input | Driver enable input; integrated weak pull-down (~2 MΩ) |
| D | 4 | Digital input | Transmission data input; integrated weak pull-up (~2 MΩ) |
| GND | 5 | Ground | Local Device ground |
| Y | 6 | Bus output | Driver non-inverting output |
| Z | 7 | Bus output | Driver inverting output |
| B | 8 | Bus input | Receiver inverting bus input |
| A | 9 | Bus input | Receiver non-inverting bus input |
| $V_{CC}$ | 10 | Power | 3 V to 5.5 V supply voltage |
| Thermal Pad | — | — | No electrical connection. Should be connected to GND plane for optimal thermal performance |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | –0.5 | 6.5 | V |
| Bus voltage | Range at any bus pin as differential or common-mode with respect to GND | –70 | 70 | V |
| Input voltage | Range at any logic pin (D, DE, or $\overline{RE}$) | –0.3 | 5.7 | V |
| Receiver output current | $I_O$ | –24 | 24 | mA |
| Storage temperature | $T_{stg}$ | –65 | 170 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | Bus terminals and GND | ±16,000 | V |
| | | | All pins except bus terminals and GND | ±4,000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | | ±1,500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 ESD Ratings [IEC]

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ [1] | Electrostatic discharge | Contact discharge, per IEC 61000-4-2 | Bus terminals and GND | ±8,000 | V |
| | | Air-gap discharge, per IEC 61000-4-2 | Bus terminals and GND | ±8,000 | |
| $V_{(EFT)}$ | Electrical fast transient | Per IEC 61000-4-4 | Bus terminals | ±4,000 | V |

(1) For optimised IEC ESD performance, it is recommended to have series resistor (≥ 50 Ω) on all logic inputs to minimize transient currents going into or out of the logic pins.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | | 5.5 | V |
| $V_I$ | Input voltage at any bus terminal (separately or common mode)[(1)] | | –25 | | 25 | V |
| $V_{IH}$ | High-level input voltage (driver, driver enable, and receiver enable inputs) | | 2 | | 5.5 | V |
| $V_{IL}$ | Low-level input voltage (driver, driver enable, and receiver enable inputs) | | 0 | | 0.8 | V |
| $V_{ID}$ | Differential input voltage bus pins | | –25 | | 25 | V |
| $I_O$ | Output current, driver | | –60 | | 60 | mA |
| $I_{OR}$ | Output current, receiver | | –8 | | 8 | mA |
| $R_L$ | Differential load resistance | | 54 | 60 | | Ω |
| $1/t_{UI}$ | Signaling rate | THVD2412 | | | 250 | kbps |
| | | THVD2442 | | | 20 | Mbps |
| $T_A$ | Operating ambient temperature | | -40 | | 125 | °C |
| $T_J$ | Junction temperature | | -40 | | 150 | °C |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## 5.5 Thermal Information

| THERMAL METRIC[(1)] | | THVD2412 THVD2442 | UNIT |
|---|---|---|---|
| | | DRC (VSON) | |
| | | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 46.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 47.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 19.1 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.7 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 19.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 4.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.6 Power Dissipation

| PARAMETER | | TEST CONDITIONS | | | VALUE | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Driver and receiver enabled, loopback (connect A to Y, B to Z) $V_{CC}$ = 5.5 V, $T_A$ = 125 °C, random data (PRBS7) at signaling rate | Unterminated $R_L$ = 300 Ω, $C_L$ = 50 pF (driver) | THVD2412 | 250 kbps | 258 | mW |
| | | | THVD2442 | 20 Mbps | 335 | |
| | | RS-422 load $R_L$ = 100 Ω, $C_L$ = 50 pF (driver) | THVD2412 | 250 kbps | 273 | mW |
| | | | THVD2442 | 20 Mbps | 325 | |
| | | RS-485 load $R_L$ = 54 Ω, $C_L$ = 50 pF (driver) | THVD2412 | 250 kbps | 315 | mW |
| | | | THVD2442 | 20 Mbps | 355 | |

## 5.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Driver** | | | | | | |
| $\|V_{OD}\|$ | Driver differential output voltage magnitude | $R_L$ = 60 Ω, –25 V ≤ $V_{test}$ ≤ 25 V, See Figure 6-1 | 1.5 | 2.8 | | V |
| | | $R_L$ = 60 Ω, –25 V ≤ $V_{test}$ ≤ 25 V, 4.5 V ≤ $V_{CC}$ ≤ 5.5 V, See Figure 6-1 | 2.1 | 3.3 | | V |
| | | $R_L$ = 100 Ω, See Figure 6-2 | 2 | 2.9 | | V |
| | | $R_L$ = 54 Ω, See Figure 6-2 | 1.5 | 2.5 | | V |
| $Δ\|V_{OD}\|$ | Change in differential output voltage | $R_L$ = 54 Ω or 100 Ω, See Figure 6-2 | –50 | | 50 | mV |
| $V_{OC}$ | Common-mode output voltage | $R_L$ = 54 Ω or 100 Ω, See Figure 6-2 | 1 | $V_{CC}/2$ | 3 | V |
| $ΔV_{OC(SS)}$ | Change in steady-state common-mode output voltage | $R_L$ = 54 Ω or 100 Ω, See Figure 6-2 | –50 | | 50 | mV |
| $I_{OS}$ | Short-circuit output current | DE = $V_{CC}$, -70 V ≤ ($V_Y$ or $V_Z$) ≤ 70 V, or Y shorted to Z | –250 | | 250 | mA |
| **Receiver** | | | | | | |
| $I_I$ | Bus input current | DE = 0 V, $V_{CC}$ = 0 V or 5.5 V; DE = 0 V, $V_{CC}$ = 0 V or 5.5 V; $V_I$ = 12 V | | 75 | 125 | µA |
| | | $V_I$ = 25 V | | 200 | 250 | µA |
| | | $V_I$ = –7 V | –100 | –60 | | µA |
| | | $V_I$ = –25 V | –350 | –350 | | µA |
| $V_{TH+}$ | Positive-going input threshold voltage[1] | Over common-mode range of ± 25 V | 20 | 125 | 200 | mV |
| $V_{TH-}$ | Negative-going input threshold voltage[1] | Over common-mode range of ± 25 V | –200 | –125 | -20 | mV |
| $V_{HYS}$ | Input hysteresis | Over common-mode range of ± 25 V | | 250 | | mV |
| $V_{TH\_FSH}$ | Input fail-safe threshold | Over common-mode range of ± 25 V | –20 | | 20 | mV |
| $C_{A,B}$ | Input differential capacitance | Measured between A and B, f = 1 MHz | | 50 | | pF |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = –8 mA | $V_{CC}$ – 0.4 | $V_{CC}$ – 0.2 | | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 8 mA | | 0.2 | 0.4 | V |
| $I_{OZ}$ | Output high-impedance current | $V_O$ = 0 V or $V_{CC}$, $\overline{RE}$ = $V_{CC}$ | –1 | | 1 | µA |
| **Logic** | | | | | | |
| $I_{IN}$ | Input current (DE) | 3 V ≤ $V_{CC}$ ≤ 5.5 V, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | | | 5 | µA |
| $I_{IN}$ | Input current (D, $\overline{RE}$) | 3 V ≤ $V_{CC}$ ≤ 5.5 V, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | –5 | | | µA |
| **Thermal Protection** | | | | | | |
| $T_{SHDN}$ | Thermal shutdown threshold | Temperature rising | 150 | 170 | | °C |
| $T_{HYS}$ | Thermal shutdown hysteresis | | | 10 | | °C |
| **Supply** | | | | | | |
| $UV_{VCC(rising)}$ | Rising under-voltage threshold on $V_{CC}$ | | | 2.3 | 2.6 | V |
| $UV_{VCC(falling)}$ | Falling under-voltage threshold on $V_{CC}$ | | 1.95 | 2.2 | | V |
| $UV_{VCC(hys)}$ | Hysteresis on under-voltage of $V_{CC}$ | | | 150 | | mV |

## 5.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current (quiescent), $V_{CC}$ = 4.5 V to 5.5 V | Driver and receiver enabled | $\overline{RE}$ = 0 V, DE = $V_{CC}$, No load | | 3.5 | 5.3 | mA |
| | | Driver enabled, receiver disabled | $\overline{RE}$ = $V_{CC}$, DE = $V_{CC}$, No load | | 2.5 | 4.2 | mA |
| | | Driver disabled, receiver enabled | $\overline{RE}$ = 0 V, DE = 0 V, No load | | 1.8 | 2.4 | mA |
| | | Driver and receiver disabled | $\overline{RE}$ = $V_{CC}$, DE = 0 V, D = open, No load | | 0.1 | 7 | µA |
| $I_{CC}$ | Supply current (quiescent), $V_{CC}$ = 3 V to 3.6 V | Driver and receiver enabled | $\overline{RE}$ = 0 V, DE = $V_{CC}$, No load | | 3 | 4.1 | mA |
| | | Driver enabled, receiver disabled | $\overline{RE}$ = $V_{CC}$, DE = $V_{CC}$, No load | | 2 | 3 | mA |
| | | Driver disabled, receiver enabled | $\overline{RE}$ = 0 V, DE = 0 V, No load | | 1.6 | 2.2 | mA |
| | | Driver and receiver disabled | $\overline{RE}$ = $V_{CC}$, DE = 0 V, D = open, No load | | 0.1 | 5 | µA |

(1) Under any specific conditions, $V_{TH+}$ is specified to be at least $V_{HYS}$ higher than $V_{TH–}$.

## 5.8 Switching Characteristics_250kbps

250-kbps (THVD2412) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V , unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Driver** | | | | | | | |
| $t_r$, $t_f$ | Differential output rise/fall time | $R_L$ = 54 Ω, $C_L$ = 50 pF See Figure 6-3 | $V_{CC}$ = 3 to 3.6 V, Typical at 3.3V | 450 | 650 | 1200 | ns |
| | | | $V_{CC}$ = 4.5 to 5.5 V, Typical at 5 V | 500 | 710 | 1200 | ns |
| $t_{PHL}$, $t_{PLH}$ | Propagation delay | | $V_{CC}$ = 3 to 3.6 V, Typical at 3.3V | | 525 | 750 | ns |
| | | | $V_{CC}$ = 4.5 to 5.5 V, Typical at 5 V | | 560 | 770 | ns |
| $t_{SK(P)}$ | Pulse skew, $\|t_{PHL} – t_{PLH}\|$ | | $V_{CC}$ = 3 to 3.6 V, Typical at 3.3V | | 30 | 70 | ns |
| | | | $V_{CC}$ = 4.5 to 5.5 V, Typical at 5 V | | 30 | 70 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time | $\overline{RE}$ = X | See Figure 6-4 and Figure 6-5 | | 33 | 75 | ns |
| $t_{PZH}$, $t_{PZL}$ | Enable time | $\overline{RE}$ = 0 V | | | 400 | 280 | ns |
| | | $\overline{RE}$ = $V_{CC}$ | | | 2 | 4.5 | μs |
| $t_{SHDN}$ | Time to shutdown | $\overline{RE}$ = $V_{CC}$ | | 50 | | 500 | ns |
| **Receiver** | | | | | | | |
| $t_r$, $t_f$ | Output rise/fall time | $C_L$ = 15 pF | See Figure 6-6 | | 13 | 20 | ns |
| $t_{PHL}$, $t_{PLH}$ | Propagation delay | | | | 850 | 1270 | ns |
| $t_{SK(P)}$ | Pulse skew, $\|t_{PHL} – t_{PLH}\|$ | | | | 5 | 45 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time | DE = X | See Figure 6-7 | | 30 | 40 | ns |
| $t_{PZH(1)}$ | Enable time | DE = $V_{CC}$ | See Figure 6-7 | | 90 | 120 | ns |
| $t_{PZL(1)}$ | | | | | 900 | 1320 | ns |
| $t_{PZH(2)}$, $t_{PZL(2)}$ | Enable time | DE = 0 V | See Figure 6-8 | | 3.3 | 5.4 | μs |
| $t_{D(OFS)}$ | Delay to enter fail-safe operation | $C_L$ = 15 pF | See Figure 6-9 | 7 | 11 | 18 | μs |
| $t_{D(FSO)}$ | Delay to exit fail-safe operation | | | 540 | 850 | 1260 | ns |
| $t_{SHDN}$ | Time to shutdown | DE = 0 V | See Figure 6-8 | 50 | | 500 | ns |

## 5.9 Switching Characteristics_20Mbps

20-Mbps (THVD2442) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V, unless otherwise noted

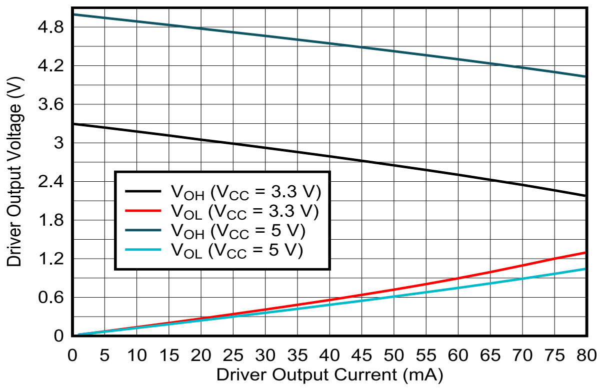
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Driver** | | | | | | | |
| $t_r$, $t_f$ | Differential output rise/fall time | $R_L$ = 54 Ω, $C_L$ = 50 pF See Figure 6-3 | $V_{CC}$ = 3 to 3.6 V, Typical at 3.3 V | 4 | 8 | 15 | ns |
| | | | $V_{CC}$ = 4.5 to 5.5 V, Typical at 5 V | 4 | 7 | 15 | ns |
| $t_{PHL}$, $t_{PLH}$ | Propagation delay | | $V_{CC}$ = 3 to 3.6 V, Typical at 3.3 V | 6 | 15 | 30 | ns |
| | | | $V_{CC}$ = 4.5 to 5.5 V, Typical at 5 V | 6 | 13 | 26 | ns |
| $t_{SK(P)}$ | Pulse skew, $\|t_{PHL} – t_{PLH}\|$ | | $V_{CC}$ = 3 to 3.6 V, Typical at 3.3 V | | 1 | 3 | ns |
| | | | $V_{CC}$ = 4.5 to 5.5 V, Typical at 5 V | | 1 | 3 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time | $\overline{RE}$ = X | See Figure 6-4 and Figure 6-5 | | 15 | 35 | ns |
| $t_{PZH}$, $t_{PZL}$ | Enable time | $\overline{RE}$ = 0 V | | | 8 | 39 | ns |
| | | $\overline{RE}$ = $V_{CC}$ | | | 2 | 4.5 | μs |
| $t_{SHDN}$ | Time to shutdown | $\overline{RE}$ = $V_{CC}$ | | 50 | | 500 | ns |

## 5.9 Switching Characteristics_20Mbps (continued)

20-Mbps (THVD2442) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V, unless otherwise noted

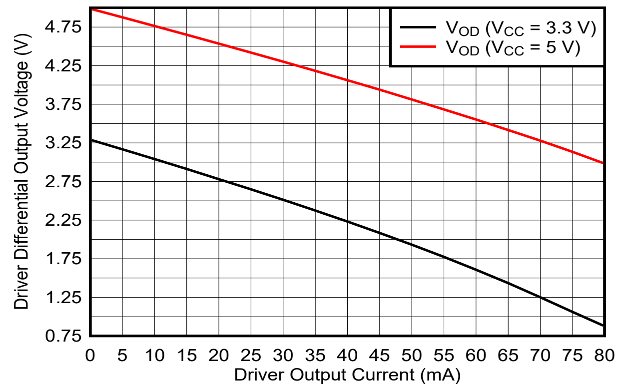
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Receiver** | | | | | | | |
| $t_r$, $t_f$ | Output rise/fall time | $C_L$ = 15 pF | See Figure 6-6 | | 1.5 | 6 | ns |
| $t_{PHL}$, $t_{PLH}$ | Propagation delay | | | | 40 | 57 | ns |
| $t_{SK(P)}$ | Pulse skew, $\|t_{PHL} – t_{PLH}\|$ | | | | | 5 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time | DE = X | See Figure 6-7 | | 11 | 25 | ns |
| $t_{PZH(1)}$, $t_{PZL(1)}$ | Enable time | DE = $V_{CC}$ | See Figure 6-7 | | 55 | 82 | ns |
| $t_{PZH(2)}$, $t_{PZL(2)}$ | Enable time | DE = 0 V | See Figure 6-8 | | 1.5 | 4.5 | μs |
| $t_{D(OFS)}$ | Delay to enter fail-safe operation | $C_L$ = 15 pF | See Figure 6-9 | 7 | 11 | 18 | μs |
| $t_{D(FSO)}$ | Delay to exit fail-safe operation | | | 22 | 25 | 50 | ns |
| $t_{SHDN}$ | Time to shutdown | DE = 0 V | See Figure 6-8 | 50 | | 500 | ns |

## 5.10 Typical Characteristics



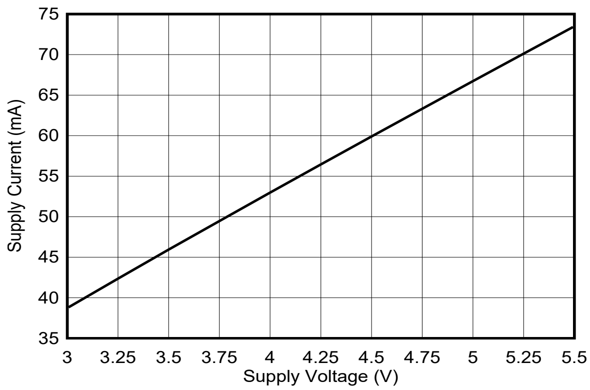

DE = $V_{CC}$ D = 0 V $T_A$ = 25 °C

**Figure 5-1. Driver Output Voltage vs Driver Output Current**




DE = $V_{CC}$ D = 0 V $T_A$ = 25 °C

**Figure 5-2. Driver Differential Output voltage vs Driver Output Current**




$T_A$ = 25 °C DE = D = $V_{CC}$ $R_L$ = 54 Ω

**Figure 5-3. Supply Current vs Supply Voltage**

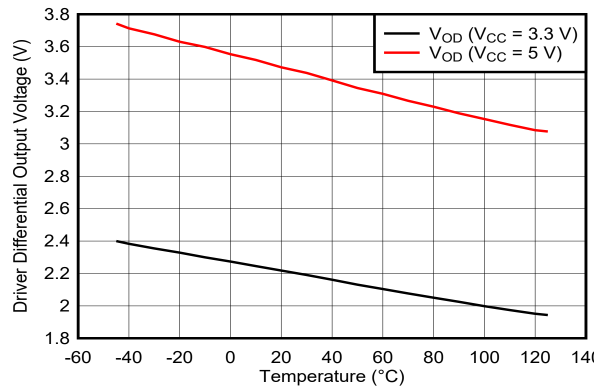
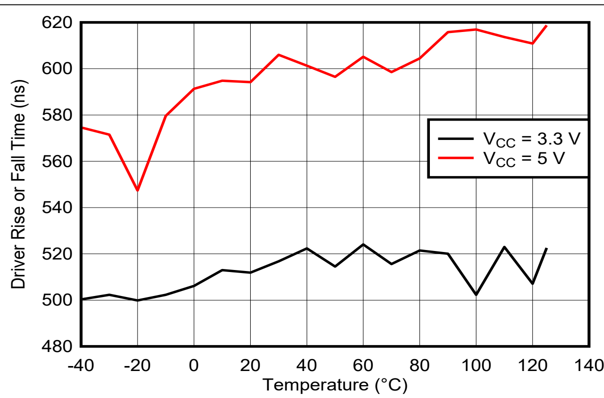
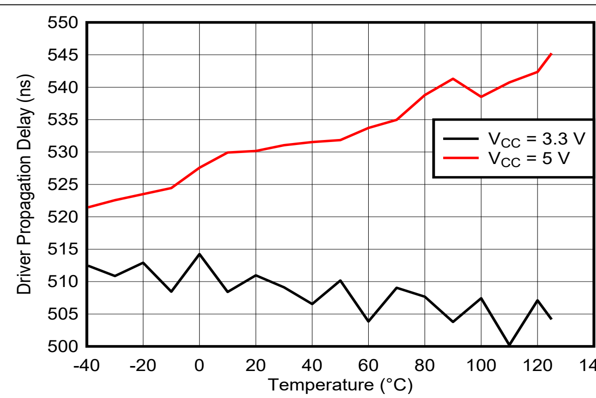



**Figure 5-4. Driver differential output voltage vs Temperature**




DE = $V_{CC}$ $R_L$ = 54 Ω $C_L$ = 50 pF

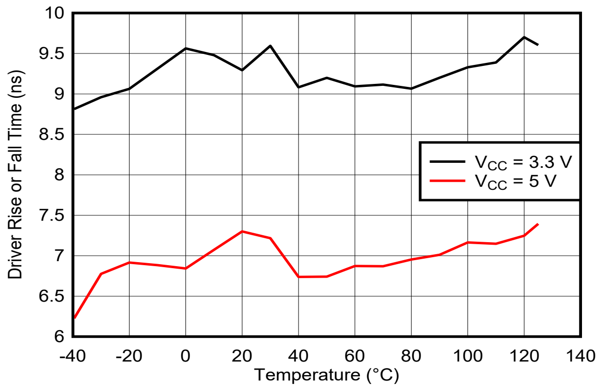
**Figure 5-5. THVD2412 250 kbps Driver Rise or Fall Time vs Temperature**




DE = $V_{CC}$ $R_L$ = 54 Ω $C_L$ = 50 pF

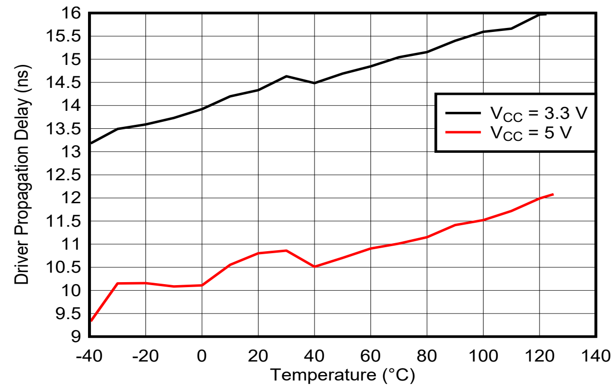
**Figure 5-6. THVD2412 250 kbps Driver Propagation Delay vs Temperature**

## 5.10 Typical Characteristics (continued)



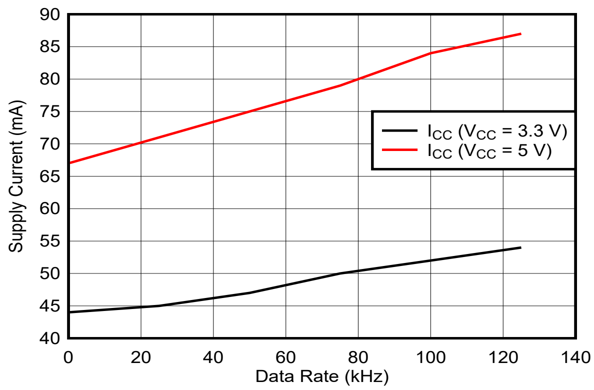

DE = $V_{CC}$ $R_L$ = 54 Ω $C_L$ = 50 pF

**Figure 5-7. THVD2442 20 Mbps Driver Rise or Fall Time vs Temperature**



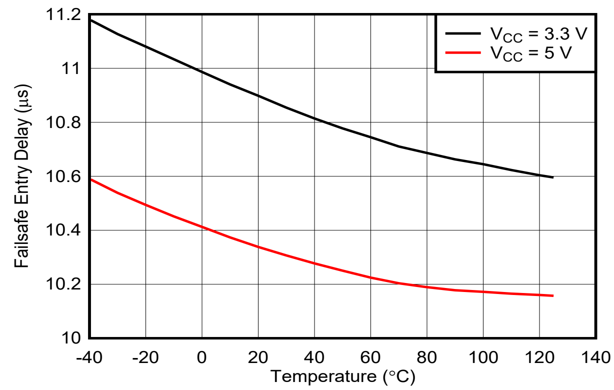

DE = $V_{CC}$ $R_L$ = 54 Ω $C_L$ = 50 pF

**Figure 5-8. THVD2442 20 Mbps Driver Propagation Delay vs Temperature**



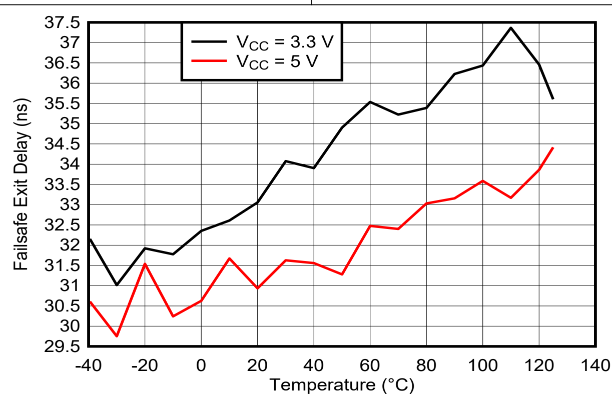

$T_A$ = 25 °C $R_L$ = 54 Ω DE = $V_{CC}$

**Figure 5-9. THVD2412 Supply Current vs Signal Rate**




$\overline{RE}$ = GND $C_{L(RXD)}$ = 15 pF

**Figure 5-10. Failsafe entry delay vs Temperature**




$\overline{RE}$ = GND $C_{L(RXD)}$ = 15 pF

**Figure 5-11. Failsafe exit delay vs Temperature**

# 6 Parameter Measurement Information

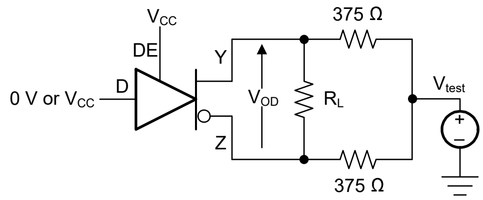



**Figure 6-1. Measurement of Driver Differential Output Voltage With Common-Mode Load**

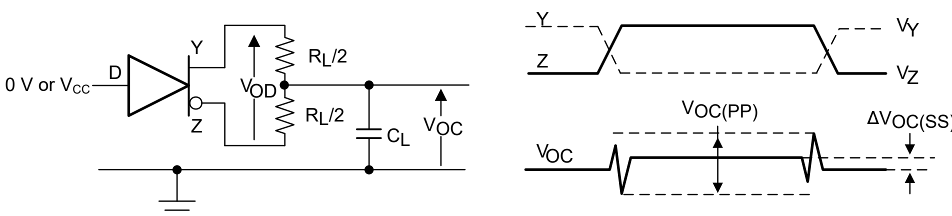



**Figure 6-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load**

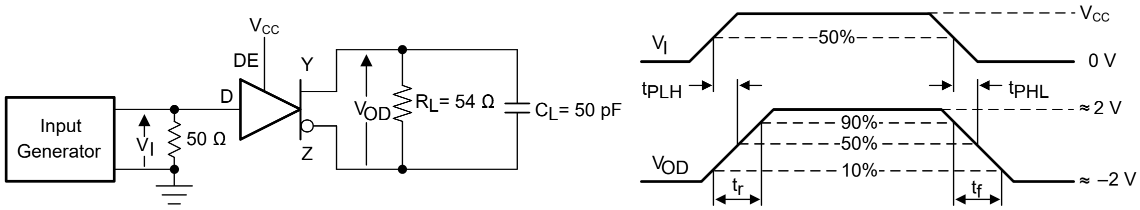



**Figure 6-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays**

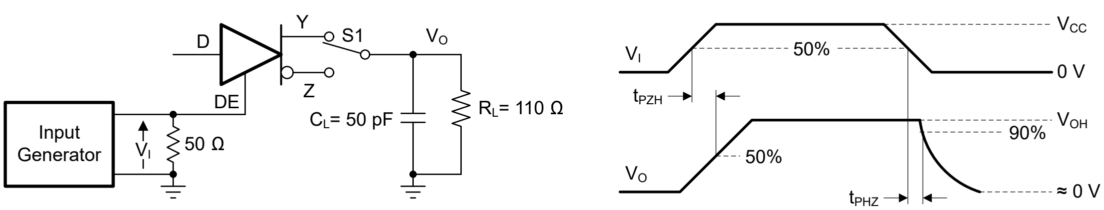



**Figure 6-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load**

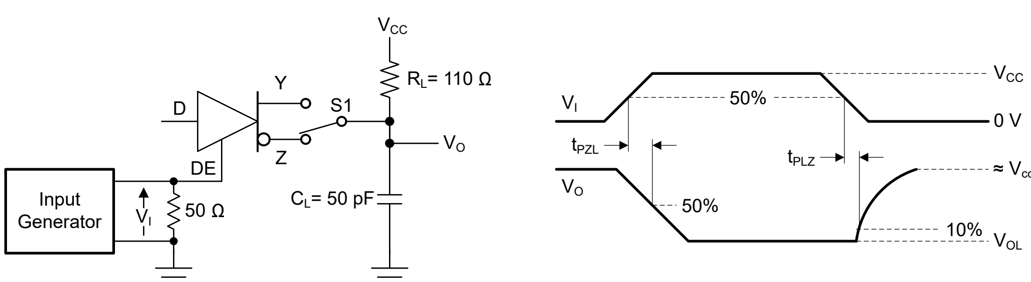



**Figure 6-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load**

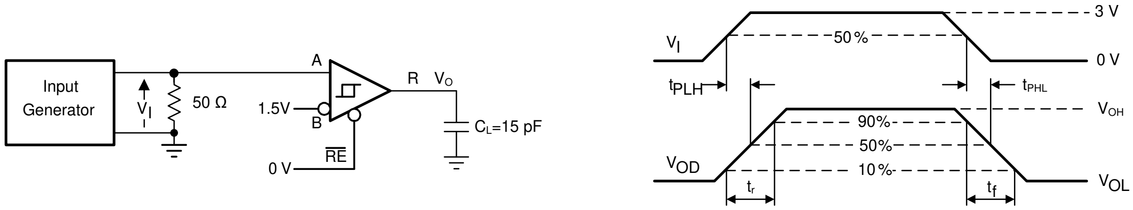



**Figure 6-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays**

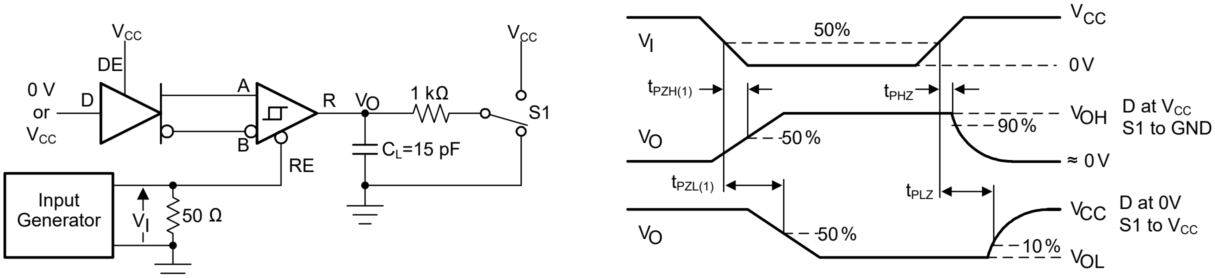
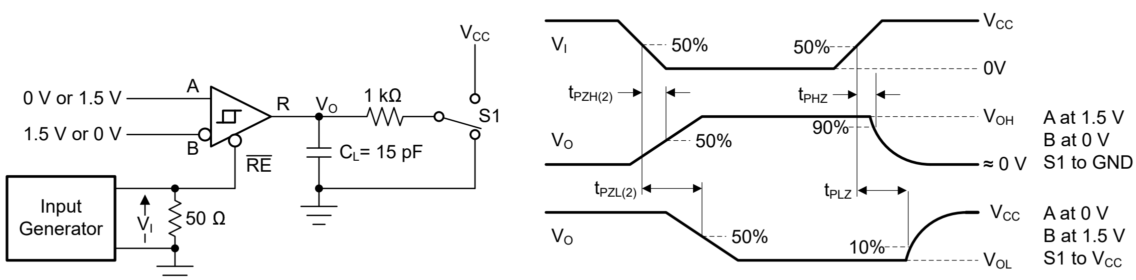



**Figure 6-7. Measurement of Receiver Enable/Disable Times With Driver Enabled**



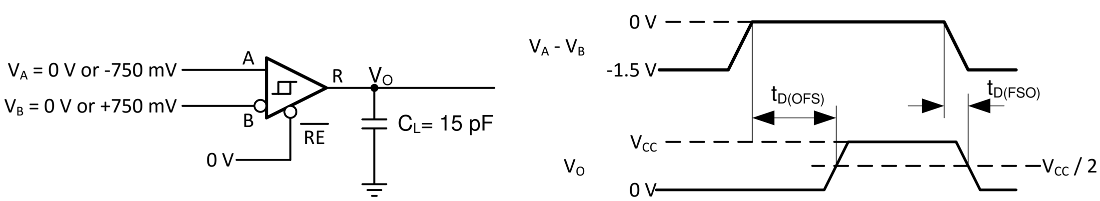




**Figure 6-8. Measurement of Receiver Enable Times With Driver Disabled**



**Figure 6-9. Measurement of Fail-Safe Delay**

# 7 Detailed Description

## 7.1 Overview

THVD2412 and THVD2442 are fault-protected, full-duplex RS-485/RS-422 transceivers available in 10-VSON package. THVD2412 allows for data transmission up to 250kbps, while THVD2442 is suitable for data transmission up to 20Mbps. The devices have active-high driver enable and active-low receiver enable. A shutdown current of less than 10µA can be achieved by disabling both driver and receiver.

## 7.2 Functional Block Diagrams

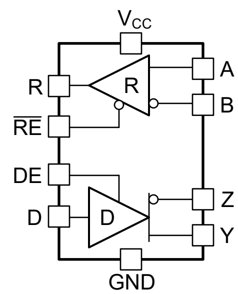



**Figure 7-1. THVD24x2 Block Diagram**

## 7.3 Feature Description

### 7.3.1 ±70-V Fault Protection

THVD24x2 transceivers have extended bus fault protection compared to standard RS-485 devices. Transceivers that operate in rugged industrial environments are often exposed to voltage transients greater than the -7 V to +12 V defined by the TIA/EIA-485A standard. To protect against such conditions, the generic RS-485 devices with lower absolute maximum ratings requires expensive external protection components. To simplify system design and reduce overall system cost, THVD24x2 devices are protected up to ±70 V without the need for any external components.

### 7.3.2 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±8 kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV. Bus structures also protect against electrical fast transients (EFT) according to IEC 61000-4-4 for up to ±4 kV. With careful system design, integrated bus structures can enable EFT Criterion A at the system level (minimum to no data loss when transient noise is present).

### 7.3.3 Driver Overvoltage and Overcurrent Protection

The THVD24x2 drivers are protected against any DC supply shorts in the range of -70 V to +70 V. The devices internally limit the short circuit current to ±250 mA to comply with the TIA/EIA-485A standard. In addition, a fold-back current limiting circuit reduces the driver short circuit current to less than ±5 mA if the output fault voltage exceeds |±25 V|.

If the junction temperature exceeds the $T_{SHDN}$ threshold due to excessive power dissipation, the devices feature thermal shutdown protection that disables the driver and the receiver

### 7.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD24x2 feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250 mV (typical) receiver hysteresis provides enhanced noise immunity. For THVD2412, typical 700 ns of glitch filter in receiver signal chain prevents high frequency noise pulses from the bus to appear on R pin.

### 7.3.5 Receiver Fail-Safe Operation

The receivers are fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFS)}$ at less than $|V_{TH\_FSH}|$.

### 7.3.6 Low-Power Shutdown Mode

Driving DE low and $\overline{RE}$ high for longer than 500 ns puts the devices into the shutdown mode. If either DE goes high or $\overline{RE}$ goes low, the counters reset. The devices does not enter the shutdown mode if the enable pins are in disable state for less than 50 ns. This feature prevents the devices from accidentally going into shutdown mode due to skew between DE and $\overline{RE}$.

## 7.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case, the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and $V_{OD}$ is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to $V_{CC}$, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

**Table 7-1. Driver Function Table**

| INPUT | ENABLE | OUTPUTS | | FUNCTION |
|---|---|---|---|---|
| D | DE | Y | Z | |
| H | H | H | L | Actively drive bus high |
| L | H | L | H | Actively drive bus low |
| X | L | Z | Z | Driver disabled |
| X | OPEN | Z | Z | Driver disabled by default |
| OPEN | H | H | L | Actively drive bus high by default |

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, $V_{TH+}$, the receiver output, R, turns high. When $V_{ID}$ is lower than the negative input threshold, $V_{TH-}$, the receiver output, R, turns low. If $V_{ID}$ is between $V_{TH+}$ and $V_{TH-}$, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of $V_{ID}$ are irrelevant. Internal biasing of the receiver inputs causes the output to go fail-safe high when the transceiver is disconnected from the bus (open-circuit), or the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

**Table 7-2. Receiver Function Table**

| DIFFERENTIAL INPUT | ENABLE | OUTPUT | FUNCTION |
|---|---|---|---|
| $V_{ID} = V_A – V_B$ | $\overline{RE}$ | R | |
| $V_{TH+} < V_{ID}$ | L | H | Receive valid bus high |
| $V_{TH-} < V_{ID} < V_{TH+}$ | L | ? | Indeterminate bus state |
| $V_{ID} < V_{TH-}$ | L | L | Receive valid bus low |
| X | H | Z | Receiver disabled |
| X | OPEN | Z | Receiver disabled by default |
| Open-circuit bus | L | H | Fail-safe high output |
| Short-circuit bus | L | H | Fail-safe high output |
| Idle (terminated) bus | L | H | Fail-safe high output |

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

THVD2412 and THVD2442 are fault-protected, full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For these devices, the driver and receiver enable pins allow for the configuration of different operating modes.

## 8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, $R_T$, whose value matches the characteristic impedance, $Z_0$, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

Also note that a full-duplex RS-485 transceiver can be used as a half-duplex transceiver in an application by externally connecting driver output pins Y and Z to receiver input pins A and B respectively.

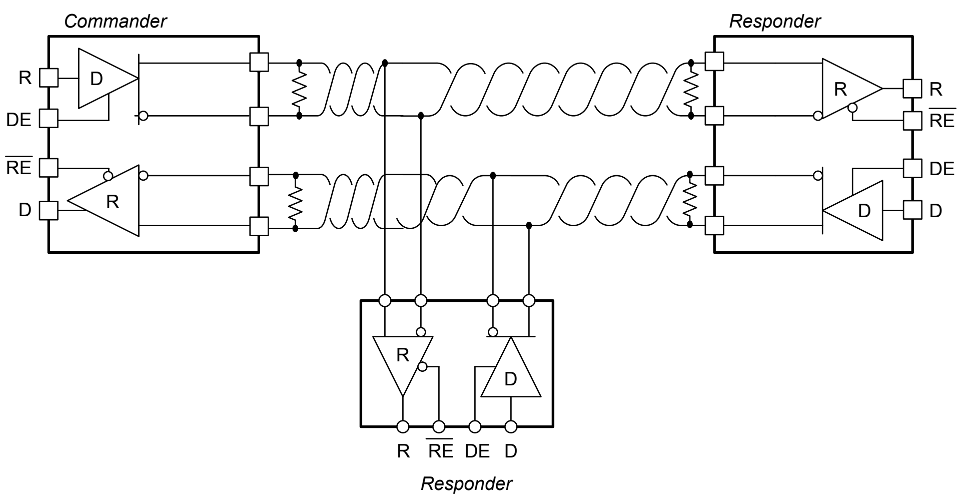



**Figure 8-1. Typical RS-485 Network With Full-Duplex Transceivers**

### 8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

#### *8.2.1.1 Data Rate and Bus Length*

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

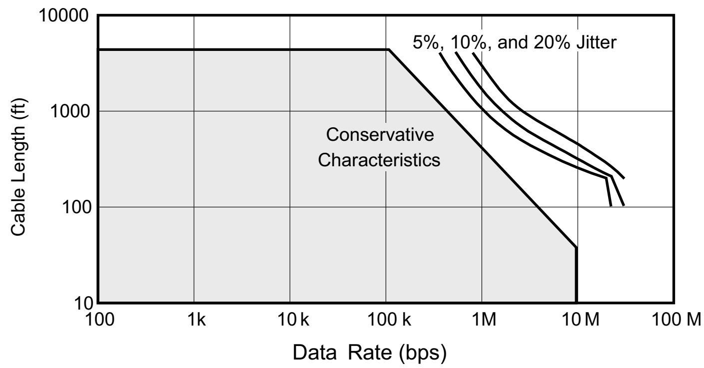



**Figure 8-2. Cable Length vs Data Rate Characteristic**

Even higher data rates are achievable (that is, 20 Mbps for the THVD2442) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

#### *8.2.1.2 Stub Length*

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- $t_r$ is the 10/90 rise time of the driver
- $c$ is the speed of light ($3 \times 10^8$ m/s)
- $v$ is the signal velocity of the cable or trace as a factor of $c$

#### *8.2.1.3 Bus Loading*

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD24x2 devices consist of 1/8 UL transceivers which is approximately 96 kΩ input impedance, connecting up to 256 receivers to the bus is possible for a limited common mode range of - 7 V to 12 V.

#### *8.2.1.4 Transient Protection*

The bus pins of the THVD24x2 transceivers include on-chip ESD protection against ±16-kV HBM and ±8-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

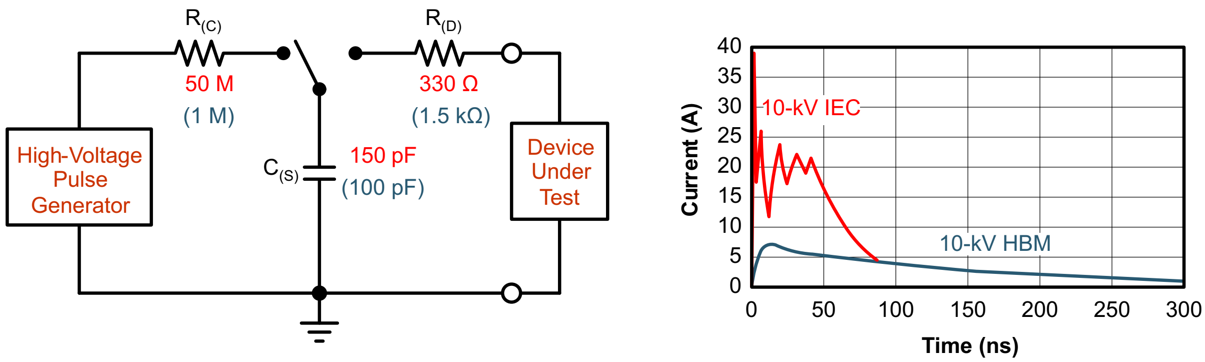



**Figure 8-3. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)**

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 8-4 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left side of Figure 8-4 shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right side of Figure 8-4 shows the pulse power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

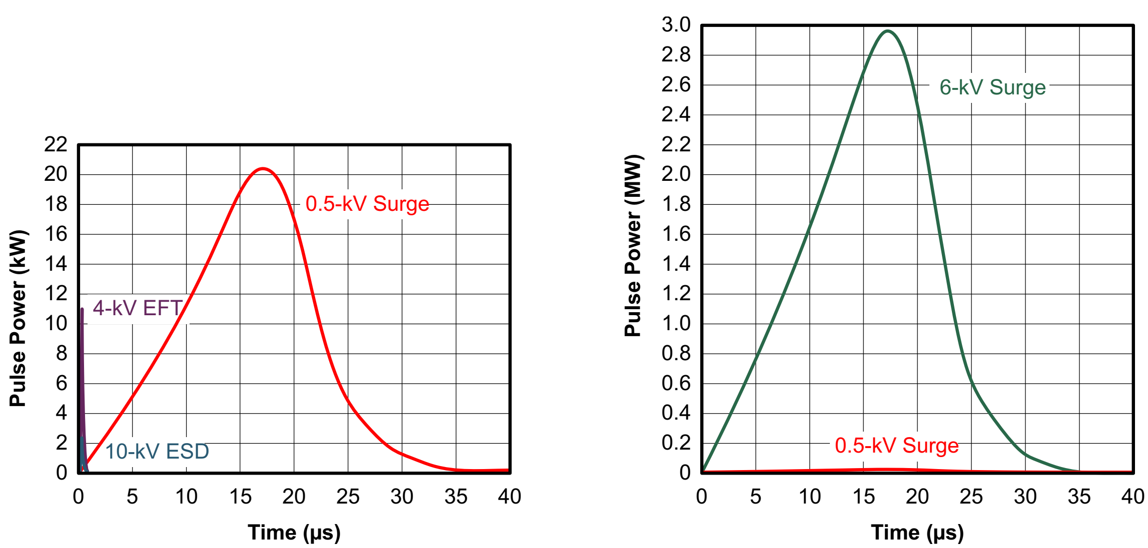



**Figure 8-4. Power Comparison of ESD, EFT, and Surge Transients**

For surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 8-5 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

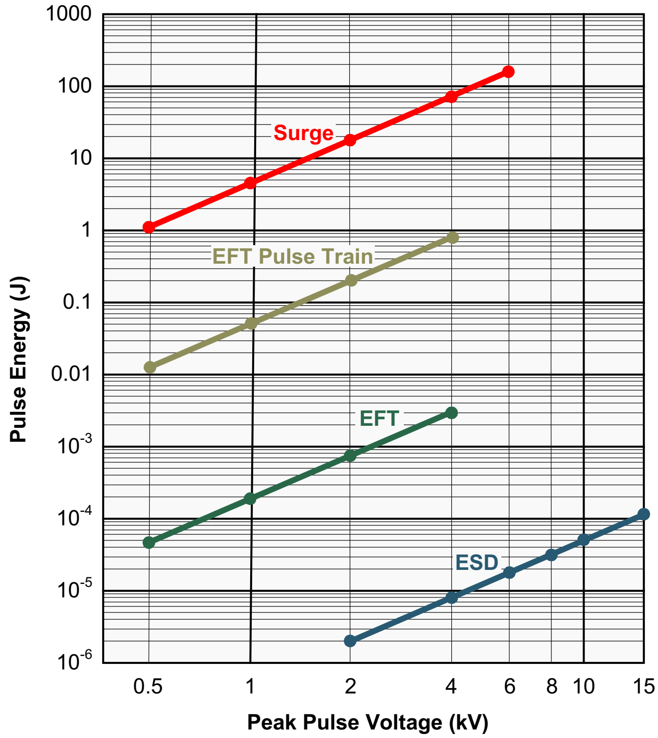



**Figure 8-5. Comparison of Transient Energies**

### 8.2.2 Detailed Design Procedure

Figure 8-6 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. Table 8-1 shows the associated bill of materials. SMAJ30CA TVS diodes are rated to operate up to 30 V. This makes sure the protection diodes do not conduct if a direct RS-485 bus shorts to 24-V DC industrial power rail.

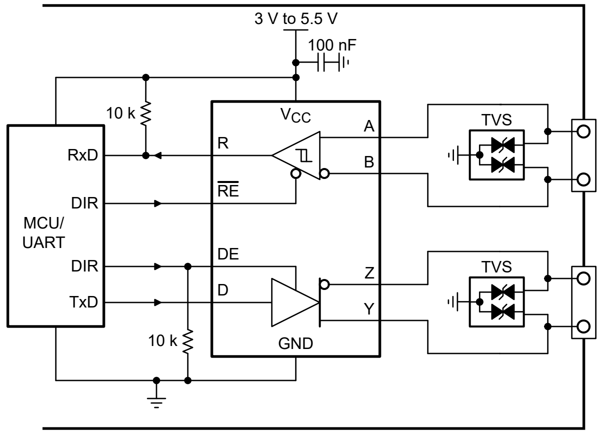


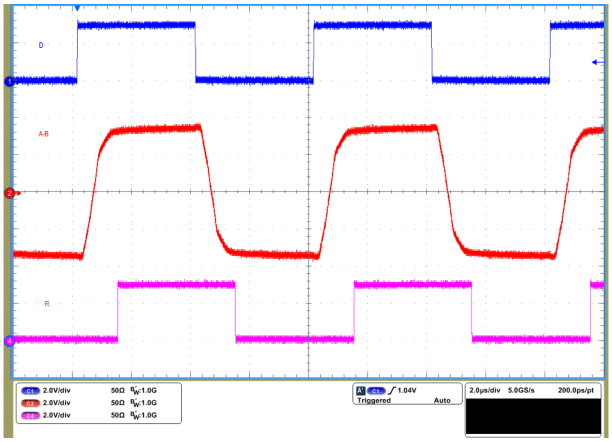

**Figure 8-6. Transient Protection Against Surge Transients for Half-Duplex Devices**

**Table 8-1. Components List**

| DEVICE | FUNCTION | ORDER NUMBER | MANUFACTURER |
|---|---|---|---|
| XCVR | RS-485 transceiver | THVD2412 or THVD2442 | TI |
| TVS | Bidirectional 400-W transient suppressor | SMAJ30CA | Littelfuse(1) |

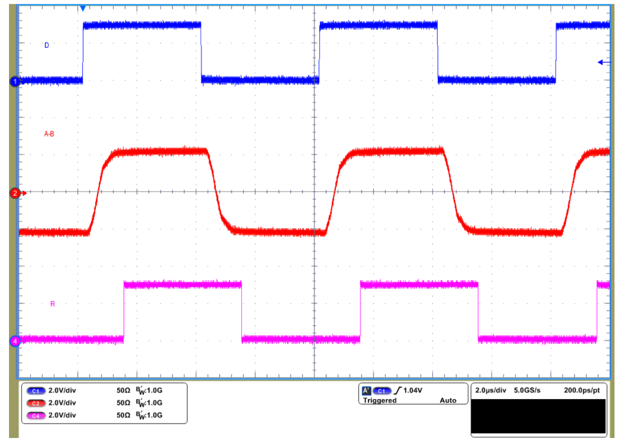
(1) See Third-Party Products

### 8.2.3 Application Curves




THVD2412 $V_{CC}$ = 5 V $R_L$ = 54 Ω
50% duty square wave on D pin at 250 kbps DE = $V_{CC}$

**Figure 8-7. THVD2412 Waveforms at $V_{CC}$ = 5 V**




THVD2412 $V_{CC}$ = 3.3 V $R_L$ = 54 Ω
50% duty square wave on D pin at 250 kbps DE = $V_{CC}$

**Figure 8-8. THVD2412 Waveforms at $V_{CC}$ = 3.3 V**

## 8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, $V_{CC}$ supply can be decoupled with a 100nF ceramic capacitor located as close to the device supply pin as possible. This reduces supply voltage ripple present on the outputs of switched-mode power supplies, and compensates for the resistance and inductance of the PCB power planes.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3MHz to 300MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use $V_{CC}$ and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100nF to 220nF decoupling capacitors as close as possible to the $V_{CC}$ pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for $V_{CC}$ and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1kΩ to 10kΩ pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.

### 8.4.2 Layout Example

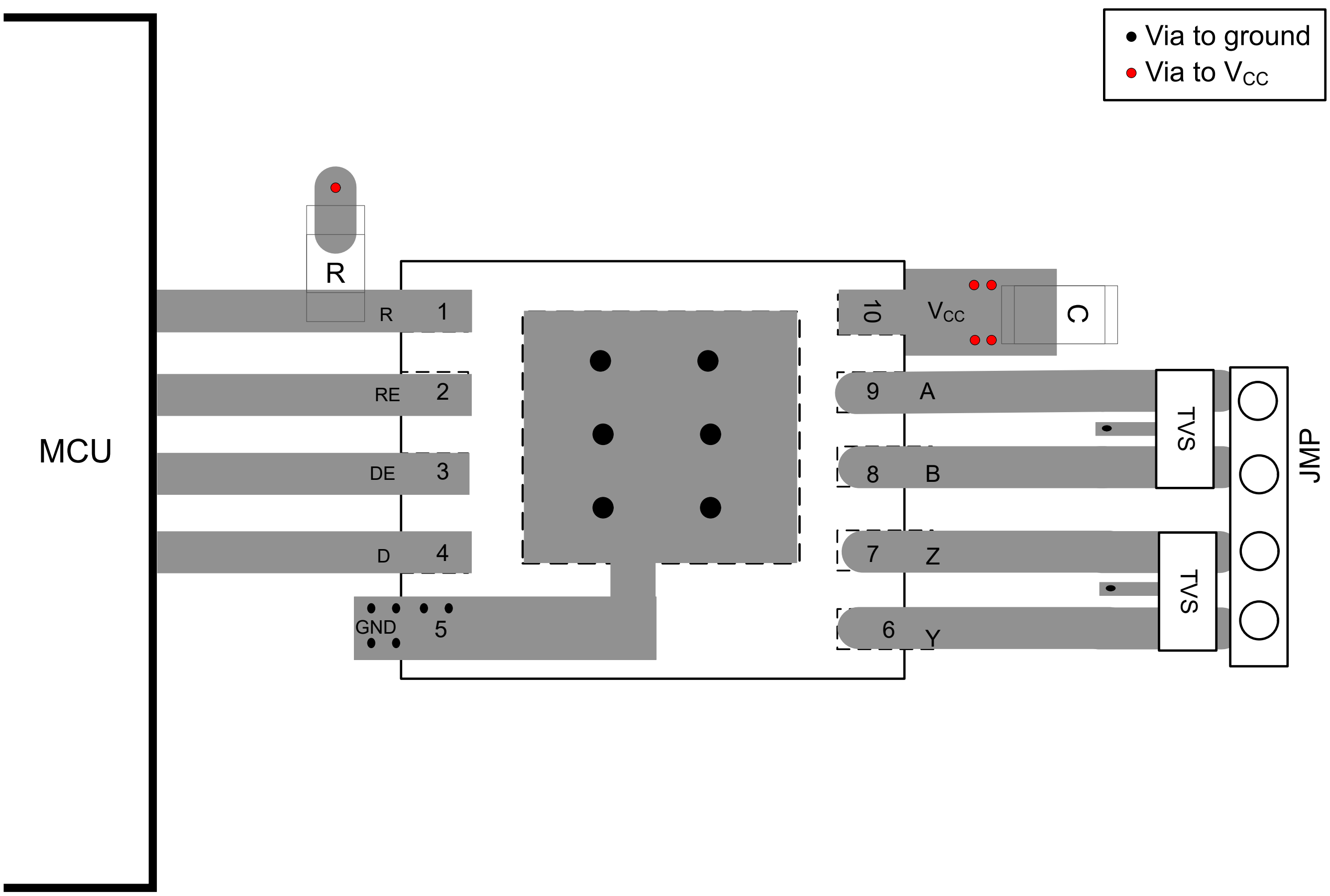



**Figure 8-9. Full-Duplex Layout Example**

# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision * (November 2023) to Revision A (March 2024)** — **Page**

- Revision A is the first public release of the datasheet.......................................................................... 1

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| THVD2412DRCR | Active | Production | VSON (DRC) \| 10 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2412 |
| THVD2412DRCR.A | Active | Production | VSON (DRC) \| 10 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2412 |
| THVD2442DRCR | Active | Production | VSON (DRC) \| 10 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2442 |
| THVD2442DRCR.A | Active | Production | VSON (DRC) \| 10 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2442 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

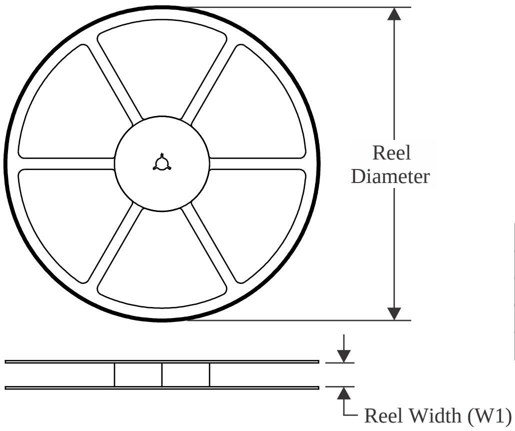
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

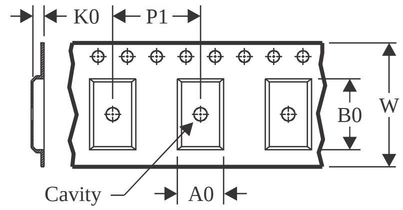
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

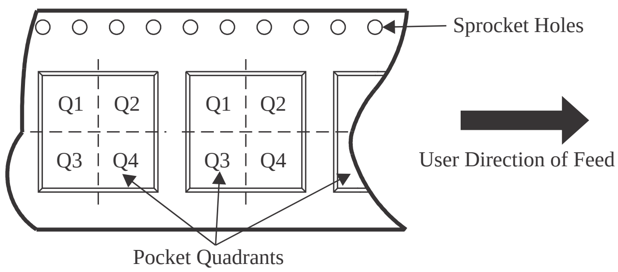



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

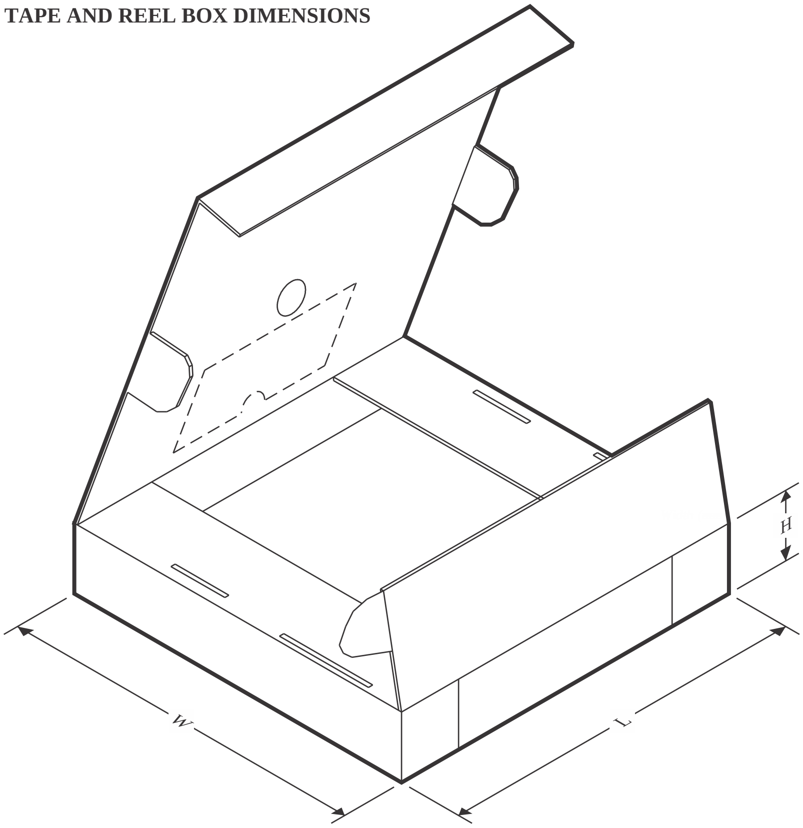
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THVD2412DRCR | VSON | DRC | 10 | 5000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| THVD2442DRCR | VSON | DRC | 10 | 5000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

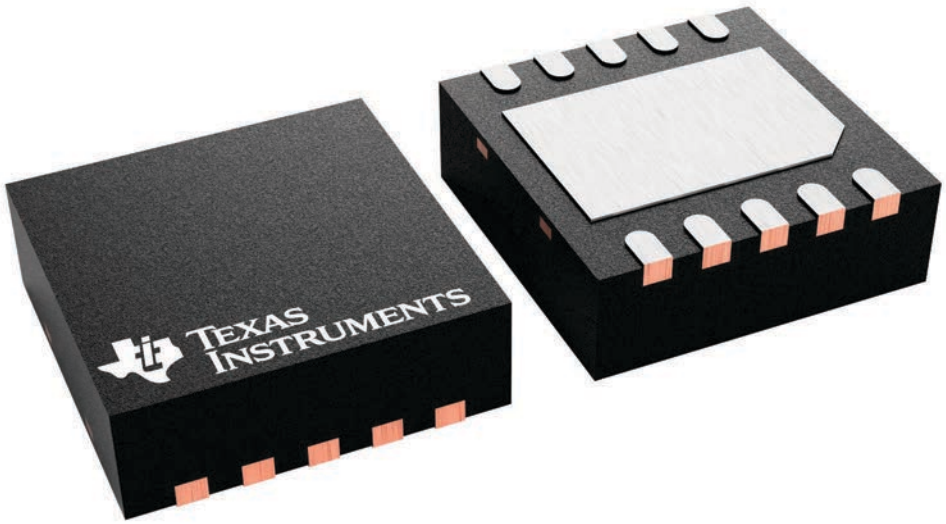
TAPE AND REEL BOX DIMENSIONS

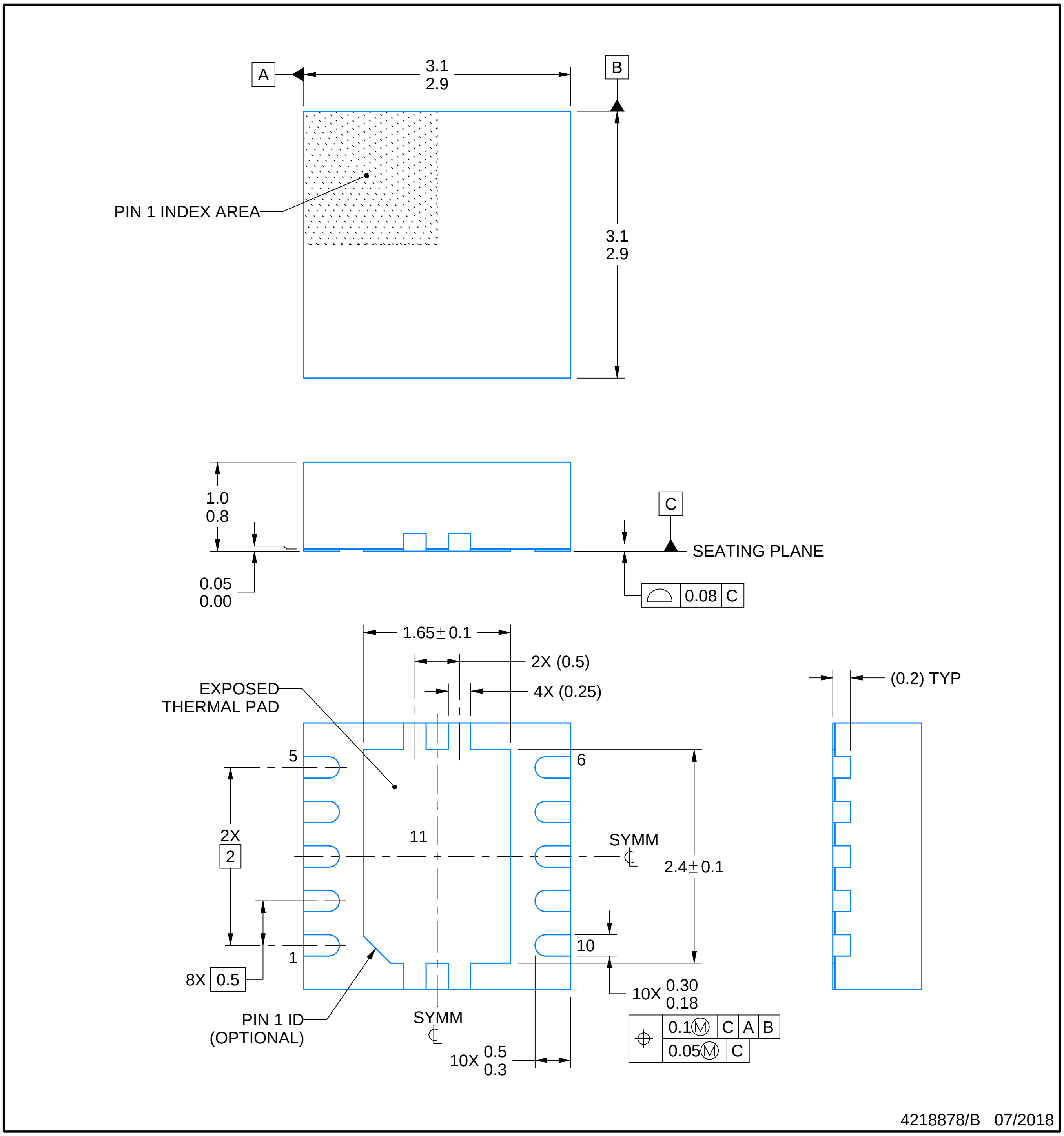



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| THVD2412DRCR | VSON | DRC | 10 | 5000 | 367.0 | 367.0 | 35.0 |
| THVD2442DRCR | VSON | DRC | 10 | 5000 | 367.0 | 367.0 | 35.0 |

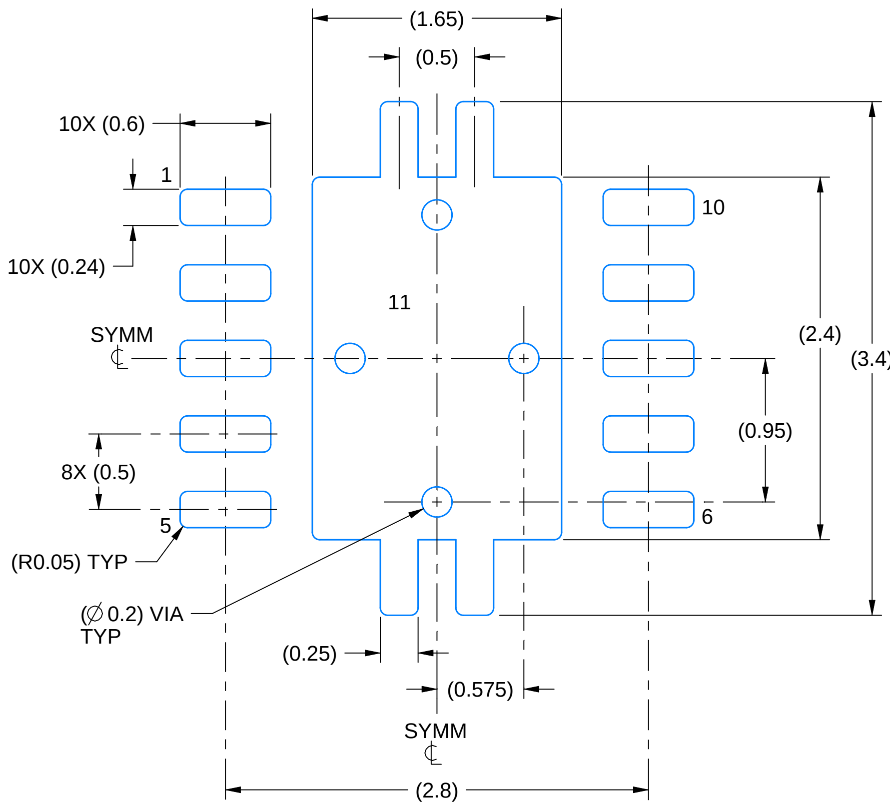
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



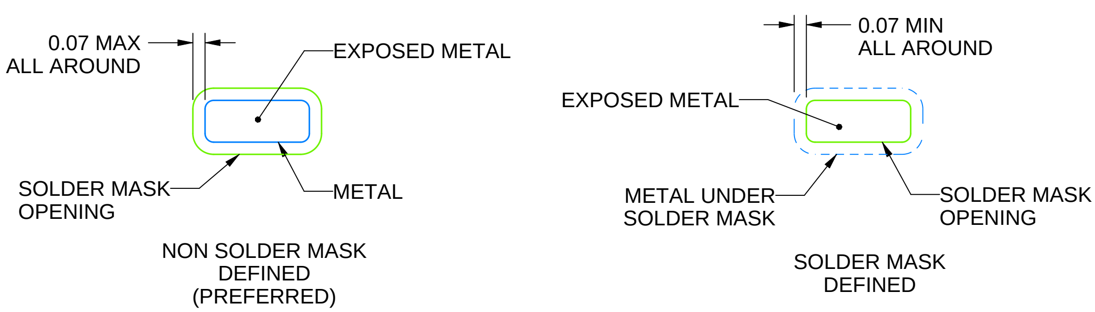



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

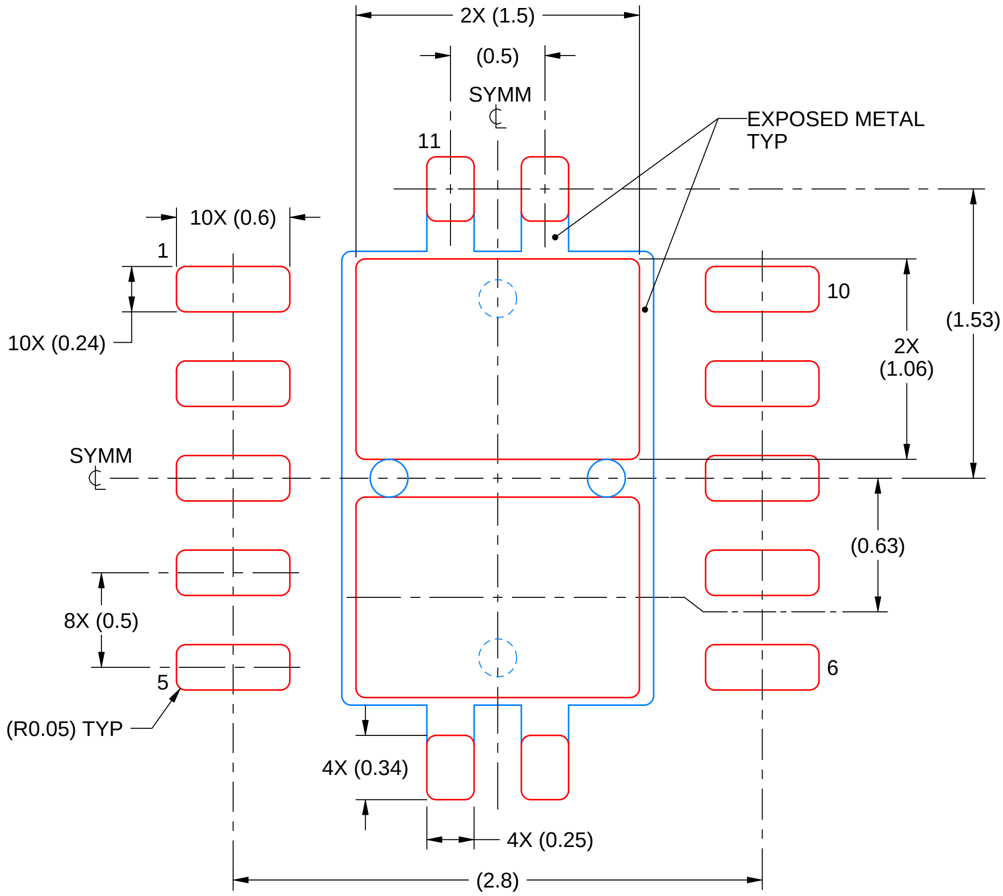



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# IMPORTANT NOTICE AND DISCLAIMER