THVD1406, THVD1426 3.3-V to 5-V RS-485 Transceivers with Auto-direction Control and ±12-kV IEC ESD Protection

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- 3-V to 5.5-V Supply voltage
- Auto-direction control using the data input pin
- Half-duplex RS-422/RS-485
- Data rates
  - THVD1406: 500 kbps
  - THVD1426: 12 Mbps
- Bus I/O protection
  - ±16-kV HBM ESD
  - ±12-kV IEC 61000-4-2 Contact discharge
  - ±15-kV IEC 61000-4-2 Air gap discharge
  - ±4-kV IEC 61000-4-4 Fast transient burst
- ±16-V bus fault protection
- Small, space-saving 8-Pin SOT package option (2.1 mm x 1.2 mm)
  - See the layout example for co-layout with standard SOIC-8 package
- Extended industrial temperature range: -40°C to 125°C
- Large receiver hysteresis for noise rejection
- Low power consumption
  - Low standby supply current: 3µA (typ)
  - Quiescent current during operation: 1.7 mA (typ)
- Glitch-free power-up, power-down for hot plug-in capability
- Open, short, and idle bus fail-safe
- 1/8 Unit load (Up to 256 bus nodes)

2 Applications

- Factory automation and control
- Building automation
- HVAC systems
- Video surveillance
- Smart meters

3 Description

The THVD14x6 (THVD1406 and THVD1426) devices are robust half-duplex RS-485 transceivers for industrial applications. These devices feature auto-direction control using the data input pin that reduces the reliance on separate pins for driver-enable and the receiver-enable functionality. This reduces the number of isolation channels needed or number of the GPIO pins needed for logic control. The bus pins are immune to high levels of IEC ESD events eliminating need of additional system level protection components.

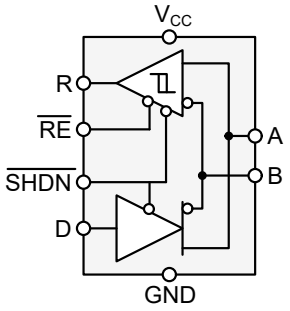
The devices operate from a single 3-V to 5.5-V supply. The wide common-mode voltage range and low input leakage on bus pins make devices suitable for multi-point applications over long cable runs.

The devices are available in industry standard 8-pin SOIC package for drop-in compatibility. The devices are also available in a small, space-saving SOT package. The devices are characterized for ambient temperatures from –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
THVD1406 THVD1426	SOIC (8)	4.90 mm × 3.91 mm
	SOT (8)	2.10 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2021) to Revision A (November 2021)	Page
• Changed document status from *Advanced Information* to *Production* data	1

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5 Pin Configuration and Functions

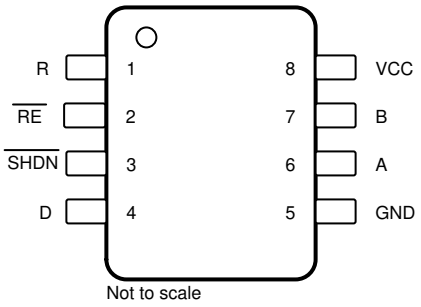

Figure 5-1. D (8-Pin SOIC) , DRL (8-Pin SOT) Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
R	1	O	Receiver data output
$\overline{RE}$	2	I	Receiver enable, active low (internal 2-MΩ pull-up)
$\overline{SHDN}$	3	I	Shutdown enable, active low (internal 2-MΩ pull-up)
D	4	I	Driver data input
GND	5	-	Device ground
A	6	I/O	Bus I/O port, A (complementary to B)
B	7	I/O	Bus I/O port, B (complementary to A)
V_{CC}	8	P	3-V to 5.5-V supply For the device.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_L	Input voltage at any logic pin (D, $\overline{SHDN}$ or $\overline{RE}$)	–0.3	5.7	V
V_A, V_B	Voltage at A or B inputs	–16	16	V
I_O	Receiver output current	–24	24	mA
T_J	Junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Between bus terminals (A, B) and GND	±16,000	V
			All other pins	±4,000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±1,500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND	±12,000	V
		IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND	±15,000	
		IEC 61000-4-4 EFT (Fast transient or burst), bus terminals and GND	±4,000	

6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{ID}	Differential input voltage		–12		12	V
V_I	Input voltage at any bus terminal(1)		–7		12	V
V_{IH}	High-level input voltage (D, $\overline{SHDN}$, and $\overline{RE}$ inputs)		2		5.5	V
V_{IL}	Low-level input voltage (D, $\overline{SHDN}$, and $\overline{RE}$ inputs)		0		0.8	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate: THVD1406				500	kbps
$1/t_{UI}$	Signaling rate: THVD1426				12	Mbps
T_J	Junction temperature		–40		150	°C
T_A (2)	Operating ambient temperature		–40		125	°C
T_{SHDN}	Thermal shutdown threshold (temperature rising)	Thermal shutdown threshold (temperature rising)	150	170		°C
T_{HYS}	Thermal shutdown hysteresis	Thermal shutdown hysteresis		15		°C

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

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(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

6.5 Thermal Information

THERMAL METRIC[1]		THVD1406, THVD1426		UNIT
		DRL (SOT)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	126.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.4	66.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.1	69.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	18.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	68.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS			VALUE	UNIT
P_D	Power dissipation, driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125°C, 50% duty cycle square-wave signal at maximum signaling rate	Unterminated R_L = 300 Ω, C_L = 50 pF	THVD1406	500 kbps	150	mW
			THVD1426	12 Mbps	155	
		RS-422 load R_L = 100 Ω, C_L = 50 pF	THVD1406	500 kbps	175	
			THVD1426	12 Mbps	180	
		RS-485 load R_L = 54 Ω, C_L = 50 pF	THVD1406	500 kbps	220	
			THVD1426	12 Mbps	225	

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6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Driver								
$\lvert V_{OD} \rvert$	Driver differential-output voltage magnitude	R_L = 60 Ω, -7 V ≤ V_{test} ≤ 12 V		See Figure 7-1	1.5	2		V
		RL = 60 Ω, -7 V ≤ Vtest ≤ 12 V, 4.5 V ≤ Vcc ≤ 5.5 V			2.1	3		
		R_L = 100 Ω, C_L = 50 pF		See Figure 7-2	2	2.5		
		R_L = 54 Ω, C_L = 50 pF			1.5	2		
		R_L = 54 Ω, 4.5 V ≤ V_{cc} ≤ 5.5 V			2.1	3		
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of driver differential-output voltage	R_L = 54 Ω or 100 Ω, C_L = 50 pF		See Figure 7-2	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage				1	V_{CC} / 2	3	V
ΔV_{OC}	Change in differential driver common-mode output voltage				–50		50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	R_L = 54 Ω or 100 Ω, C_L = 50 pF, V_{CC} = 3.3 V		See Figure 7-2		200		mV
$\lvert I_{OS} \rvert$	Driver short-circuit output current	-7 V ≤ [V_A or V_B] ≤ 12 V, or A pin shorted to B pin			-250		250	mA
Receiver								
I_I	Bus input current (driver disabled)	V_{CC} = 0 V or 5.5 V		V_I = 12 V		75	100	µA
				V_I = –7 V	–97	–70		
V_{IT+}	Positive-going receiver differential-input voltage threshold	-7 V ≤ V_{CM} ≤ 12 V				–70	–45	mV
$V_{IT–}$	Negative-going receiver differential-input voltage threshold				–200	–150		mV
V_{HYS} (1)	Receiver differential-input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)				30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –4 mA			V_{CC} – 0.4	V_{CC} – 0.2		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 4 mA				0.2	0.4	V
I_{OZ}	Receiver high-impedance output current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}			–1		1	µA
Logic								
I_{IN}	Input current (D, $\overline{SHDN}$, $\overline{RE}$)				–5		5	µA
Supply								
I_{CC}	Supply current (quiescent)	V_{CC} = 3.6 V	Driver and receiver enabled	$\overline{SHDN}$ = V_{CC}, $\overline{RE}$ = 0 D = 0, no load		1500	1800	µA
			Driver enabled, receiver disabled	$\overline{SHDN}$ = V_{CC}, $\overline{RE}$ = V_{CC}, D=0, no load		1000	1500	µA
			Driver and receiver disabled	$\overline{SHDN}$ = 0, no load		2	4.1	µA
I_{CC}	Supply current (quiescent)	V_{CC} = 5.5 V	Driver and receiver enabled	$\overline{SHDN}$ = V_{CC}, $\overline{RE}$ = 0 D = 0, no load		1700	3000	µA
			Driver enabled, receiver disabled	$\overline{SHDN}$ = V_{CC}, $\overline{RE}$ = V_{CC}, D=0, no load		1300	2500	µA
			Driver and receiver disabled	$\overline{SHDN}$ = 0, no load		3	6.9	µA

(1) Under any specific conditions, V_{IT+} isspecified to be at least V_{HYS} higher than$V_{IT–}$.

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6.8 Switching Characteristics (THVD1406)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Driver differential output rise and fall times		See Figure 7-3	200	300	600	ns
t_{PHL}, t_{PLH}	Driver propagation delay				275	500	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					10	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 7-4 and Figure 7-5		80	200	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			200	650	ns
		Receiver disabled			5	10	µs
$t_{device\_auto-dir}$	Driver active time in the auto-direction mode when $\overline{SHDN}$ is high and D switches from low to high	Driver active time in the auto-direction mode when $\overline{SHDN}$ is high and D turns from low to high	Figure 7-8	4	8	14	µs
Receiver							
t_r, t_f	Receiver output rise and fall times		See Figure 7-6		6	20	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				40	110	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					7	ns
t_{PHZ}, t_{PLZ}	Receiver disable time	See Figure 7-7			15	60	ns
$t_{PZL(1)}$, $t_{PZH(1)}$	Receiver enable time	Driver enabled	See Figure 7-7		80	150	ns

6.9 Switching Characteristics (THVD1426)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Driver differential output rise and fall times		See Figure 7-3		8	25	ns
t_{PHL}, t_{PLH}	Driver propagation delay				17	35	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					3.5	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 7-4 and Figure 7-5		15	38	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			15	70	ns
		Receiver disabled			5	10	µs
$t_{device\_auto-dir}$	Driver active time in the auto-direction mode when $\overline{SHDN}$ is high and D turns from low to high	Driver active time in the auto-direction mode when $\overline{SHDN}$ is high and D switches from low to high	Figure 7-8	0.4	0.8	1.45	µs
Receiver							
t_r, t_f	Receiver output rise and fall times		See Figure 7-6		4	16	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				40	75	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					5	ns
t_{PHZ}, t_{PLZ}	Receiver disable time	See Figure 7-7			15	25	ns
$t_{PZL(1)}$, $t_{PZH(1)}$	Receiver enable time	Driver enabled	See Figure 7-7		80	170	ns

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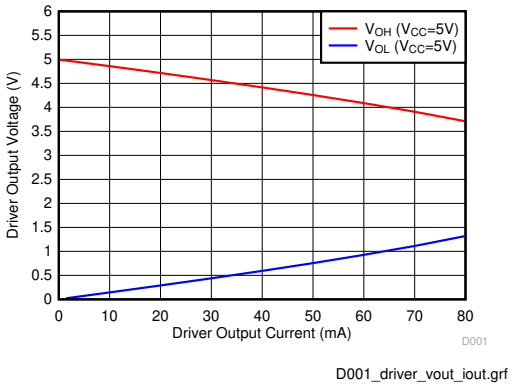
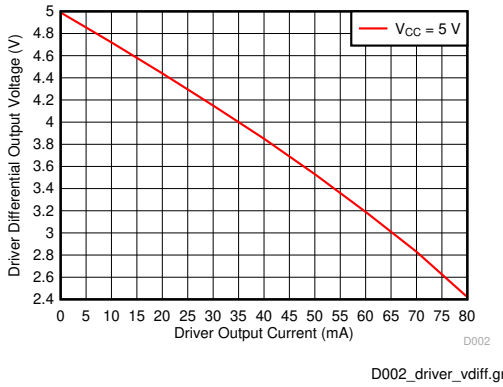
6.10 Typical Characteristics



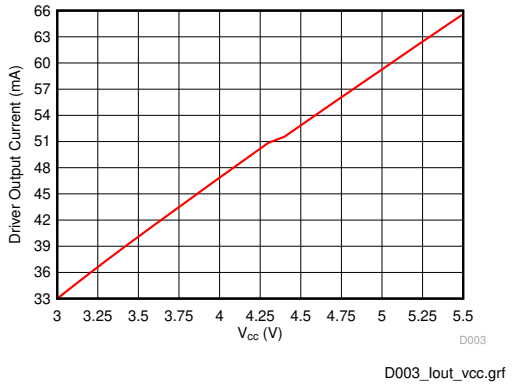
DE = V_{CC} T_A = 25°C

Figure 6-1. Driver Output voltage vs Driver Output Current



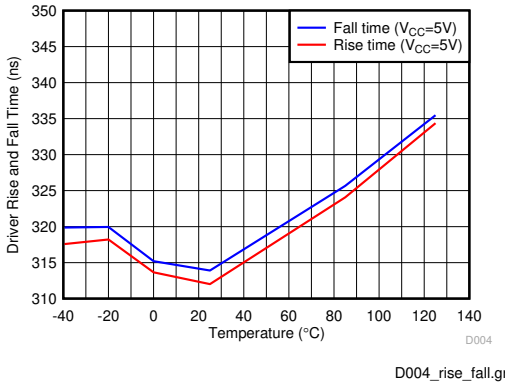
D = 0 V DE = V_{CC} T_A = 25°C

Figure 6-2. Driver Differential Output voltage vs Driver Output Current



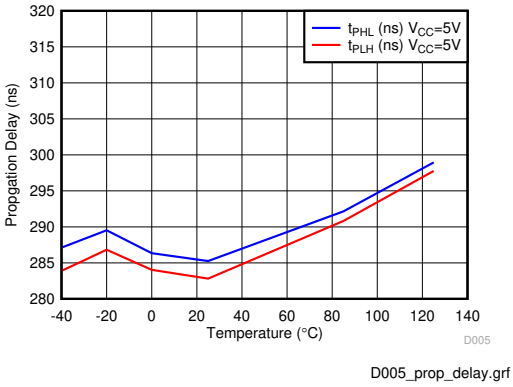
R_L = 54 Ω DE = V_{CC} D = V_{CC}
T_A = 25°C

Figure 6-3. Driver Output Current vs Supply Voltage



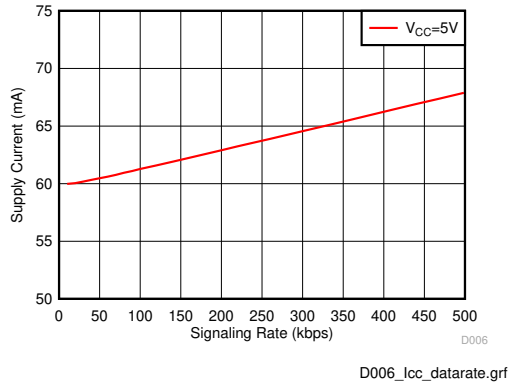
R_L = 54 Ω C_L = 50 pF

Figure 6-4. Driver Rise or Fall Time vs Temperature (THVD1406)



R_L = 54 Ω C_L = 50 pF

Figure 6-5. Driver Propagation Delay vs Temperature (THVD1406)



R_L = 54 Ω T_A = 25°C

Figure 6-6. Supply Current vs Signal Rate (THVD1406)

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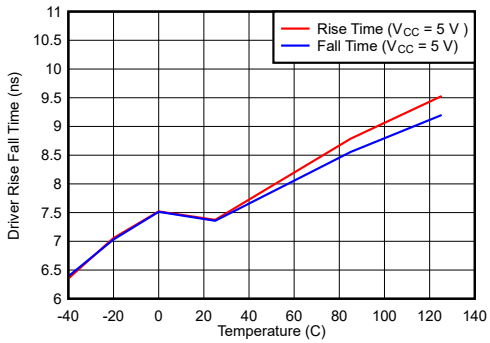
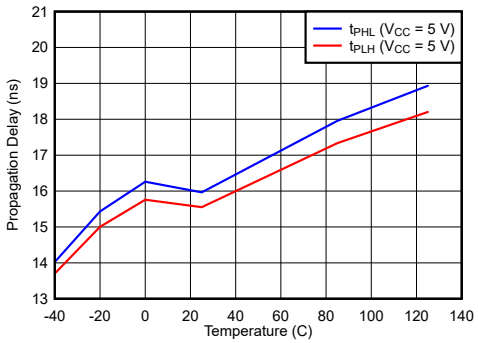


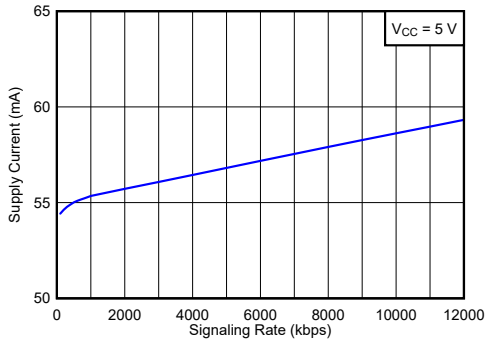
R_L = 54 Ω C_L = 50 pF

Figure 6-7. Driver Rise or Fall Time vs Temperature (THVD1426)



R_L = 54 Ω C_L = 50 pF

Figure 6-8. Driver Propagation Delay vs Temperature (THVD1426)



R_L = 54 Ω T_A = 25°C

Figure 6-9. Supply Current vs Signal Rate (THVD1426)

7 Parameter Measurement Information

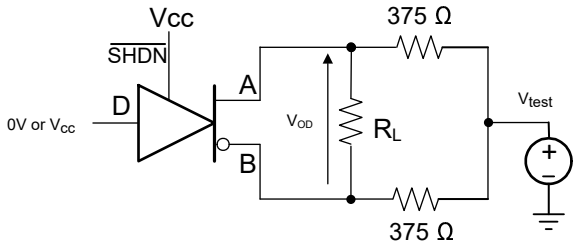


Figure 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

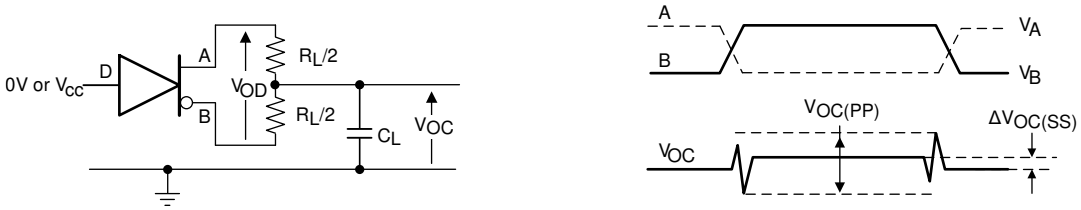


Figure 7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

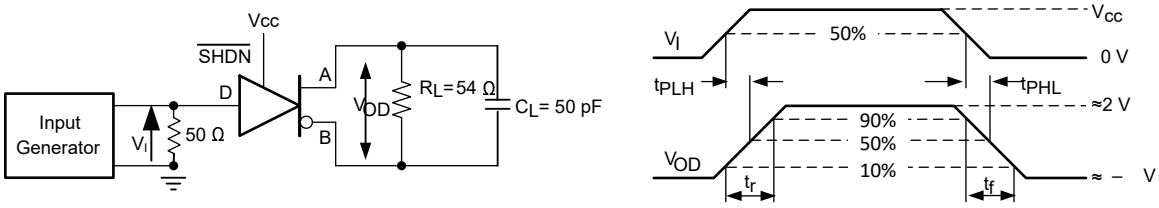


Figure 7-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

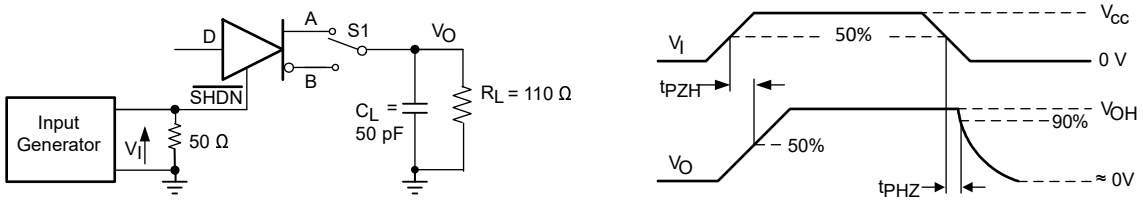


Figure 7-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

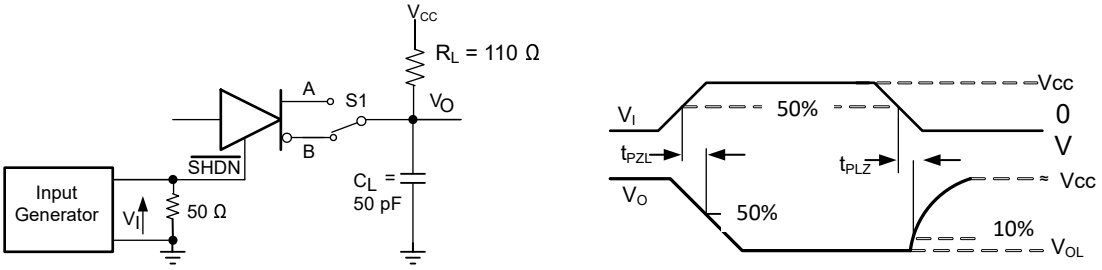


Figure 7-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

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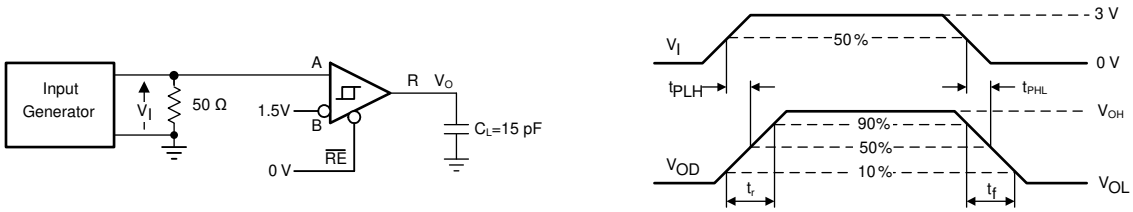


Figure 7-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

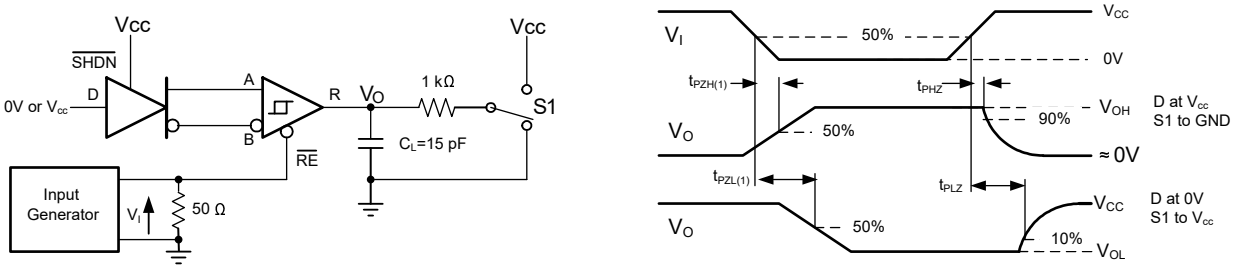


Figure 7-7. Measurement of Receiver Enable/Disable Times With Driver Enabled

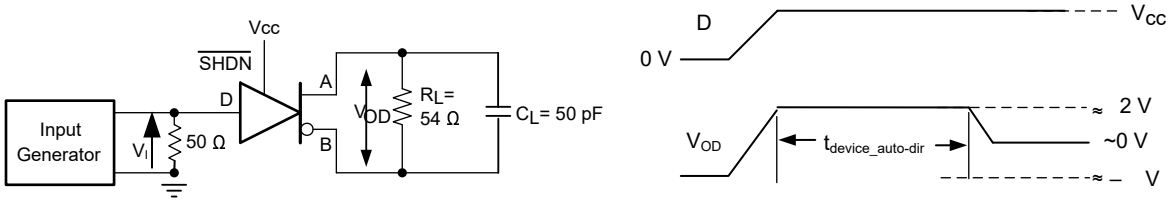


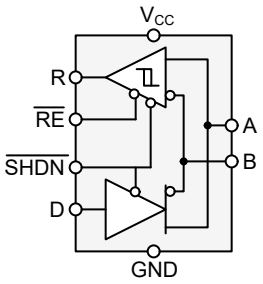
Figure 7-8. Measurement of Auto-direction Control Timing Parameter ($t_{device\_auto-dir}$)

8 Detailed Description

8.1 Overview

The THVD1406 is a low-power, half-duplex RS-485 transceiver suitable for data transmission up to 500 kbps. The THVD1426 is a low-power, half-duplex RS-485 transceiver suitable for data transmission up to 12 Mbps.

8.2 Functional Block Diagrams



8.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ±12 kV (Contact Discharge), ±15 kV (Air Gap Discharge) and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV.

8.4 Device Functional Modes

When the shutdown pin, $\overline{SHDN}$, is logic high, the differential outputs A and B follow the logic states at data input D. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative. A logic high at D causes A to turn high and B to turn low for a duration. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive for $t_{device\text{-}auto\text{-}dir}$. After this duration, the driver turns off and the receiver is enabled. The device can be used in auto-direction mode by tying $\overline{SHDN}$ and $\overline{RE}$ pins together to logic high and controlling the driver and receiver using the data input pin, D. This enables reducing the number of GPIO pins or the number of isolation channels required to operate the device. Please refer to Driver Function Table and Receiver Function Table for further details.

When $\overline{SHDN}$ is low, both the driver and the receiver are turned off and the device is in shutdown mode. In this condition, the logic state at D is irrelevant. The $\overline{SHDN}$ pin has an internal pull-up resistor to VCC; thus, when left open, the driver is status is dependent on the status of the D pin. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled for $t_{device\text{-}auto\text{-}dir}$, before bring disabled.

Table 8-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	$\overline{SHDN}$	A	B	
H	H/OPEN	H	L	Actively drive bus high for $t_{device\text{-}auto\text{-}dir}$ and then bus is in high impedance
L	H/OPEN	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled. Device in shutdown mode.
OPEN	H/OPEN	H	L	Actively drive bus high for $t_{device\text{-}auto\text{-}dir}$ and then bus is in high impedance

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open and D input is logic low, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go

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failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

When $\overline{RE}$ is logic high or left open and D input switches from logic low to logic high, the receiver output is high-impedance for the duration of $t_{device\text{-}auto\text{-}dir}$. After the duration of $t_{device\text{-}auto\text{-}dir}$, the receiver turns ON and outputs a logic high or low depending upon the differntial bus input voltage.

Table 8-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	INPUT	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	D	R	
$V_{IT+} < V_{ID}$	L	X	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	X	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	X	L	Receive valid bus low
X	H/OPEN	L	Z	Receiver disabled
X	H/OPEN	H	Z for $t_{device\_autodir}$ followed by L or H depending upon bus input voltage	Receiver disabled by for $t_{device\_autodir}$ after D switches from L to H. Receiver output follows bus input voltage after $t_{device\_autodir}$
Open-circuit bus	L	X	H	Fail-safe high output
Short-circuit bus	L	X	H	Fail-safe high output
Idle (terminated) bus	L	X	H	Fail-safe high output

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9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The THVD14x6 devices are half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. The device can be used in auto-direction mode by tying $\overline{SHDN}$ and $\overline{RE}$ pins together to logic high and controlling the driver and receiver using the data input pin, D. This enables reducing the number of GPIO pins or the number of isolation channels required to operate the device. Please refer to Driver Function Table and Receiver Function Table for further details.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

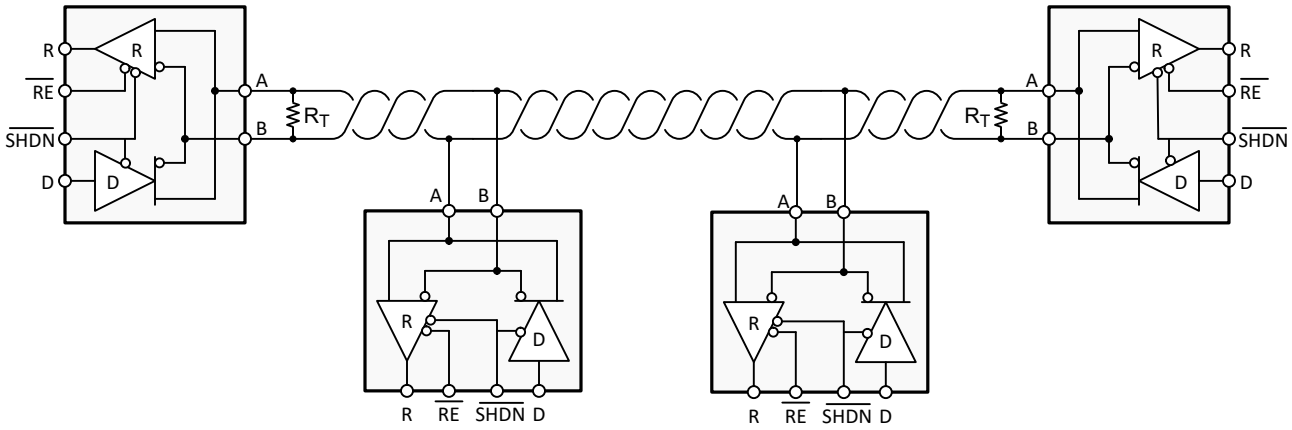

Figure 9-1. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 300 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

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9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD14x6 devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

9.2.1.4 Receiver Failsafe

The differential receivers of the THVD14x6 are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+}, $V_{IT–}$, and V_{HYS} (the separation between V_{IT+} and $V_{IT–}$). As shown in the *Electrical Characteristics* table, differential signals more negative than –200 mV always causes a low receiver output, and differential signals more positive than 200 mV always causes a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{IT+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{IT+}.

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9.2.1.5 Transient Protection

The bus pins of the THVD14x6 transceiver family include on-chip ESD protection against ±16-kV HBM and ±8-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model.

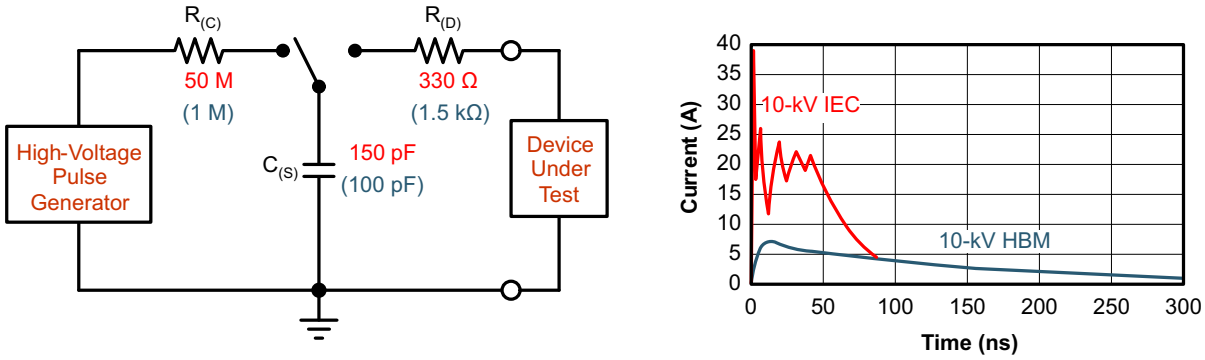

Figure 9-2. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 9-3 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

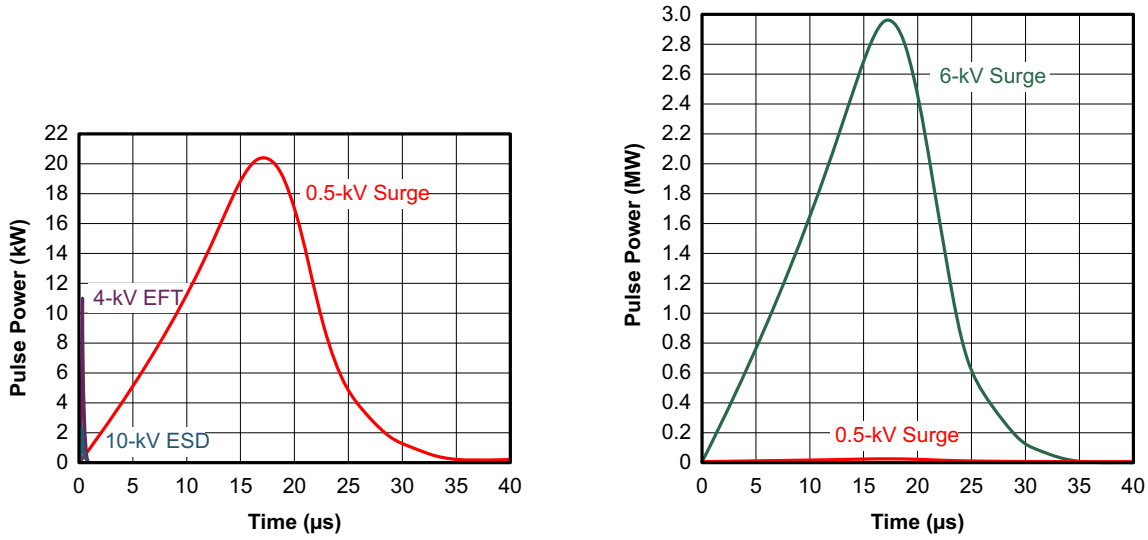

Figure 9-3. Power Comparison of ESD, EFT, and Surge Transients

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In the event of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 9-4 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

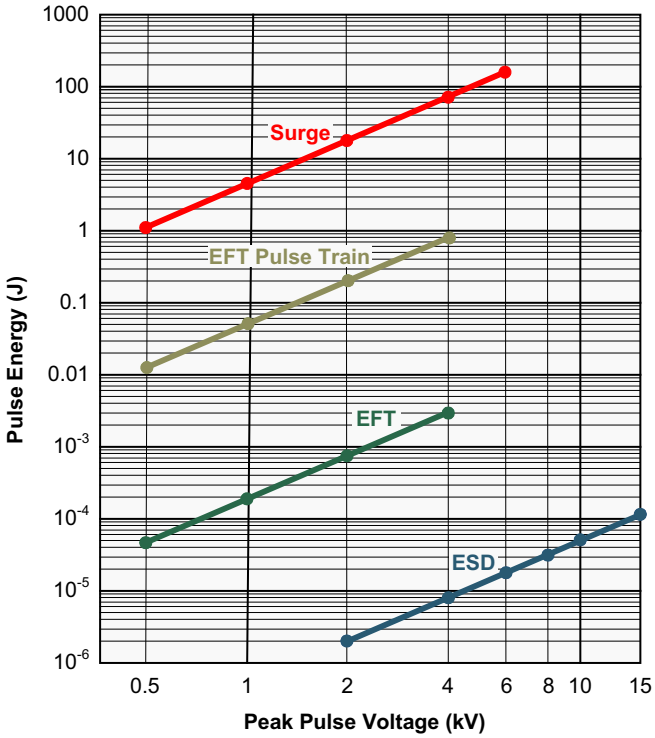


Figure 9-4. Comparison of Transient Energies

9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. Figure 9-5 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. Table 9-1 shows the associated bill of materials.

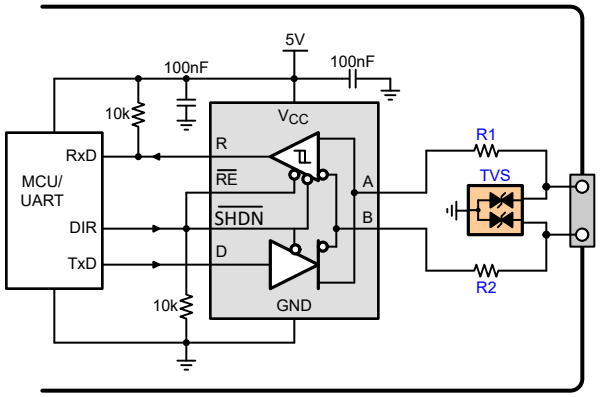


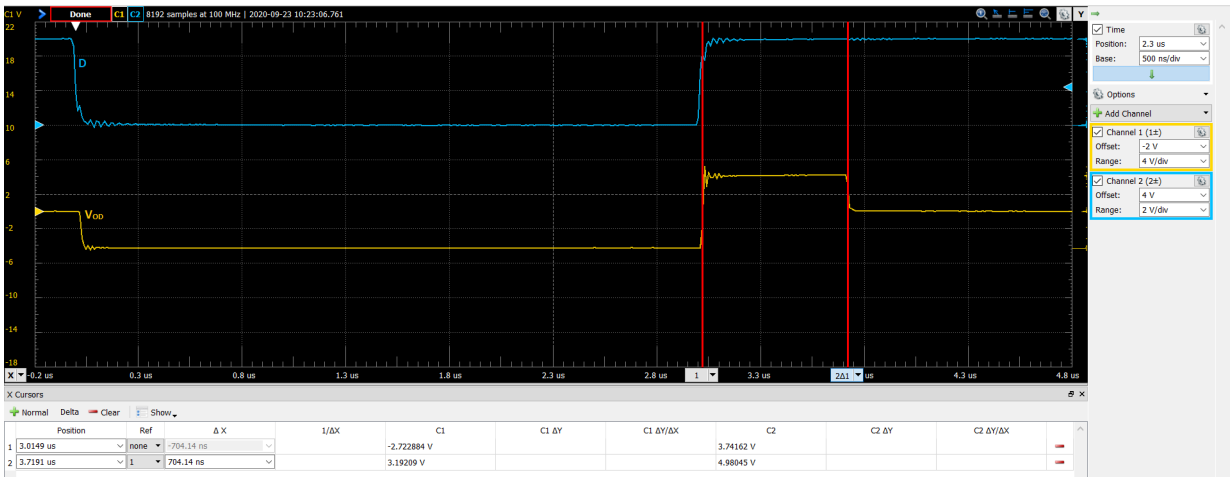
Figure 9-5. Transient Protection Against Surge Transients for Half-Duplex Devices

Table 9-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER(1)
XCVR	RS-485 transceiver	THVD1406	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

(1) See the Third-Party Products Disclaimer

9.2.3 Application Curves



$\overline{SHDN}$ = $\overline{REB}$ = 5 V V_{CC} = 5 V T_A = 25 °C

Figure 9-6. THVD1426 Waveforms Showing Auto-Direction Control Using D Input

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

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11 Layout

11.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pull-up resistors for $\overline{RE}$ and $\overline{SHDN}$ lines to connect them together to V_{CC} to reduce the number of GPIO lines to MCU or the number of isolation channels.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2 Layout Example

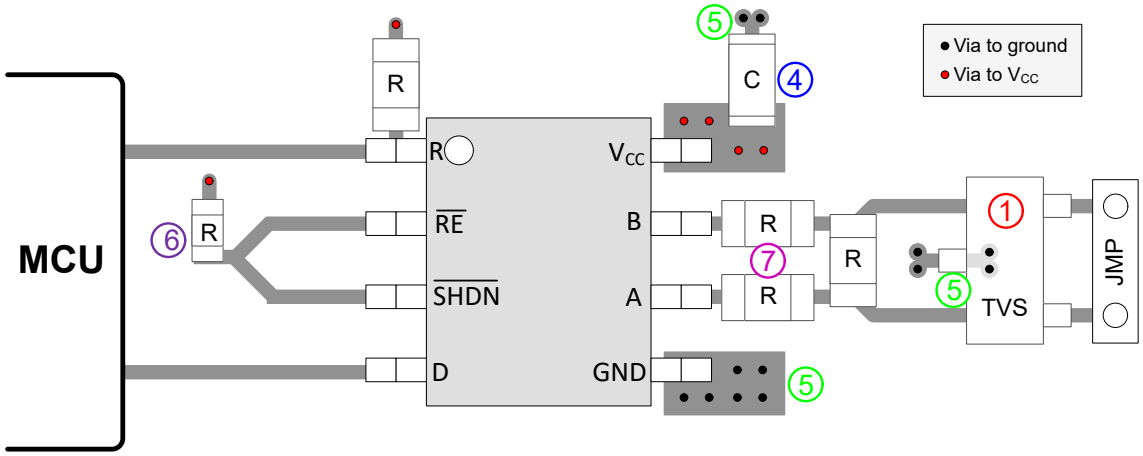

Figure 11-1. Layout Example

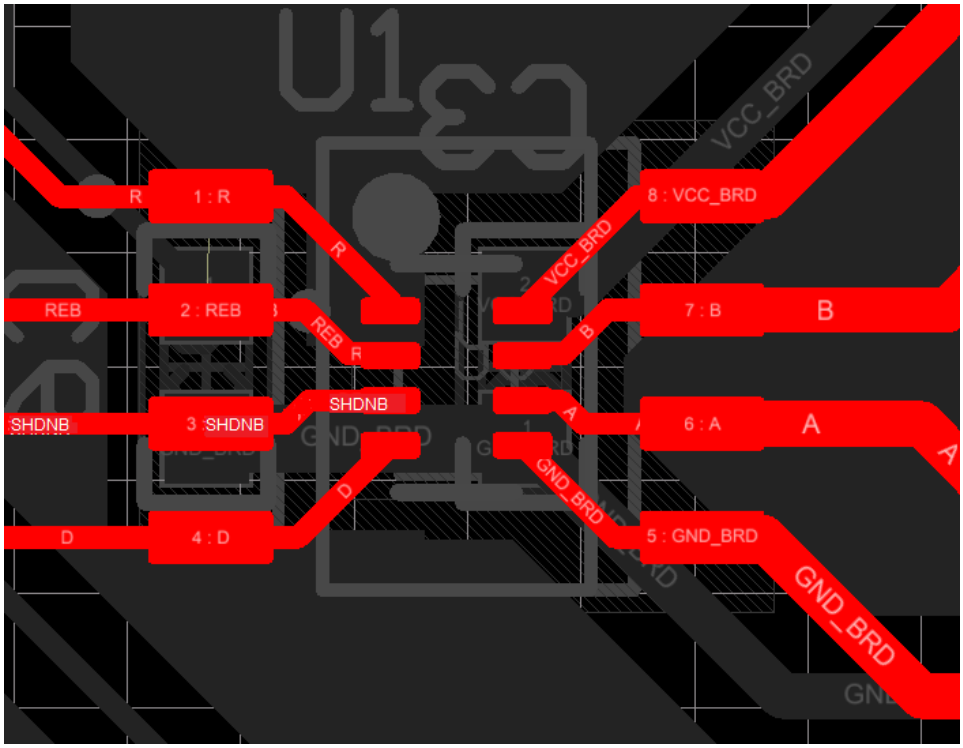

Figure 11-2. Layout Example for Co-layout of SOIC (D) and SOT (DRL) Packages

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Receiving Notification of Documentation Updates

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12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1406DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1406
THVD1406DRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	T406
THVD1426DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1426
THVD1426DRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	T426

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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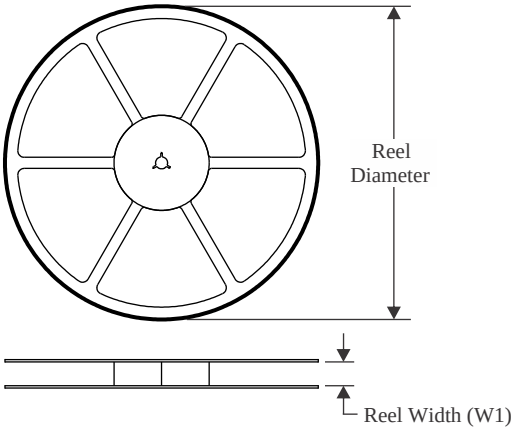
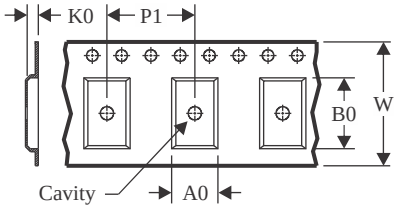
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

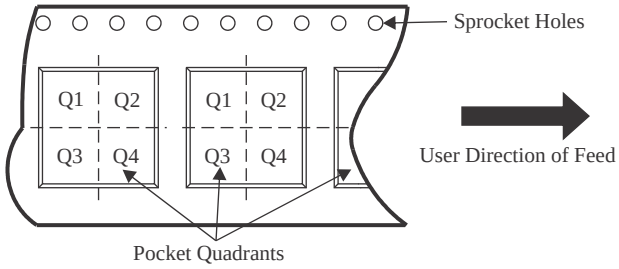


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

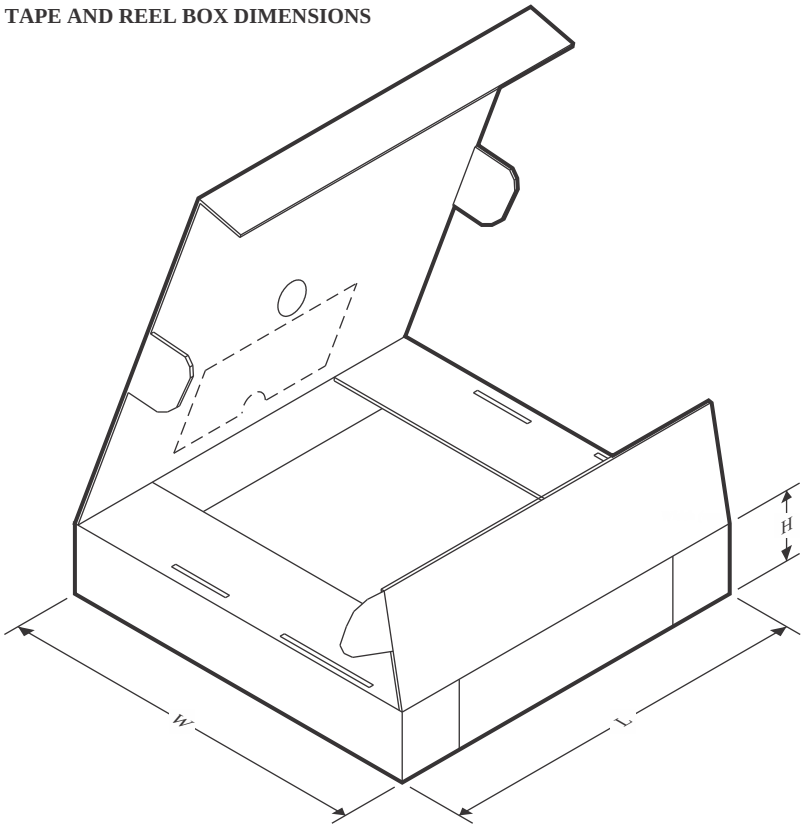
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1406DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1406DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
THVD1426DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1426DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

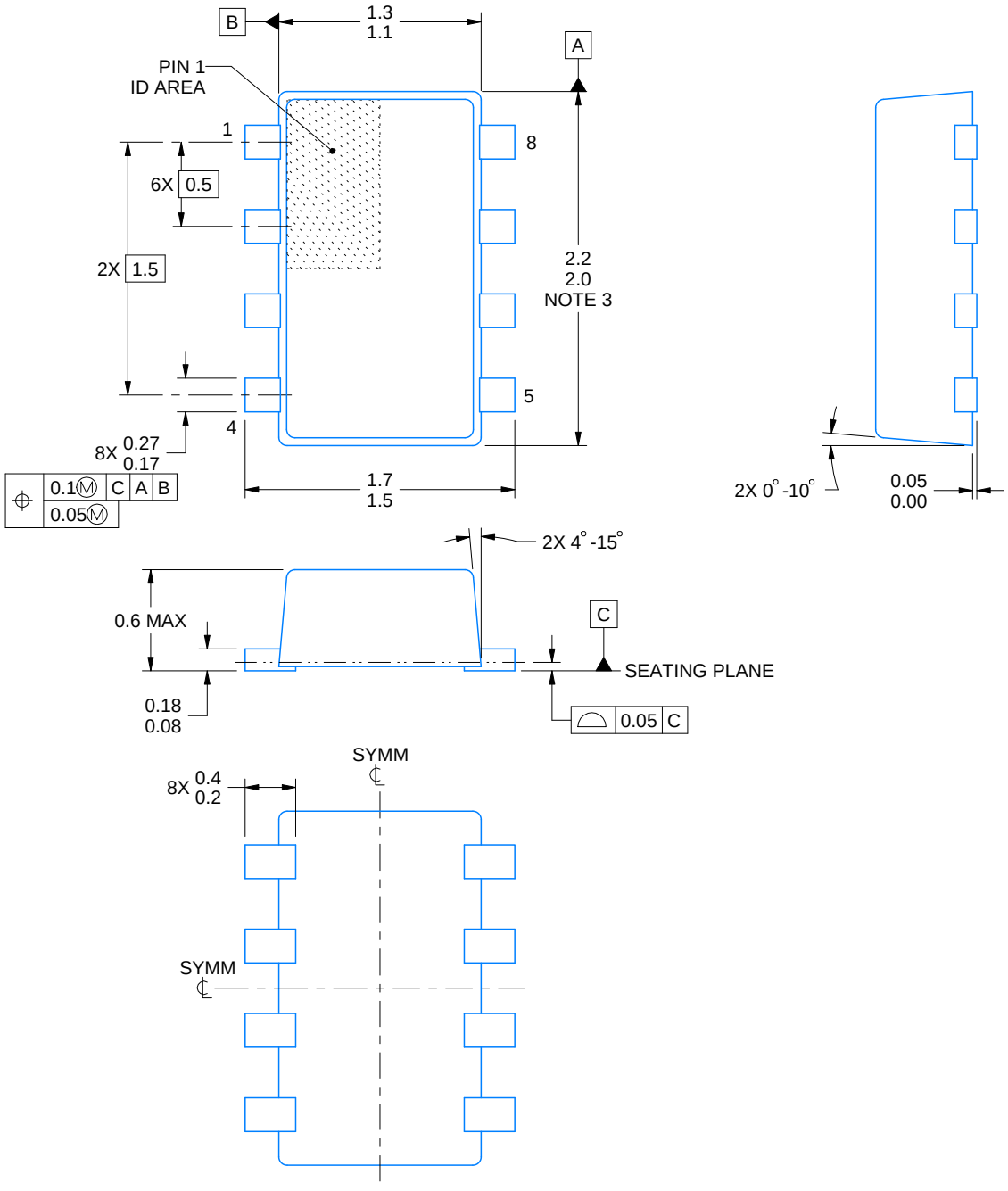
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1406DR	SOIC	D	8	3000	356.0	356.0	35.0
THVD1406DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
THVD1426DR	SOIC	D	8	3000	356.0	356.0	35.0
THVD1426DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



4224486/G 11/2024

NOTES:

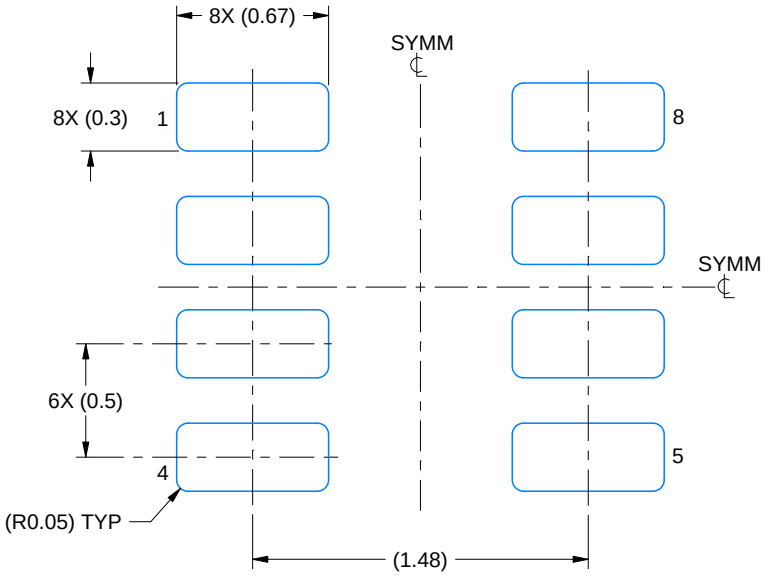
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

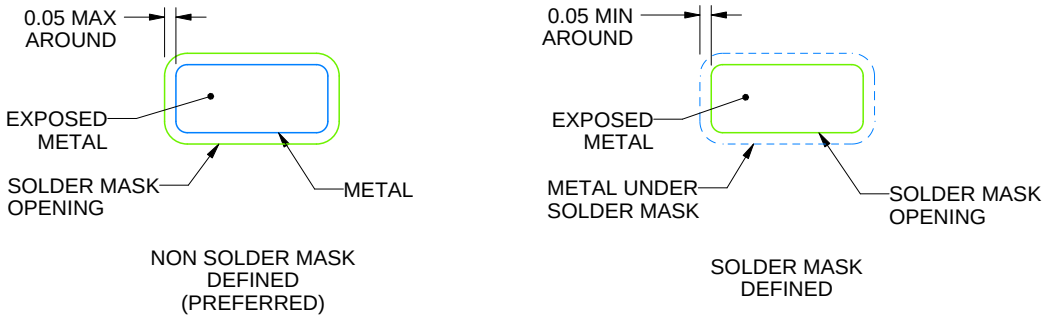
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

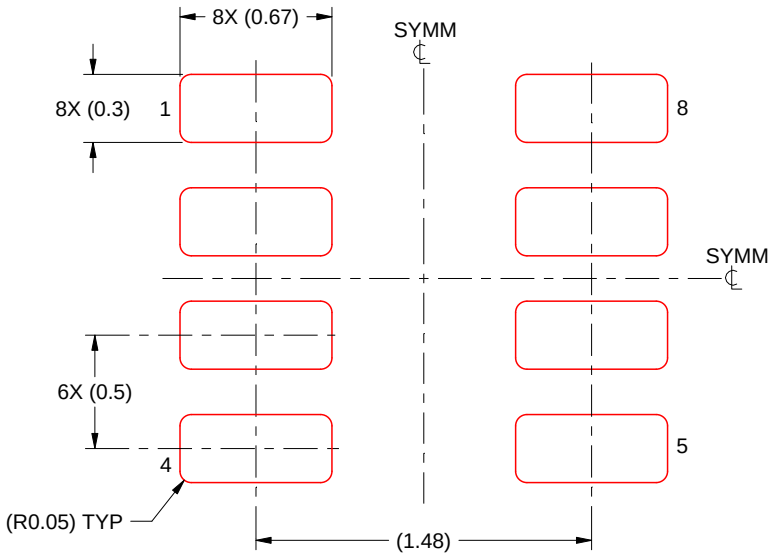
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE

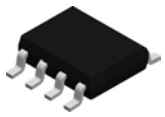


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

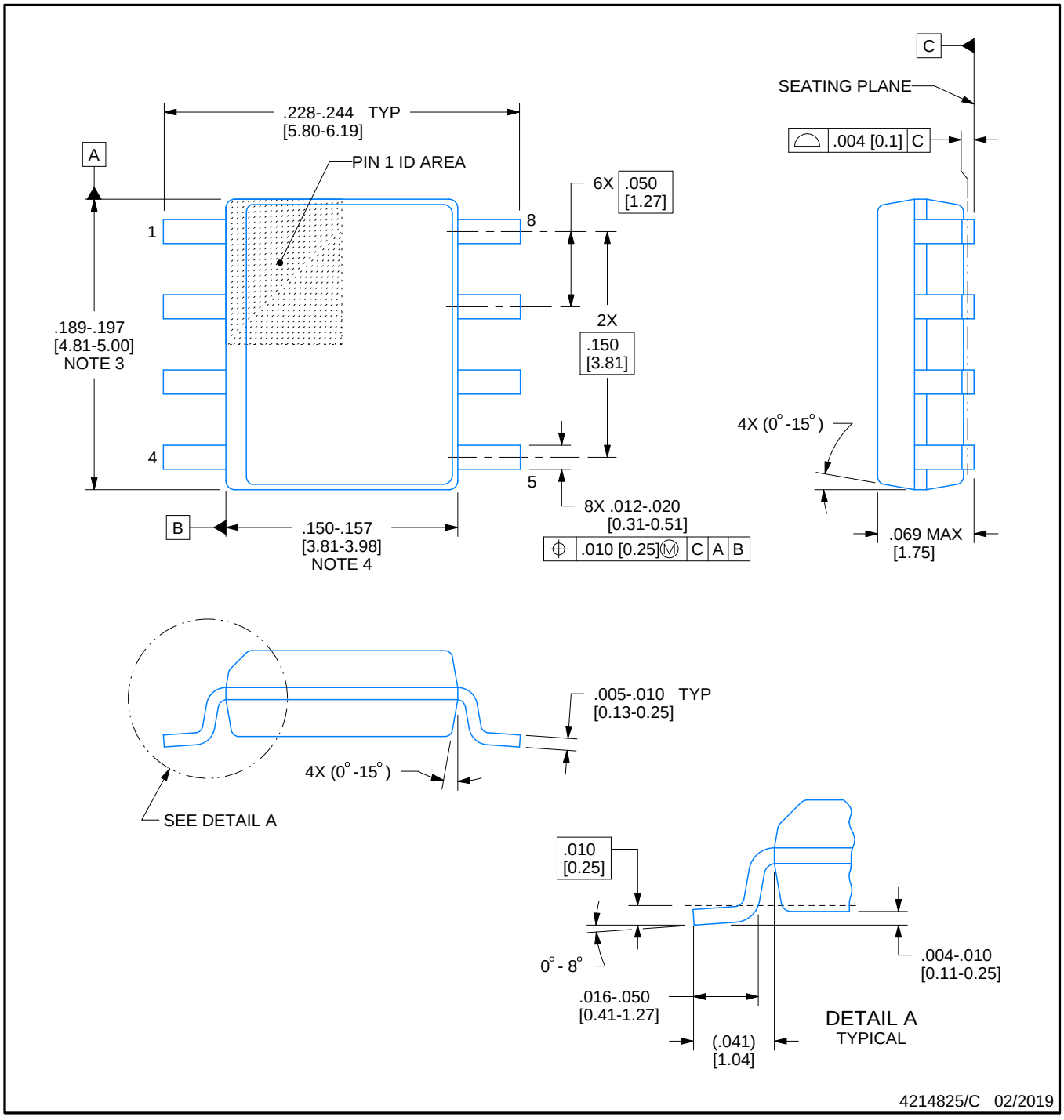


PACKAGE OUTLINE

D0008A

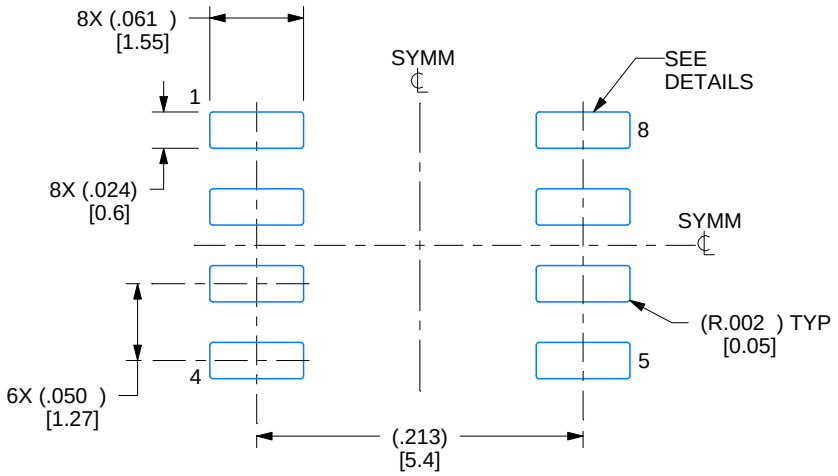
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

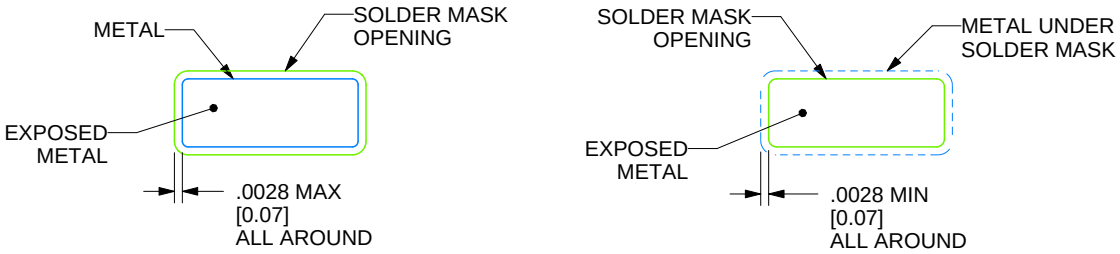


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

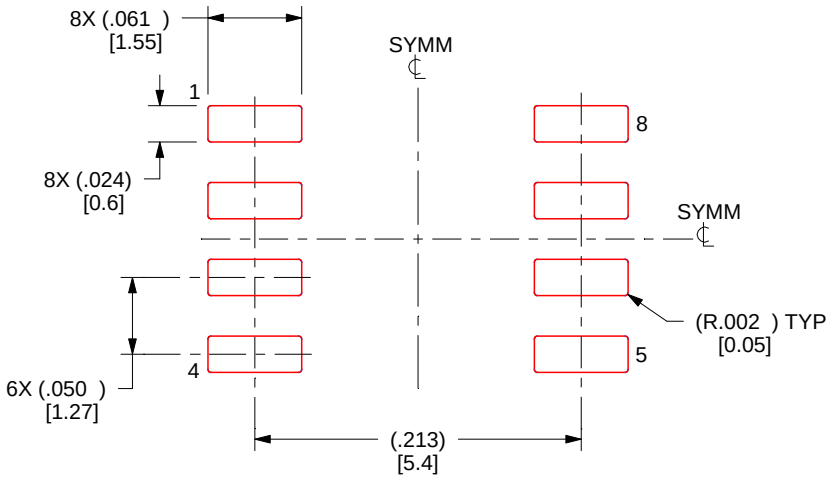
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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