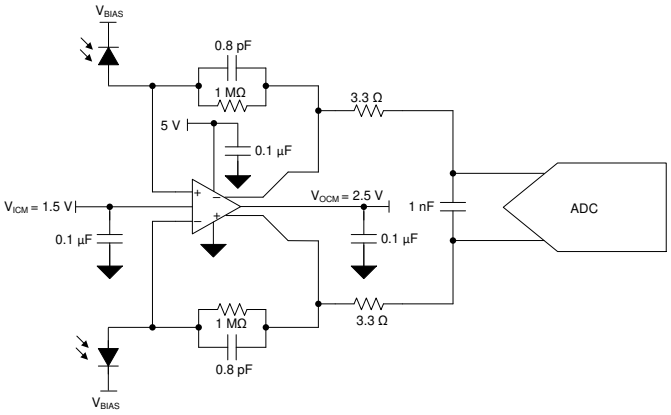
THS4567 220 MHz, High Input Impedance, Fully Differential Amplifier with Independent Input and Output Common-Mode Control

1 Features

- Gain Bandwidth Product (GBWP): 220 MHz
- Slew Rate: 500 V/µs
- Bandwidth: 42 MHz (G = 10 V/V)
- Voltage Noise: 4.2 nV/√Hz
- Supply Current (I_Q): 2 mA
- I_Q : 28 µA (Shutdown)
- Rail-to-Rail Output (RRO)
- High Impedance CMOS Inputs
- Independent Input and Output Common-Mode Control
- Disable Input Common-Mode Loop to Use as a Standard Fully Differential Amplifier (FDA)
- Single-Supply Range: 3.3 V to 5.5 V
- Split-Supply Range: ±1.65 V to ±2.75 V
- Operating Temperature Range: -40°C to 125°C

2 Applications

- Absolute Optical Encoder
- AC Drive Position Feedback
- Linear Motor Position Sensor
- Clinical Pulse Oximeter
- Optical Coherence Tomography



Single-Stage Differential-Input to Differential-Output, TIA and ADC Driver for Optical Encoders

3 Description

The THS4567 device is a novel fully-differential amplifier (FDA) that includes independent input common-mode (VICM) and output-common mode (VOCM) control. Standard FDAs only possess output common-mode control. The THS4567 is a decompensated amplifier with a minimum stable gain of 10 V/V.

The THS4567 operates as a fully differential transimpedance amplifier (TIA) and analog-to-digital converter (ADC) driver in a single integrated stage.

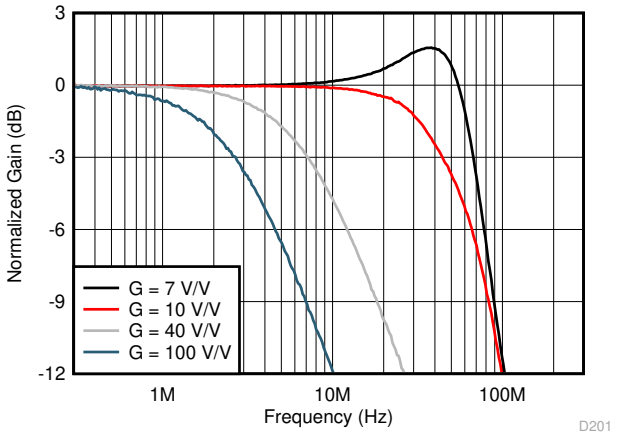
The VICM loop decouples the reverse bias across the photodiode(PD) from the amplifiers input and output swing compliance ranges thereby allowing the designer to maximize the PD reverse bias and minimize the PD capacitance. The VICM loop can be disabled which then allows the THS4567 to operate as a standard FDA.

The VOCM loop sets the differential output common-mode voltage and is typically set at the subsequent ADC stage common-mode reference voltage.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4567	WQFN (10)	2.00 mm × 2.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Small-Signal Frequency Response vs Gain

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial Release

5 Pin Configuration and Functions

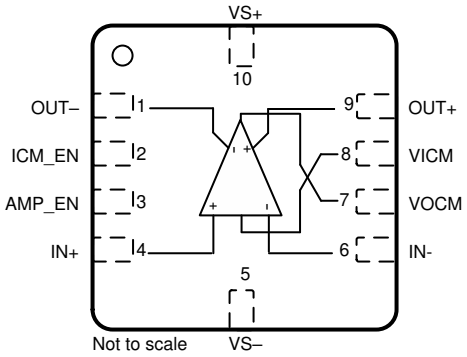


Figure 5-1. RUN Package
10-Pin WQFN
Top View

Table 5-1. Pin Functions

NAME	PIN NO.	I/O	DESCRIPTION
AMP_EN	3	I	Amplifier enable. HIGH (Default) = normal operation; LOW = power-off mode.
ICM_EN	2	I	Input common-mode loop enable. HIGH (Default) = ICM loop enabled (TIA mode); ICM loop disabled (FDA mode).
IN+	4	I	Noninverting (positive) amplifier input (V_{IN+} = voltage measured at pin 4).
IN–	6	I	Inverting (negative) amplifier input ($V_{IN–}$ = voltage measured at pin 6).
OUT+	9	O	Noninverting (positive) amplifier output (V_{OUT+} = voltage measured at pin 9).
OUT–	1	O	Inverting (negative) amplifier output ($V_{OUT–}$ = voltage measured at pin 1).
VICM	8	I	Input common-mode voltage input (VICM = voltage applied at pin 8, V_{ICM} = voltage measured at pin 8).
VOCM	7	I	Output common-mode voltage input (VOCM = voltage applied at pin 7, V_{OCM} = average output voltage).
VS+	10	–	Positive power-supply input (V_{S+} = voltage applied at pin 10).
VS–	5	–	Negative power-supply input ($V_{S–}$ = voltage applied at pin 5).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+} – V_{S-})		5.75	V
	Input, output, enable and common-mode pin voltage range	(V_{S-}) – 0.5	(V_{S+}) + 0.5	V
	Differential input pin voltage		±1	V
I_{IN}	Continuous input current		±10	mA
I_{OUT}	Continuous output current(2)		±20	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	3.3	5	5.5	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		THS4567 RUN (WQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics: Differential TIA Mode, ICM loop enabled

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = Open, VICM = Open, R_F = 1 MΩ, C_F = 0.4 pF, C_{IN} = 10 pF (on each input pin), AMP_EN = 2.5 V, ICM loop enabled (ICM_EN = 2.5 V) and T_A = 25°C. (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE (ICM LOOP)						
GBWP	Differential-transimpedance gain bandwidth product	V_{OUT} = 100 mV_{PP}		220		MHz
	Input Common-Mode control loop small-signal bandwidth	V_{OUT} = 100 mV_{PP}		5		MHz
i_N	Input differential current noise	f = 100 kHz, ICM loop disabled		0.02		pA/√Hz
		f= 100 kHz, output current of ICM loop, I_{CM_CTL} (3) < 750 nA		0.35		
		f= 100 kHz, Output current of ICM loop, I_{CM_CTL} (3) < 2.8 µA		0.5		
		f= 100 kHz, Output current of ICM loop, I_{CM_CTL} (3) < 5.5 µA		0.65		
		f= 100 kHz, Output current of ICM loop, I_{CM_CTL} (3) < 17 µA		1.1		
		f= 100 kHz, Output current of ICM loop, I_{CM_CTL} (3) < 55 µA		1.9		
DC PERFORMANCE (ICM LOOP)						
VICM(1)	VICM pin default voltage above $V_{S–}$	VICM pin open (voltage measured at pin 8)	1.4	1.55	1.75	V
V_{ICM} (1)	Default input common-mode voltage above $V_{S–}$	VICM pin open, V_{ICM} = (V_{IN+} + $V_{IN–}$)/2	1.4	1.55	1.75	V
$\Delta V_{ICM}/\Delta T_A$	Input common-mode voltage drift	T_A = –40°C to +125°C, VICM pin open		160		µV/°C
$\Delta V_{ICM}/\Delta I_{CM\_CTL}$	Input common-mode voltage vs. I_{CM_CTL} current (2) (3)	I_{CM_CTL} variation = 5 µA to 20 µA	2	2.8	3.6	mV/µA
$\Delta V_{ICM}/\Delta T_A$	Input common-mode voltage offset drift	T_A = –40°C to +125°C, VICM pin driven to midsupply		22		µV/°C
V_{IN_OS}	Input common-mode offset error	VICM pin driven to midsupply, I_{CM_CTL} = 0(2), V_{IN_OS} = (V_{ICM} – VICM)	–25	±2.5	25	mV
	VICM pin DC input resistance	VICM pin driven to midsupply		200		kΩ
	VICM input high	≤ ±20-mV shift from midsupply offset, I_{CM_CTL} ≤ 100 µA	V_{S+} – 1.5	V_{S+} – 1.3		V
	VICM input low	≤ ±20-mV shift from midsupply offset, I_{CM_CTL} ≤ 100 µA		$V_{S–}$ + 0.8	$V_{S–}$ + 1	V
I_{CM_OS}	Input common-mode control current offset mismatch between inputs	I_{CM_OS} = $\Delta I_{(CM\_CTL,\ IN+/IN–)}$/Average I_{CM_CTL}, I_{CM_CTL} = 10 µA		0.5%		

(1) V_{ICM} refers to the common-mode or average voltage at the FDA inputs (IN+ and IN–). When the input common-mode (ICM) control function is enabled (ICM_EN = HIGH), the device generates matched source/sink control currents to drive the input pins towards the VICM pin reference voltage. Therefore VICM represents the voltage at pin 8, while V_{ICM} represents the average input voltage.

(2) I_{CM_CTL} refers to the magnitude of the matched source/sink control currents generated by the ICM loop at the device I_{IN+} and $I_{IN–}$ pins.

(3) A positive I_{CM_CTL} current is defined as a sinking (pull-down) current, generated by the ICM control loop to balance the total currents (external common-mode + feedback) that flow into the FDA input pins.

6.6 Electrical Characteristics: FDA operation, ICM loop disabled

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = Open, VICM = Open, R_F = 5 kΩ, Gain = 10 V/V, ICM loop disabled (ICM_EN = –2.5 V), R_L = 1 kΩ and T_A = 25°C. (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} (2) = 100 mV_{PP}		43		MHz
LSBW	Large-signal bandwidth	V_{OUT} (2) = 8 V_{PP}		28		MHz
GBWP	Gain bandwidth product			220		MHz
	Slew rate	V_{OUT} = 8V Step, 20% ↔ 80%		500		V/µs
t_R, t_F	Rise and fall time	V_{OUT} = 100 mV_{PP}, 10% ↔ 90%		8		ns
	0.1% settling time	V_{OUT} = 8V Step		65		ns
	0.001% settling time			175		
HD2	Second-order harmonic distortion	f= 100 kHz, V_{OUT} = 2 V_{PP}		–115		dBc
		f= 100 kHz, V_{OUT} = 8 V_{PP}		–105		
HD3	Third-order harmonic distortion	f= 100 kHz, V_{OUT} = 2 V_{PP}		–118		dBc
		f= 100 kHz, V_{OUT} = 8 V_{PP}		–108		
e_N	Input differential voltage noise	f = 100 kHz		4.2		nV/√Hz
i_N	Input current noise, each input			10		fA/√Hz
Z_{OUT}	Closed-loop differential output impedance			0.2		Ω
DC PERFORMANCE						
A_{OL}	Open-loop gain		104	117		dB
V_{OS}	Input-referred offset voltage	V_{OS} = (V_{IN+} – $V_{IN–}$)	–10	0.2	10	mV
$\Delta V_{OS}/\Delta T_A$	Input-referred offset voltage drift	T_A = –40°C to +125°C		1		µV/°C
I_{BN}, I_{BI}	Input bias current	Noninverting and inverting inputs		20		pA
I_{OS}	Input offset current	(I_{BN} – I_{BI})		±20		pA
INPUT						
	Differential input resistance	Effective shunt resistance between inputs		1		GΩ
	Common-mode input resistance	Effective shunt resistance to AC GND at each input		1		
	Differential input capacitance	Effective shunt capacitance between inputs		0.6		pF
	Common-mode input capacitance	Effective shunt capacitance to AC GND at each input		0.9		
CMRR	Common-mode rejection ratio	CMRR = ($\Delta V_{CM}/\Delta V_{OS}$). Inputs shifted ±500 mV around midsupply	70	80		dB
CMIR+	Common-mode input high	T_A = 25°C, A_{OL} > 90 dB	V_{S+} – 1.85	V_{S+} – 1.6		V
		T_A = –40°C to +125°C, A_{OL} > 90 dB		V_{S+} – 1.65		
CMIR–	Common-mode input low	T_A = 25°C, A_{OL} > 90 dB	$V_{S–}$ + 0.2	$V_{S–}$ – 0.2		V
		T_A = –40°C to +125°C, A_{OL} > 90 dB		$V_{S–}$ – 0.1		

6.6 Electrical Characteristics: FDA operation, ICM loop disabled (continued)

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = Open, VICM = Open, R_F = 5 kΩ, Gain = 10 V/V, ICM loop disabled (ICM_EN = –2.5 V), R_L = 1 kΩ and T_A = 25°C. (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Output voltage range to either supply	R_L= 20 kΩ, T_A = 25°C, input driven to ±V_S/Gain	V_S – 0.125	V_S – 0.075		V
	Output voltage range to either supply	R_L= 20 kΩ, T_A = 25°C, V_{OS} shift < 150 µV from default offset	V_S – 0.175	V_S – 0.125		V
	Output voltage range to either supply	R_L= 20 kΩ, T_A = –40°C to +125°C, V_{OS} shift < 150 µV from default offset		V_S – 0.175		V
	Output voltage range to either supply	R_L= 1 kΩ, T_A = 25°C, V_{OS} shift < 150 µV from default offset	V_S – 0.25	V_S – 0.2		V
	Output voltage range to either supply	R_L= 1 kΩ, T_A = –40°C to +125°C, V_{OS} shift < 150 µV from default offset		V_S – 0.25		V
OUTPUT COMMON-MODE (VOCM) CONTROL						
	Output common-mode loop SSBW	VOCM[3] pin driven ± 0.5 mV around midsupply		5		MHz
	Output common-mode loop LSBW	VOCM pin driven ± 0.5 V around midsupply		4.5		MHz
ΔV_{OUT} /ΔV_{OCM}	DC output balance [2] [3]	VOCM = ±1 V		80		dB
ΔV_{OCM} /ΔVOCM	Output common-mode gain [3]	VOCM pin driven ±1 V around midsupply	0.99	1	1.01	V/V
	Input DC bias current of VOCM pin	VOCM pin driven to midsupply		100		nA
	Input impedance of VOCM pin	VOCM pin driven ± 0.5 mV around midsupply		200||1		kΩ || pF
	VOCM input pin voltage offset from mid-supply [4]	VOCM pin open	–8	–2	4	mV
V_{OCM_OS}	Output common-mode voltage offset from midsupply	VOCM pin open	–30	±2.5	30	mV
ΔV_{OCM_OS} /T_A	Output common-mode voltage offset drift	T_A = –40°C to +125°C, VOCM pin open		–22		µV/°C
V_{OCM_OS}	Output common-mode voltage offset from midsupply	VOCM pin driven to midsupply	–25	±1.5	25	mV
ΔV_{OCM_OS} /T_A	Output common-mode voltage offset drift	T_A = –40°C to +125°C, VOCM pin driven to midsupply		–18		µV/°C
	VOCM input headroom to V_{S+}	≤ ±10 mV shift from V_{OCM_OS}		0.9	1	V
	VOCM input headroom to V_{S+}	T_A = –40°C to +125°C, ≤ ±10 mV shift from V_{OCM_OS}		1		V
	VOCM input headroom from $V_{S–}$	≤ ±10 mV shift from V_{OCM_OS}		0.9	1	V
	VOCM input headroom from $V_{S–}$	T_A = –40°C to +125°C, ≤ ±10 mV shift from V_{OCM_OS}		1		V
ΔV_{OCM_OS} /ΔV_{S+}	Positive power-supply rejection ratio	VOCM = 0 V (driven)		76		dB
ΔV_{OCM_OS} /$\Delta V_{S–}$	Negative power-supply rejection ratio			80		

6.6 Electrical Characteristics: FDA operation, ICM loop disabled (continued)

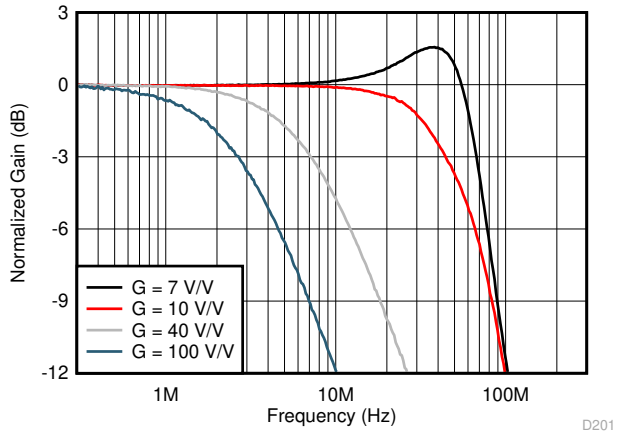
V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = Open, VICM = Open, R_F = 5 kΩ, Gain = 10 V/V, ICM loop disabled (ICM_EN = –2.5 V), R_L = 1 kΩ and T_A = 25°C. (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current	T_A = 25°C	1.4	1.9	2.5	mA
I_Q	Quiescent current	VICM loop enabled	1.5	2	2.7	mA
I_Q	Disabled quiescent current	AMP_EN = $V_{S–}$	10	28	40	µA
+PSRR	Power-supply rejection ratio to V_{S+}	VOCM is driven	70	94		dB
–PSRR	Power-supply rejection ratio to $V_{S–}$	VOCM is driven	90	110		dB
POWER DOWN						
V_{IH}	Enable voltage (Amplifier ON above this voltage)	AMP_EN and ICM_EN		V_{S+} – 0.7	V_{S+} – 0.5	V
V_{IL}	Disable voltage threshold (Amplifier OFF below this voltage)		V_{S+} – 2	V_{S+} – 1.8		
I_{IH}	Control pin HIGH Input bias current	AMP_EN and ICM_EN driven to (V_{S+}) – 0.25 V		3.5	7	µA
	External pull-down current required to switch ON→OFF (1)			175		µA
I_{IL}	Control pin LOW Input bias current	AMP_EN and ICM_EN driven to $V_{S–}$	–5	–1.1		µA
t_{AMP_ON}	Turn-ON time delay (Main amplifier)	Time to V_{OUT} stabilized within 1% of the final value		1.5		µs
t_{AMP_OFF}	Turn-OFF time delay (Main amplifier)	Time to supply current ≤ 100 µA		0.9		µs

(1) Leaving the AMP_EN pin floating is not recommended. When using a pull-up resistor ensure that the necessary bias current can be supplied.
(2) V_{OUT} is the differential output voltage, ($V_{OUT–}$ – V_{OUT+}).
(3) VOCM refers to the voltage measured at pin 7. V_{OCM} = [(V_{OUT+} + $V_{OUT–}$)/2] refers to the average output voltage.
(4) The offset between the voltage measured at the VOCM pin and the midsupply voltage.

6.7 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 5$ V

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = open, VICM = open, R_F = 5 kΩ, G = 10 V/V, ICM loop disabled, R_L = 1 kΩ, single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25°C$, 1 (unless otherwise noted).



V_{OUT} = 100 mV_{PP}

Figure 6-1. Small-Signal Frequency Response vs Gain

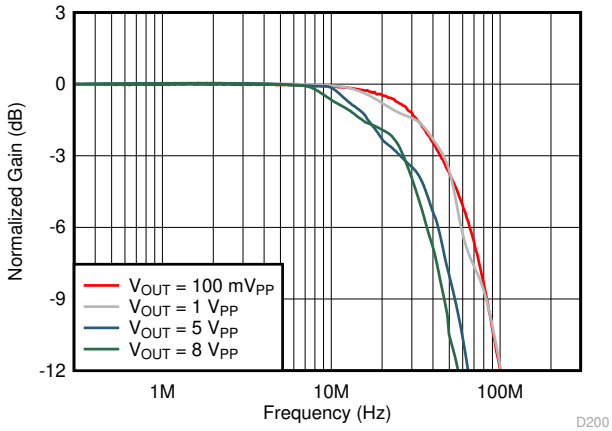


Figure 6-2. Frequency Response vs V_{OUT}

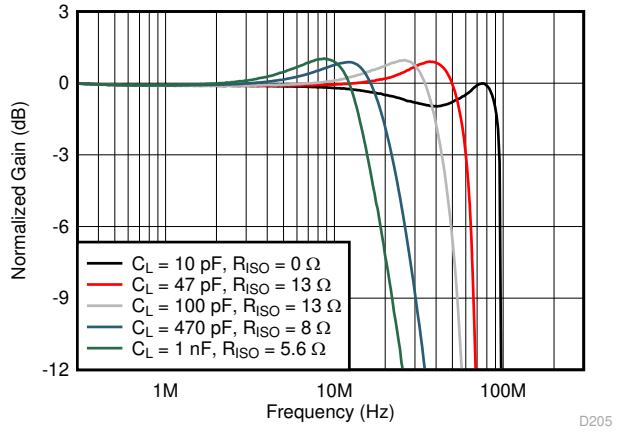
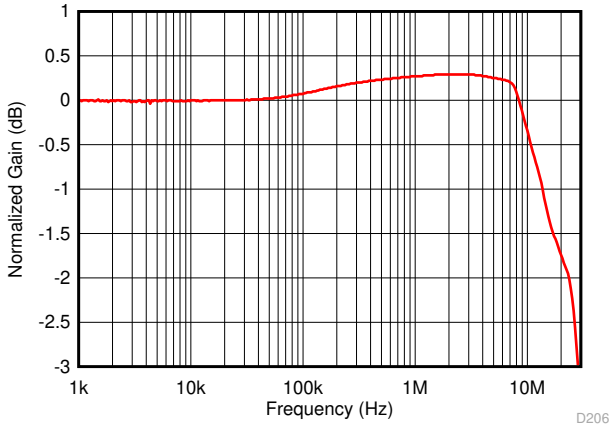


Figure 6-3. Small-Signal Frequency Response vs C_L



V_{OUT} = 8 V_{PP}

Figure 6-4. Large-Signal Frequency Response Flatness

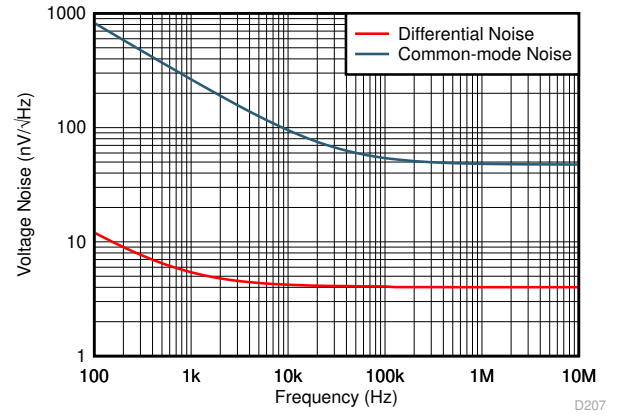
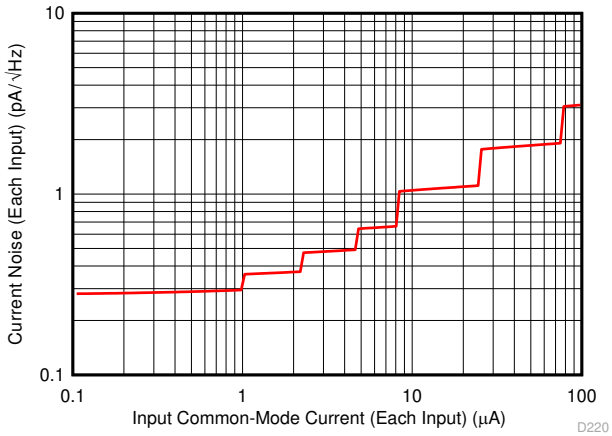


Figure 6-5. Input Referred Voltage Noise vs Frequency



f = 100 kHz, ICM loop enabled

Figure 6-6. Input Referred Current Noise vs I_{CM_CTL}

6.7 Typical Characteristics: $(V_{S+}) – (V_{S–})$ = 5 V (continued)

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = open, VICM = open, R_F = 5 kΩ, G = 10 V/V, ICM loop disabled, R_L = 1 kΩ, single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25°C$, 1 (unless otherwise noted).

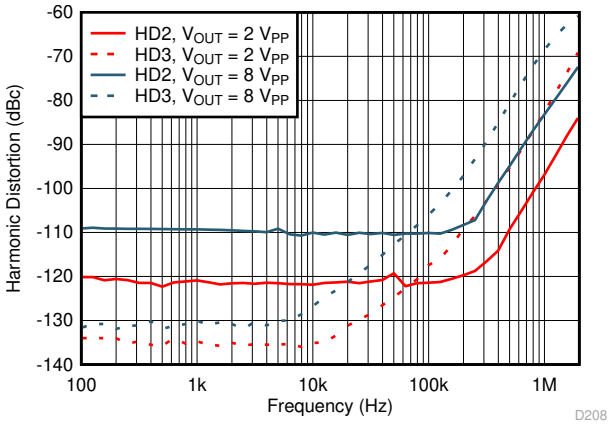


Figure 6-7. Harmonic Distortion vs Frequency

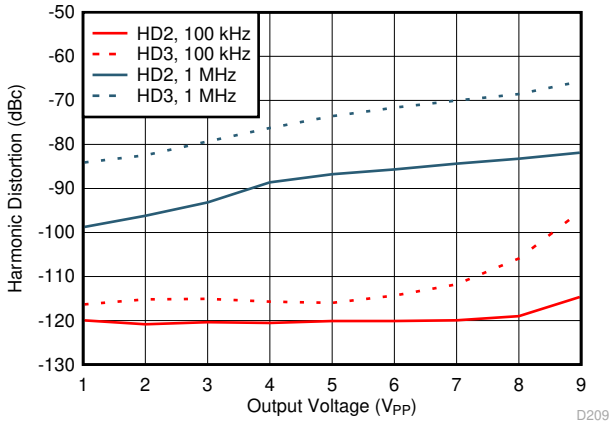
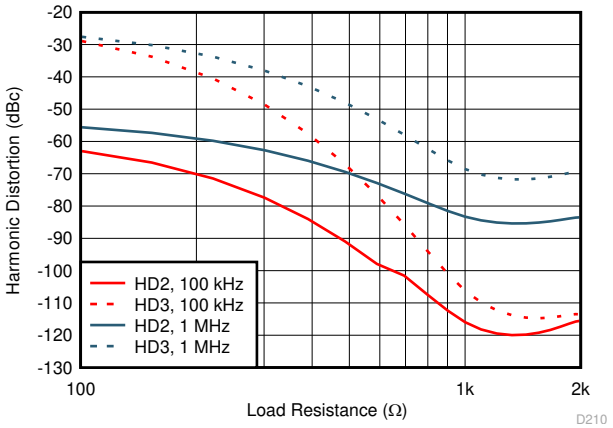
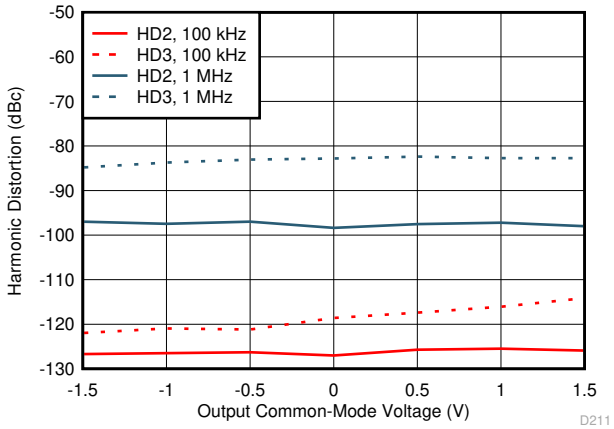


Figure 6-8. Harmonic Distortion vs V_{OUT}



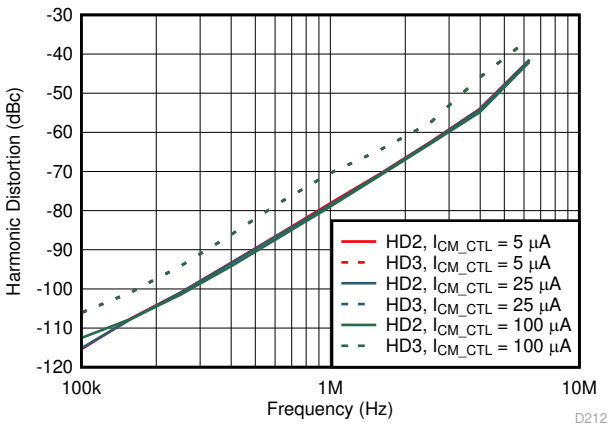
V_{OUT} = 8 V_{PP}

Figure 6-9. Harmonic Distortion vs R_L



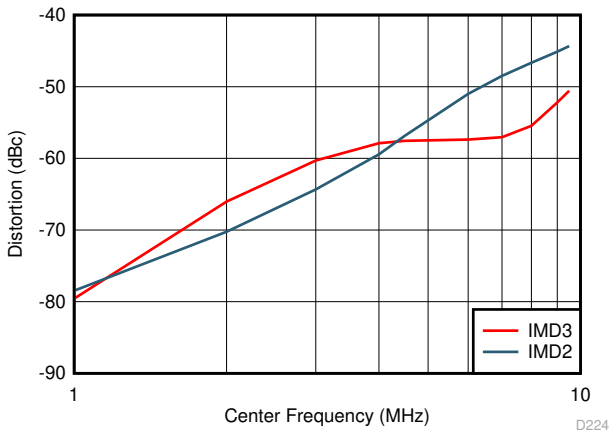
V_{OUT} = 8 V_{PP}

Figure 6-10. Harmonic Distortion vs V_{OCM}



V_{OUT} = 8 V_{PP}; Differential input to differential output; ICM Loop Enabled

Figure 6-11. Harmonic Distortion vs I_{CM_CTL}

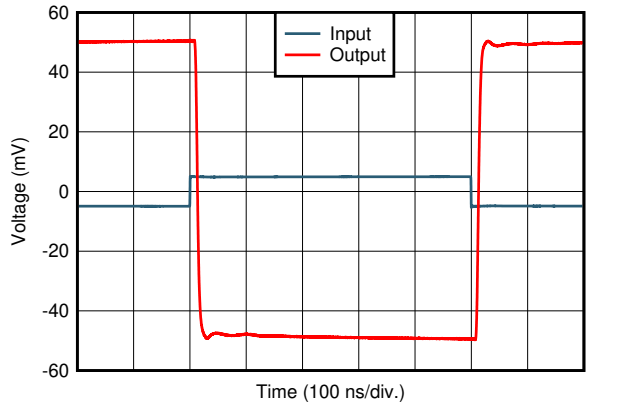


V_{OUT} = 2 V_{PP} (each tone), Tone separation from center frequency = 100 kHz

Figure 6-12. Intermodulation Distortion vs Frequency

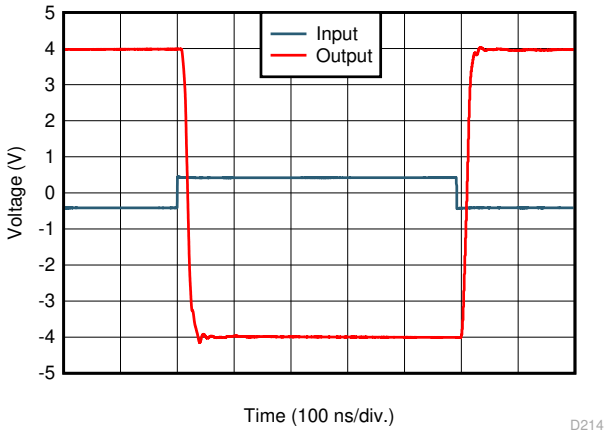
6.7 Typical Characteristics: (V_{S+}) – ($V_{S–}$) = 5 V (continued)

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = open, VICM = open, R_F = 5 kΩ, G = 10 V/V, ICM loop disabled, R_L = 1 kΩ, single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25°C$, 1 (unless otherwise noted).



t_R/t_F = 8 ns

Figure 6-13. Small-Signal Transient Response



Slew rate (rising and falling) = 500 V/µs

Figure 6-14. Large-Signal Transient Response

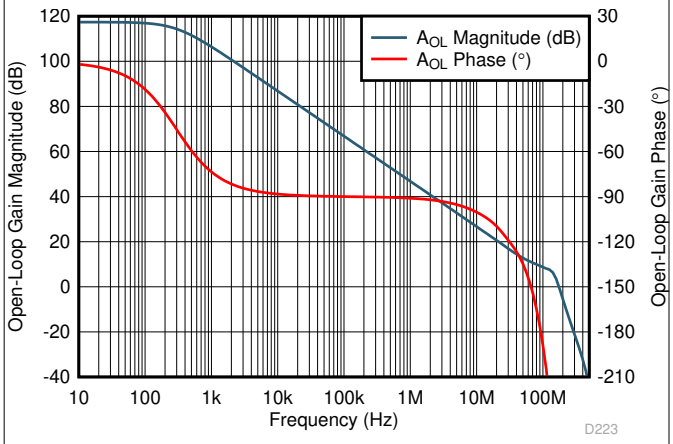
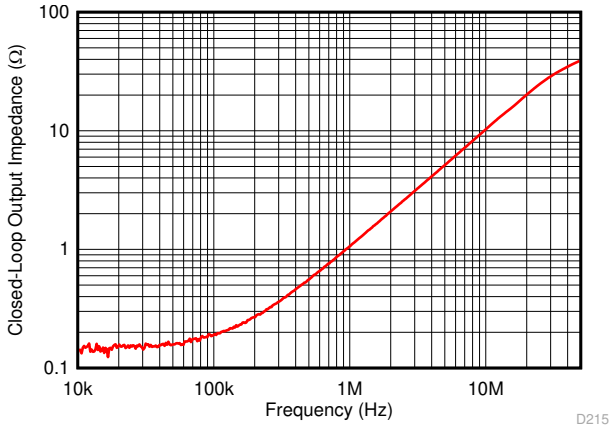


Figure 6-15. Open-Loop Gain



G = 1 V/V, V_{OUT} = 2 V_{PP}, with V_{OCM} adjusted

Figure 6-16. Closed-Loop Output Impedance vs Frequency

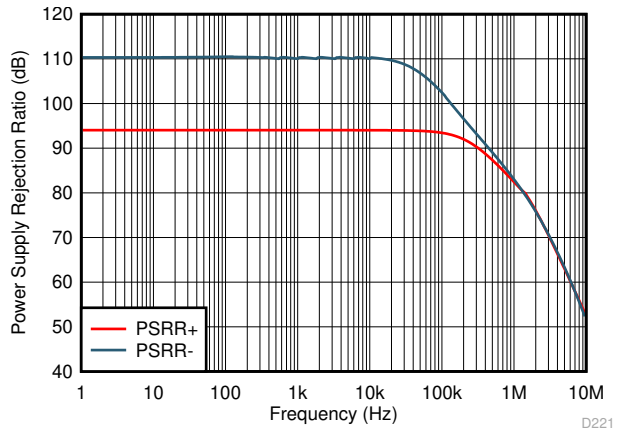


Figure 6-17. Power-Supply Rejection Ratio vs Frequency

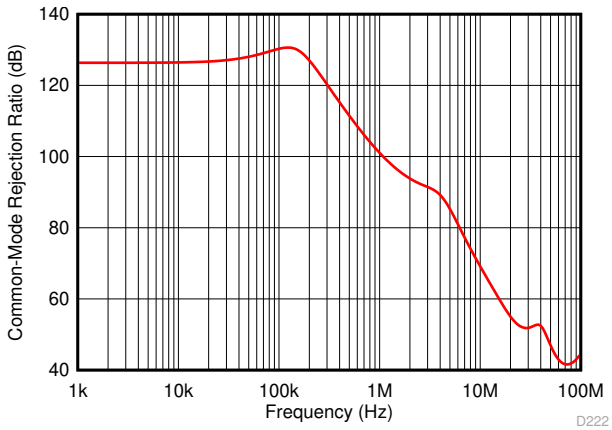
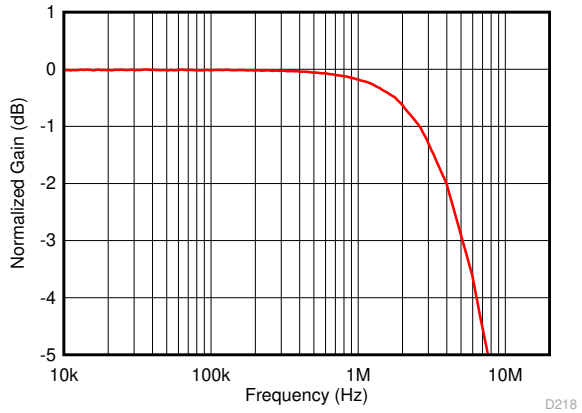


Figure 6-18. Common-Mode Rejection Ratio vs Frequency

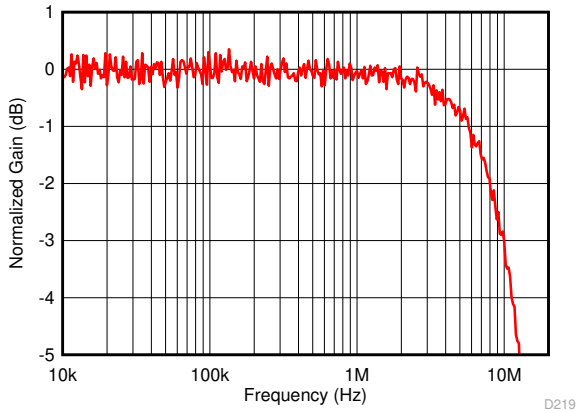
6.7 Typical Characteristics: $(V_{S+}) – (V_{S–})$ = 5 V (continued)

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = open, VICM = open, R_F = 5 kΩ, G = 10 V/V, ICM loop disabled, R_L = 1 kΩ, single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25°C$, 1 (unless otherwise noted).



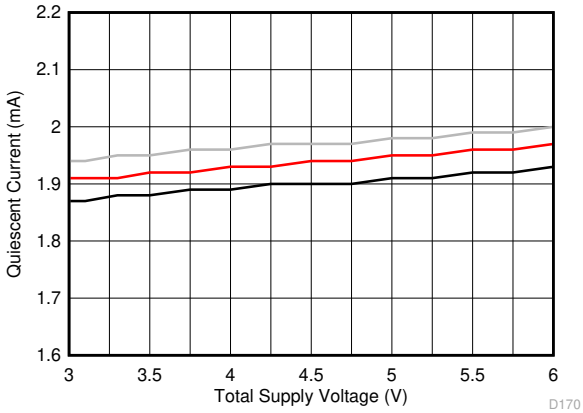
VOCM pin driven with 100 mV_{PP} signal. Average output voltage measured.

Figure 6-19. VOCM Loop Small-Signal Frequency Response



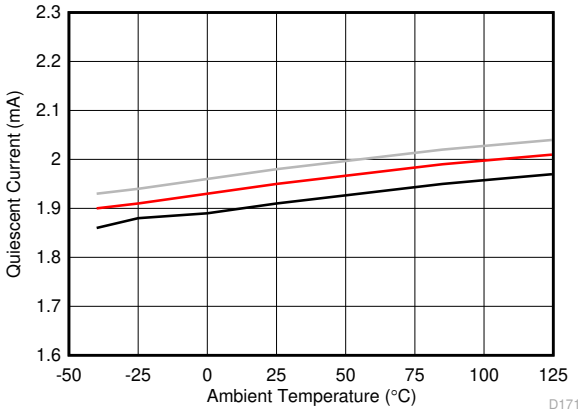
VICM pin driven with 100 mV_{PP} signal. Average input voltage measured.

Figure 6-20. VICM Loop Small-Signal Frequency Response



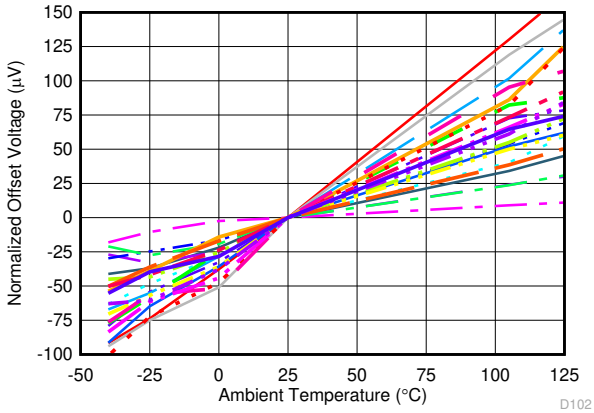
3 Typical Units

Figure 6-21. Quiescent Current vs Total Supply Voltage



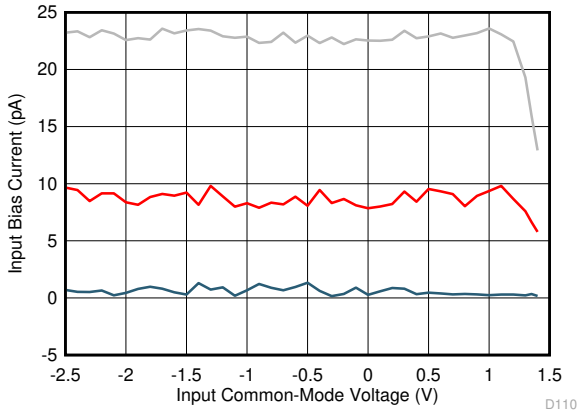
Typical Unit

Figure 6-22. Quiescent Current vs Ambient Temperature



V_{OS} normalized at 25°C

Figure 6-23. Offset Voltage vs Ambient Temperature

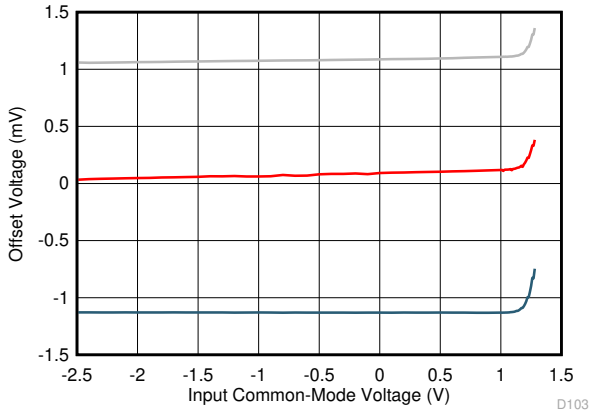


3 Typical Units

Figure 6-24. Input Bias Current vs Input Common-Mode Voltage

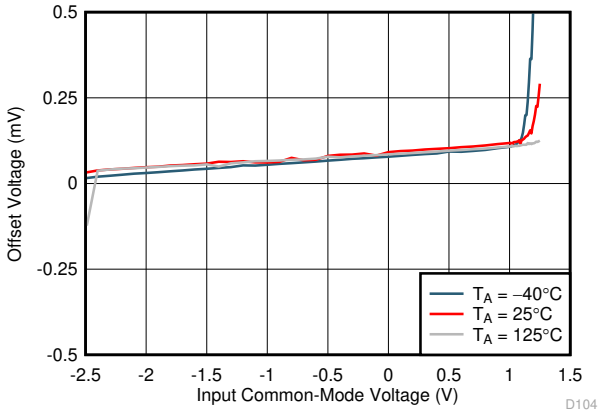
6.7 Typical Characteristics: (V_{S+}) – ($V_{S–}$) = 5 V (continued)

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = open, VICM = open, R_F = 5 kΩ, G = 10 V/V, ICM loop disabled, R_L = 1 kΩ, single-ended input, differential output, and input and output referenced to midsupply and T_A ≈ 25°C, 1 (unless otherwise noted).



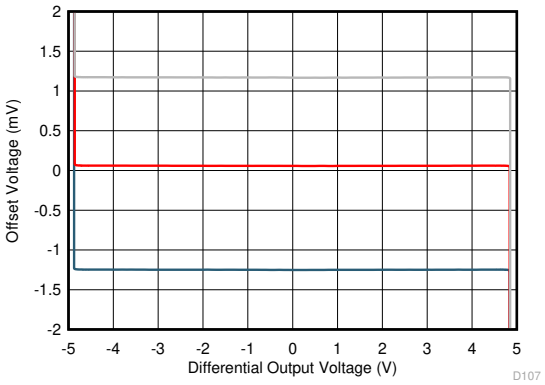
3 Typical Units

Figure 6-25. Offset Voltage vs Input Common-Mode Voltage



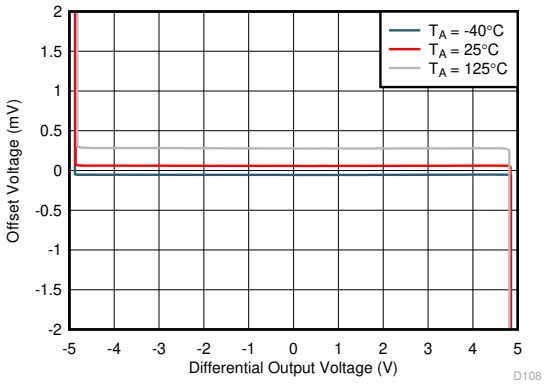
3 Typical Units

Figure 6-26. Offset Voltage vs Input Common-Mode Voltage vs Ambient Temperature



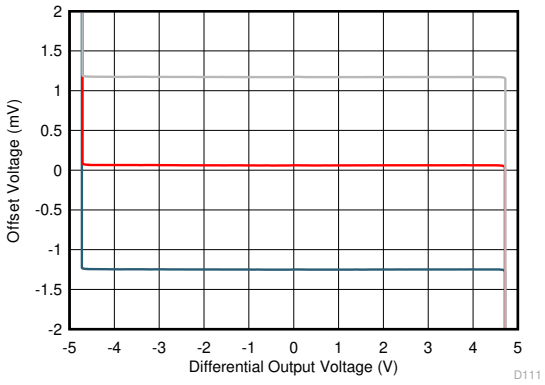
3 Typical Units, R_L = 20 kΩ

Figure 6-27. Offset Voltage vs Differential Output Voltage



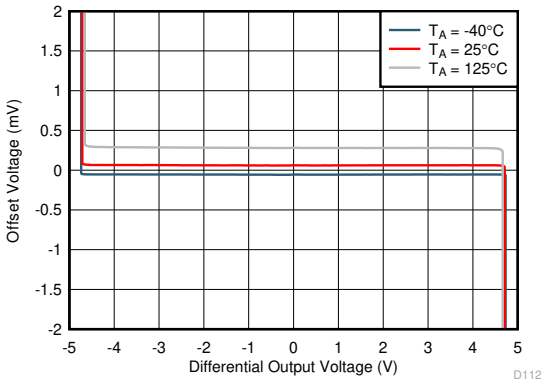
Typical Unit, R_L = 20 kΩ

Figure 6-28. Offset Voltage vs Differential Output Voltage vs Ambient Temperature



3 Typical Units, R_L = 1 kΩ

Figure 6-29. Offset Voltage vs Differential Output Voltage

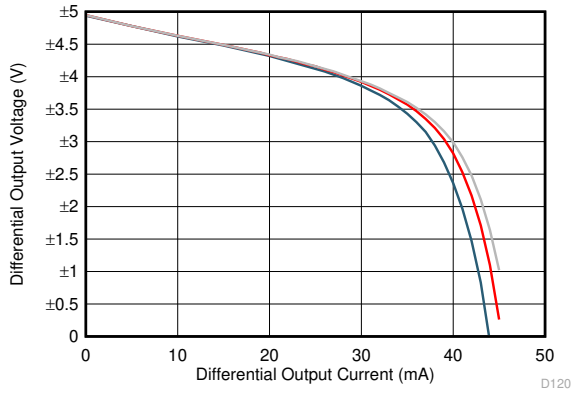


Typical Unit, R_L = 1 kΩ

Figure 6-30. Offset Voltage vs Differential Output Voltage vs Ambient Temperature

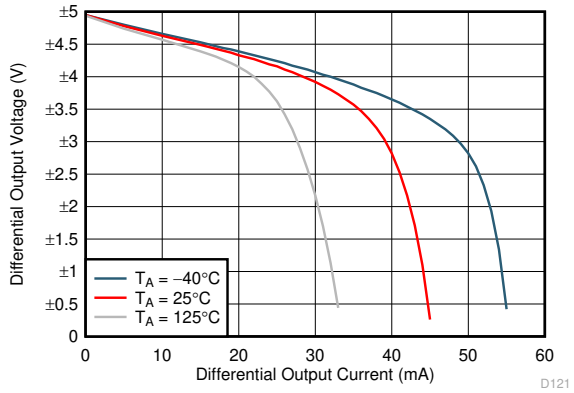
6.7 Typical Characteristics: $(V_{S+}) – (V_{S–}) = 5$ V (continued)

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = open, VICM = open, R_F = 5 kΩ, G = 10 V/V, ICM loop disabled, R_L = 1 kΩ, single-ended input, differential output, and input and output referenced to midsupply and $T_A \approx 25°C$, 1 (unless otherwise noted).



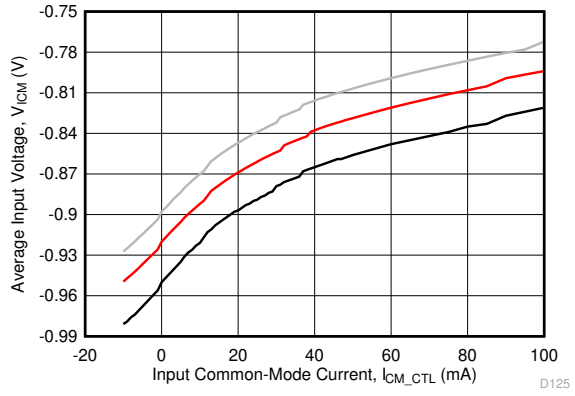
3 Typical Units

Figure 6-31. Differential Output Voltage vs Load Current



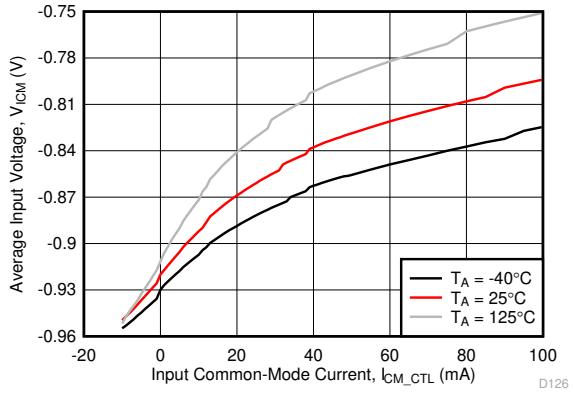
Typical Unit

Figure 6-32. Differential Output Voltage vs Load Current vs Ambient Temperature



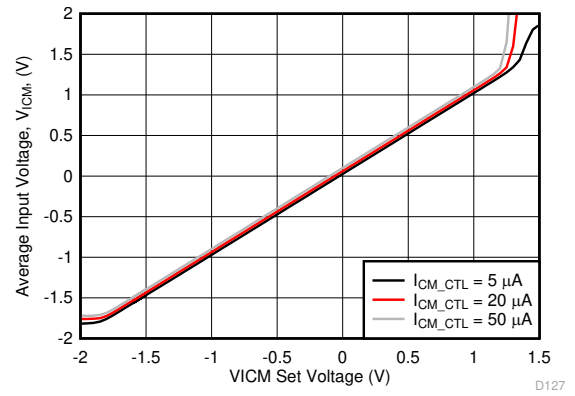
VICM pin floating, 3 Typical Units

Figure 6-33. Average input Voltage vs Input Common-Mode Current



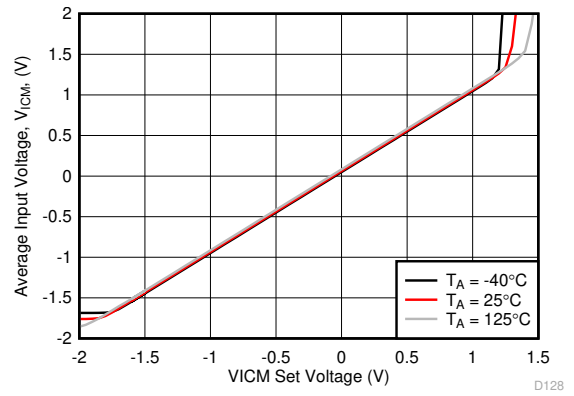
VICM pin floating, Typical Unit

Figure 6-34. Average Input Voltage vs Input Common-Mode Current vs Ambient Temperature



Typical Unit

Figure 6-35. Average Input Voltage vs VICM Set Voltage

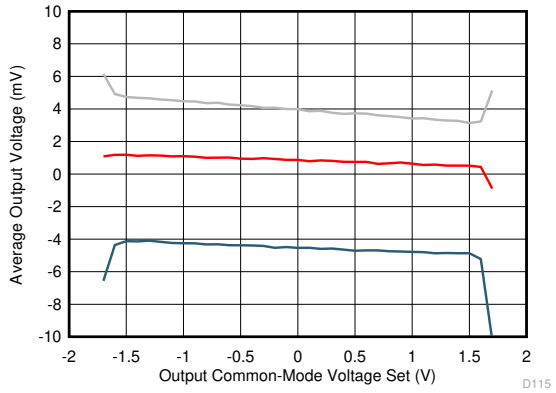


I_{CM_CTL} = 20 µA, Typical Unit

Figure 6-36. Average Input Voltage vs VICM Set Voltage vs Ambient Temperature

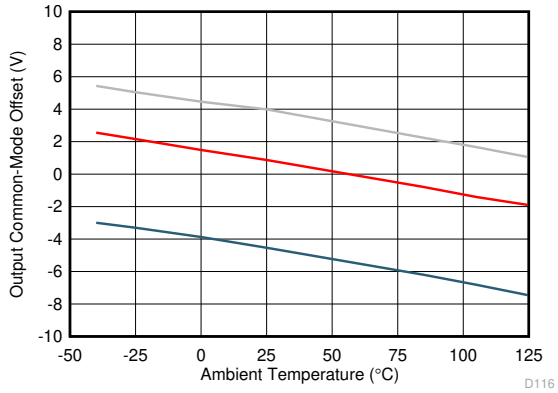
6.7 Typical Characteristics: (V_{S+}) – ($V_{S–}$) = 5 V (continued)

V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, VOCM = open, VICM = open, R_F = 5 kΩ, G = 10 V/V, ICM loop disabled, R_L = 1 kΩ, single-ended input, differential output, and input and output referenced to midsupply and T_A ≈ 25°C, 1 (unless otherwise noted).



VOCM offset = (VOCM - V_{OCM}), 3 Typical Units

Figure 6-37. Output Common-Mode Offset Voltage vs Output Common-Mode Set Voltage



VOCM = 0 V, 3 Typical Units

Figure 6-38. Output Common-Mode Offset Voltage vs Ambient Temperature

7 Detailed Description

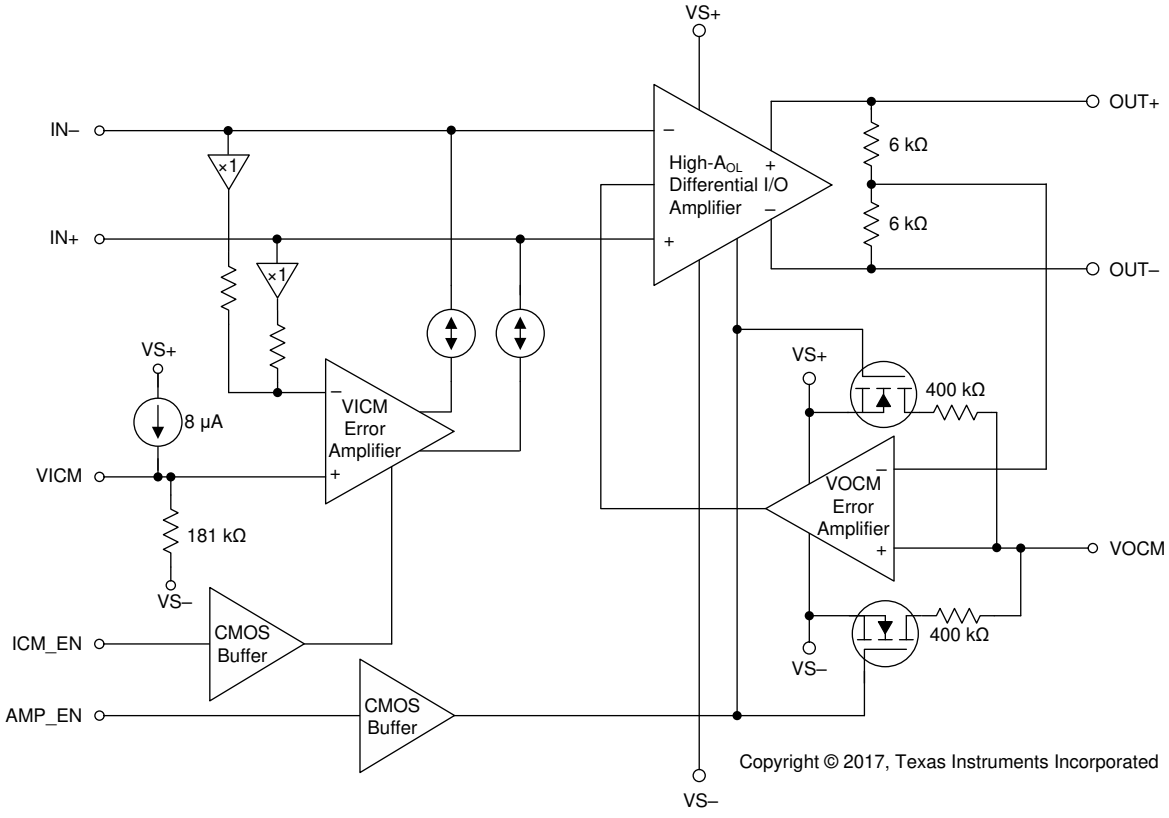
7.1 Overview

The THS4567 device is a unique fully differential amplifier that features an input common-mode control loop in addition to the output common-mode control loop typically found in all fully differential amplifiers. The THS4567 device has a high impedance CMOS input stage with a very low input bias current. The independent input and output common-mode control along with the high impedance CMOS inputs make the THS4567 device an ideal high-gain, low-noise, fully-differential transimpedance amplifier.

The input common-mode loop of the THS4567 device may be disabled by setting the ICM_EN pin below its turnoff threshold voltage, turning it into a standard fully differential amplifier with output common-mode control only. The THS4567 device operates over a wide power supply voltage range from 3.3 V to 5.5 V, which makes this device an excellent choice for driving differential ADCs and buffering DAC outputs.

This device features a low-power mode with a unique active pullup resistor that improves EMI reliability of the shutdown pin when left floating. The AMP_EN and ICM_EN pins draw very little bias current when the logic voltage is outside the switching threshold region. Within the switching threshold region, the bias current increases, especially close to the transition region. The increased bias current prevents the logic from inadvertently switching in the presence of EMI.

7.2 Functional Block Diagram



7.3 Feature Description

The THS4567 architecture features three main building blocks:

1. A high open loop gain differential I/O main amplifier.
2. An output common-mode control error amplifier that sets the common-mode of the differential outputs of the main amplifier.
3. An input common-mode control error amplifier that sets the common-mode of the differential inputs of the main amplifier, independent of the output common-mode.

7.3.1 Main Amplifier

The main differential I/O amplifier has a wide gain bandwidth product of 220 MHz and is stable in gain configurations > 10 V/V. Figure 6-15 shows the open-loop response of the main amplifier. The main amplifier has a high-impedance CMOS input stage with very low input bias currents, which makes it ideal for use in high-gain transimpedance systems or as a voltage amplifier with large feedback and gain resistors.

7.3.2 Output Common-Mode Control

The output common-mode loop works by sensing the average voltage between the two outputs of the main amplifier through the two 6-kΩ resistors internal resistors in Section 7.2 and comparing it against the voltage at the VOCM pin. The VOCM error amplifier then adjusts the internal bias of the main amplifier to minimize the error voltage between its input pins. The voltage at the VOCM node defaults to midsupply through the two 400-kΩ internal bias string resistors between VS+ and VS–. When using the VOCM at its default voltage, connect an external capacitor to the VOCM pin to bypass the noise from the internal 400-kΩ resistors. When the amplifier is disabled, the default midsupply bias string is disabled to save power. The THS4567 device output common-mode can also be set by driving the VOCM pin externally through a low output impedance source. Ensure that the source is capable of driving the input impedance of the VOCM pin.

7.3.3 Input Common-Mode Control

The THS4567 device features a unique input common-mode control error amplifier that sets the input common-mode voltage independent of the output common-mode voltage. The VICM error amplifier works by sensing the average voltage at the main amplifiers inputs and then sourcing or sinking an equal amount of current into both the input nodes of the main amplifier to maintain the input common-mode voltage equal to voltage at the VICM pin. If the VICM pin is left floating, its input voltage defaults to 1.5-V above VS–. This voltage is set by the combination of the 8-µA current source and the 181-kΩ resistor shown in Section 7.2. When using the VICM at its default voltage, connect an external capacitor to the VICM pin to bypass the noise from the internal 181-kΩ resistor. The VICM voltage can be set to an arbitrary value by driving the VICM pin externally through a low output impedance source. The input common-mode control loop can be disabled by setting ICM_EN pin low. With the input common-mode loop disabled the THS4567 device behaves like a standard fully-differential amplifier (FDA).

7.4 Device Functional Modes

7.4.1 Shutdown Mode

For proper shutdown mode operation, the amplifier enable (AMP_EN) pin must be asserted to the desired voltage. An internal pullup resistor is provided on the AMP_EN pin so that if the pin is floated, then the device defaults to an ON state. For applications that require the device to be constantly powered on when the supplies are present, tie the AMP_EN pin to the positive supply voltage (VS+).

The disable operation is referenced from the positive supply. For an OFF state condition, the disable control pin must be 2 V below the positive supply.

7.4.2 Differential Transimpedance Amplifier Mode

The primary use case of the input common-mode control loop is in differential transimpedance amplifier applications where two photodiodes are excited by a differential input. Any ambient light that is incident on both photodiodes will produce a DC offset current which is subsequently rejected by the input common-mode loop. The input common-mode loop enables the use of very high feedback resistors to amplify the differential photodiode current while simultaneously rejecting common-mode currents. Disabling the input common-mode loop allows the common-mode current to flow through the feedback resistors thereby reducing the effective output swing for the differential signal component. The THS4567 device can reject sourcing or sinking photodiode currents.

The high impedance CMOS inputs of the THS4567 device minimizes the amplifiers input current noise enabling the use of very high transimpedance gains (>100 kΩ), while the low input voltage noise maximizes the system signal-to-noise ratio (SNR). The high gain bandwidth product of the THS4567 device allows it be used as a single-stage differential transimpedance amplifier while driving a high performance ADC driver.

7.4.3 Fully Differential Amplifier (FDA) Mode

With the input common-mode loop disabled, the THS4567 device behaves like a standard FDA. It can convert a single-ended input signal to a differential output or a differential input to a differential output with independent output common-mode control. For a detailed understanding of FDA operation check out the training video.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Noise Analysis

To simplify the noise calculation of an FDA configured as a TIA, split the circuit into two identical halves and treat each half as an independent op amp circuit. The noise of an op amp configured as a TIA is shown in Transimpedance Considerations for High-Speed Amplifiers and is repeated in Equation 1. The equivalent noise circuit is shown in Figure 8-1. The amplifiers voltage noise e_{NOP} in Figure 8-1 is the specified input-referred voltage noise of the THS4567 (e_N) divided by 1.414. This method enables us to analyze the FDA as two identical and uncorrelated halves. The total noise of the FDA is the total noise of each half multiplied by 1.414.

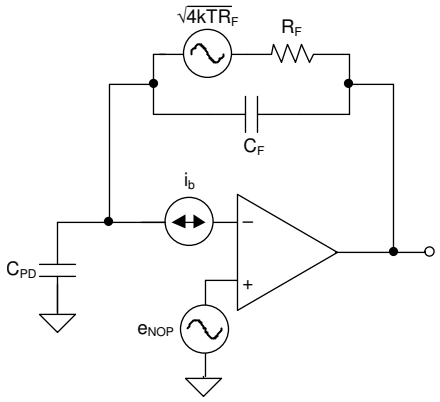


Figure 8-1. Transimpedance Amplifier Noise Analysis Circuit

To minimize the total noise of a TIA the circuit designer should:

1. Minimize the current noise of the op amp (i_b). Since the THS4567 device has CMOS inputs its current noise contribution can be ignored.
2. Maximize the transimpedance gain (R_F).
3. Minimize the amplifiers voltage noise (e_N). The THS4567 possesses a class leading 4.2 nV/ $\overline{Hz}$ of broadband voltage noise while consuming less than 2.5 mA of quiescent current.
4. Minimize the photodiode capacitance (C_{PD}).

The capacitance of a photodiode can be minimized by increasing its reverse bias. The THS4567 input and output common-mode can be independently controlled. The independent control feature allows the circuit designer to set photodiode's anode close to the negative supply voltage while tying its cathode close to the positive supply voltage to maximize the reverse bias across the photodiode. The output common-mode is then set to match the next stage ADCs input common-mode range. In a standard op amp TIA, the input common-mode is biased close to the positive supply to maximize the output swing of the amplifier. This bias configuration limits the reverse bias across the photodiode thereby increasing its input capacitance. The THS4567 device is optimized to reduce total system noise by optimizing the noise source from each contributing source in Equation 1.

$$i_{EQ} = \sqrt{i_b^{\,2} + \frac{4kT}{R_F} + \left[\left(\frac{e_n}{R_F}\right)^2 + \frac{\left(e_n \cdot 2\pi \cdot F \cdot C_s\right)^2}{3}\right] / 2} \tag{1}$$

where

- i_b = current noise of the THS4567 device
- 4kT = 16 × 10^{-21}J at 290 degrees Kelvin
- R_F = feedback resistor
- e_N = voltage noise of the THS4567 device
- C_S = total input capacitance from the THS4567, photodiode and any PCB parasitics
- F = noise integration frequency limit

8.2 Typical Application

The primary use case for the THS4567 input common-mode loop is in differential transimpedance applications that have a large common-mode offset due to ambient light. In this section we compare the performance of the THS4567 device with the input common-mode loop enabled (TIA mode) as shown in Figure 8-2 versus a differential TIA implementation built using two discrete op amp channels (OPA mode) as shown in Figure 8-3.

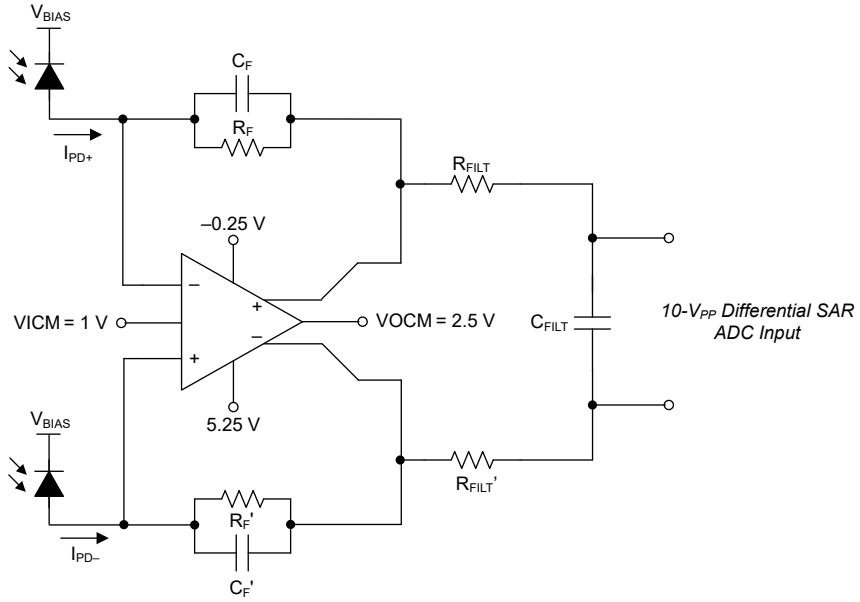


Figure 8-2. THS4567 with Integrated Differential TIA + ADC Driver

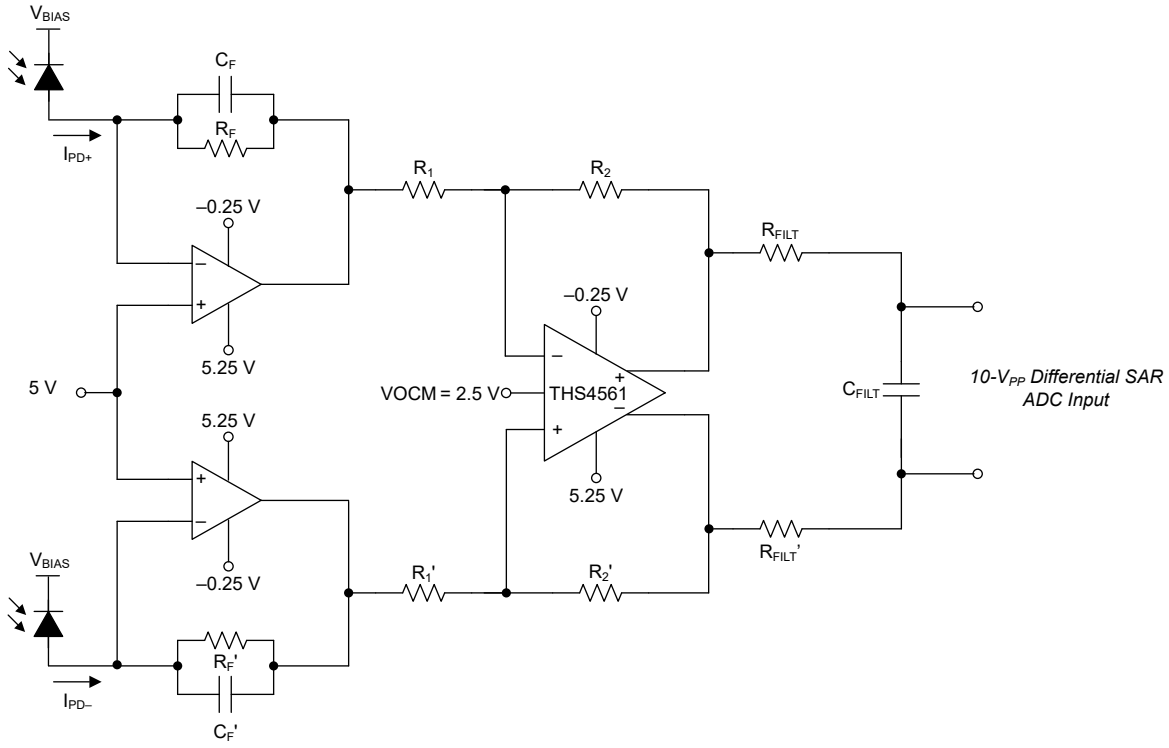


Figure 8-3. Discrete Differential Op Amp TIA + 2nd Stage ADC Driver

8.2.1 Design Requirements

The requirements for this application are:

- Supply voltage: 5.5 V
- ADC full-scale range: 10 V_{PP} differential
- ADC input common-mode voltage: 2.5 V
- Ambient light current offset (DC): 10 µA
- Single-sided signal current: 5 μA_{PP} (each photodiode). Differential signal current = 10 μA_{PP}
- Input signal frequency: 100 kHz

8.2.2 Detailed Design Procedure (THS4567 in TIA Mode)

The output current from each photodiode is shown in Figure 8-4. A detailed procedure on how to set the various bias voltages and select the optimal value of transimpedance gain follows.

- Set V_{S+} = 5.25 V and $V_{S–}$ = –0.25 V to allow the THS4567 to swing 10 V_{PP} (differential) without introducing distortion due to limited headroom.
- Set ICM_EN = logic high to enable the THS4567 TIA mode of operation.
- Set VOCM to 2.5 V to match the ADC input common-mode range.
- With the photodiodes (PDs) configured with a cathode bias as shown in Figure 8-2 both PDs will source current when light is incident on them. To maximize the reverse bias across the PD, V_{BIAS} is typically set to the amplifiers positive supply voltage or the highest available positive supply voltage.
- The maximum output current from the PD is the sum of the ambient light current and the maximum signal current.

$$I_{TOTAL} = I_{AMBIENT} + I_{SIGNAL} = 10\ \mu A + 5\ \mu A = 15\ \mu A \quad (2)$$

- In the TIA mode, VICM is set to its minimum input common-mode compliance limit (1.25 V) to maximize the reverse bias across the PDs thereby reducing the PD capacitance.

$$\text{Reverse bias across the photodiodes} = (5.25\ V - 1.25\ V) = 4\ V \quad (3)$$

- In the TIA mode, the ICM loop cancels the common-mode input current due to ambient light (10 µA) at the amplifier's input pin and only the differential signal current flows through the feedback resistors R_F and R_F'. The maximum TIA gain is therefore the ratio of the maximum differential output swing and the maximum differential signal current as shown in Equation 4.

$$\text{Maximum TIA gain} = (10\ V_{PP} / 10\ \mu A) = 1\ M\Omega \quad (4)$$

- Once the feedback resistor value is set, select the value of feedback capacitance as described in Transimpedance Considerations for High-Speed Amplifiers.

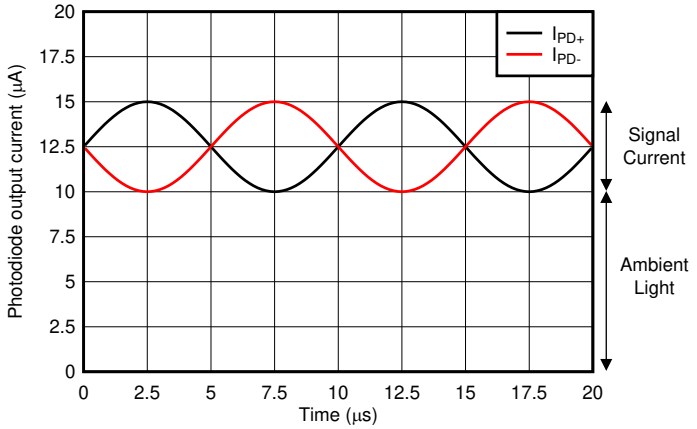


Figure 8-4. Photodiode Differential Output Current

8.2.2.1 OPA Mode Configuration

The OPA mode configuration is shown in Figure 8-3. This configuration results in a reverse bias of (5.25 V - 5 V = 0.25 V) across the PD thereby greatly increasing the PD capacitance compared to the TIA mode.

In the OPA mode there is no input common-mode current cancellation so the maximum value of feedback resistance (R_F, R_F') is the ratio of the maximum single-ended output swing and the maximum single-ended input current as shown in Equation 5.

$$\text{Maximum TIA gain} = (5\ \text{V}/15\ \mu\text{A}) = 333.33\ \text{k}\Omega \tag{5}$$

The total differential swing is 333.33 kΩ × 10 μA_{PP} = 3.33 V. To maximize the ADC gain range a subsequent amplifier gain stage is needed. The second gain stage which is typically implemented with a standard FDA like the THS4561 will also adjust the output common-mode to match the ADCs input common-mode compliance range.

As the level of ambient light increases relative to the differential signal from the PD, the maximum gain configuration in the OPA mode will decrease while it stays constant for the THS4567 TIA mode.

8.2.3 Application Curves

Figure 8-5 shows the output of the THS4567 device in TIA mode. The output common-mode is centered on VOCM = 2.5 V and the differential output of 10 V_{PP} maximizes the subsequent ADCs entire common-mode range.

Figure 8-6 shows the output of the first stage transimpedance amplifier setup shown in Figure 8-3. The output common-mode is centered on 0.83 V. The offset in the common-mode is caused by the offset due to the ambient light. More importantly the differential output swing is only 3.33 V. To maximize the ADC dynamic range the subsequent THS4561 differential amplifier stage is configured in a signal gain of 3 V/V. The THS4561 device will also perform a level shift to center the output common-mode to 2.5 V.

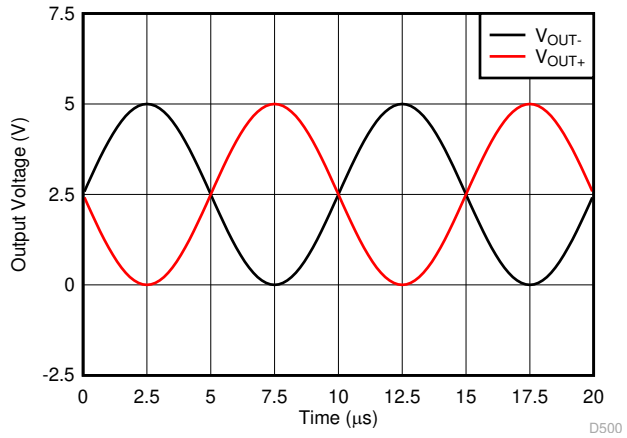


Figure 8-5. Output of THS4567 (TIA Mode)

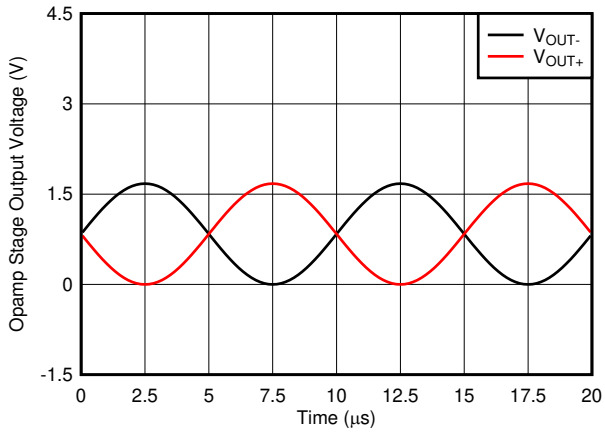


Figure 8-6. Output of the 1st Stage Discrete Op Amp Transimpedance Amplifier (OPA Mode)

The noise performance of the THS4567 device (half-circuit) is then compared against the noise of the OPA607 and the OPA365 in OPA mode. Using Equation 1 we can estimate the total input referred spot noise for the THS4567 device. Transimpedance Considerations for High-Speed Amplifiers is used to estimate the noise of the OPA607 and OPA365 transimpedance amplifier stage in OPA mode.

A PD capacitance of 5 pF is assumed. In a real world system the PD capacitance will be higher in OPA mode because of the lower reverse bias across the PD. The calculated noise results are shown in Table 8-1 where the benefit of the THS4567 device can clearly be seen. The spot noise has been normalized to the closed loop bandwidth. The OPA mode architecture would require a second gain stage to maximize the ADCs input full scale range. The second stage would increase the power consumption and degrade the noise.

Table 8-1. Noise Comparison

Amplifier Specification	THS4567	OPA607	OPA365
Photodiode Capacitance (pF)	5	5	5
Amplifier Input Capacitance (pF)	1	17	8
Amplifier Voltage Noise (nV/√Hz)	4.2	3.8	4.5
TIA Gain (kΩ)	1000	333.33	333.33
Closed Loop Bandwidth (MHz)	2.4	1	1.4
Input-Referred Spot Noise (pA/√Hz)	0.2	0.39	0.36

8.3 Differential TIA with 0-V Biased Photodiode

The circuit in Figure 8-7 can be used for a differential TIA with 0-V reverse bias across the photodiode. The VICM loop should be disabled in this configuration since the loop can only source or sink DC current. Any DC current generated by the photodiode in the configuration shown will be differential in nature.

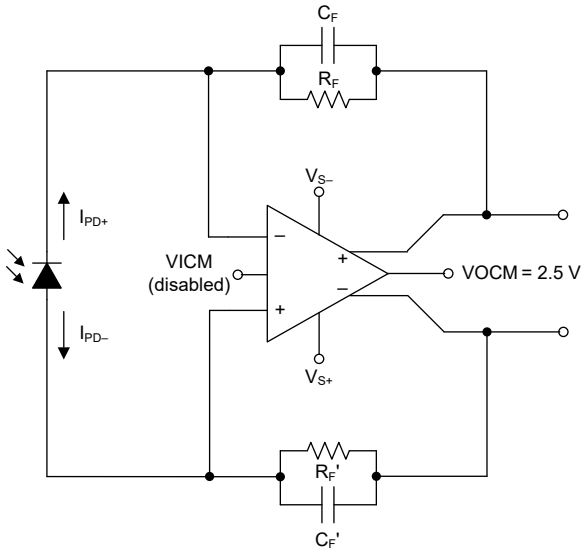


Figure 8-7. Differential TIA with 0-V Biased Photodiode

8.4 Differential AC Coupled TIA

The circuit in Figure 8-8 can be used as a differential AC-coupled TIA with variable reverse bias across the photodiode. Since no DC current flows in the feedback network due to the AC coupling the VICM loop can be disabled.

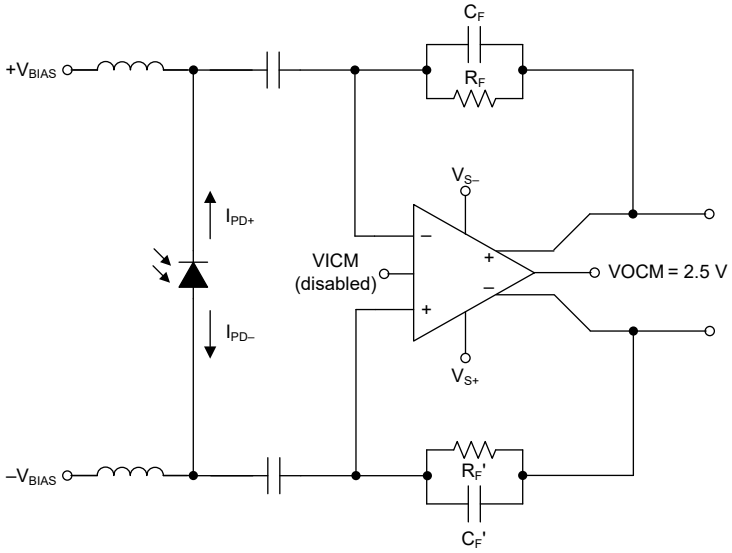


Figure 8-8. Differential AC Coupled TIA

9 Power Supply Recommendations

The THS4567 device is principally intended to operate with a nominal single-supply voltage of 3.3 V to 5.5 V. Split (or bipolar) supplies can be used with the THS4567 device, as long as the total value across the device remains less than 5.5 V. A low power-supply source impedance must be maintained across frequency so use multiple bypass capacitors in parallel. Place the bypass capacitors as close to the supply pins as possible. Place the smallest capacitor (< 10 nF) on the same side of the PCB as the THS4567 device. Larger capacitors (> 1 µF) can be placed further away and shared among different devices in the system.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations

Similar to all high-speed devices, best system performance is achieved with close attention to board layout. General high-speed signal path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, both ground and power planes must be opened up around the capacitive sensitive input and output device pins. When the signal goes to a resistor, parasitic capacitance becomes more of a band-limiting issue and less of a stability issue.
- Good high-frequency decoupling capacitors (0.01 µF) are required to a ground plane at the device power pins. Additional higher-value capacitors (2.2 µF) are also required but can be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- Differential signal routing over any appreciable distance must use microstrip layout techniques with matched impedance traces.
- The THS4567 outputs are sensitive to capacitive loading. Isolate the output of the THS4567 from any capacitive load by placing series isolation resistors close to the amplifiers output pins.

10.2 Layout Example

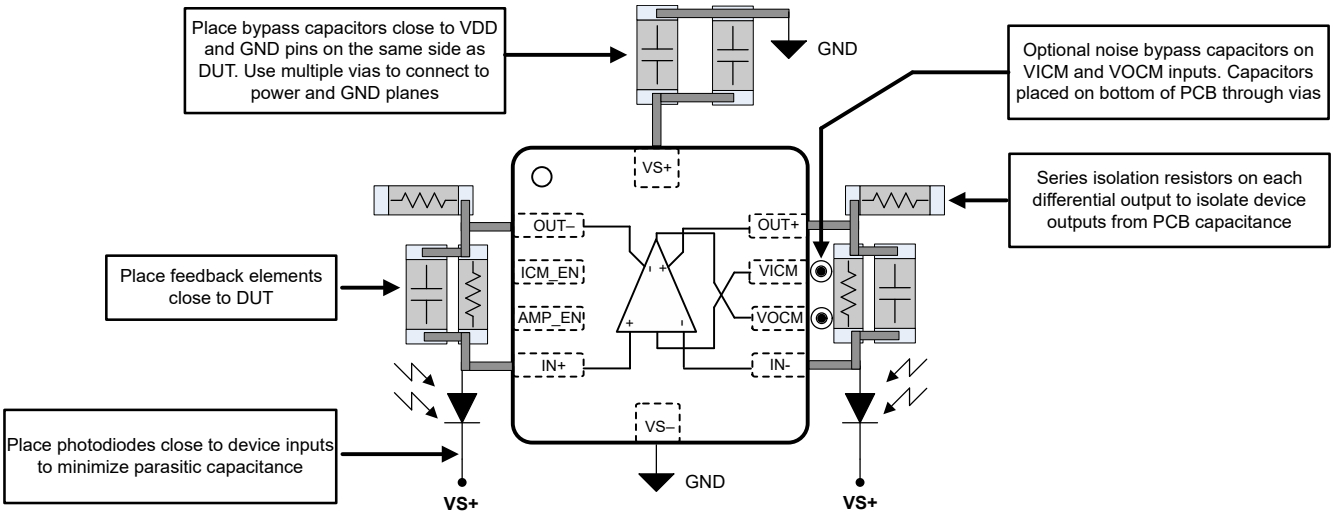


Figure 10-1. Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments,*RUN_FDA_4567 EVM user's guide*
- Texas Instruments, *Fully-Differential Amplifiers application note*
- Texas Instruments, *Fully Differential Amplifiers TI Precision Labs*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4567IRUNR	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SN67
THS4567IRUNR.B	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SN67

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

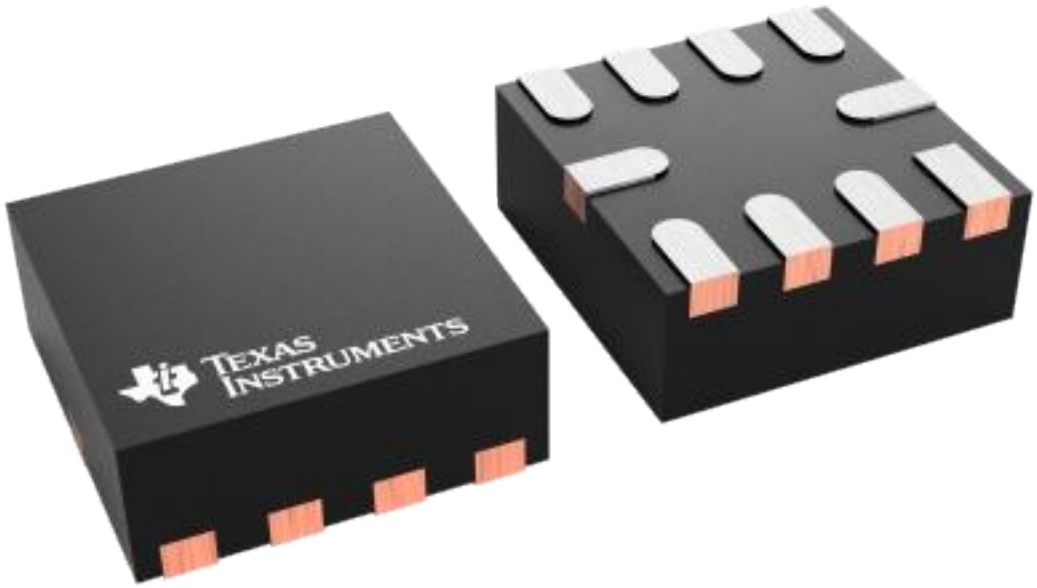
RUN 10

WQFN - 0.8 mm max height

2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



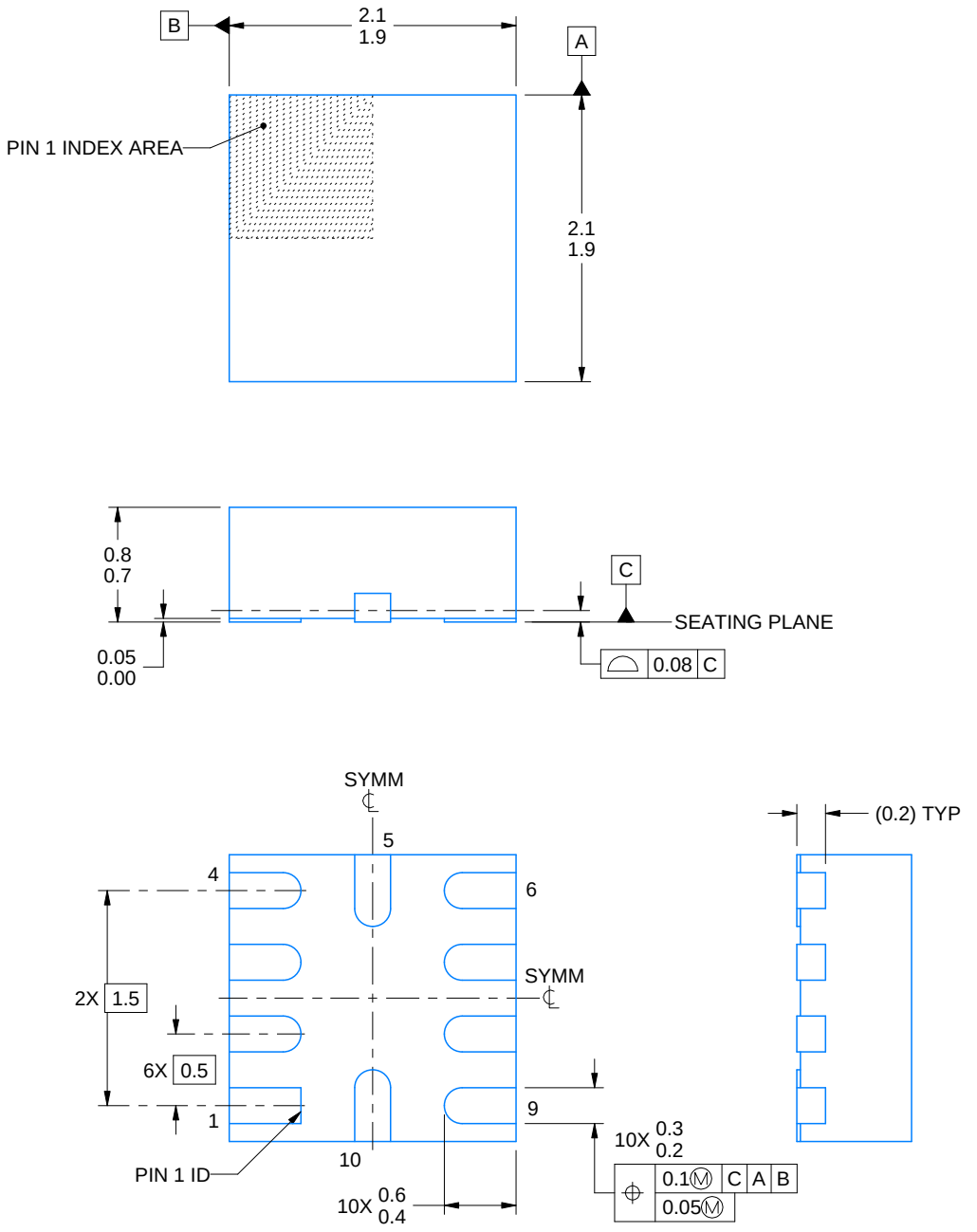
4228249/A

RUN0010A

PACKAGE OUTLINE

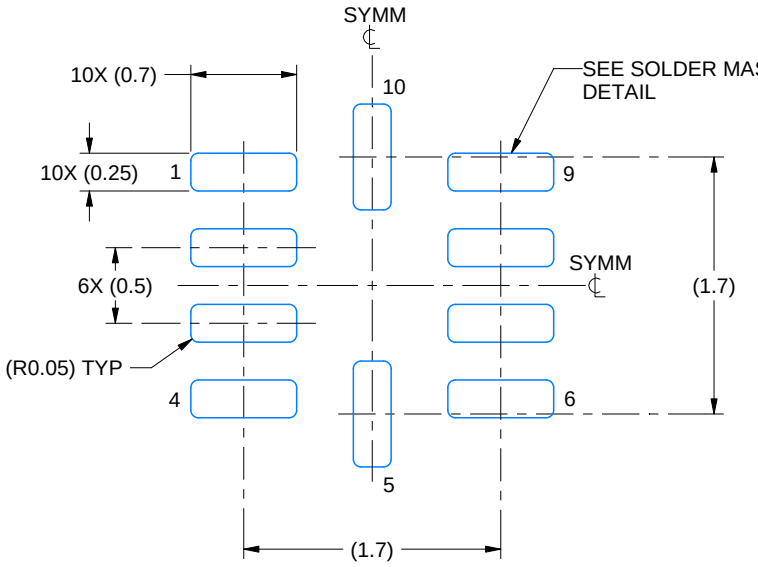
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

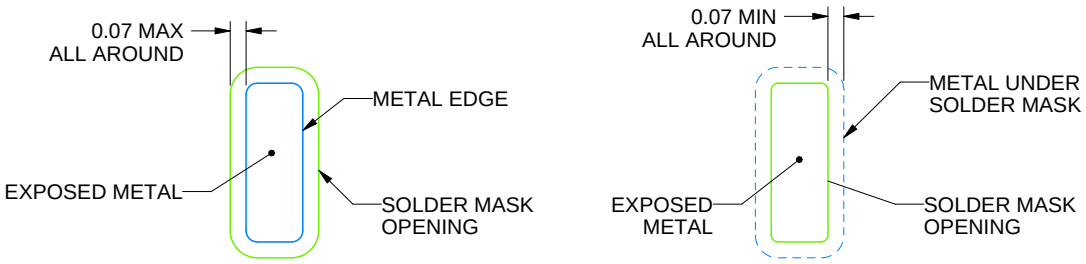


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4220470/A 05/2020

NOTES: (continued)

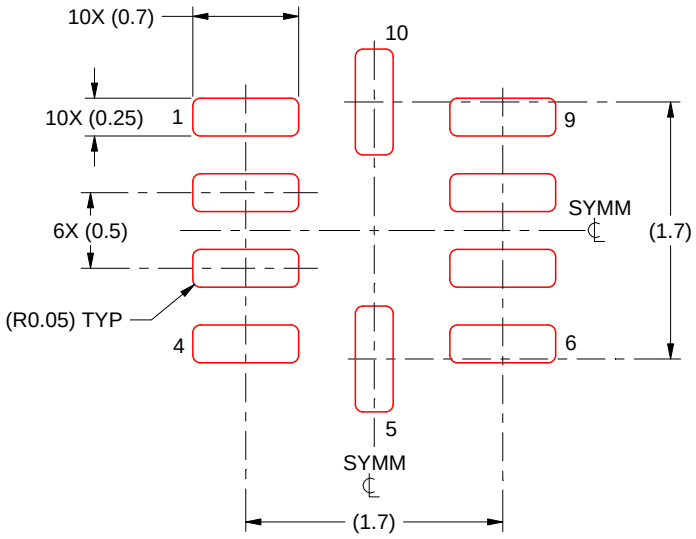
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4220470/A 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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