TCAN6062-Q1 Automotive CAN XL Transceiver with Standby Mode

1 Features

- AEC Q100 Qualified for automotive applications
- Meets the requirements of ISO 11898-2:2024 Annex A: HS-PMA with SIC mode and FAST mode (CAN XL)
- Functional Safety-Capable
  - Documentation will be available upon device release to aid in functional safety system design
- Supports up to 20Mbps signaling rate in FAST mode and up to 8Mbps in SIC mode
  - FAST TX mode and FAST RX mode allow for CAN XL data signaling
  - Actively improves the bus signal by reducing ringing effects in complex topologies
  - Mixed mode network with CAN FD, CAN SIC possible
- V_{IO} level shifting supports 1.71V to 5.5V
- Support for 12V and 24V battery applications
- Receiver common mode input voltage: ±12V
- Protection features:
  - IEC ESD protection on bus pins
  - Bus fault protection: ±58V
  - Undervoltage protection on V_{CC} and V_{IO} supply terminals
  - TXD dominant time-out (TXD DTO)
  - Thermal shutdown protection (TSD)
- Operating Modes
  - Normal mode: SIC, FAST TX, FAST RX
  - Low-power standby mode supporting remote wake-up request
- Passive behavior when unpowered
  - Bus and logic terminals are high impedance (no load to operating bus or application)
  - Hot plug capable: power up/down glitch free operation on bus and RXD output
  - Defined device behavior with floating logic pins and in undervoltage supply conditions
- Available in SOIC (8) and leadless 3mm × 3mm VSON (8) package with wettable flanks for improved automated optical inspection (AOI) capability

2 Applications

- Automotive gateway
- Advanced driver assistance system (ADAS)
- Body electronics and lighting
- Hybrid, electric and powertrain systems
- Automotive infotainment and cluster

3 Description

The TCAN6062-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2024 Annex A (CAN XL) specification. The device supports PWM decoding on TXD pin allowing it to operate in SIC mode, FAST TX mode, and FAST RX mode. For SIC mode, the device reduces signal ringing at dominant-to-recessive edge and enables higher throughput in complex network topologies. For FAST TX mode, device uses H-bridge architecture to actively drive logic states. This driver architecture along with FAST RX thresholds centered around zero and input logic buffer (TXD) threshold centered around 50% enables high speed communication up to 20Mbps in multidrop networks. FAST RX mode uses a high-speed comparator to detect bus traffic up to 20Mbps and convert it to received logic data.

The TCAN6062-Q1 includes internal logic level translation via the V_{IO} logic supply terminal to allow for interfacing directly to 1.8V, 2.5V, 3.3V, or 5V controllers. The transceiver supports low power standby mode which allows remote wake-up via CAN bus compliant with the ISO 11898-2:2024 Annex A defined wake-up pattern (WUP). The device also includes many protection features, including undervoltage detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and ±58V bus fault protection.

These devices are pin-compatible to 8-pin CAN FD and CAN SIC transceivers such as TCAN1044A(V)-Q1 and/or TCAN1472(V)-Q1.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN6062-Q1 TCAN6062V-Q1	VSON (8, DRB)	3mm × 3mm
	SOIC (8, D)	4.9mm × 6mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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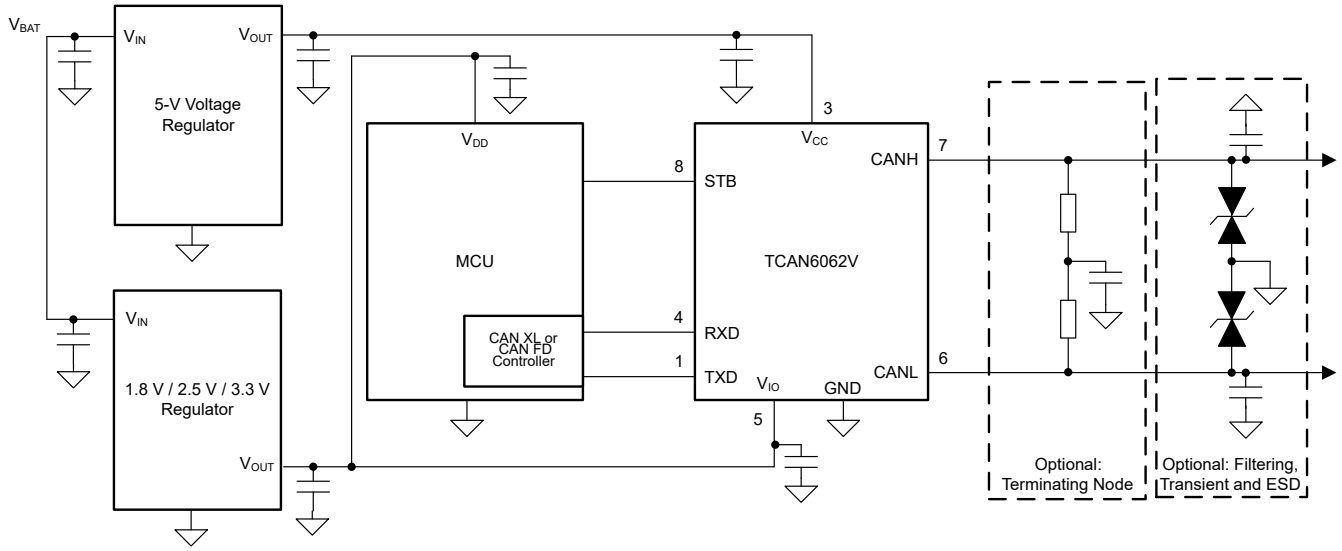

Simplified Block Diagram

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4 Pin Configurations and Functions

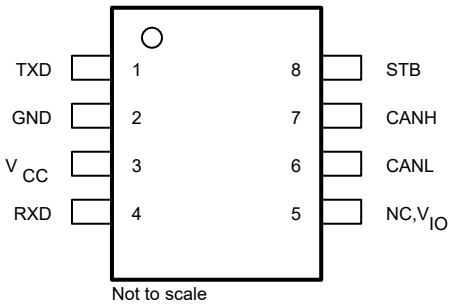

Figure 4-1. SOIC (D) Package, 8 Pin (Top View)

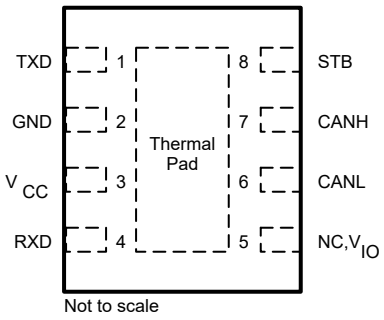

Figure 4-2. VSON (DRB) Package, 8 Pin (Top View)

Table 4-1. Pin Functions

PINS		TYPE	DESCRITION
NAME	NO.		
TXD	1	Digital Input	CAN transmit data input
GND	2	GND	Ground connection
V_{CC}	3	Supply	5V supply voltage
RXD	4	Digital Output	CAN receive data output, tristate when powered off
NC	5	—	Not internally connected; devices without V_{IO}
V_{IO}		Supply	Logic supply voltage; devices with V_{IO}
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby mode control input, integrated pull-up
Thermal Pad (VSON only)		—	Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

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5 Specifications

5.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN bus I/O voltage range on CANH and CANL w.r.t. ground (device powered with TXD static or toggling, device unpowered)	–58	58	V
V_{DIFF}	Max differential voltage between CANH and CANL V_{DIFF} = (CANH - CANL)	–45	45	V
V_{Logic_Input}	Logic pin input voltage (TXD, STB)	–0.3	6	V
V_{RXD}	Logic output voltage range (RXD)	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Junction temperature	–40	165	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±4000	V
			HBM classification level 3B for global pins CANH and CANL with respect to GND	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings, IEC Transients

				VALUE	UNIT
V_{ESD}	System level electrostatic discharge	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605 Powered contact discharge	±8000	V
			SAE J2962-2 per ISO 10605 Powered air discharge	±15000	V
			IEC 62228-3 per ISO 10605	±8000	V
V_{Tran}	ISO 7637-2 Transient immunity(1)		Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	Direct capacitor coupling, SAE J2962-2 per ISO 7637-3(2)		DCC slow transient pulse	±30	V

(1) Tested according to IEC 62228-3:2019 CAN Transcievers Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(2) Tested according to SAE J2962-2

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IO}	Supply voltage for I/O level shifter	1.71		5.5	V

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		MIN	NOM	MAX	UNIT
$I_{OH(RXD)}$	RXD terminal high-level output current	–1.5			mA
$I_{OL(RXD)}$	RXD terminal low-level output current			1.5	mA
T_J	Junction temperature	–40		150	°C

5.5 Thermal Characteristics

THERMAL METRIC(1)		TCAN6062V-Q1		UNIT
		D (SOIC)	DRB (VSON)	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	109		°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	46.4		°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	56.5		°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.8		°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55.6		°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a		°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Supply Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current SIC mode	Dominant	TXD = 0 V, STB = 0 V R_L = 60 Ω, C_L = open		57	75	mA
		Dominant	TXD = 0 V, STB = 0 V R_L = 50 Ω, C_L = open		61	80	mA
		Recessive	TXD = V_{IO}, STB = 0 V R_L = 50 Ω, C_L = open		13	18	mA
		Dominant with bus fault	TXD = 0 V, STB = 0 V CANH = CANL = ±25 V R_L = open, C_L = open			135	mA
I_{CC}	Supply current Fast TX mode	Level_0 or Level_1	TXD = PWM symbol, STB = 0 V, R_L = 45 Ω		45	60	mA
			TXD = PWM symbol, STB = 0 V, R_L = 50 Ω		45	60	mA
I_{CC}	Supply current Fast RX mode	Fast-RX Mode	TXD = PWM symbol, STB = 0 V, C_{RXD} = 15 pF		12	19	mA
I_{CC}	Supply current standby mode (devices with V_{IO})		TXD = STB = V_{IO}, R_L = 50 Ω, C_L = open, Tj <= 85 °C			1	µA
			TXD = STB = V_{IO}, R_L = 50 Ω, C_L = open, Tj <= 125 °C		0.2	2	
			TXD = STB = V_{IO}, R_L = 50 Ω, C_L = open, Tj <= 150 °C			5	
I_{CC}	Supply current standby mode (devices without V_{IO})		TXD = STB = V_{CC}, R_L = 50 Ω, C_L = open, Tj <= 85 °C			13.5	µA
			TXD = STB = V_{CC}, R_L = 50 Ω, C_L = open, Tj <= 125 °C			15	
			TXD = STB = V_{CC}, R_L = 50 Ω, C_L = open, Tj <= 150 °C			16	
I_{IO}	I/O supply current SIC mode Devices with V_{IO}	Dominant	TXD = 0 V, STB = 0 V R_L = 50 Ω, C_L = open RXD floating		125	170	µA
		Recessive	TXD = V_{IO}, STB = 0 V R_L = 50 Ω, C_L = open RXD floating		25	80	µA

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IO}	I/O supply current standby mode Devices with V_{IO}	TXD = V_{IO}, STB = V_{IO} R_L = 50 Ω, C_L = open RXD floating, Tj <= 85 °C			13.5	µA
		TXD = V_{IO}, STB = V_{IO} R_L = 50 Ω, C_L = open RXD floating, Tj <= 125 °C		8.5	15	
		TXD = V_{IO}, STB = V_{IO} R_L = 50 Ω, C_L = open RXD floating, Tj <= 150 °C			16	
$UV_{CC(R)}$	Undervoltage detection V_{CC} rising	Ramp up		4.2	4.4	V
$UV_{CC(F)}$	Undervoltage detection on V_{CC} falling	Ramp down	3.5	4		V
$UV_{VCC(HYS)}$	Hysteresis voltage for V_{CC} undervoltage lockout			200		mV
$UV_{IO(R)}$	Undervoltage detection V_{IO} rising (Devices with V_{IO})	Ramp up		1.6	1.65	V
$UV_{IO(F)}$	Undervoltage detection on V_{IO} falling (Devices with V_{IO})	Ramp down	1.4	1.5		V
$UV_{VIO(HYS)}$	Hysteresis voltage for V_{IO} undervoltage lockout			45		mV

5.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 3.3 V, T_J = 27°C, R_L = 60Ω, C_L = 100 pF, C_{L_RXD} = 15 pF TXD input = 250 kHz 50% duty cycle square wave: Device in SIC mode		TBD		mW
		V_{CC} = 5.5 V, V_{IO} = 5.5 V, T_J = 150°C, R_L = 50Ω, C_L = 100 pF, C_{L_RXD} = 15 pF TXD input = 2.5 MHz 50% duty cycle square wave: Device in SIC mode		TBD		mW
		V_{CC} = 5 V, V_{IO} = 3.3 V, T_J = 27°C, R_L = 50Ω, C_L = 25 pF, C_{L_RXD} = 15 pF TXD input =10 Mbps Logical_0 PWM symbol pulse: Device in Fast TX mode		TBD		mW
		V_{CC} = 5.5 V, V_{IO} = 5.5 V, T_J = 150°C, R_L = 45Ω, C_L = 25 pF, C_{L_RXD} = 15 pF TXD input =20 Mbps Logical_0 PWM symbol pulse: Device in Fast TX mode		TBD		mW
T_{TSD}	Thermal shutdown temperature			192		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			10		

5.8 Electrical Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver - SIC mode							
$V_{CANH(D)}$	Dominant output voltage SIC mode	CANH	V_{CC} = 4.5 V to 5.5 V, TXD = 0 V, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_L = open	2.75	3.5	4.5	V
$V_{CANL(D)}$		CANL		0.5	1.3	2.25	V
$V_{CANH(D)}$	Dominant output voltage SIC mode	CANH	V_{CC} = 4.75 V to 5.25 V, TXD = 0 V, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_L = open	3	3.5	4.26	V
$V_{CANL(D)}$		CANL		0.75	1.3	2.01	V
$V_{CANH(R)}$, $V_{CANL(R)}$	Recessive output voltage SIC mode	CANH, CANL w.r.t GND	V_{CC} = 4.5 V to 5.5 V, TXD = V_{IO}, STB = 0 V R_L = open (no load), C_L = open	2	2.5	3	V
$V_{CANH(R)}$, $V_{CANL(R)}$	Recessive output voltage normal mode	CANH, CANL w.r.t GND	V_{CC} = 4.75 V to 5.25 V, TXD = V_{IO}, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω , C_L = 4.7 nF	2.256	2.5	2.756	V

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parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DIFF(D)}$	Differential output voltage SIC mode Dominant	CANH - CANL	TXD = 0 V, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_L = open	1.5		3	V
			TXD = 0 V, STB = 0 V 45 Ω ≤ R_L ≤ 70 Ω, C_L = open	1.5		3.3	V
			TXD = 0 V, STB = 0 V R_L = 2240 Ω, C_L = open	1.5		5	V
$V_{DIFF(R)}$	Differential output voltage SIC mode: Recessive	CANH - CANL	TXD = V_{IO}, STB = 0 V R_L = open, C_L = open	–50		50	mV
			TXD = V_{IO}, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_{SPLIT} = 4.7 nF, C_L = open	–50		50	mV
V_{SYM}	Driver symmetry in SIC mode ($V_{O(CANH)}$ + $V_{O(CANL)}$)/($V_{CANH(R)}$ + $V_{CANL(R)}$)		TXD toggling at 250 kHz, 1 MHz, 2.5 MHz, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_{SPLIT} = 4.7 nF, C_L = open	0.95		1.05	V/V
$R_{ID(DOM)}$	Differential input resistance in SIC dominant phase		TXD= 0 V, STB = 0 V		40		ohm
$R_{SE\_SIC\_ACT\_REC}$	Single ended resistance CANH/CANL in active recessive phase		2 V ≤ $V_{CANH/L}$ ≤ V_{CC} - 2 V	37.5	50	66.5	Ω
$R_{DIFF\_SIC\_ACT\_REC}$	Differential input resistance in active recessive phase		2 V ≤ $V_{CANH/L}$ ≤ V_{CC} - 2 V	75	100	133	Ω
$V_{CANH(INACT)}$	Bus output voltage standby mode	CANH	TXD = STB = V_{IO} R_L = open, C_L = open	-0.1		0.1	V
$V_{CANL(INACT)}$		CANL		-0.1		0.1	V
$V_{DIFF(INACT)}$		CANH - CANL		-0.2		0.2	V
I_{OS}	Short-circuit bus output current,TXD is dominant or recessive or toggling, SIC mode		$V_{(CANH)}$ = -15 V to 40 V, CANL = open, TXD = 0 V or V_{IO} or 250 khz, 2.5 Mhz square wave	–115		115	mA
			$V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open, TXD = 0 V or V_{IO} or 250 khz, 2.5 Mhz square wave	–115		115	mA
Driver - FAST TX mode							
V_{CAN_H0}	Single ended voltage on CANH	Level_0	TXD = Level_0 PWM symbol, STB = 0 V 45 Ω ≤ R_L ≤ 60 Ω, C_L = open	2.55		3.51	V
V_{CAN_H1}		Level_1	TXD = Level_1 PWM symbol, STB = 0 V 45 Ω ≤ R_L ≤ 60 Ω, C_L = open	1.5		2.46	V
V_{CAN_L0}	Single ended voltage on CANL	Level_0	TXD = Level_0 PWM symbol, STB = 0 V 45 Ω ≤ R_L ≤ 60 Ω, C_L = open	1.5		2.46	V
V_{CAN_L1}		Level_1	TXD = Level_1 PWM symbol, STB = 0 V 45 Ω ≤ R_L ≤ 60 Ω, C_L = open	2.55		3.51	V
V_{DIFF0}	Differential output voltage Fast TX mode	Level_0	TXD = Level_0 PWM symbol, STB = 0 V 45 Ω ≤ R_L ≤ 60 Ω, C_L = open	0.6		1.5	V
V_{DIFF1}		Level_1	TXD = Level_1 PWM symbol, STB = 0 V 45 Ω ≤ R_L ≤ 60 Ω, C_L = open	-1.5		-0.6	V
V_{SYM}	Driver symmetry in Fast TX mode ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		TXD = PWM symbol of 5 Mbps, 10 Mbps, 20 Mbps, STB = 0 V 45 Ω ≤ R_L ≤ 60 Ω, C_{SPLIT} = 4.7 nF, C_L = open	0.95		1.05	V/V
I_{OS}	Short-circuit bus output current,TXD is Level_0 PWM or Level_1 PWM, Fast TX mode		$V_{(CANH)}$ = -15 V to 40 V, CANL = open, TXD =Level_0 PWM or Level_1 PWM 5 Mbps, 10Mbps, 20Mbps	–115		115	mA
			$V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open, TXD =Level_0 PWM or Level_1 PWM 5 Mbps, 10Mbps, 20Mbps	–115		115	mA
Receiver - SIC and Standby mode							
V_{IT}	Input threshold voltage SIC mode		-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, R_L = Open, C_L = open	500		900	mV
$V_{IT(STB)}$	Input threshold voltage standby mode		-12 V ≤ V_{CM} ≤ 12 V, STB= V_{IO}, R_L = Open, C_L = open	400		1150	mV

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parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DIFF\_RX(D)}$	SIC mode dominant state differential input voltage range	-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, R_L = Open, C_L = open	0.9		9	V
$V_{DIFF\_RX(R)}$	SIC mode recessive state differential input voltage range	-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, R_L = Open, C_L = open	-4		0.5	V
$V_{DIFF\_RX(D\_INACT)}$	Standby mode dominant state differential input voltage range	STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V, R_L = Open, C_L = open	1.15		9	V
$V_{DIFF\_RX(R\_INACT)}$	Standby mode recessive state differential input voltage range	STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V, R_L = Open, C_L = open	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold SIC mode	-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V,		100		mV
V_{CM}	Common mode range SIC, Fast and standby modes		–12		12	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			10	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO}			50	pF
C_{ID}	Differential input capacitance	TXD = V_{IO}			25	pF
$R_{DIFF\_PAS\_REC}$	Differential input resistance in passive recessive phase	TXD = V_{IO}, STB = 0 V -12 V ≤ V_{CM} ≤ 12 V, Delta V/Delta I	12		100	kΩ
$R_{SE\_PAS\_REC}$	Single ended input resistance in passive recessive phase (CANH or CANL)		6		50	kΩ
$R_{IN(M)}$	Input resistance matching 2* [$R_{IN(CANH)}$ - $R_{IN(CANL)}$] / [$R_{IN(CANH)}$ + $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V	–3		3	%
Receiver - FAST RX mode						
$V_{IT(FAST)}$	Input threshold voltage Fast RX	-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, R_L = Open, C_L = open	-100		100	mV
$V_{ID(Level\_0)}$	Fast mode Level_0 state differential input voltage range	-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, R_L = Open, C_L = open	0.1		9	V
$V_{ID(Level\_1)}$	Fast mode Level_1 state differential input voltage range	-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, R_L = Open, C_L = open	-9		-0.1	V
OOB Comparator						
$V_{IT(OOB)}$	Input threshold voltage OOB comparator SIC mode	-12 V ≤ V_{CM} ≤ 12 V, STB= V_{IO}	-450		-250	mV
$V_{ID\ (OOB\_Low)}$	Low state differential input voltage range: OOB comparator SIC mode	-12 V ≤ V_{CM} ≤ 12 V, STB= V_{IO}	-8		-0.45	V
$V_{ID\ (OOB\_High)}$	High state differential input voltage range: OOB comparator SIC mode	-12 V ≤ V_{CM} ≤ 12 V, STB= V_{IO}	-0.25		8	V
TXD Terminal (CAN Transmit Data Input)						
$V_{(TXD)THRESH}$	TXD input threshold voltage	Devices with V_{IO}	0.95*(V_{IO}/2)		1.05*(V_{IO}/2)	V
$V_{(TXD)LOW}$	TXD input low voltage range	Devices with V_{IO}	0		0.95*(V_{IO}/2)	V
$V_{(TXD)HIGH}$	TXD input high voltage range	Devices with V_{IO}	1.05*(V_{IO}/2)		V_{IO}	V
$R_{(TXD)PU}$	Pull-up resistance on TXD input		20		80	kΩ
$R_{(TXD)PD}$	Pull-down resistance on TXD input		20		80	kΩ
$m_{R(TXD)}$	Pull-up and pull-down impedance matching	2 × ($R_{(TXD)PU}$ − $R_{(TXD)PD}$) / ($R_{(TXD)PU}$ + $R_{(TXD)PD}$)	-0.05		0.05	Ohm/ Ohm
I_{IH}	High-level input leakage current	TXD = V_{IO} = 5.5 V	-1		1	µA
I_{IL}	Low-level input leakage current	TXD = 0 V, V_{IO} = 5.5 V	-1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1		1	µA
C_I	Input capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t) + 2.5 V		5		pF
RXD Terminal (CAN Receive Data Output)						

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parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_O = –1.5 mA, Devices with V_{IO}	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	Devices with V_{IO} I_O = 1.5 mA, Devices with V_{IO}			0.2 V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1		1	µA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = STB = 5.5 V	–2		2	µA
I_{IL}	Low-level input leakage current	V_{CC} = V_{IO} = 5.5 V, STB = 0 V	–20		–2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5V, V_{CC}= V_{IO} = 0 V	–1		1	µA

5.9 Switching Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{FastTOSIC}$	PWM detection time (Detection time to switch between FAST RX mode / FAST TX mode and SIC mode)	Measured between 50% of TXD edge to next 50% edge (rising to rising or falling to falling)	210		245	ns
$t_{SymbolNom}$	PWM symbol acceptance length		45		205	ns
t_{Select}	Mode pre-selection time		500		980	ns
t_{Decode}	PWM detection resolution				5	ns
$t_{Logical\_0\_Tx}$	PWM ratio detected as logical_0 FAST TX		t_{Decode}		0.5*$t_{SymbolNom}$ - t_{Decode}	ns
$t_{Logical\_1\_Tx}$	PWM ratio detected as logical_1 FAST TX		0.5*$t_{SymbolNom}$ + t_{Decode}		$t_{SymbolNom}$ - t_{Decode}	ns
$t_{Logical\_Rx}$	PWM ratio detected FAST RX		t_{Decode}		$t_{SymbolNom}$ - t_{Decode}	ns
$t_{(LOOP1)}$	SIC mode: Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	, normal mode, V_{IO} = 4.5 V to 5.5 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		95	155	ns
		, normal mode, V_{IO} = 3 V to 3.6 V, 45 Ω ≤ R_L ≤ 65 Ω C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	165	ns
		, normal mode, V_{IO} = 2.25 V to 2.75 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		105	175	ns
		, normal mode, V_{IO} = 1.71 V to 1.89 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		120	190	ns
$t_{(LOOP2)}$	SIC mode: Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	, normal mode, V_{IO} = 4.5 V to 5.5 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		110	165	ns
		, normal mode, V_{IO} = 3 V to 3.6 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		115	175	ns
		, normal mode, V_{IO} = 2.25 V to 2.75 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		120	185	ns
		, normal mode, V_{IO} = 1.71 V to 1.89 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		135	190	ns
t_{MODE}	Mode change time, from SIC to standby or from standby to SIC				30	µs

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parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{Prop(BusDom-BusLevel0)}$	Propagation delay from mode change to bus level_0 (SIC mode to Fast TX mode)	45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
$t_{Prop(BusLevel0-Rec)}$	Propagation delay from mode change to bus recessive in FAST TX and FAST RX Mode (Fast mode to SIC mode)	45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	325	ns
$t_{\Delta Bit(Bus)ADS/DAS}$	Transmitter propagation delay symmetry ADS/DAS	$t_{\Delta Bit(Bus)ADS/DAS}$ = tProp(TXD-BusDom) – tProp(TXD-BusLevel0) 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF	-30		30	ns
$t_{\Delta Bit(RXD)ADS/DAS}$	Receiver propagation delay symmetry ADS/DAS	$t_{\Delta Bit(RXD)ADS/DAS}$ = tProp(BusDom-RXD) – tProp(BusLevel0-RXD) 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF	-20		20	ns
t_{FILTER}	Filter time for a valid wake-up pattern		0.5		0.95	µs
t_{WAKE}	Bus wake-up timeout value		0.8		6	ms
t_{Flag}	Wake-up pattern signaling				250	µs
Driver Switching - SIC mode						
$t_{prop(TxD-busrec)}$	Propagation delay time, low-to-high TXD edge to driver recessive (dominant to recessive)	STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, V_{IO} = 4.5 V to 5.5 V		45	75	ns
		STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, V_{IO} = 3 V to 3.6 V		45	75	ns
		STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, V_{IO} = 2.25 V to 2.75 V		45	75	ns
		STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, V_{IO} = 1.71 V to 1.89 V		45	80	ns
$t_{prop(TxD-busdom)}$	Propagation delay time, high-to-low TXD edge to driver dominant (recessive to dominant)	STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, V_{IO} = 4.5 V to 5.5 V		45	75	ns
		STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, V_{IO} = 3 V to 3.6 V		45	75	ns
		STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, V_{IO} = 2.25 V to 2.75 V		45	75	ns
		STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, V_{IO} = 1.71 V to 1.89 V		45	80	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{prop(TxD-busrec)} - t_{prop(TxD-busdom)} \rvert$)	STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF		3.5	10	ns
t_R	Differential output signal rise time	STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF		22	30	ns
t_F	Differential output signal fall time	STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF		22	30	ns
t_{DOM}	Transmit dominant timeout (SIC mode)	45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, STB = 0 V	0.8		6.0	ms
Receiver Switching - SIC mode						
$t_{prop(busrec-RXD)}$	Propagation delay time, bus recessive input to RXD high output (dominant to recessive)	STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 4.5 V to 5.5 V		67	90	ns
		STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 3 V to 3.6 V		65	95	ns
		STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 2.25 V to 2.75 V		70	105	ns
		STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 1.71 V to 1.89 V		80	110	ns
$t_{prop(busdom-RXD)}$	Propagation delay time, bus dominant input to RXD low output (recessive to dominant)	STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 4.5 V to 5.5 V		56	80	ns
		STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 3 V to 3.6 V		61	90	ns
		STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 2.25 V to 2.75 V		65	100	ns
		STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 1.71 V to 1.89 V		75	110	ns

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parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	RXD output signal rise time	STB = 0 V, $C_{L(RXD)}$ = 15 pF		7	20	ns
t_F	RXD output signal fall time			9	25	ns
$t_{OOB\_LOW\ (RXD)}$	RXD low pulse width during fast data traffic, at the bit rate 10 Mbit/s	$t_{SymbolNom}$ = 100 ns	30			ns
	RXD low pulse width during fast data traffic, at the bit rate 20 Mbit/s	$t_{SymbolNom}$ = 50 ns	15			ns
Driver Switching- FAST TX mode						
t_{SIC_data}	Signal improvement time in FAST TX Mode	45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	775	ns
$t_{Prop(TXD-BusLevel0)}$	Propagation delay from TXD logical 0 to bus level_0	V_{IO} = 4.5 V to 5.5 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
		V_{IO} = 3 V to 3.6 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
		V_{IO} = 2.25 V to 2.75 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
		V_{IO} = 1.71 V to 1.89 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
$t_{Prop(TXD-BusLevel1)}$	Propagation delay from TXD logical 1 to bus level_1	V_{IO} = 4.5 V to 5.5 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
		V_{IO} = 3 V to 3.6 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
		V_{IO} = 2.25 V to 2.75 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
		V_{IO} = 1.71 V to 1.89 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
$t_{Busfall}$	Fall time V_{Diff}	45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF	6	12	20	ns
$t_{Busrise}$	Rise time V_{Diff}	45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF	6	12	20	ns
$t_{\Delta Bit(Bus)Level1}$	Transmitted level_1 bit width variation in FAST TX Mode	Bus level_1 bit length variation relative to TXD tBit_data length $t_{\Delta Bit(Bus)Level1} = t_{Bit(Bus)\ Level1} - k * t_{Bit\_data}$ 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF	- 5		5	ns
$t_{\Delta Bit(RxD)Logical1}$	Received logical 1 bit width variation in FAST TX Mode	RXD logical 1 bit length variation relative to TXD tBit_data length $t_{\Delta Bit(RxD)\ Logical1} = t_{Bit(RxD)\ Logical1} - k * t_{Bit\_data}$ 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF	- 10		10	ns
Receiver Switching - FAST RX mode						
$t_{SIC\_FAST\_RX\_dis}$	SIC disable time after Fast RX detection	V_{IO} = 1.7 to 5.5 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
$t_{Prop(BusLevel0-RXD)}$	Propagation delay from bus level_0 to RXD logical 0	V_{IO} = 4.5 V to 5.5 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
		V_{IO} = 3 V to 3.6 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	90	ns
		V_{IO} = 2.25 V to 2.75 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	100	ns
		V_{IO} = 1.71 V to 1.89 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	110	ns

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parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{Prop(BusLevel1-RXD)}$	Propagation delay from bus level_1 to RXD logical 1	V_{IO} = 4.5 V to 5.5 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	80	ns
		V_{IO} = 3 V to 3.6 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	90	ns
		V_{IO} = 2.25 V to 2.75 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	100	ns
		V_{IO} = 1.71 V to 1.89 V, 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF		TBD	110	ns
$t_{\Delta REC\_Logical1}$	Logical 1 receiver timing symmetry in FAST RX Mode	RXD logical 1 bit length variation relative to bus level_1 bit length $t_{\Delta REC\_Logical1}$ = $t_{Bit(RxD)\ Logical1}$ - $t_{Bit(\ Bus)\ Level1}$ 45 Ω ≤ R_L ≤ 60 Ω, C_L = 25 pF, C_{SPLIT} = 0, $C_{L(RXD)}$ = 15 pF	-5		5	ns
Signal Improvement Timing Characteristics						
$t_{PAS\_REC\_START}$	Start time of passive recessive phase	Time duration from TXD rising 50% edge (<5ns slope) to start of passive recessive phase		TBD	530	ns
$t_{ACT\_REC\_START}$	Start time of active signal improvement phase	Time duration from TXD rising 50% edge (<5ns slope) to start of passive recessive phase		TBD	120	ns
$t_{ACT\_REC\_END}$	End time of active signal improvement phase		355	TBD		ns
$t_{\Delta\ Bit(Bus)}$	Transmitted bit width variation	$t_{\Delta\ Bit(Bus)}$ = $t_{Bit(Bus)}$ - $t_{Bit(TxD)}$ STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)	–10		10	ns
$t_{\Delta\ BIT(RxD)}$	Received bit width variation	$t_{\Delta\ BIT(RxD)}$ = $t_{Bit(RxD)}$ - $t_{Bit(TxD)}$ STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)	–30		20	ns
$t_{\Delta\ REC}$	Receiver timing symmetry	$t_{\Delta\ REC}$ = $t_{Bit(RxD)}$ - $t_{Bit(Bus)}$ STB = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF (≤ ±1%)	–20		15	ns

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6 Parameter Measurement Information

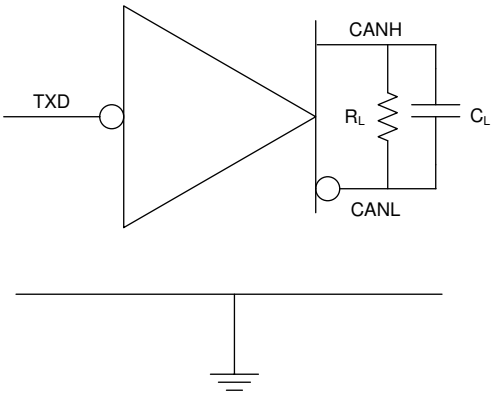


Figure 6-1. I_{CC} Test Circuit

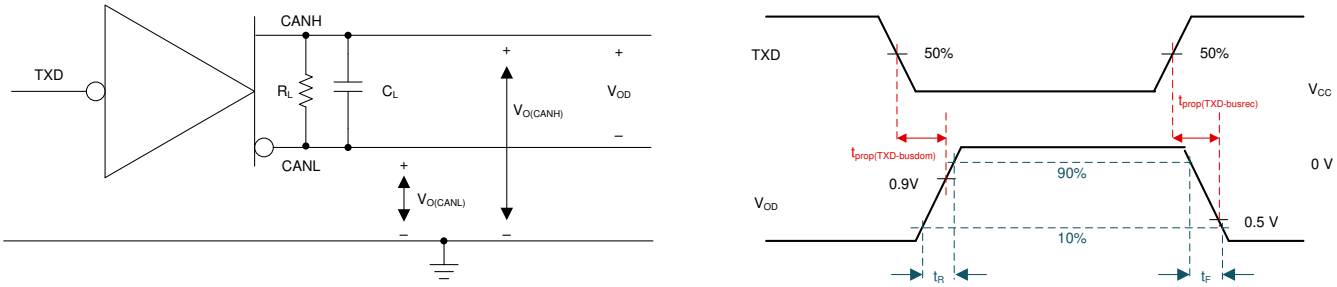


Figure 6-2. Driver Test Circuit and Measurement

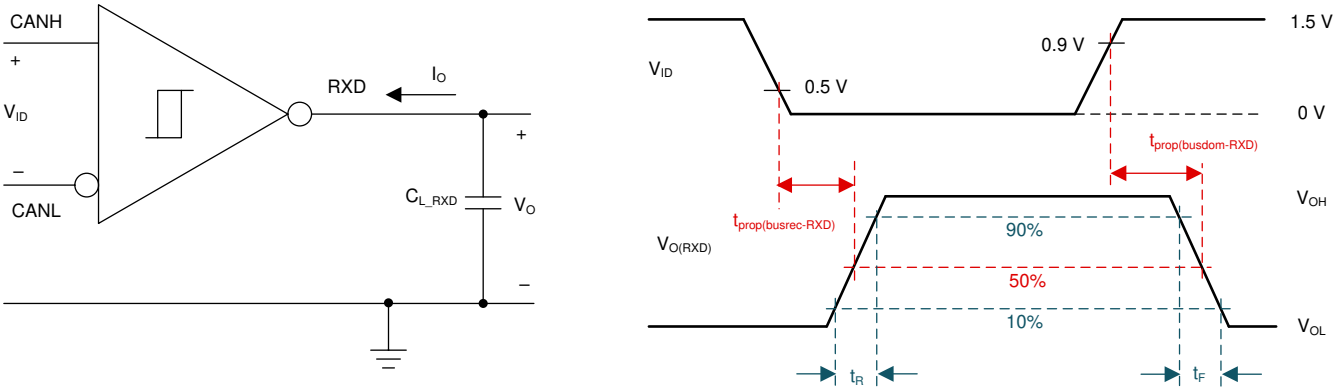
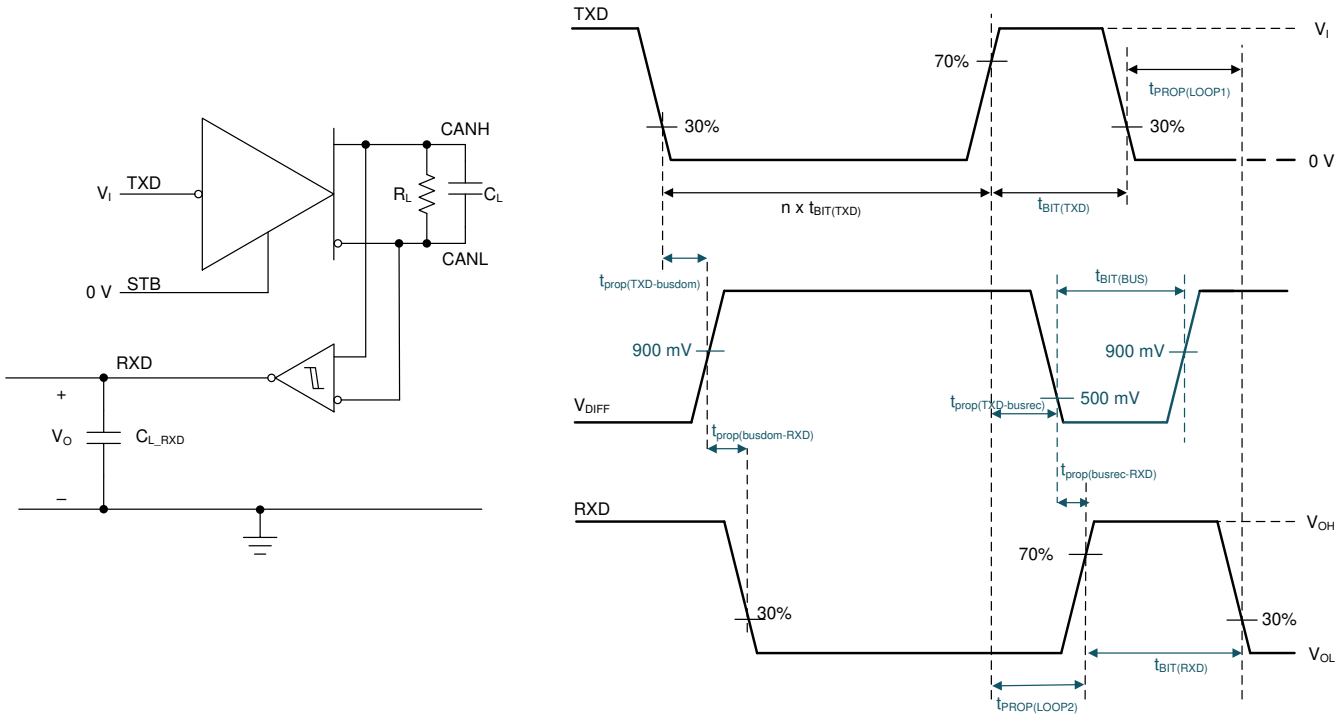


Figure 6-3. Receiver Test Circuit and Measurement



n = 1 to 5;
TXD rise/fall time < 10 ns

Figure 6-4. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

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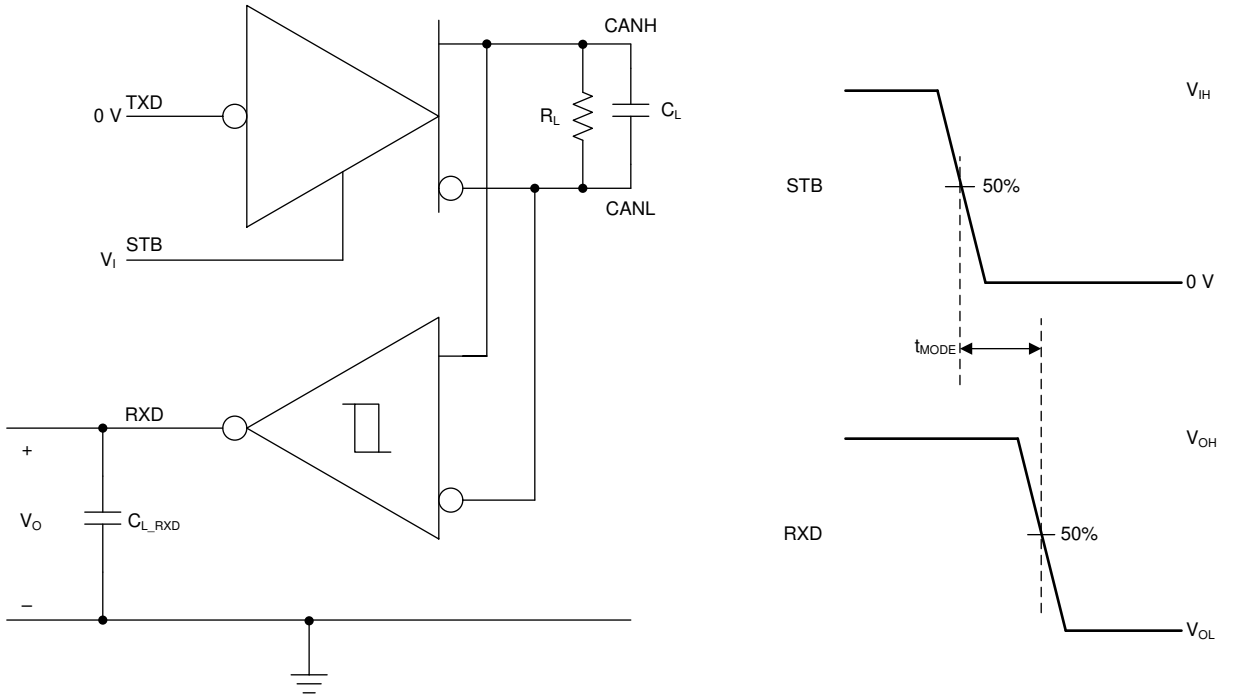

Figure 6-5. t_{MODE} Test Circuit and Measurement

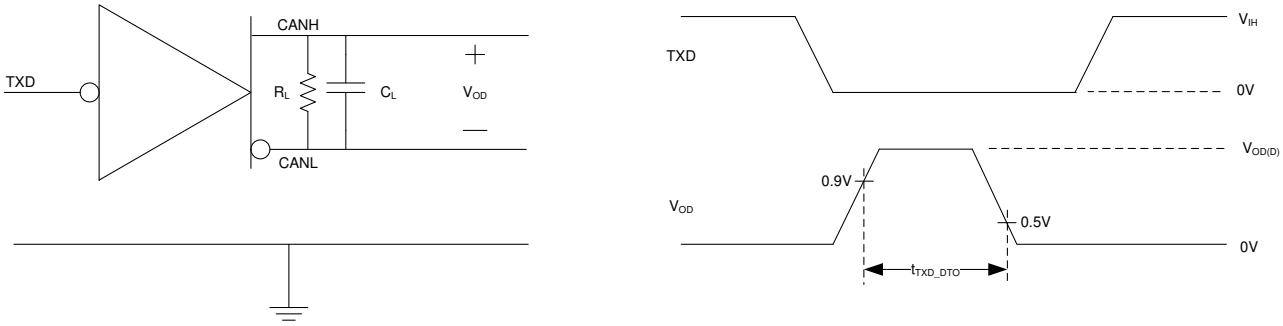

Figure 6-6. TXD Dominant Timeout Test Circuit and Measurement

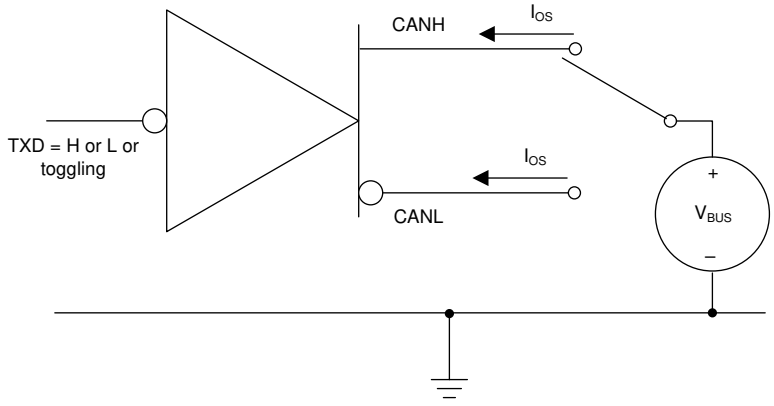

Figure 6-7. Driver Short-Circuit Current Test and Measurement

7 Detailed Description

7.1 Overview

The TCAN6062(V)-Q1 devices meet or exceed the specifications of the ISO 11898-2:2024 high speed CAN (Controller Area Network) physical layer standard including Annex A for SIC mode and FAST mode, allowing for CAN XL operation up to 20Mbps. The devices are data rate agnostic making them backward compatible for supporting classic CAN applications while also supporting CAN FD networks up to 8Mbps. These devices have standby mode support which puts the transceiver in ultra-low current consumption mode. Upon receiving valid wake-up pattern on CAN bus, device signals to the microcontroller through the RXD pin. The MCU can then put the device into normal mode using the STB pin.

The TCAN6062V-Q1 has two separate supply rails, V_{CC} bus-side supply and V_{IO} logic supply for logic-level translation for interfacing directly to 1.8V, 2.5V, 3.3V, or 5V controllers.

7.1.1 Signal Improvement Capability

Signal Improvement Capability (SIC) is an additional feature added to the transceiver that enhances the maximum data rate achievable in complex star topologies by minimizing signal ringing. Signal ringing is the result of reflections caused by impedance mismatch at various points in a CAN network due to the nodes that act as stubs.

An example of a complex network is shown in Figure 7-1.

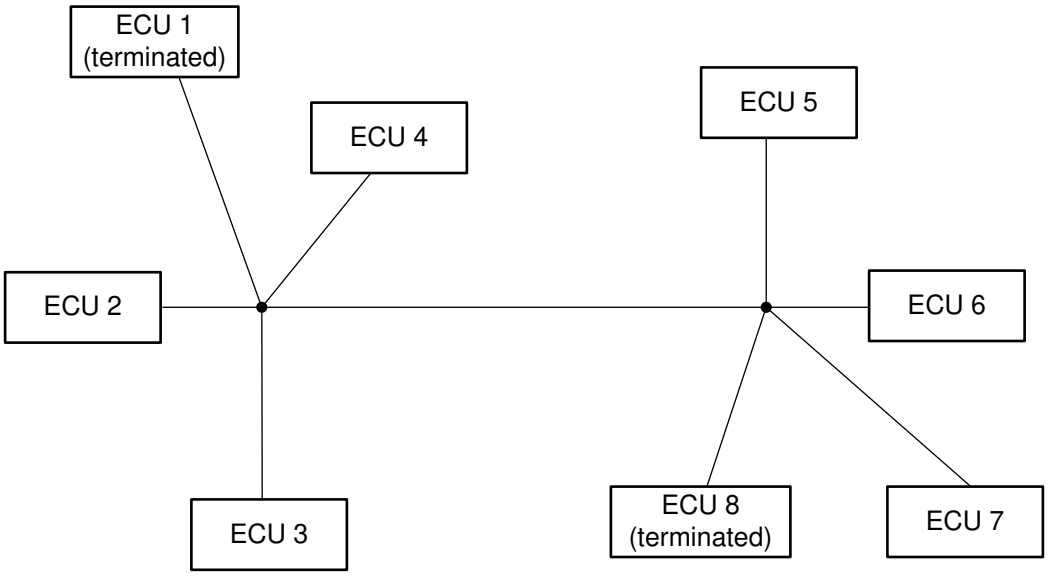

Figure 7-1. CAN Network: Star topology

The recessive-to-dominant signal edge is usually clean and is strongly driven by the transmitter. Transmitter output impedance of CAN transceiver is approximately 50Ω and matches to the network characteristic impedance. For a regular CAN FD transceiver, dominant-to-recessive edge is when the driver output impedance goes to approximately 60kΩ and signal reflected back experiences impedance mismatch which causes ringing. TCAN6062-Q1 resolves this issue by using TX-based SIC when in SIC mode. The TCAN6062-Q1 continues to drive the bus recessive until $t_{ACT\_REC\_end}$, so the reflections die down and the recessive bit is clean at sampling point. In the active recessive phase, transmitter output impedance is low (approximately 100Ω). After this phase is over and device goes to passive recessive phase, driver output impedance goes to high-Z. This phenomenon is explained with Figure 7-2.

For more information on the TI signal improvement technology and the compares with similar devices in market, please refer to the white paper *How Signal Improvement Capability Unlocks the Real Potential of CAN-FD Transceivers*.

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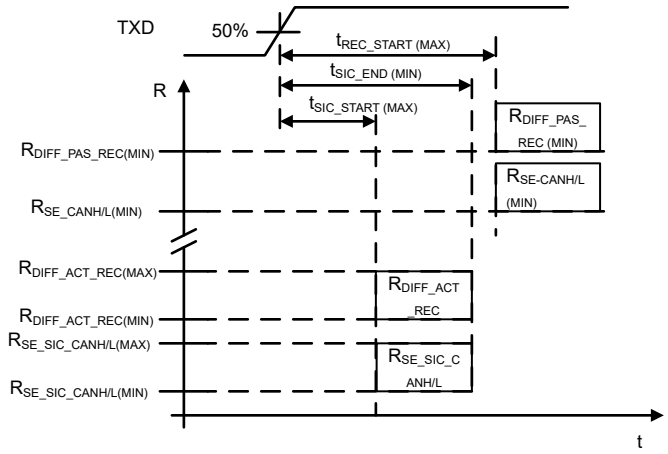


Figure 7-2. TX based SIC

7.1.2 CAN XL and FAST Mode

CAN XL introduces an additional drive state to the CAN transceiver for use during the data phase of a CAN frame. After the arbitration phase has concluded and a single node has won priority of the CAN bus there is no longer risk of multiple devices trying to simultaneously drive contending drive states. CAN XL takes advantage of this by switching the driver to a push-pull driver architecture during the data phase of the CAN frame. The FAST TX mode driver has two strongly driven drive states as opposed to only the single strong dominant drive state of the SIC mode driver. This allows much higher data rates to be used during the data phase compared to typical CAN HS or CAN FD.

For the transceiver to change drive states into FAST TX mode a PWM signal is driven on the TXD pin by the CAN XL controller. Depending on the duty cycle of this PWM signal the driver outputs either a Level_0 or Level_1 state which correspond to logic 0 and logic 1 states respectively. The timing of the TXD signal required to change driver modes is detailed further in Section 7.3.3.3.

The CAN XL FAST mode uses differential logic thresholds that are different than those used by CAN FD and CAN SIC transceivers. This means that an additional FAST mode receiver is needed, so that FAST TX mode drive states can be decoded. For the device receiver to switch between SIC mode and FAST RX mode a PWM signal is driven on the TXD by the receiving CAN XL controller. This is uniquely different from standard CAN which has the TXD signal of all receiving nodes remain high during the data phase of a received frame. The timing of the TXD signal required to change receiver modes is detailed further in Section 7.3.3.2.

An out of bounds (OOB) comparator is used to indicate when a CAN XL drive state is detected on the CAN bus while the device is in SIC mode and FAST RX mode is not active. See Section 7.3.4 for details.

7.2 Functional Block Diagram

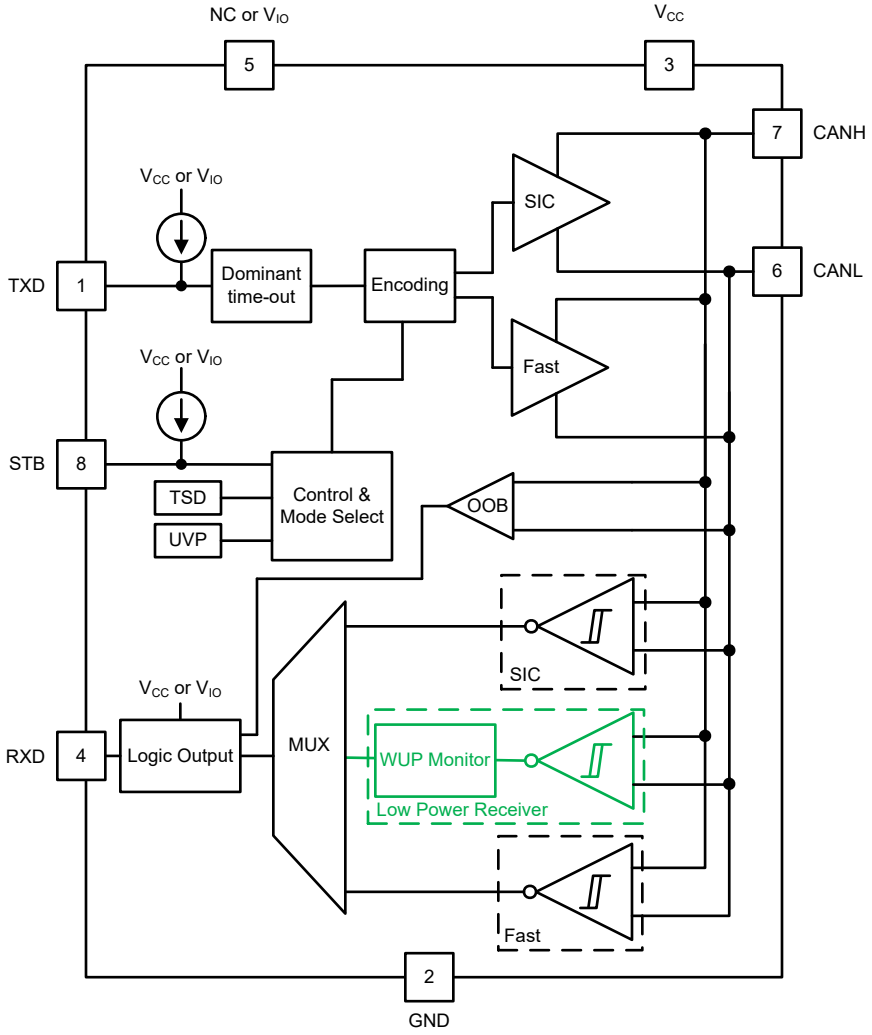


Figure 7-3. Block Diagram

7.3 Feature Description

7.3.1 Pin Description

7.3.1.1 TXD

The TXD input is a logic-level signal from a CAN controller to the transceiver. It is referenced to V_{IO} (or V_{CC} for devices without V_{IO}). In SIC mode, the logic level input of the TXD pin controls the state of the SIC transmitter.

The TXD input is also used to control the operation of the FAST TX transmitter and FAST RX receiver. Applying a PWM signal to this input (as described in Section 7.3.3) activates the FAST RX receiver and can also be used to encode transmitted CAN XL data using the FAST TX transmitter.

7.3.1.2 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

7.3.1.3 V_{CC}

V_{CC} provides the 5V power supply to the CAN transceiver.

7.3.1.4 RXD

The RXD output is a logic-level signal from the CAN transceiver to the CAN controller. RXD is referenced to V_{CC} for TCAN6062-Q1 or to V_{IO} for TCAN6062V-Q1. For TCAN6062V-Q1, RXD is only driven once V_{IO} is present.

When a wake event takes place RXD is driven low.

7.3.1.5 V_{IO} (only for TCAN6062V-Q1)

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage; thus, avoiding the requirement for a level shifter. The pin supports voltages from 1.7V to 5.5V providing the widest range of controller support.

7.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

7.3.1.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, the STB pin can be tied directly to GND.

7.3.2 CAN Bus States

The CAN bus has multiple logical states during operation. In SIC mode, the two states are *recessive* and *dominant*. See Figure 7-4. A dominant bus state occurs when the bus is driven differentially with $V_{DIFF} \geq +1.5V$ and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins. A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN6062-Q1 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 7-4 and Figure 7-6.

In FAST mode, the CAN bus has two additional logical states: *level_0* and *level_1*. See Figure 7-5. A level_0 bus state occurs when the bus is driven differentially with $+1.5V \geq V_{DIFF} \geq +0.6V$, corresponding to a logic low on the RXD pin and a low duty cycle on TXD as shown in Figure 7-10. A level_1 bus state occurs when the bus is driven differentially with $-0.6V \geq V_{DIFF} \geq -1.5V$, corresponding to a logic high on the RXD pin and a high duty cycle on RXD as shown in Figure 7-11.

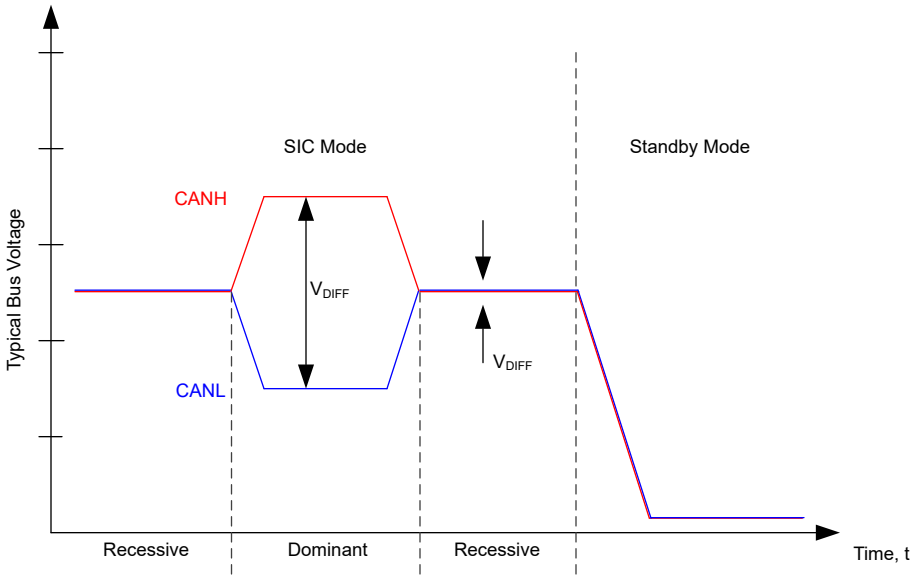


Figure 7-4. Bus States in SIC Mode and Standby Mode

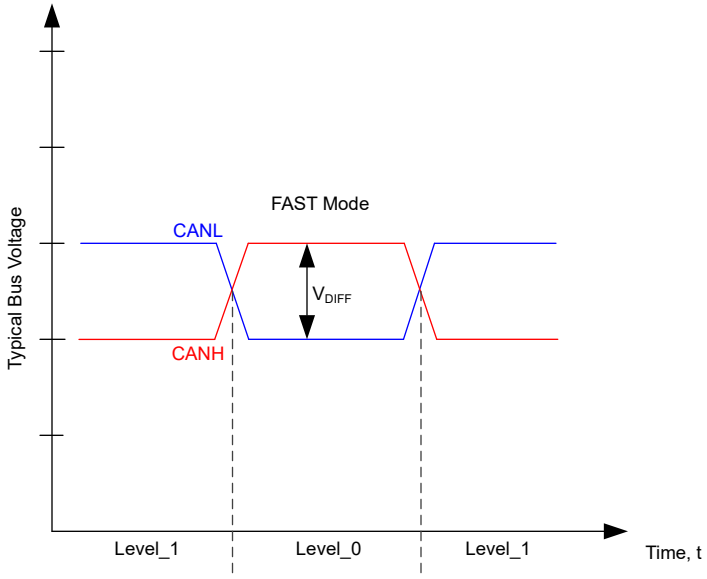
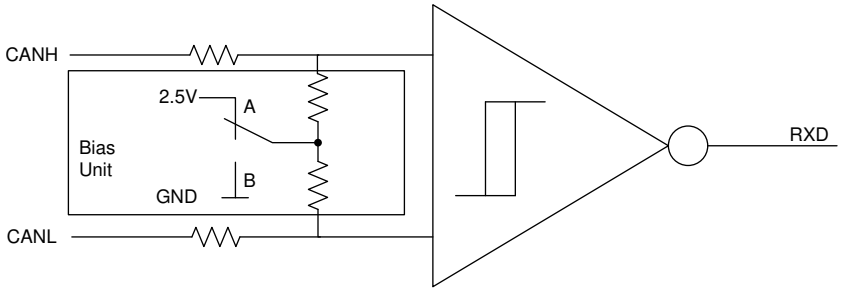


Figure 7-5. Bus States in FAST Mode



A. Normal Mode
B. Standby Mode

Figure 7-6. Simplified Recessive Common Mode Bias Unit and Receiver

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7.3.3 Pulse-Width Modulation (PWM) for FAST Mode Signaling

CAN XL controllers that implement ISO 11898-1:2024 or a similar CAN XL compatible data link layer will implement FAST mode communication using pulse-width modulation (PWM) on the TXD input of the TCAN6062-Q1.

7.3.3.1 PWM Detection and Timing

Two consecutive similar edges on TXD that occur faster than $t_{FastTOSIC}$ determine the PWM signal period time, defined as $t_{SymbolNom}$. The TCAN6062-Q1 determines that the input signal is a valid PWM if $t_{SymbolNom}$ falls within $t_{SymbolNom(min)}$ and $t_{SymbolNom(max)}$ as given in the Switching Characteristics. If this occurs, the device switches from SIC mode into either FAST RX mode or FAST TX mode as described in Section 7.3.3.2 and Section 7.3.3.3 respectively. The device remains in FAST TX or FAST RX mode as long as the device is in Normal mode and the PWM signal period time on TXD remains within $t_{SymbolNom(min)}$ and $t_{SymbolNom(max)}$.

When the device is in SIC mode, the TXD pin is used for pre-selection of FAST RX mode or FAST TX mode.

7.3.3.2 Transition from SIC Mode to FAST RX Mode

When the TXD pin is HIGH for at least t_{SELECT}, FAST RX mode becomes pre-selected. After this pre-selection, two valid consecutive high-to-low falling edges on TXD within $t_{SymbolNom}$ will cause the device to transition to FAST RX mode as shown in Figure 7-7 below.

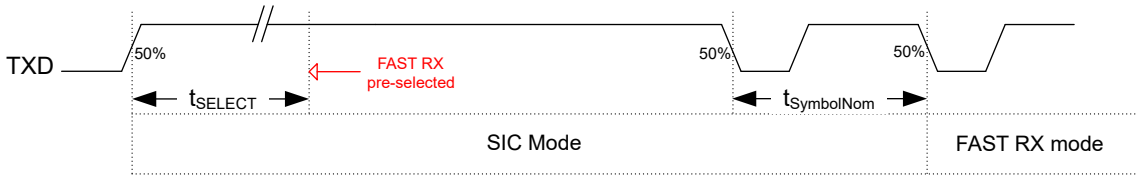

Figure 7-7. FAST RX Mode Selection

In FAST RX mode, the device remains high-impedance to the bus and the FAST receiver decodes the information on the CAN bus using FAST RX thresholds and passes this information to RXD as given in Table 7-6.

7.3.3.3 Transition from SIC Mode to FAST TX Mode

When the TXD pin is LOW for at least t_{SELECT}, FAST TX mode becomes pre-selected. After this pre-selection, two valid consecutive low-to-high rising edges on TXD within $t_{SymbolNom}$ will cause the device to transition to FAST TX mode as shown in Figure 7-8 below. The CAN transmitter will switch from dominant to level_0 within $t_{Prop(BusDom-BusLevel0)}$ after the second valid consecutive low-to-high rising edge on TXD.

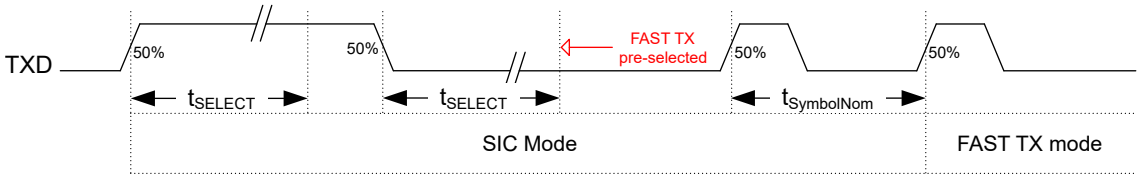

Figure 7-8. FAST TX Mode Selection

In FAST TX mode, both the FAST receiver and FAST transmitter are active. The FAST receiver decodes the information on the CAN bus using FAST RX thresholds and passes this information to RXD. The FAST transmitter decodes the PWM on the TXD pin and drives the corresponding level_0 or level_1 signal onto the CAN bus. See Table 7-5 and Section 7.3.3.4.3.

7.3.3.4 PWM Decoding

The controller's input PWM to the TXD pin defines $t_{SymbolNom}$, which must fall within the limits given in the Switching Characteristics. In FAST RX mode, this is measured based upon consecutive high-to-low falling edges of the TXD signal. In FAST TX mode, this is measured based upon consecutive low-to-high rising edges of the TXD signal.

7.3.3.4.1 PWM Detection Resolution t_{DECODE}

The transceiver's PWM detection resolution is given by t_{Decode}. The minimum separation between consecutive edges in any PWM signal must be greater than t_{Decode} to ensure proper detection by the PWM decoder. Input signal edges that occur within t_{Decode} may be missed.

7.3.3.4.2 PWM Decoding in FAST RX Mode

In FAST RX mode, the PWM decoder recognizes any input PWM. Changing the PWM duty cycle does not alter the behavior of the FAST transmitter and/or receiver as long as $t_{SymbolNom}$ and t_{Decode} requirements continue to be met.

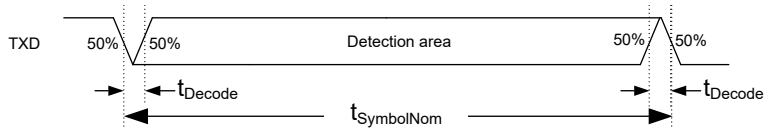

Figure 7-9. PWM Detection on TXD in FAST RX Mode

7.3.3.4.3 PWM Decoding in FAST TX Mode

In FAST TX mode, the duty cycle of the TXD input determines the transmitter's output to the CAN bus. When the input PWM to TXD is low for more than 50% of $t_{SymbolNom}$, corresponding to a PWM duty cycle less than 50%, the FAST transmitter transmits a level_0 output to the CAN bus.

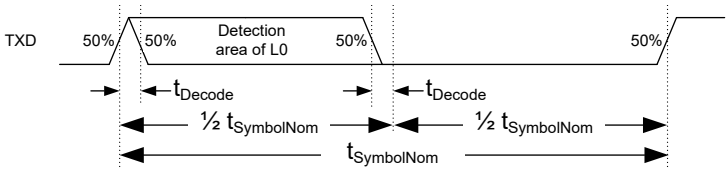

Figure 7-10. Level_0 Detection on TXD in FAST TX Mode

When the input PWM to TXD is high for more than 50% of $t_{SymbolNom}$, corresponding to a PWM duty cycle greater than 50%, the FAST transmitter transmits a level_1 output to the CAN bus.

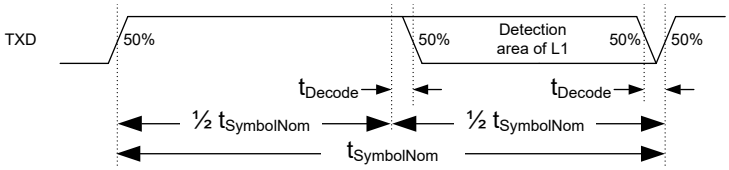

Figure 7-11. Level_1 Detection on TXD in FAST TX Mode

7.3.3.5 Transition from FAST RX/TX Modes to SIC Mode

Halting the PWM input to TXD causes the transceiver to transition back into SIC mode. This occurs once $t_{FastTOSIC}$ expires before a second consecutive high-to-low transition occurs in FAST RX mode, or before a second consecutive low-to-high transition occurs in FAST TX mode.

Receiver thresholds changes from FAST mode thresholds to SIC mode thresholds once $t_{FastTOSIC}$ expires after the last valid TXD edge. When transitioning from FAST TX mode to SIC mode, the transmitter output changes from level_0 to recessive within $t_{Prop(BusLevel0-Rec)}$ after the last valid low-to-high rising edge on TXD.

7.3.4 Out-of-Bounds (OOB) Comparator

In SIC mode, an out-of-bounds (OOB) comparator is active, which monitors CANH and CANL to determine whether level_1 signals occur on the bus inputs. These events are signaled as low-level outputs on RXD, allowing CAN controllers to detect when unexpected FAST mode CAN XL activity is occurring on the bus while the node transceiver is still in SIC mode.

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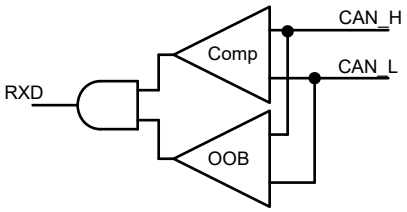

Figure 7-12. OOB Comparator Output to RXD

The OOB comparator serves as a protection against false idle events. The SIC receiver thresholds are above the output requirements for level_0 and level_1 signals for transmitters, causing SIC receivers to detect all of this activity as recessive. This can cause situations where the controller is unaware of CAN XL FAST mode activity on the CAN bus if the transceiver is still in SIC mode. The OOB comparator initiates activity on RXD pin, allowing the CAN XL controller to detect this activity.

Signals detected by the OOB comparator are considered invalid signals for CAN FD and other non-XL communication schemes, so this feature does not pose a compatibility risk when the TCAN6062-Q1 is used for legacy CAN, CAN FD, and CAN SIC applications where FAST mode is not implemented.

7.3.5 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin; thus, clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1 .

$$\text{Minimum Data Rate} = \frac{11 \text{ bits}}{t_{TXD\_DTO}} = \frac{11\ bits}{0.8\ ms} = 13.8 \text{ kbps} \quad (1)$$

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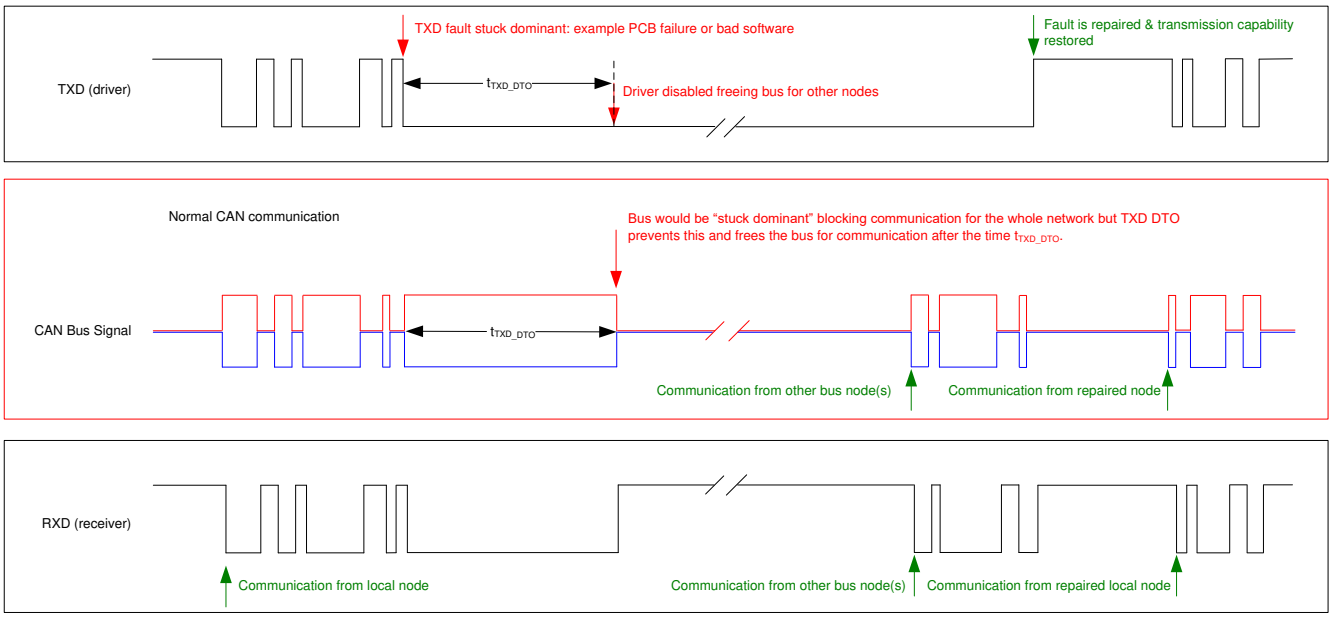

Figure 7-13. Example Timing Diagram for TXD Dominant Timeout

7.3.6 CAN Bus short-circuit current limiting

The TCAN6062-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in all driver states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between multiple states; therefore, the short-circuit current may be viewed as either the current during each bus state or as a weighted average DC current. When selecting termination resistors or a common mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used.

The average short-circuit current of the bus depends on the weighted average of each driver state during the fault and each state's respective short-circuit current. The average short-circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC\_Bits} \times I_{OS(SS)\_REC}) + (\%\ \text{DOM\_Bits} \times I_{OS(SS)\_DOM}) + (\%\ \text{XL\_Bits} \times I_{OS(SS)\_XL}] + [\%\ \text{Receive} \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- % XL_Bits is the percentage of FAST TX bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current
- $I_{OS(SS)\_XL}$ is the FAST TX mode steady state short-circuit current

This short-circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceiver's V_{CC} supply.

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7.3.7 Thermal Shutdown (TSD)

If the junction temperature of the TCAN6062V-Q1 exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The TCAN6062V-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

7.3.8 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 7-1. Undervoltage Lockout - TCAN6062-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	Protected	High impedance	High impedance

Table 7-2. Undervoltage Lockout - TCAN6062V-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = V_{IO}: standby mode	High impedance	V_{IO}: Remote wake request(1)
		STB = GND: Protected		Recessive
> UV_{VCC}	< UV_{VIO}	Protected		High impedance
< UV_{VCC}	< UV_{VIO}	Protected		High impedance

(1) See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

Once the undervoltage condition is cleared and t_{MODE} has expired, the TCAN6062V-Q1 transitions to normal mode and the host controller can send and receive CAN traffic again.

7.3.9 Unpowered Device

The TCAN6062V-Q1 is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so the pins do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so the pins do not load other circuits which may remain powered.

7.3.10 Floating pins

The TCAN6062V-Q1 has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This ensures that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 7-3 for details on pin bias conditions.

Table 7-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

7.4 Device Functional Modes

7.4.1 Operating Modes

The TCAN6062V-Q1 has two main operating modes: normal mode and standby mode. The operating mode selection is made by applying a high or low level to the STB pin.

Table 7-4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received (1)
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

(1) See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

7.4.2 Normal Mode

This is the normal operating mode. In this mode, CAN communication is bidirectional. The driver and receiver can be switched between SIC mode and FAST mode based upon the presence or absence of a PWM input on TXD (see Section 7.3.3.1).

In SIC mode, the driver is translating a digital signal on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD pin based upon SIC mode input thresholds.

In FAST TX mode, the driver is translating a PWM signal on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD pin based upon FAST mode input thresholds.

In FAST RX mode, the driver remains high-impedance to the bus. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD pin based upon FAST mode input thresholds.

7.4.3 Standby Mode

This is the low-power mode of the device. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in TBD. The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode; see Figure 7-4 and Figure 7-6.

In standby mode, only the V_{IO} supply is required; therefore, the V_{CC} may be switched off for additional system level current savings.

7.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN6062-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from ISO 11898-2:2024 Annex A to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN6062-Q1.

The Wake-Up Pattern (WUP) comprises four pulses: a filtered dominant, followed by a filtered recessive, then another filtered dominant, and finally another filtered recessive. After the first filtered dominant pulse, the bus monitor waits for a filtered recessive without being reset by other bus traffic and does the same until second filtered recessive pulse. Upon receiving the second filtered recessive pulse, WUP is recognized. RXD is set permanently low upon subsequent dominant pulses.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP, and therefore, no wake request is generated. Bus state

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times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 7-14 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2024 standard has defined wakeup filter time to enable 1Mbps arbitration.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \le t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in the current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 7-14 for the timing diagram of the wake-up pattern with wake timeout feature.

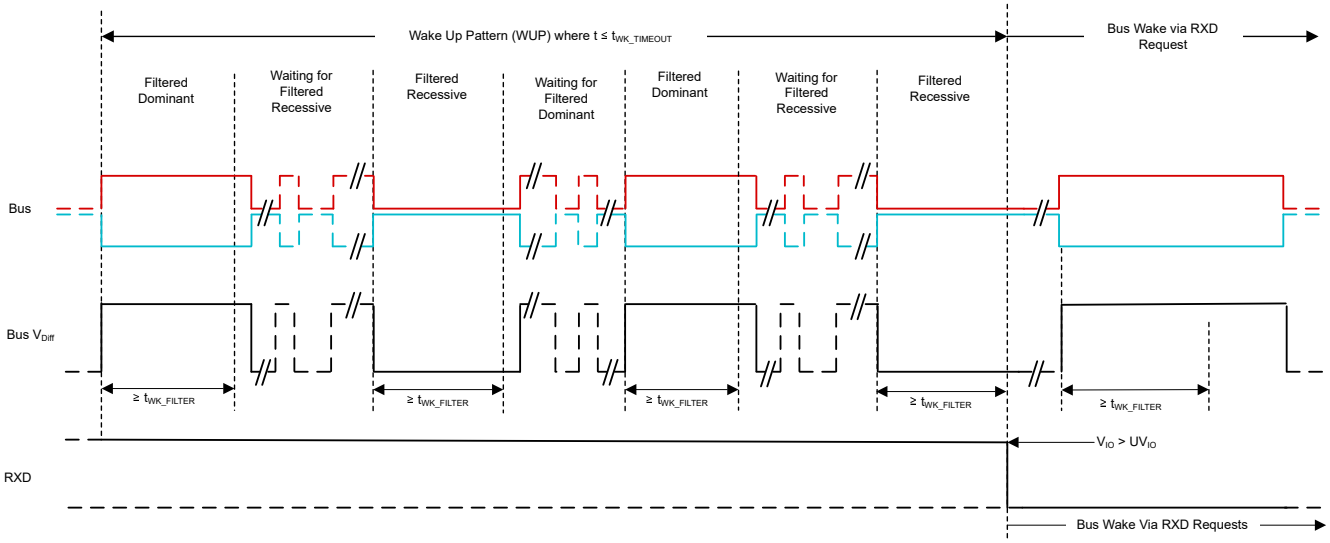

Figure 7-14. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

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7.4.4 Driver and Receiver Function

The digital logic input and output levels for the device are CMOS levels with respect to V_{CC}. For TCAN6062V-Q1, these are referred to V_{IO} for compatibility with MCUs having 1.8V, 2.5V, 3.3V, or 5V supply.

Table 7-5. Driver Function Table

Device Mode	Driver/ Receiver Mode(1)	TXD Input	Bus Outputs		Driven Bus State(4)
			CANH	CANL	
Normal	SIC mode	Low	High	Low	Dominant
		High or open	High impedance	High impedance	Biased recessive
	FAST TX mode	PWM low(2)	High	Low	Level_0
		PWM high(2)	Low	High	Level_1
	FAST RX mode	PWM(2)	High impedance	High impedance	Biased recessive
Standby		X(3)	High impedance	High impedance	Biased to ground

(1) See Section 7.4.2 and Section 7.4.3 for an overview of driver/receiver modes
(2) See Section 7.3.3.4
(3) X = irrelevant
(4) For bus state and bias see Figure 7-4, Figure 7-5, and Figure 7-6

Table 7-6. Receiver Function Table

Device Mode	Driver/Receiver Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	SIC mode	$V_{ID} \geq 0.9V$	Dominant	Low
		$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
		$V_{IT(OOB)} < V_{ID} \leq 0.5V$	Recessive	High
		Open ($V_{ID} \approx 0V$)	Open	
		$V_{ID} \leq V_{IT(OOB)}$	Out of bounds(1)	Low
	FAST TX mode or FAST RX mode	$V_{ID} \geq 0.1V$	Level_0	Low
		$-0.1V < V_{ID} < 0.1V$	Undefined	Undefined
		Open ($V_{ID} \approx 0V$)	Open	
		$V_{ID} \leq -0.1V$	Level_1	High
Standby		$V_{ID} \geq 1.15V$	Dominant	High Low if a remote wake event occurred See Figure 7-14
		$0.4V < V_{ID} < 1.15V$	Undefined	
		$V_{ID} \leq 0.4V$	Recessive	
		Open ($V_{ID} \approx 0V$)	Open	

(1) See Out-of-Bounds (OOB) Comparator

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application

The TCAN6062-Q1 is typically used in applications with a host microprocessor that includes a CAN controller which is responsible for the data link layer of the CAN protocol. For a system to implement CAN XL, the CAN controller needs to support CAN XL as described in the ISO 11898-1:2024 standard. The CAN XL controller is able to generate the PWM signals required to switch the TCAN6062-Q1 into FAST TX and FAST RX modes while transmitting and receiving CAN XL frames. The TCAN6062-Q1 can also be used with CAN controllers that support Classic CAN (CAN CC) or CAN with Flexible Data Rate (CAN FD) as defined in current or prior editions of ISO 11898-1 or similar CAN protocol standards as shown in Figure 8-4, for example. The TCAN6062-Q1 remains in SIC mode for data rates and communication methods used in these protocols.

Figure 8-1 shows a typical configuration for 5V controller applications. The bus termination is shown for illustrative purposes.

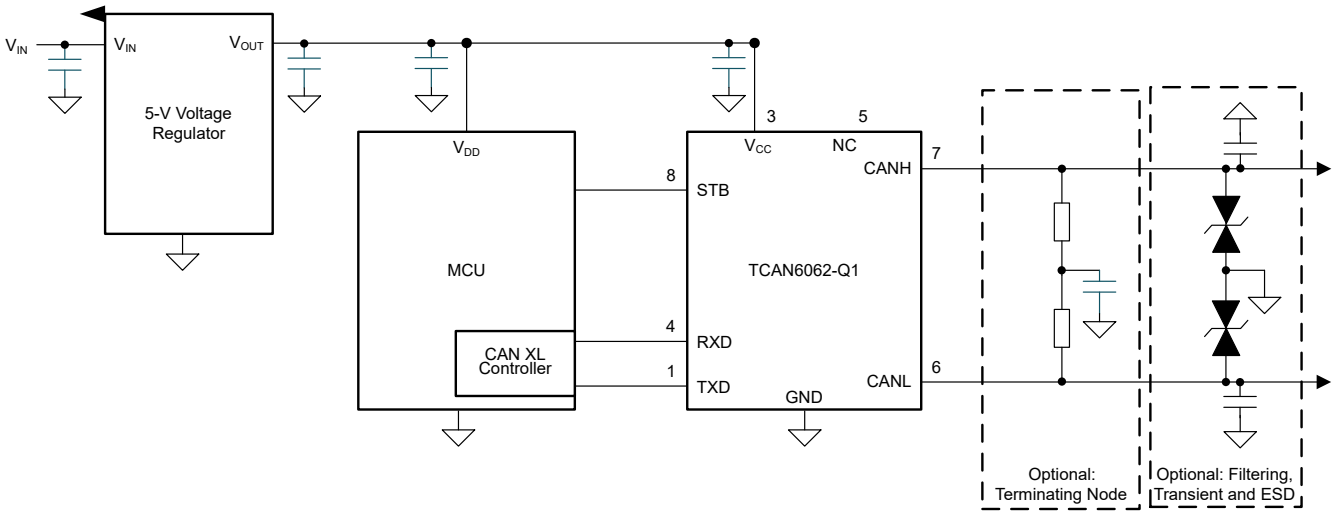

Figure 8-1. Transceiver Application Using 5V I/O Connections

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8.1.1 Design Requirements

8.1.1.1 CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used, see Figure 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

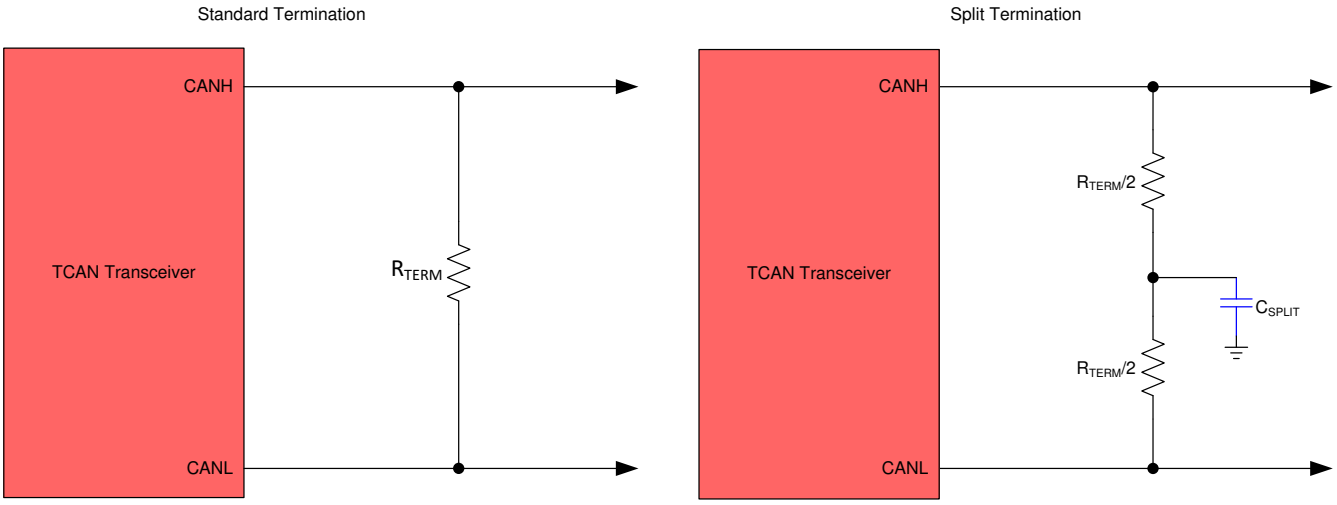

Figure 8-2. CAN Bus Termination Concepts

8.1.2 Detailed Design Procedures

8.1.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN6062-Q1. Additionally, since TCAN6062(V)-Q1 has SIC and FAST TX, in a given network size, higher data rate can be achieved because signal ringing is attenuated.

CAN XL is intended for use in point-to-point or multi-point networks that require higher data throughput than what can be achieved by CAN FD or Ethernet 10BASE-T systems. This higher-speed connection can be used in zonal architectures to connect other lower-speed networks together without the need to translate CAN traffic to another protocol. Zonal systems can use a combination of CAN FD, Ethernet, and CAN XL to achieve high reliability connectivity across a large number of devices.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2024 Annex A specification, the driver differential output is specified with a bus load that can range from 45Ω to 65Ω where the differential output must be greater than 1.5V. This bus load range is extended to 45Ω by Annex A, which contains additional transceiver design specifications targeted toward CAN XL applications. The TCAN6062-Q1 family is specified to meet the 1.5V requirement down to 45Ω. This widened driver capability allows use cases with 50Ω termination, such as Cat5 or coaxial cable applications.

The differential input resistance of the TCAN6062-Q1 is a minimum of 40kΩ. If 100 TCAN6062-Q1 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TCAN6062-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must

ADVANCE INFORMATION

be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity; therefore, a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design for robust network operation.

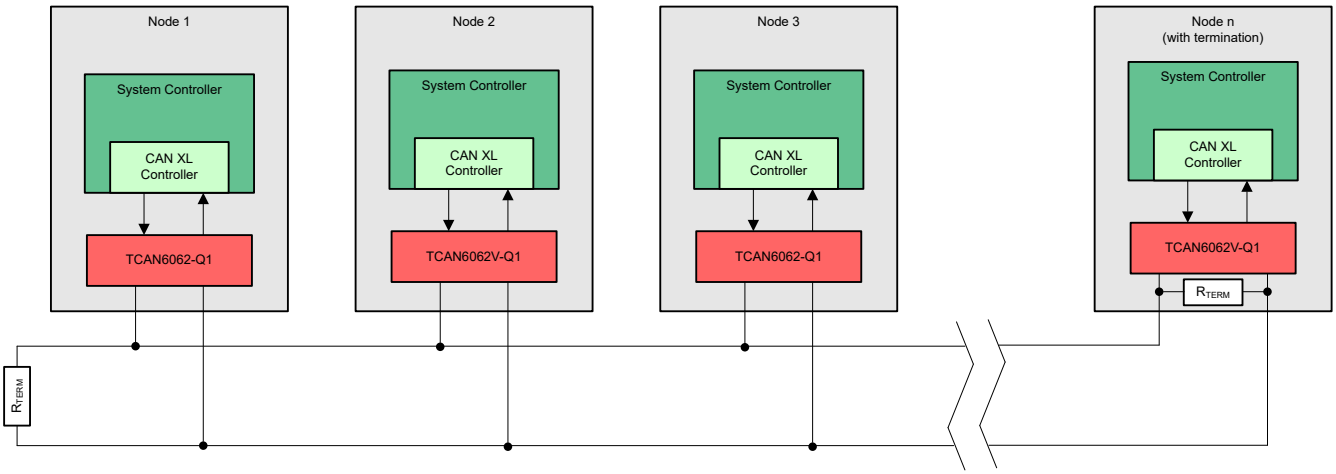

Figure 8-3. Typical CAN XL Bus

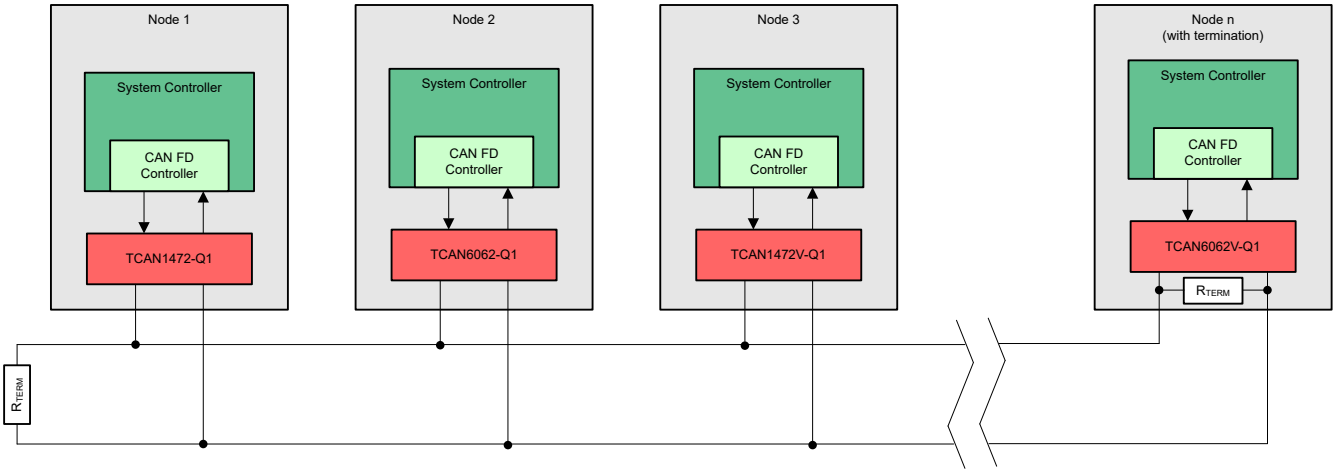

Figure 8-4. Typical CAN FD Bus with CAN SIC and CAN XL Transceivers

8.2 System Examples

The TCAN6062(V)-Q1 CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8V, 2.5V, or 3.3V application is shown in Figure 8-5. The bus termination is shown for illustrative purposes.

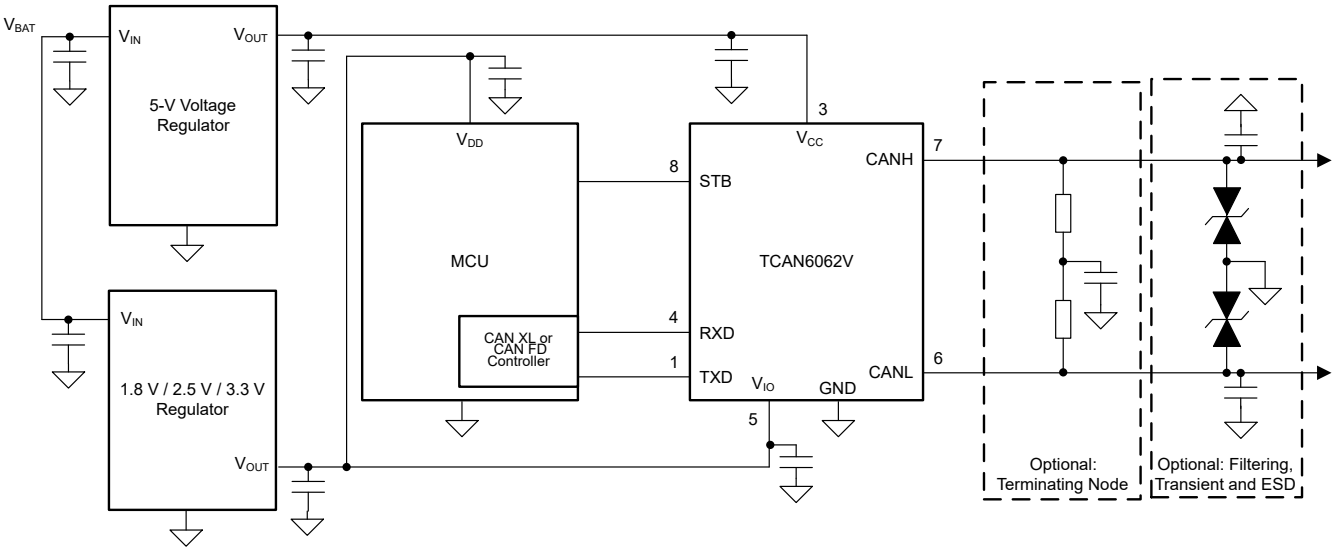

Figure 8-5. Typical Transceiver Application Using 1.8V, 2.5V, 3.3V IO Connections

8.3 Power Supply Recommendations

The device transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.75V and 5.25V. The TCAN6062V-Q1 implements an IO level shifting supply input, V_{IO}, designed for a range between 1.71V and 5.5V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100nF, should be placed near the CAN transceiver main V_{CC} supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100nF, should be placed near the CAN transceiver's V_{IO} supply pin in addition to bypass capacitors.

8.4 Layout

8.4.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Note

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R4 and R5, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. See CAN Termination, and CAN Bus Short Circuit Current Limiting for information on termination concepts and power ratings needed for the termination resistor(s).

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8.4.2 Layout Example

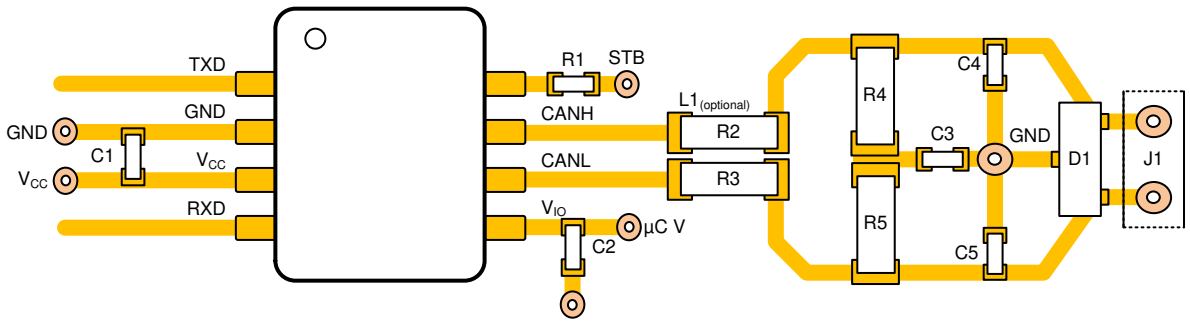

Figure 8-6. Layout Example

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
September 2025	*	Initial Revision

11 Mechanical, Packaging, and Orderable Information

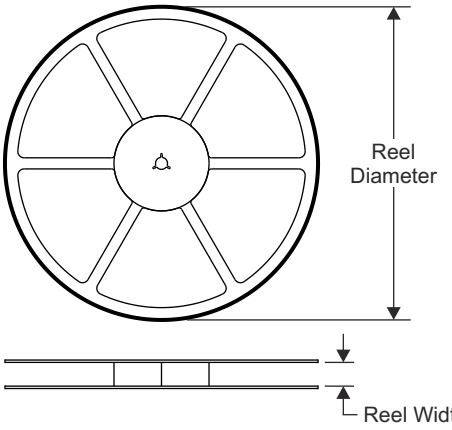
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

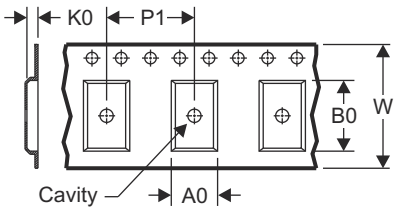
ADVANCE INFORMATION

11.1 Tape and Reel Information

REEL DIMENSIONS

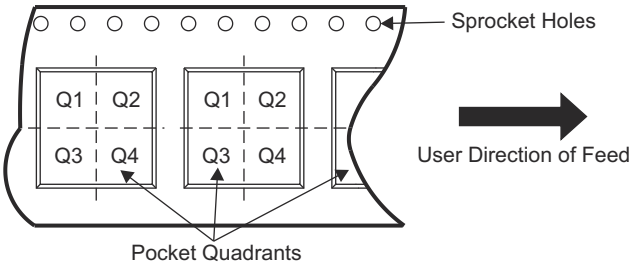


TAPE DIMENSIONS



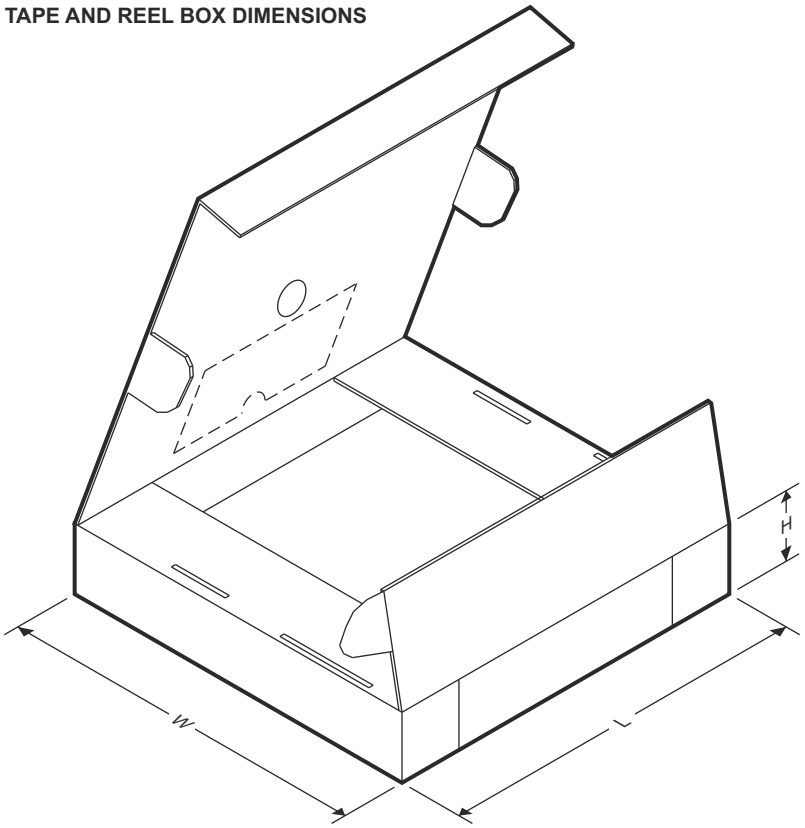
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN6062VDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN6062VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

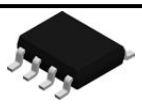
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN6062VDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TCAN6062VDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0

ADVANCE INFORMATION

ADVANCE INFORMATION

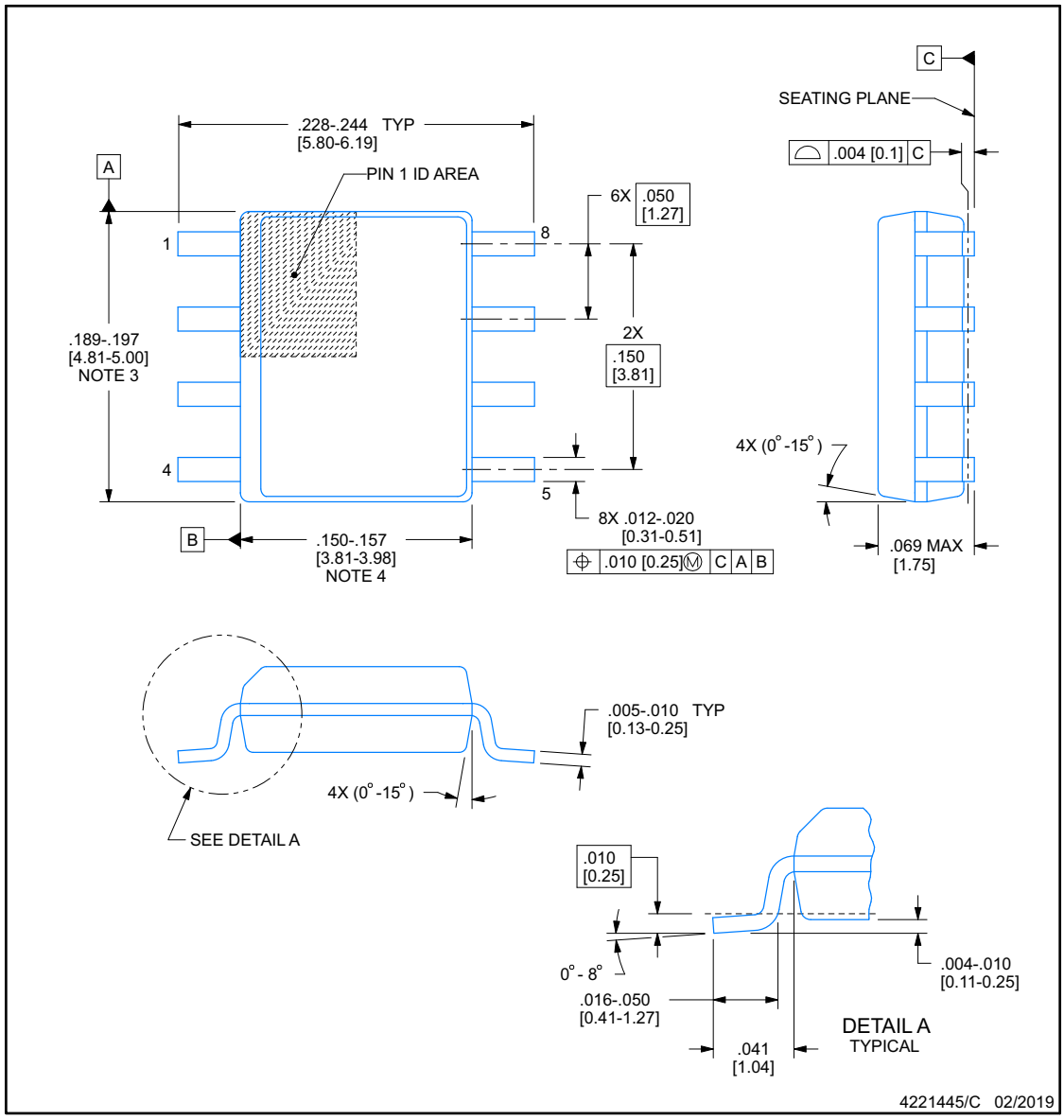


PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

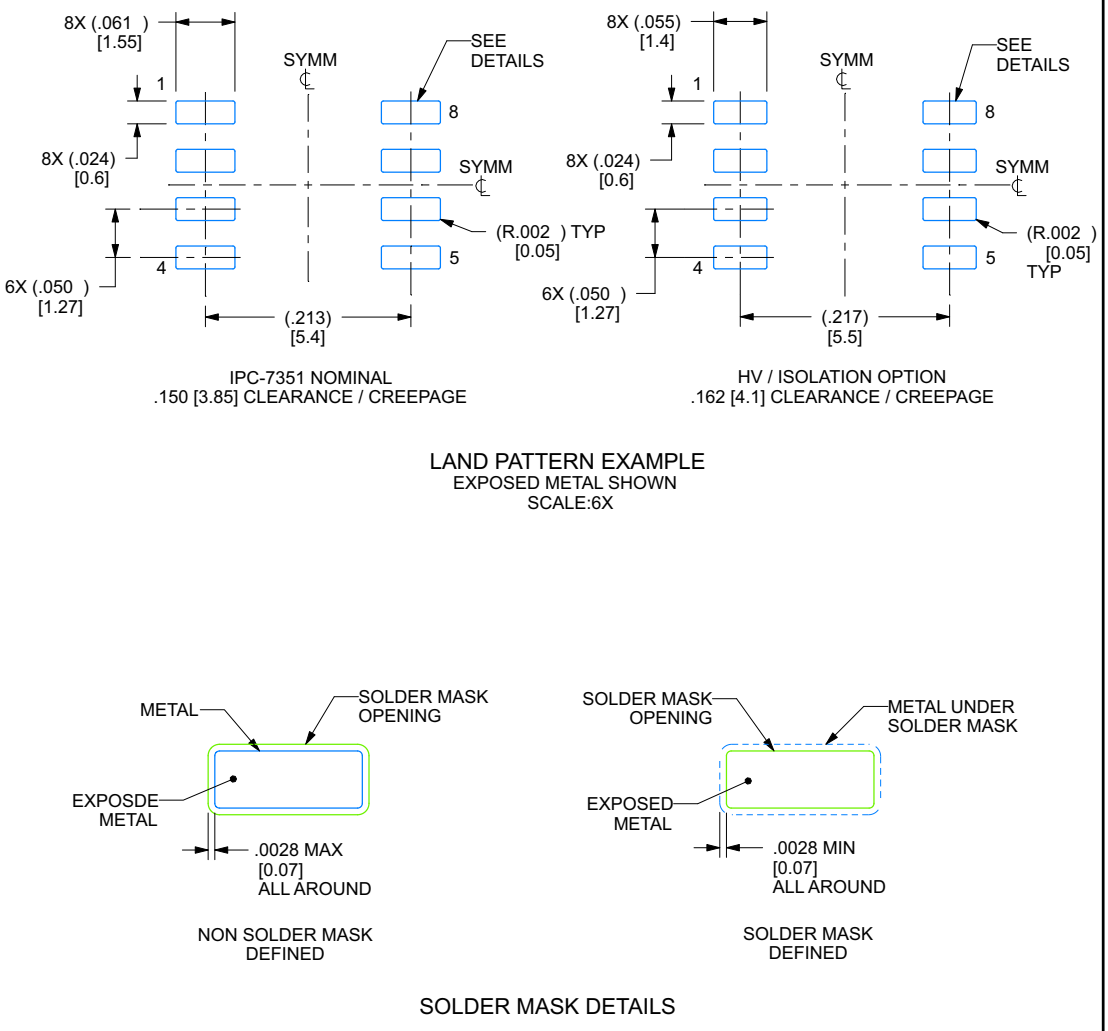
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

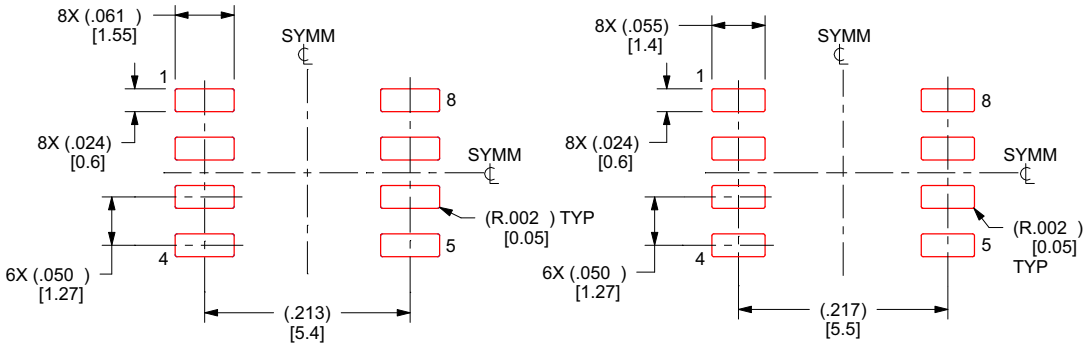
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

D0008B — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

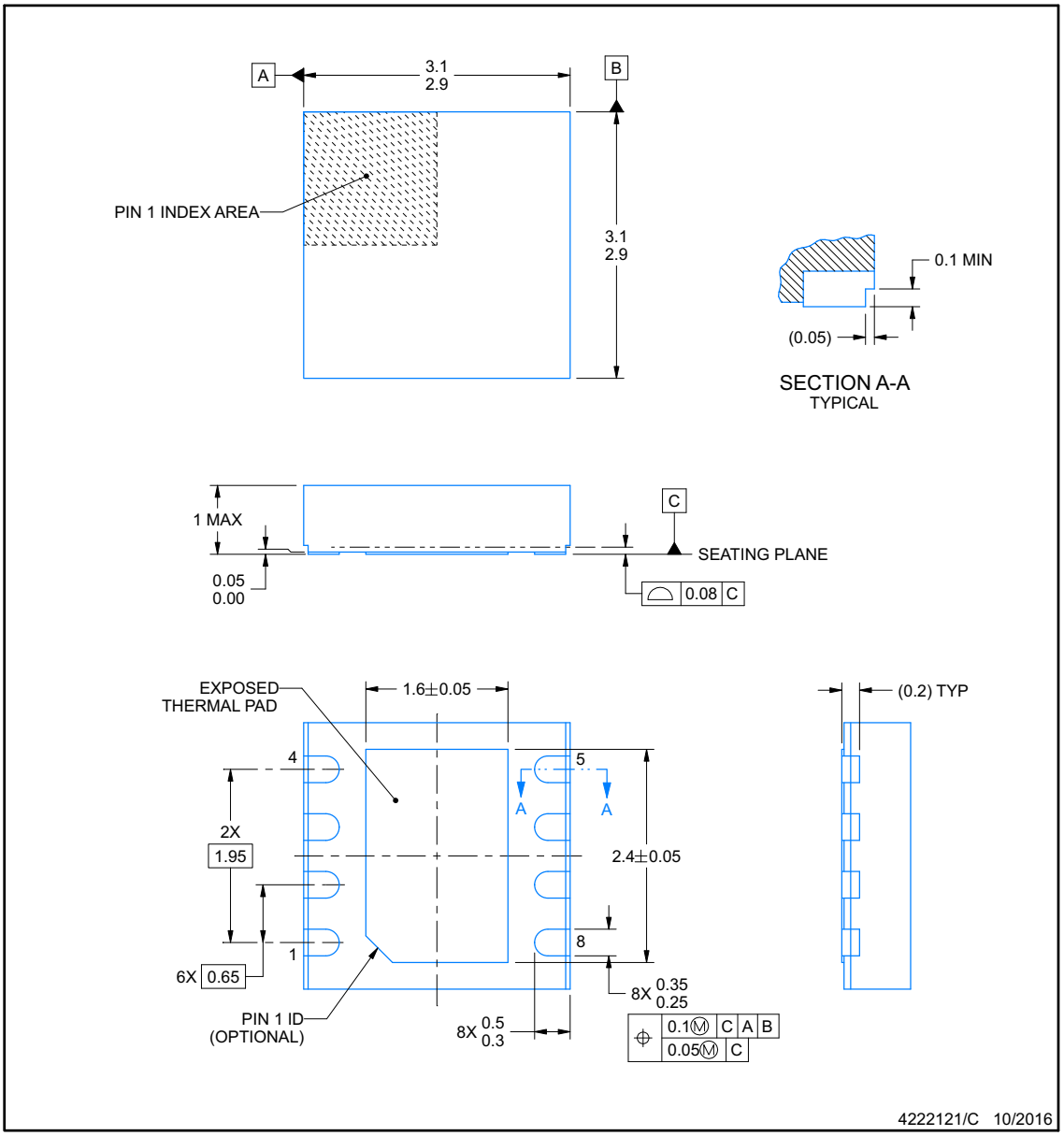
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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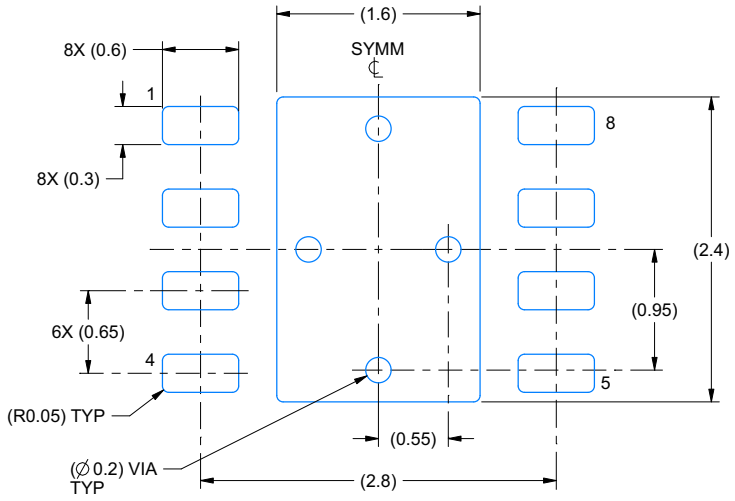
ADVANCE INFORMATION

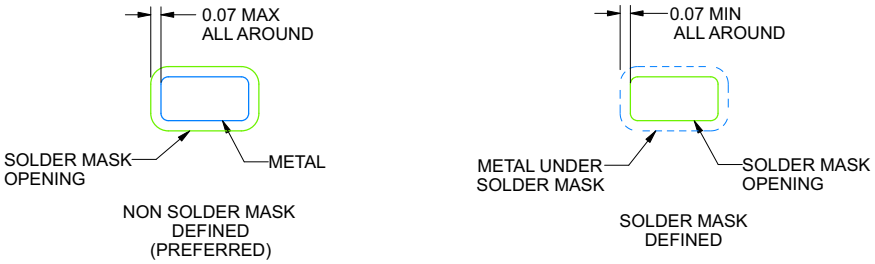
EXAMPLE BOARD LAYOUT

DRB0008F — VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222121/C 10/2016

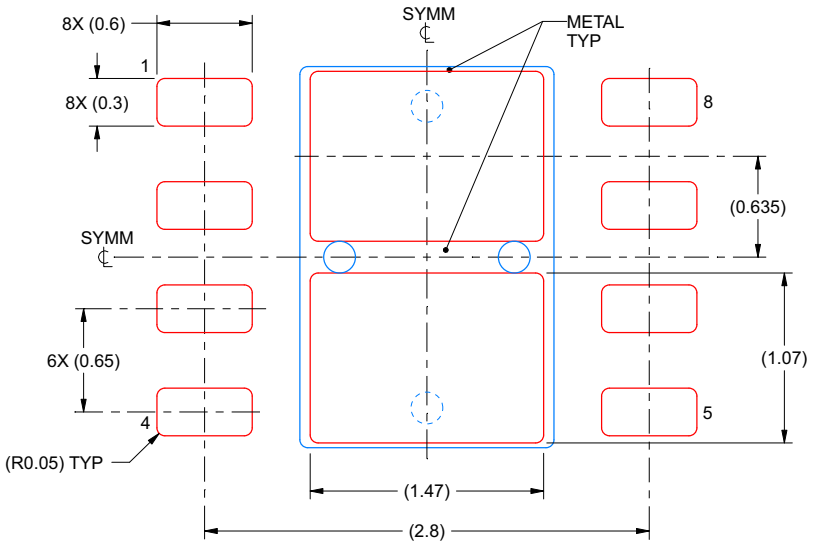
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008F — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222121/C 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTCAN6062DRBRQ1	Active	Preproduction	SON (DRB) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN6062DRQ1	Active	Preproduction	SOIC (D) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN6062VDRBRQ1	Active	Preproduction	SON (DRB) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN6062VDRQ1	Active	Preproduction	SOIC (D) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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