# TCAN1046A-Q1 Automotive Dual CAN FD Transceiver with Standby Mode

## 1 Features

- AEC-Q100 (Grade 1): Qualified for automotive applications
- Two independent high-speed CAN FD transceivers with mode control
- Meets the requirements of ISO 11898-2:2016 physical layer standard
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- Support of classical CAN and optimized CAN FD performance at 2, 5, and 8 Mbps
  - Short and symmetrical propagation delays for enhanced timing margin
- Support for 12-V and 24-V battery applications
- Receiver common-mode input voltage: ±12 V
- Protection features:
  - Bus fault protection: ±58 V
  - Undervoltage protection
  - TXD-dominant time-out (DTO)
    - Data rates down to 9.2 kbps
  - Thermal-shutdown protection (TSD)
- Operating modes:
  - Normal mode
  - Low power standby mode supporting remote wake-up request
- Optimized behavior when unpowered
  - Bus and logic pins are high impedance (no load to operating bus or application)
  - Hot-plug capable: power-up and power-down glitch-free operation on bus and RXD output
- Junction temperatures from: –40°C to 150°C
- Available in SOIC (14) and leadless VSON (14) packages (4.5 mm x 3.0 mm) with improved automated optical inspection (AOI) capability

## 2 Applications

- Automotive and transportation
  - Body control modules
  - Automotive gateway
  - Advanced driver assistance system (ADAS)
  - Infotainment

## 3 Description

The TCAN1046A-Q1 is a dual high-speed controller area network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification.

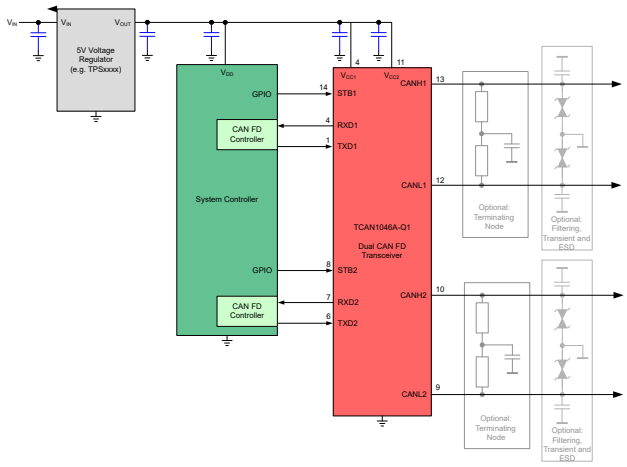
The device supports both classical CAN and CAN FD networks up to 8 megabits per second (Mbps). The device has two CAN FD channels with independent supply, $V_{CC1}$ and $V_{CC2}$, and mode control, STB1 and STB2 pins, allowing for true independent operation of each CAN channel. The ability to operate each channel independent of one another is important in applications that require redundancy or additional CAN FD channels to act as a back-up in the event of a system failure.

The device includes many protection and diagnostic features including thermal-shutdown (TSD), TXD-dominant time-out (DTO), and bus fault protection up to ±58 V. The device has defined failsafe behavior in supply under-voltage or floating pin scenarios.

**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| TCAN1046A-Q1 | VSON (DMT) (14) | 4.50 mm x 3.00 mm |
| | SOIC (D) (14) | 8.65 mm x 3.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Simplified Schematic**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (July 2021) to Revision A (December\2021) | Page |
|---|---|
| • Changed the document status from: *Advanced Information* to: *Production* data | 1 |

# 5 Pin Configuration and Functions

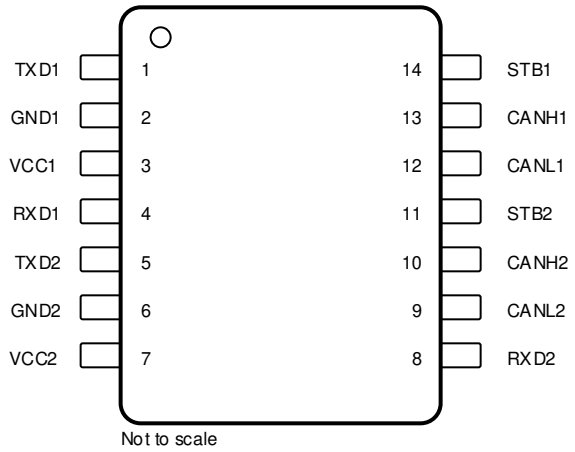



**Figure 5-1. D Package, 14 Pin SOIC, Top View**

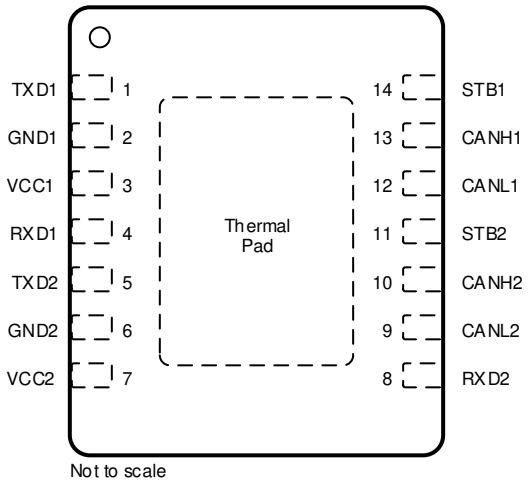



**Figure 5-2. DMT Package, 14 Pin VSON, Top View**

**Table 5-1. Pin Functions**

| Pins | | Type | Description |
|---|---|---|---|
| Name | No. | | |
| TXD1 | 1 | Digital Input | CAN transmit data input channel 1; integrated pull-up |
| GND1 | 2 | GND1 | Ground connection, channel 1 |
| $V_{CC1}$ | 3 | Supply | 5-V supply voltage, channel 1 |
| RXD1 | 4 | Digital Output | CAN receive data output channel 1; tri-state when $V_{CC} < UV_{VCC}$ |
| TXD2 | 5 | Digital Input | CAN transmit data input channel 2; integrated pull-up |
| GND2 | 6 | GND2 | Ground connection, channel 2 |
| $V_{CC2}$ | 7 | Supply | 5-V supply voltage, channel 2 |
| RXD2 | 8 | Digital Output | CAN receive data output channel 2; tri-state when $V_{CC} < UV_{VCC}$ |
| CANL2 | 9 | Bus IO | Low-level CAN bus channel 2 input/output line |
| CANH2 | 10 | Bus IO | High-level CAN bus 2 input/output line |
| STB2 | 11 | Digital Input | Standby input of channel 2 for mode control; integrated pull-up |
| CANL1 | 12 | Bus IO | Low-level CAN bus channel 1 input/output line |
| CANH1 | 13 | Bus IO | High-level CAN bus channel 1 input/output line |
| STB1 | 14 | Digital Input | Standby input of channel 1 for mode control; integrated pull-up |
| Thermal Pad (VSON only) | | — | Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply voltage | –0.3 | 6 | V |
| $V_{BUS}$ | CAN Bus I/O voltage<br>CANH1, CANL1, CANH2, CANL2 | –58 | 58 | V |
| $V_{DIFF}$ | Max differential voltage between CANHx and CANLx | –45 | 45 | V |
| $V_{Logic\_Input}$ | Logic input terminal voltage | –0.3 | 6 | V |
| $V_{RXDx}$ | RXDx output terminal voltage range | –0.3 | 6 | V |
| $I_{O(RXDx)}$ | RXDx output current | –8 | 8 | mA |
| $T_J$ | Junction temperature | –40 | 165 | °C |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | HBM classification level 3A for all pins | ±4000 | V |
| | | | HBM classification level 3B for global pins CANHx and CANLx with respect to GND | ±10000 | V |
| | | Charged-device model (CDM), per AEC Q100-011<br>CDM classification level C5 for all pins | | ±750 | V |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 ESD Ratings — IEC Specifications

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | System level Electrostatic discharge | CAN bus terminals to GND<br>CANH1, CANL1, CANH2, CANL2 | Unpowered contact discharge per ISO 10605 (1) | ±8000 | V |
| | | | SAE J2962-2 per ISO 10605 Powered Contact Discharge (2) | ±8000 | V |
| | | | SAE J2962-2 per ISO 10605 Powered Air Discharge (2) | ±15000 | V |
| $V_{Tran}$ | Transient voltage per ISO 7637-2(3) | | Pulse 1 | –100 | V |
| | | | Pulse 2a | 75 | V |
| | | | Pulse 3a | –150 | V |
| | | | Pulse 3b | 100 | V |
| | Transient voltage per ISO 7637-3(4) | | DCC slow transient pulse | ±30 | V |

(1) Tested according to IEC 62228-3:2019 CAN Transceivers
(2) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(3) Tested according to IEC 62228-3:2019 CAN Transceivers
(4) Tested according to SAE J2962-2

## 6.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $I_{OH(RXDx)}$ | RXDx terminal high-level output current | –2 | | | mA |
| $I_{OL(RXDx)}$ | RXDx terminal low-level output current | | | 2 | mA |
| $T_J$ | Operating junction temperature | -40 | | 150 | ℃ |

## 6.5 Thermal Characteristics

| THERMAL METRIC(1) | | TCAN1046A-Q1 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DMT (VSON) | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 75.8 | 38.1 | ℃/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 35.8 | 38.7 | ℃/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 37.4 | 15.0 | ℃/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 6.6 | 2.0 | ℃/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 37.0 | 15.0 | ℃/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | 5.9 | ℃/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.6 Supply Characteristics

Over recommended operating conditions with $T_J$ = -40°C to 150°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current Normal mode | Dominant One Channel(1) | TCAN1046A: STB1 = STB2 = 0 V<br>TXDx = 0 V, TXDy = $V_{CC2}$<br>$R_{L1}$ = $R_{L2}$ = 60 Ω, $C_L$ = open;<br>See Figure 7-1 | | 50 | 77.5 | mA |
| | | Dominant One Channel(1) | TCAN1046A: STB1 = STB2 = 0 V<br>TXDx = 0 V, TXDy = $V_{CC2}$<br>$R_{L1}$ = $R_{L2}$ = 50 Ω, $C_L$ = open;<br>See Figure 7-1 | | 55 | 87.5 | mA |
| | | Dominant Two channels(1) | TCAN1046A: STB1 = STB2 = 0 V<br>TXDx = TXDy = 0 V<br>$R_{L1}$ = $R_{L2}$ = 60 Ω, $C_L$ = open;<br>See Figure 7-1 | | 95 | 140 | |
| | | Dominant Two channels(1) | TCAN1046A: STB1 = STB2 = 0 V<br>TXDx = TXDy = 0 V<br>$R_{L1}$ = $R_{L2}$ = 50 Ω, $C_L$ = open;<br>See Figure 7-1 | | 100 | 160 | |
| | | Recessive Two channels | TCAN1046A: STB1 = STB2 = 0 V<br>TXDx =$V_{CC1}$, TXDy = $V_{CC2}$<br>$R_{L1}$ = $R_{L2}$ = 50 Ω, $C_L$ = open;<br>See Figure 7-1 | | 10 | 15 | mA |
| | | CANx dominant with bus fault CANy recessive(1) (2) | TCAN1046A: STB1 = STB2 = 0 V<br>TXDx =$V_{CC1}$, TXDy = $V_{CC2}$<br>CANHx = CANLx = ±25 V<br>$R_{Lx}$ = open, $R_{Ly}$ = 50 Ω, $C_L$ = open;<br>See Figure 7-1 | | 90 | 137.5 | mA |
| | | CANx dominant with bus fault CANy dominant(1) (2) | TCAN1046A: STB1 = STB2 = 0 V<br>TXDx = TXDy = 0 V<br>CANHx = CANLx = ±25 V<br>$R_{Lx}$ = open, $R_{Ly}$ = 50 Ω, $C_L$ = open;<br>See Figure 7-1 | | 135 | 210 | mA |
| | | CANx and CANy dominant with bus fault(1) (2) | TCAN1046A: STB1 = STB2 = 0 V<br>TXDx = TXDy = 0 V<br>CANH1 = CANL1 = ±25 V<br>CANH2 = CANL2 = ±25 V<br>$R_{Lx}$ = $R_{Ly}$ = open , $C_L$ = open;<br>See Figure 7-1 | | 170 | 260 | mA |
| | Supply current Standby mode | | TCAN1046A: STB1 =$V_{CC1}$, STB2 = $V_{CC2}$<br>TXDx =$V_{CC1}$, TXDy = $V_{CC2}$<br>$R_{Lx}$ = $R_{Ly}$ = 60 Ω, $C_L$ = open<br>See Figure 7-1 | | 17.5 | 32 | µA |
| $UV_{CC}$ | Rising undervoltage detection on $V_{CC1/2}$ | | | | 4.2 | 4.4 | V |
| | Falling undervoltage detection on $V_{CC1/2}$ | | | 3.5 | 4 | 4.25 | V |
| $V_{HYS(UVCC)}$ | Hysteresis voltage on $UV_{CC1/2}$ | | | | 200 | | mV |

(1) TXD1 and TXD2 are interchangeable for TXDx and TXDy
(2) CAN1 and CAN2 are interchangeable for CANx and CANy

## 6.7 Dissipation Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | One channel average power dissipation Normal mode | $V_{CC}$ = 5 V, $T_J$= 27°C, $R_L$ = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF | | 95 | | mW |
| | | $V_{CC}$ = 5.5 V, $T_J$= 150°C, $R_L$ = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF | | 120 | | mW |
| $T_{TSD}$ | Thermal shutdown temperature | | 175 | 195 | 210 | °C |
| $T_{TSD(HYS)}$ | Thermal shutdown hysteresis | | | 12 | | °C |

## 6.8 Electrical Characteristics

Over recommended operating conditions with $T_J$ = -40°C to 150°C (unless otherwise noted), CAN electrical parameters apply to both channels

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Driver Electrical Characteristics** | | | | | | | |
| $V_{O(DOM)}$ | Dominant output voltage<br>Normal mode | CANH | STB = 0 V<br>TXD = 0 V<br>50 Ω ≤ $R_L$ ≤ 65 Ω, $C_L$ = open;<br>See Figure 7-2 and Figure 8-3 | 2.75 | | 4.5 | V |
| | | CANL | | 0.5 | | 2.25 | V |
| $V_{O(REC)}$ | Recessive output voltage<br>Normal mode | CANH and CANL | STB = 0 V<br>TXD = $V_{CC}$<br>$R_L$ = open (no load);<br>See Figure 7-2 and Figure 8-3 | 2 | 0.5 $V_{CC}$ | 3 | V |
| $V_{SYM}$ | Driver symmetry<br>($V_{O(CANH)}$ + $V_{O(CANL)}$)/$V_{CC}$ | | STB = 0 V<br>TXD = 250 kHz, 1 MHz, 2.5 MHz<br>$R_L$ = 60 Ω, $C_{SPLIT}$ = 4.7 nF, $C_L$ = open;<br>See Figure 7-2 and Figure 8-3 | 0.9 | | 1.1 | V/V |
| $V_{SYM\_DC}$ | DC output symmetry<br>($V_{CC}$ - $V_{O(CANH)}$ - $V_{O(CANL)}$) | | STB = 0 V<br>$R_L$ = 60 Ω, $C_L$ = open;<br>See Figure 7-2 and Figure 8-3 | –400 | | 400 | mV |
| $V_{OD(DOM)}$ | Differential output voltage<br>Normal mode<br>Dominant | CANH - CANL | STB = 0 V<br>TXD = 0 V<br>50 Ω ≤ $R_L$ ≤ 65 Ω, $C_L$ = open;<br>See Figure 7-2 and Figure 8-3 | 1.5 | | 3 | V |
| | | | STB = 0 V<br>TXD = 0 V<br>45 Ω ≤ $R_L$ ≤ 70 Ω, $C_L$ = open;<br>See Figure 7-2 and Figure 8-3 | 1.4 | | 3.3 | V |
| | | | STB = 0 V<br>TXD = 0 V<br>$R_L$ = 2240 Ω, $C_L$ = open;<br>See Figure 7-2 and Figure 8-3 | 1.5 | | 5 | V |
| $V_{OD(REC)}$ | Differential output voltage<br>Normal mode<br>Recessive | CANH - CANL | STB = 0 V<br>TXD = $V_{CC}$<br>$R_L$ = 60 Ω, $C_L$ = open;<br>See Figure 7-2 and Figure 8-3 | –120 | | 12 | mV |
| | | | STB = 0 V<br>TXD = $V_{CC}$<br>$R_L$ = open, $C_L$ = open;<br>See Figure 7-2 and Figure 8-3 | –50 | | 50 | mV |
| $V_{O(STB)}$ | Bus output voltage<br>Standby mode | CANH | STB = $V_{CC}$<br>$R_L$ = open;<br>See Figure 7-2 and Figure 8-3 | -0.1 | | 0.1 | V |
| | | CANL | | -0.1 | | 0.1 | V |
| | | CANH - CANL | | -0.2 | | 0.2 | V |
| $I_{OS(SS\_DOM)}$ | Short-circuit steady-state output current, dominant<br>Normal mode | | STB = 0 V<br>TXD = 0 V<br>$V_{(CANH)}$ = -15 V to 40 V, CANL = open;<br>See Figure 7-7 and Figure 8-3 | –115 | | | mA |
| | | | STB = 0 V<br>TXD = 0 V<br>$V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open;<br>See Figure 7-7 and Figure 8-3 | | | 115 | mA |
| $I_{OS(SS\_REC)}$ | Short-circuit steady-state output current, recessive<br>Normal mode | | STB = 0 V<br>TXD = $V_{CC}$<br>–27 V ≤ $V_{BUS}$ ≤ 32 V, where $V_{BUS}$ = CANH = CANL;<br>See Figure 7-7 and Figure 8-3 | –5 | | 5 | mA |
| **Receiver Electrical Characteristics** | | | | | | | |
| $V_{IT}$ | Input threshold voltage<br>Normal mode | | STB = 0 V<br>-12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-5 | 500 | | 900 | mV |
| $V_{IT(STB)}$ | Input threshold<br>Standby mode | | STB = $V_{CC}$<br>-12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-5 | 400 | | 1150 | mV |

## 6.8 Electrical Characteristics (continued)

Over recommended operating conditions with $T_J$ = -40℃ to 150℃ (unless otherwise noted), CAN electrical parameters apply to both channels

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DOM}$ | Dominant state differential input voltage range Normal mode | STB = 0 V<br>-12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-5 | 0.9 | | 9 | V |
| $V_{REC}$ | Recessive state differential input voltage range Normal mode | STB = 0 V<br>-12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-5 | -4 | | 0.5 | V |
| $V_{DOM(STB)}$ | Dominant state differential input voltage range Standby mode | STB = $V_{CC}$<br>-12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-5 | 1.15 | | 9 | V |
| $V_{REC(STB)}$ | Recessive state differential input voltage range Standby mode | STB = $V_{CC}$<br>-12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-5 | -4 | | 0.4 | V |
| $V_{HYS}$ | Hysteresis voltage for input threshold Normal mode | STB = 0 V<br>-12 V ≤ $V_{CM}$ ≤ 12 V;<br>See Figure 7-3 and Table 8-5 | | 115 | | mV |
| $V_{CM}$ | Common mode range Normal and standby modes | See Figure 7-3 and Table 8-5 | –12 | | 12 | V |
| $I_{LKG(IOFF)}$ | Unpowered bus input leakage current (measured individually for each channel) | CANH = CANL = 5 V, $V_{CC}$ = GND | | | 5 | µA |
| $C_I$ | Input capacitance to ground (CANH or CANL) | TXD = $V_{CC}$ | | | 20 | pF |
| $C_{ID}$ | Differential input capacitance | | | | 10 | pF |
| $R_{ID}$ | Differential input resistance | STB = 0 V<br>TXD = $V_{CC}$<br>-12 V ≤ $V_{CM}$ ≤ 12 V | 40 | | 90 | kΩ |
| $R_{IN}$ | Single ended input resistance (CANH or CANL) | | 20 | | 45 | kΩ |
| $R_{IN(M)}$ | Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 % | $V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V | –1 | | 1 | % |
| **TXD Terminal (CAN Transmit Data Input)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7 $V_{CC}$ | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.3 $V_{CC}$ | V |
| $I_{IH}$ | High-level input leakage current | TXD = $V_{CC}$ = 5.5 V | –2.5 | 0 | 1 | µA |
| $I_{IL}$ | Low-level input leakage current | TXD = 0 V<br>$V_{CC}$= 5.5 V | –200 | -100 | –20 | µA |
| $I_{LKG(OFF)}$ | Unpowered leakage current | TXD = 5.5 V<br>$V_{CC}$= 0 V | –1 | 0 | 1 | µA |
| $C_I$ | Input capacitance | $V_{IN}$ = 0.4×sin(2×π×2×$10^6$×t)+2.5 V | | 5 | | pF |
| **RXD Terminal (CAN Receive Data Output)** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_O$ = –2 mA;<br>See Figure 7-3 | 0.8 $V_{CC}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_O$ = 2 mA;<br>See Figure 7-3 | | | 0.2 $V_{CC}$ | V |
| $I_{LKG(OFF)}$ | Unpowered leakage current | RXD = 5.5 V<br>$V_{CC}$ = 0 V | –1 | 0 | 1 | µA |
| **STB Terminal (Standby Mode Input)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7 $V_{CC}$ | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.3 $V_{CC}$ | V |
| $I_{IH}$ | TCAN1046A high-level input leakage current STB | STB = $V_{CC}$ = 5.5 V | –2 | | 2 | µA |
| $I_{IL}$ | TCAN1046A low-level input leakage current STB | STB = 0 V<br>$V_{CC}$ = 5.5 V, | –20 | | –2 | µA |
| $I_{LKG(OFF)}$ | TCAN1046A unpowered leakage current | STB = 5.5V<br>$V_{CC}$ = 0 V | –1 | | 1 | µA |

## 6.9 Switching Characteristics

Over recommended operating conditions with $T_J$ = -40°C to 150°C (unless otherwise noted). Parameters apply to both channels.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Device Switching Characteristics** | | | | | | |
| $t_{PROP(LOOP1)}$ | Total loop delay<br>Driver input (TXD) to receiver output (RXD), recessive to dominant | STB = 0 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF;<br>See Figure 7-4 | | 125 | 210 | ns |
| $t_{PROP(LOOP2)}$ | Total loop delay<br>Driver input (TXD) to receiver output (RXD), dominant to recessive | STB = 0 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF;<br>See Figure 7-4 | | 150 | 210 | ns |
| $t_{MODE}$ | Mode change time, from normal to standby or from standby to normal | See Figure 7-5 | | | 20 | µs |
| $t_{WK\_FILTER}$ | Filter time for a valid wake-up pattern | | 0.5 | | 1.8 | µs |
| $t_{WK\_TIMEOUT}$ | Bus wake-up timeout | | 0.8 | | 6 | ms |
| **Driver Switching Characteristics** | | | | | | |
| $t_{pHR}$ | Propagation delay time, high TXD to driver recessive (dominant to recessive) | STB = 0 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF;<br>See Figure 7-2 | | 80 | | ns |
| $t_{pLD}$ | Propagation delay time, low TXD to driver dominant (recessive to dominant) | | | 70 | | ns |
| $t_{sk(p)}$ | Pulse skew (\|tpHR - tpLD\|) | | | 14 | | ns |
| $t_R$ | Differential output signal rise time | | | 28 | | ns |
| $t_F$ | Differential output signal fall time | | | 50 | | ns |
| $t_{TXD\_DTO}$ | Dominant timeout | STB = 0 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF;<br>See Figure 7-6 | 1.2 | | 4.0 | ms |

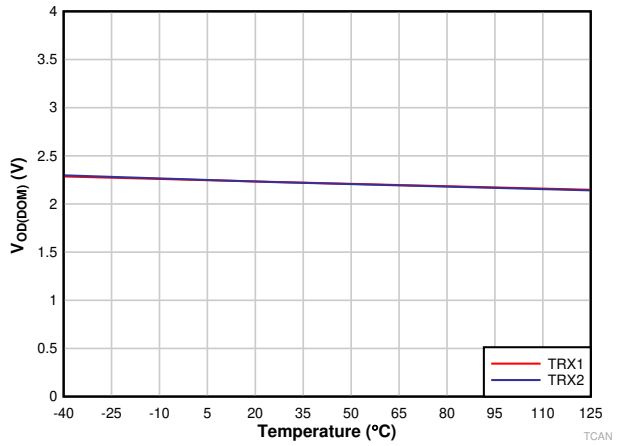
## 6.9 Switching Characteristics (continued)

Over recommended operating conditions with $T_J$ = -40℃ to 150℃ (unless otherwise noted). Parameters apply to both channels.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Receiver Switching Characteristics** | | | | | | |
| $t_{pRH}$ | Propagation delay time, bus recessive input to high output (dominant to recessive) | STB = 0 V<br>$C_{L(RXD)}$ = 15 pF<br>See Figure 7-3 | | 81 | | ns |
| $t_{pDL}$ | Propagation delay time, bus dominant input to low output (recessive to dominant) | | | 66 | | ns |
| $t_R$ | RXD output signal rise time | | | 10 | | ns |
| $t_F$ | RXD output signal fall time | | | 10 | | ns |
| **FD Timing Characteristics** | | | | | | |
| $t_{BIT(BUS)}$ | Bit time on CAN bus output pins<br>$t_{BIT(TXD)}$ = 500 ns | STB = 0 V<br>$R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF<br>$\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ ;<br>See Figure 7-4 | 450 | | 525 | ns |
| | Bit time on CAN bus output pins<br>$t_{BIT(TXD)}$ = 200 ns | | 160 | | 205 | ns |
| | Bit time on CAN bus output pins<br>$t_{BIT(TXD)}$ = 125 ns(1) | | 85 | | 130 | ns |
| $t_{BIT(RXD)}$ | Bit time on RXD output pins<br>$t_{BIT(TXD)}$ = 500 ns | | 410 | | 540 | ns |
| | Bit time on RXD output pins<br>$t_{BIT(TXD)}$ = 200 ns | | 130 | | 210 | ns |
| | Bit time on RXD output pins<br>$t_{BIT(TXD)}$ = 125 ns(1) | | 75 | | 135 | ns |
| $t_{REC}$ | Receiver timing symmetry<br>$t_{BIT(TXD)}$ = 500 ns | | -50 | | 20 | ns |
| | Receiver timing symmetry<br>$t_{BIT(TXD)}$ = 200 ns | | -40 | | 10 | ns |
| | Receiver timing symmetry<br>$t_{BIT(TXD)}$ = 125 ns(1) | | -40 | | 10 | ns |

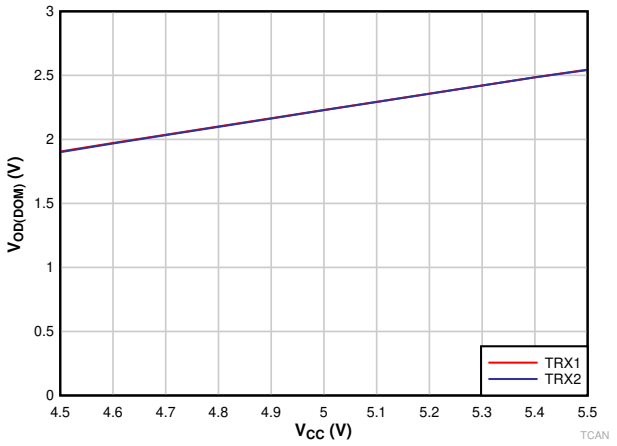
(1) Measured during characterization and not an ISO 11898-2:2016 parameter.

## 6.10 Typical Characteristics



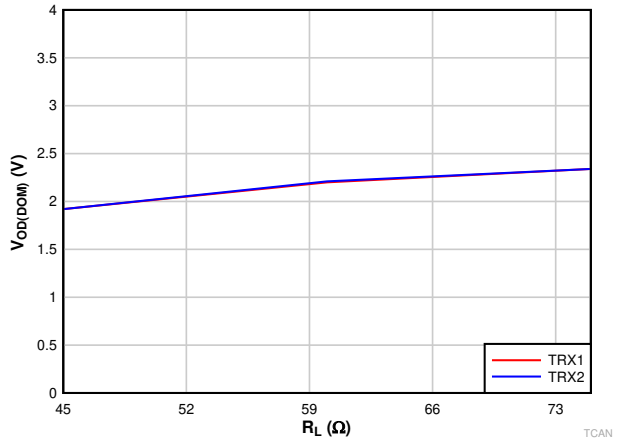

A. $V_{CC}$ = 5 V $R_L$ = 60 Ω

**Figure 6-1. $V_{OD(DOM)}$ vs Temperature Transceiver 1 and Transceiver 2**



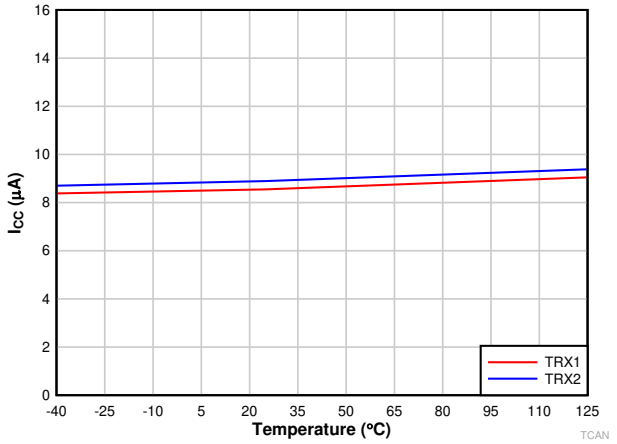

A. Temp = 25°C $R_L$ = 60 Ω

**Figure 6-2. $V_{OD(DOM)}$ vs $V_{CC}$ Transceiver 1 and Transceiver 2**




A. $V_{CC}$ = 5 V Temp = 25°C

**Figure 6-3. $V_{OD(DOM)}$ vs Load Transceiver 1 and Transceiver 2**




A. $V_{CC}$ = 5 V $R_L$ = 60 Ω

**Figure 6-4. $I_{CC}$ Standby vs Temperature Transceiver 1 and Transceiver 2**

# 7 Parameter Measurement Information

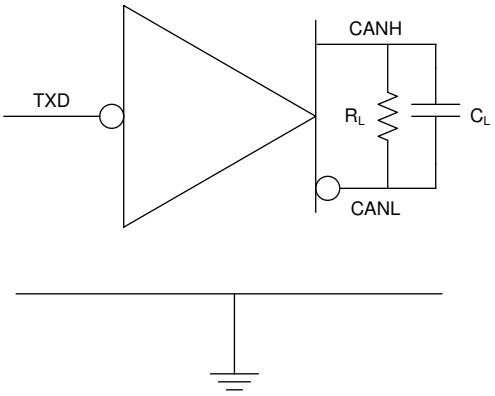



**Figure 7-1. $I_{CC}$ Test Circuit**

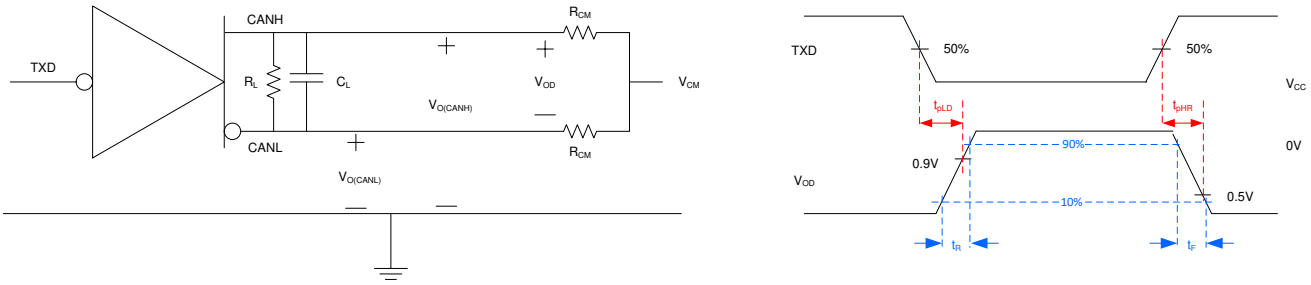



**Figure 7-2. Driver Test Circuit and Measurement**

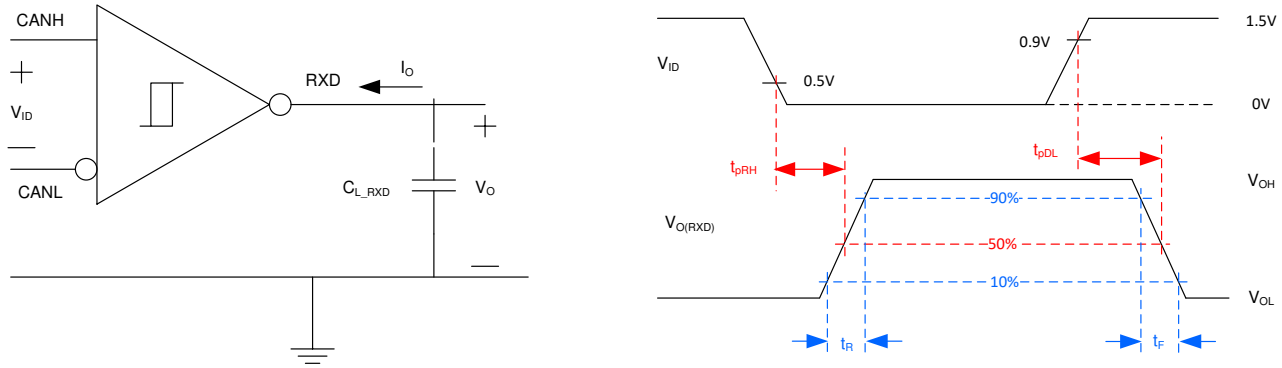



**Figure 7-3. Receiver Test Circuit and Measurement**

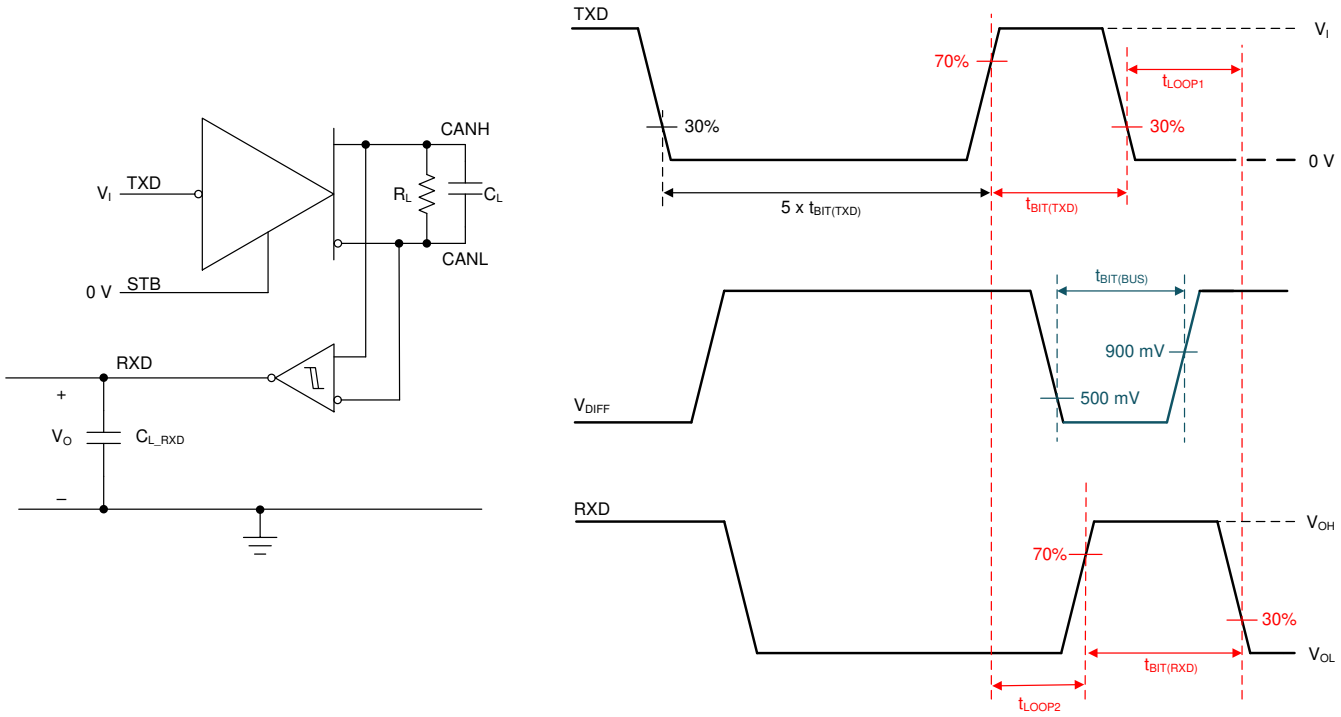



**Figure 7-4. Transmitter and Receiver Timing Test Circuit and Measurement**

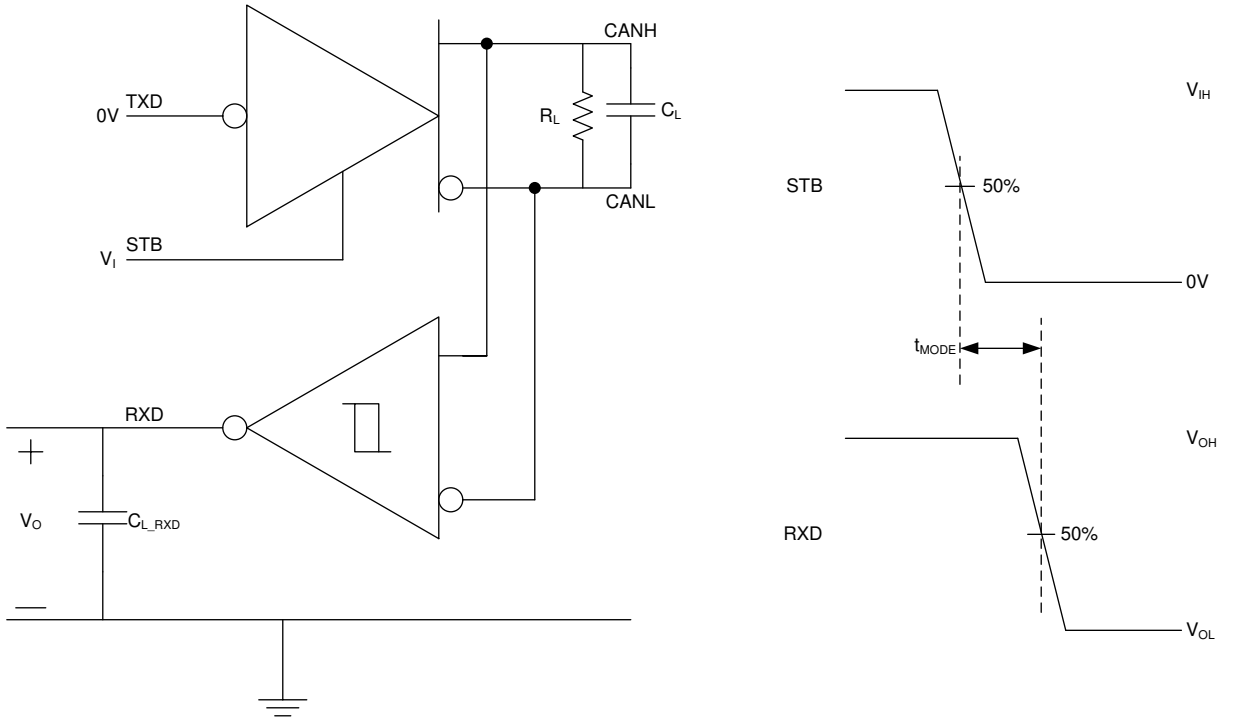



**Figure 7-5. $t_{MODE}$ Test Circuit and Measurement**

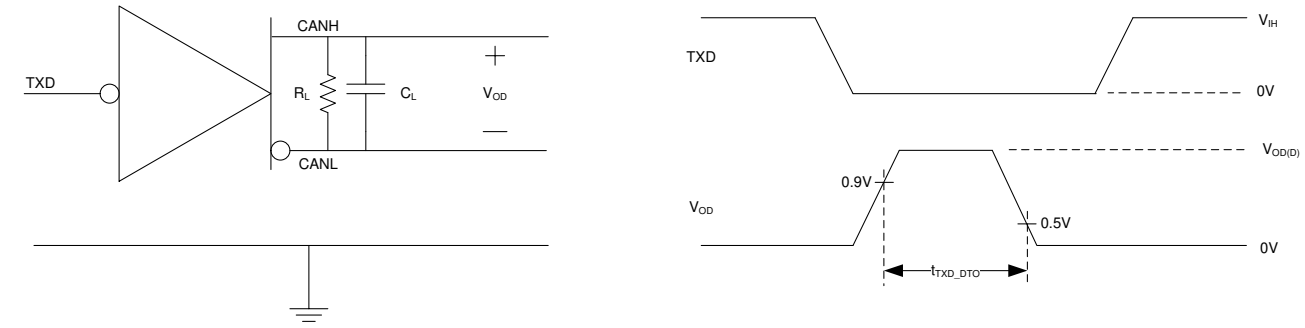



**Figure 7-6. TXD Dominant Timeout Test Circuit and Measurement**

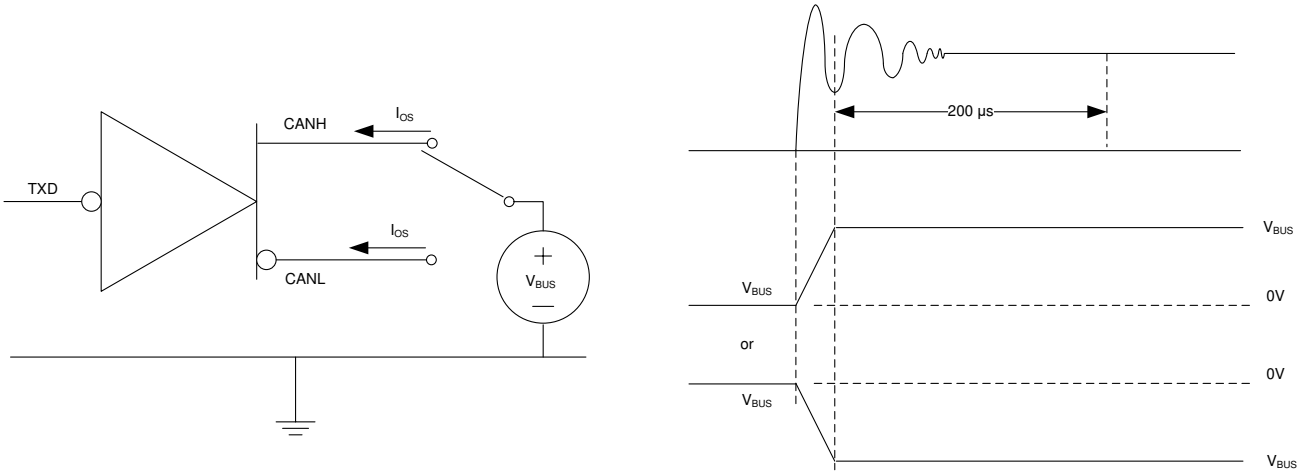



**Figure 7-7. Driver Short-Circuit Current Test and Measurement**

# 8 Detailed Description

## 8.1 Overview

The TCAN1046A-Q1 meets or exceeds the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2016 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8 Mbps.

The TCAN1046A-Q1 supports the following CAN standards:

- CAN transceiver physical layer standards:
  - ISO 11898-2:2016 High speed medium access unit
  - ISO 11898-5:2007 High speed medium access unit with low-power mode
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125 kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 2 Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 5 Mbps
- EMC requirements:
  - IEC 62228-3 EMC evaluation of transceivers - CAN transceivers
  - VeLIO (Vehicle LAN Interoperability and Optimization) CAN and CAN-FD Transceiver Requirements
  - SAE J2962-2 Communication Transceivers Qualification Requirements – CAN
- Conformance test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

## 8.2 Functional Block Diagram

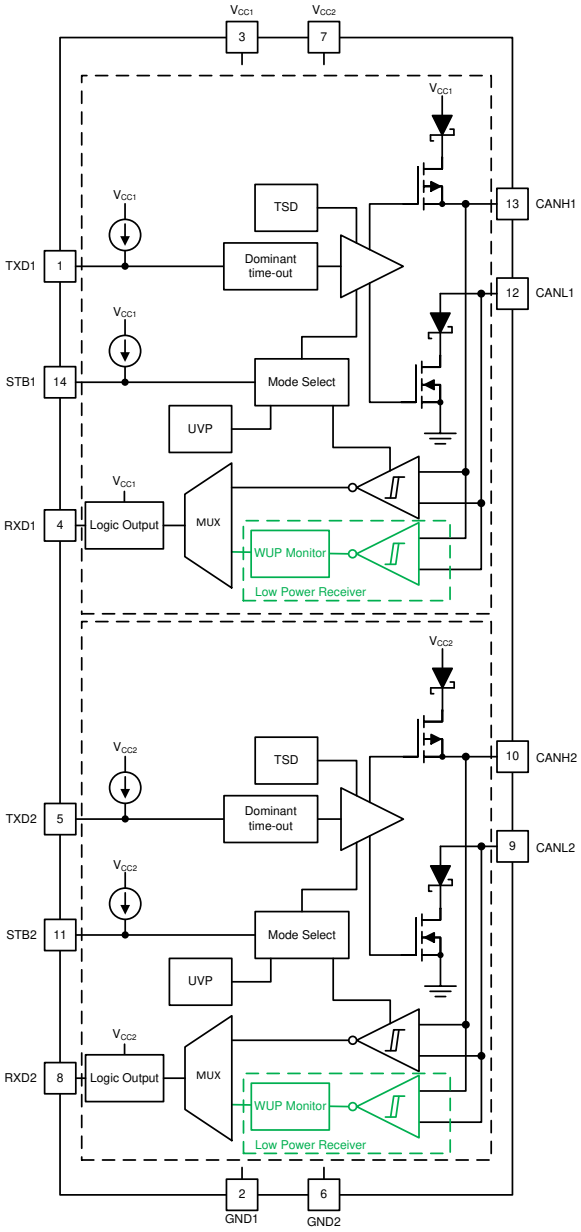



**Figure 8-1. Block Diagram**

## 8.3 Feature Description

### 8.3.1 Pin Description

#### *8.3.1.1 TXD1 and TXD2*

TXD1 and TXD2 are the logic-level signals, referenced to $V_{CC1}$/GND1 domain and $V_{CC2}$/GND2 domain respectively, from a CAN controller to the device.

#### *8.3.1.2 GND1 and GND2*

GND1 and GND2 are ground pins of the two channels integrated within the transceiver, both must be connected to the PCB ground.

#### *8.3.1.3 $V_{CC1}$ and $V_{CC2}$*

$V_{CC1}$ and $V_{CC2}$ provide the 5-V nominal power supply input to their respective CAN transceiver.

#### *8.3.1.4 RXD1 and RXD2*

RXD1 and RXD2 are the logic-level output signals from the TCAN1046A-Q1 to a CAN controller.

#### *8.3.1.5 CANH1, CANL1, CANH2, and CANL1*

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

#### *8.3.1.6 STB1 and STB2 (Standby)*

The STB1 and STB2 are input pins used for mode control of the TCAN1046A-Q1. STB1 and STB2 can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation than the STB pins can be tied directly to GND.

### 8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 8-2 and Figure 8-3.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD1, TXD2, RXD1 and RXD2 pins. A recessive bus state occurs when the bus is biased to $V_{CC}$/2 via the high-resistance internal input resistors ($R_{IN}$) of the receiver and corresponds to a logic high on the TXD1, TXD2, RXD1 and RXD2 pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN1046A-Q1 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 8-2 and Figure 8-3.

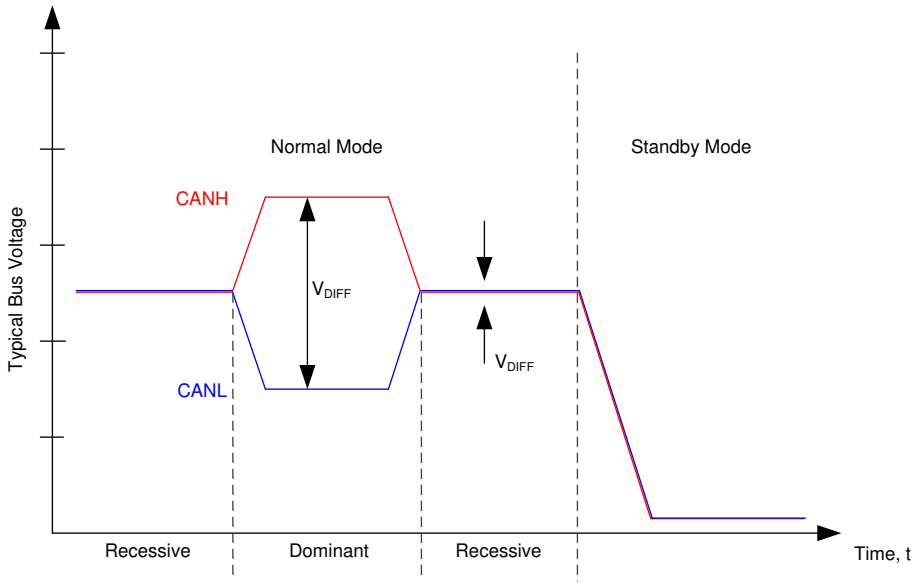
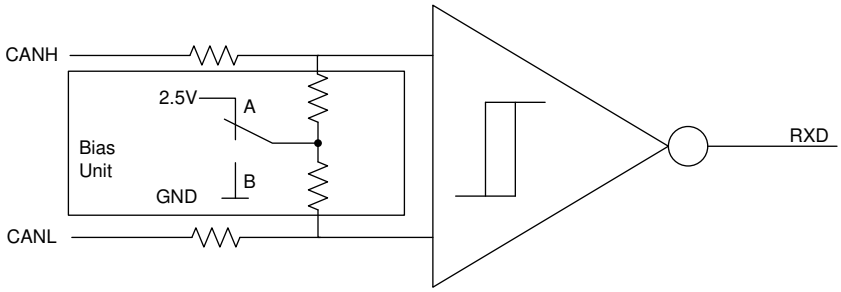



**Figure 8-2. Bus States**




A. Normal Mode
B. Standby Mode

**Figure 8-3. Simplified Recessive Common Mode Bias Unit and Receiver**

### 8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period $t_{TXD\_DTO}$. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, $t_{TXD\_DTO}$, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

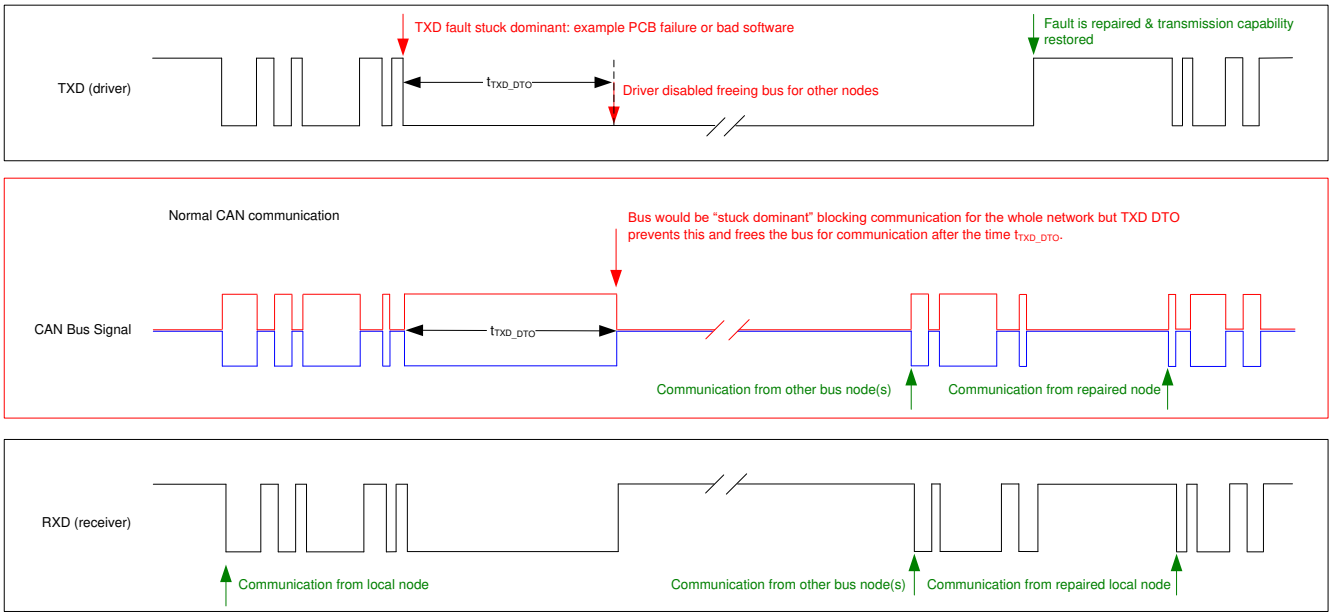



**Figure 8-4. Example Timing Diagram for TXD Dominant Timeout**

### 8.3.4 CAN Bus Short-Circuit Current Limiting

The TCAN1046A-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common-mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. The protocol allows for a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC\_Bits} \times I_{OS(SS)\_REC}) + (\%\ \text{DOM\_Bits} \times I_{OS(SS)\_DOM})] + [\%\ \text{Receive} \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers $V_{CC}$ supply.

### 8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1046A-Q1 exceeds the thermal shutdown threshold, $T_{TSD}$, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below $T_{TSD}$. The CAN bus pins are biased to $V_{CC}/2$

during a TSD fault and the receiver to RXD path remains operational. The TCAN1046A-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

### 8.3.6 Undervoltage Lockout

The supply pin, $V_{CC}$, has undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

**Table 8-1. Undervoltage Lockout**

| $V_{CC}$ | DEVICE STATE | BUS | RXD PIN |
|---|---|---|---|
| > $UV_{VCC}$ | Normal | Per TXD | Mirrors bus |
| < $UV_{VCC}$ | Protected | High impedance (1) | High impedance |

(1) $V_{CC}$ = GND, see $I_{LKG(OFF)}$

Once the undervoltage condition is cleared and $t_{MODE}$ has expired the TCAN1046A-Q1 transitions to normal mode and the host controller can send and receive CAN traffic again.

### 8.3.7 Unpowered Device

The TCAN1046A-Q1 is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

### 8.3.8 Floating pins

The TCAN1046A-Q1 has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used, an adequate external pull-up resistor must be chosen. This pull-up resistor allows the TXD output of the CAN controller to maintain acceptable bit time to the input of the CAN transceiver. See Table 8-2 for details on pin bias conditions.

**Table 8-2. Pin Bias**

| Pin | Pull-up or Pull-down | Comment |
|---|---|---|
| TXD1 and TXD2 | Pull-up | Weakly biases TXD1 and TXD2 towards recessive to prevent bus blockage or TXD DTO triggering |
| STB1 and STB2 | Pull-up | Weakly biases STB1 and STB2 towards low-power standby mode to prevent excessive system power |

## 8.4 Device Functional Modes

### 8.4.1 Operating Modes

The TCAN1046A-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB1 and STB2 pins on the device.

**Table 8-3. Operating Modes**

| STB | Device Mode | Driver | Receiver | RXD Pin |
|---|---|---|---|---|
| High | Low current standby mode with bus wake-up | Disabled | Low-power receiver and bus monitor enable | High (recessive) until valid WUP is received |
| Low | Normal Mode | Enabled | Enabled | Mirrors bus state |

### 8.4.2 Normal Mode

This is the normal operating mode of the TCAN1046A-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD1 and TXD2 inputs

to a differential output on the CANH1, CANL1 and CANH2, CANL2 bus pins. The receiver is translating the differential signal from CANH1, CANL1 and CANH2, CANL2 to a digital output on the RXD1 and RXD2 outputs.

### 8.4.3 Standby Mode

This is the low-power mode of the TCAN1046A-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD1 or RXD2 depending on the channel which received the WUP as shown in Figure 8-5. The local CAN protocol controller should monitor RXD1 and RXD2 for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB1 and STB2 pin low. The CAN bus pins are weakly pulled to GND in this mode; see Figure 8-2 and Figure 8-3.

#### *8.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode*

The TCAN1046A-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN1046A-Q1.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the $t_{WK\_FILTER}$ time. Due to variability in $t_{WK\_FILTER}$ the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 8-5 for the timing diagram of the wake-up pattern.

The pattern and $t_{WK\_FILTER}$ time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The $t_{WK\_FILTER}$ timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back-to-back bit times at 1 Mbps triggers the filter in either bus state. Any CAN frame at 500 kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 8-5 for the timing diagram of the wake-up pattern with wake timeout feature.

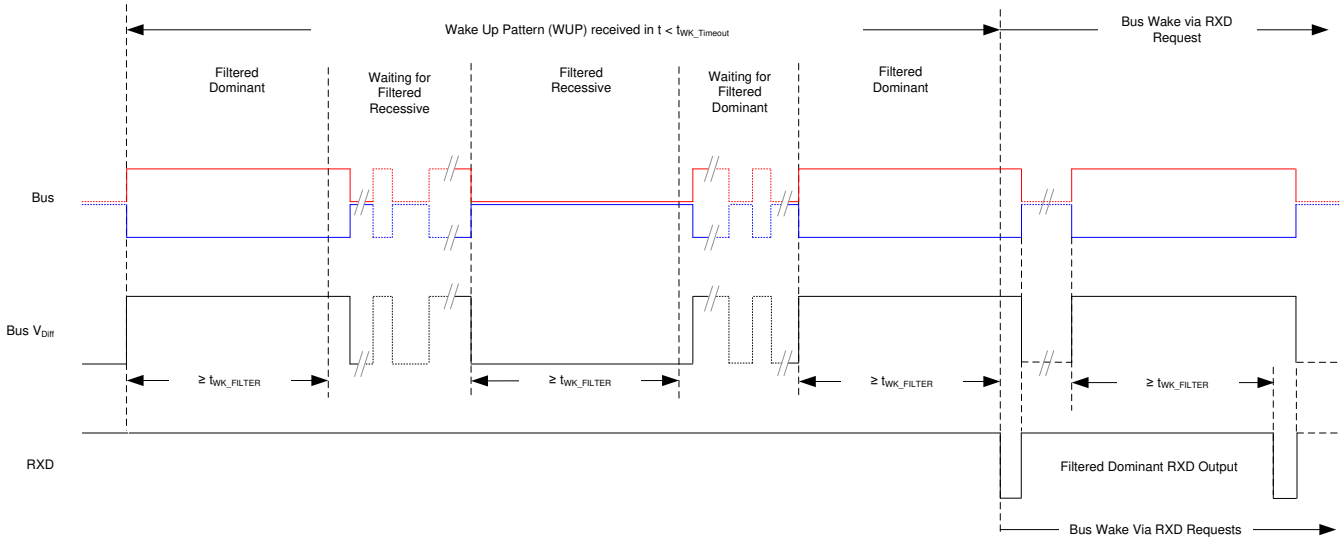



**Figure 8-5. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$**

### 8.4.4 Driver and Receiver Function

The digital logic input and output levels for the TCAN1046A-Q1 are CMOS levels with respect to $V_{CC}$ and are compatible with protocol controllers having 5-V I/O levels.

**Table 8-4. Driver Function Table**

| Device Mode | TXD Input | Bus Outputs | | Driven Bus State(2) |
|---|---|---|---|---|
| | | CANH | CANL | |
| Normal | Low | High | Low | Dominant |
| | High or open | High impedance | High impedance | Biased recessive |
| Standby | X(1) | High impedance | High impedance | Weak pull-down to ground |

(1) X = irrelevant
(2) For bus state and bias see Figure 8-2 and Figure 8-3

**Table 8-5. Receiver Function Table Normal and Standby Mode**

| Device Mode | CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$ | Bus State | RXD Pin |
|---|---|---|---|
| Normal | $V_{ID} \geq 0.9$ V | Dominant | Low |
| | 0.5 V < $V_{ID}$ < 0.9 V | Undefined | Undefined |
| | $V_{ID} \leq 0.5$ V | Recessive | High |
| Standby | $V_{ID} \geq 1.15$ V | Dominant | High<br>Low if a remote wake event occurred |
| | 0.4 V < $V_{ID}$ < 1.15 V | Undefined | |
| | $V_{ID} \leq 0.4$ V | Recessive | |
| Any | Open ($V_{ID} \approx 0$ V) | Open | High |

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

## 9.2 Typical Application

The TCAN1046A-Q1 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. Figure 9-1 shows a typical configuration for 5 V controller applications. The bus termination is shown for illustrative purposes.

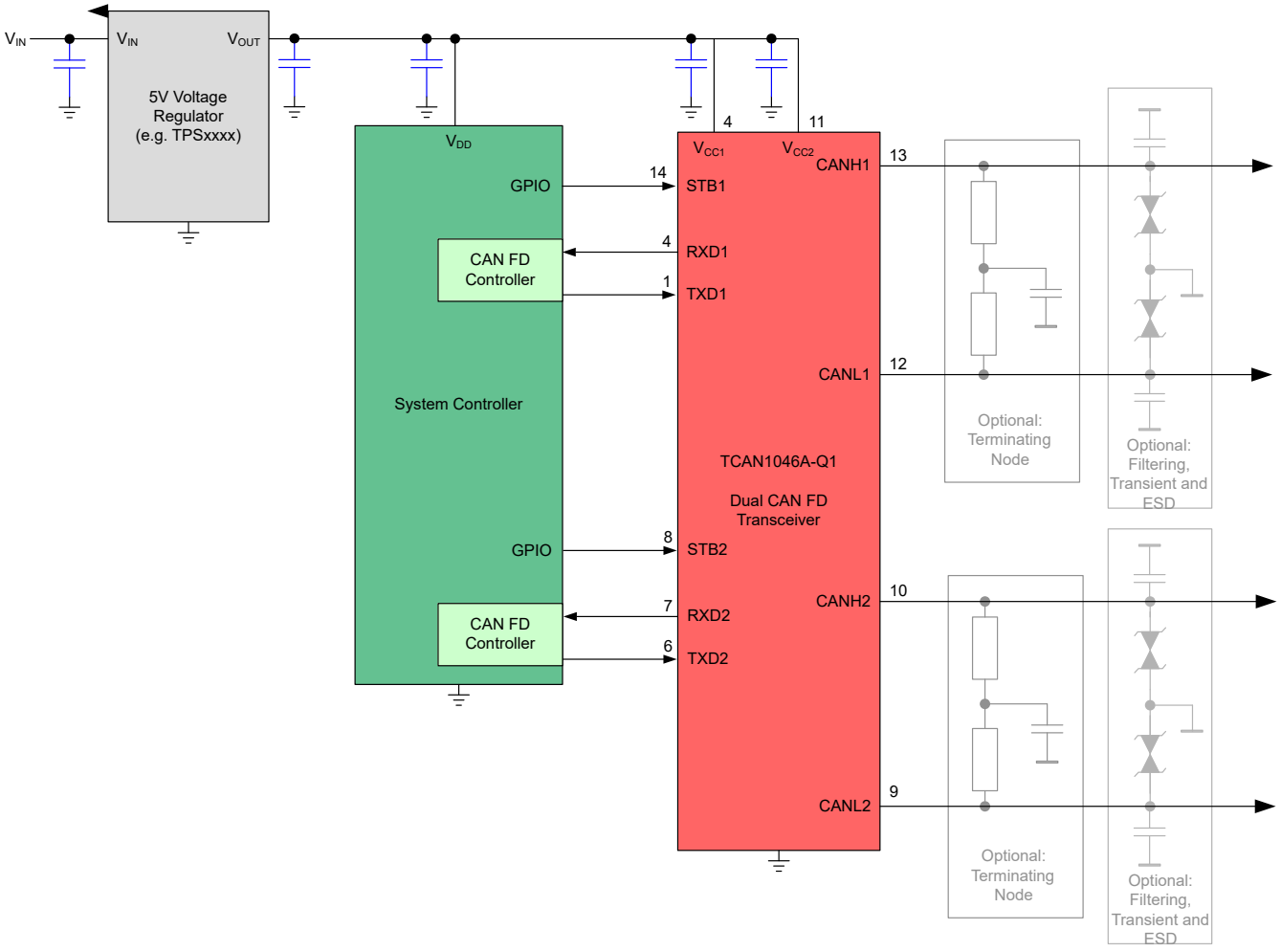



**Figure 9-1. Transceiver Application Using 5 V I/O Connections**

### 9.2.1 Design Requirements

#### *9.2.1.1 CAN Termination*

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used,

see Figure 9-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

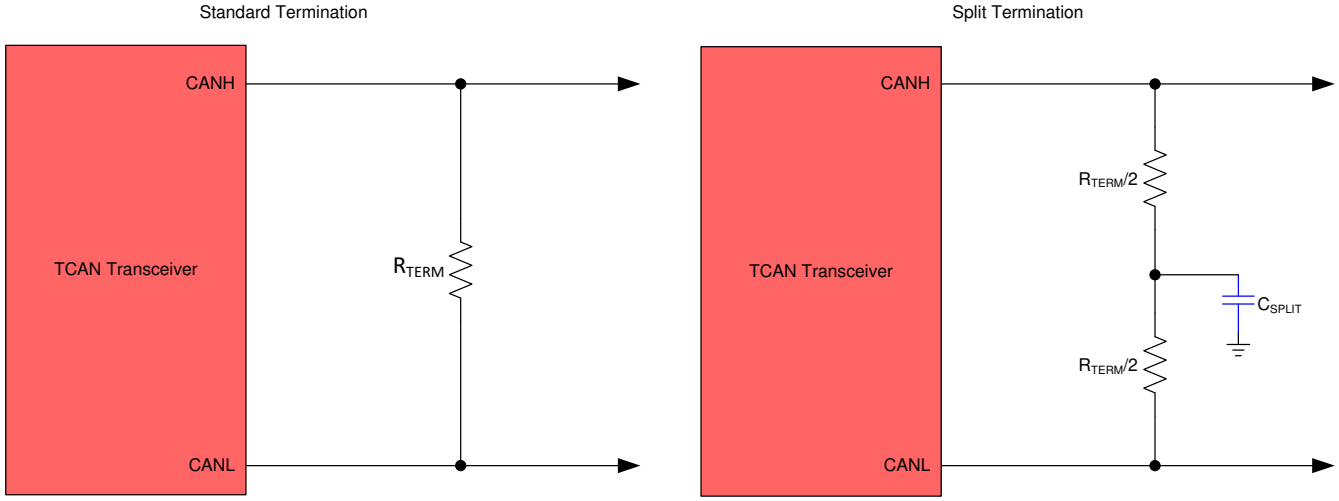



**Figure 9-2. CAN Bus Termination Concepts**

### 9.2.2 Detailed Design Procedures

#### *9.2.2.1 Bus Loading, Length and Number of Nodes*

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1046A-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system-level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems-level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1046A-Q1 is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance of the TCAN1046A-Q1 is a minimum of 40 kΩ. If 100 TCAN1046A-Q1 transceivers are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately 52 Ω. Therefore, the TCAN1046A-Q1 theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity; thus, a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility. the CAN network system must be design for robust network operation.

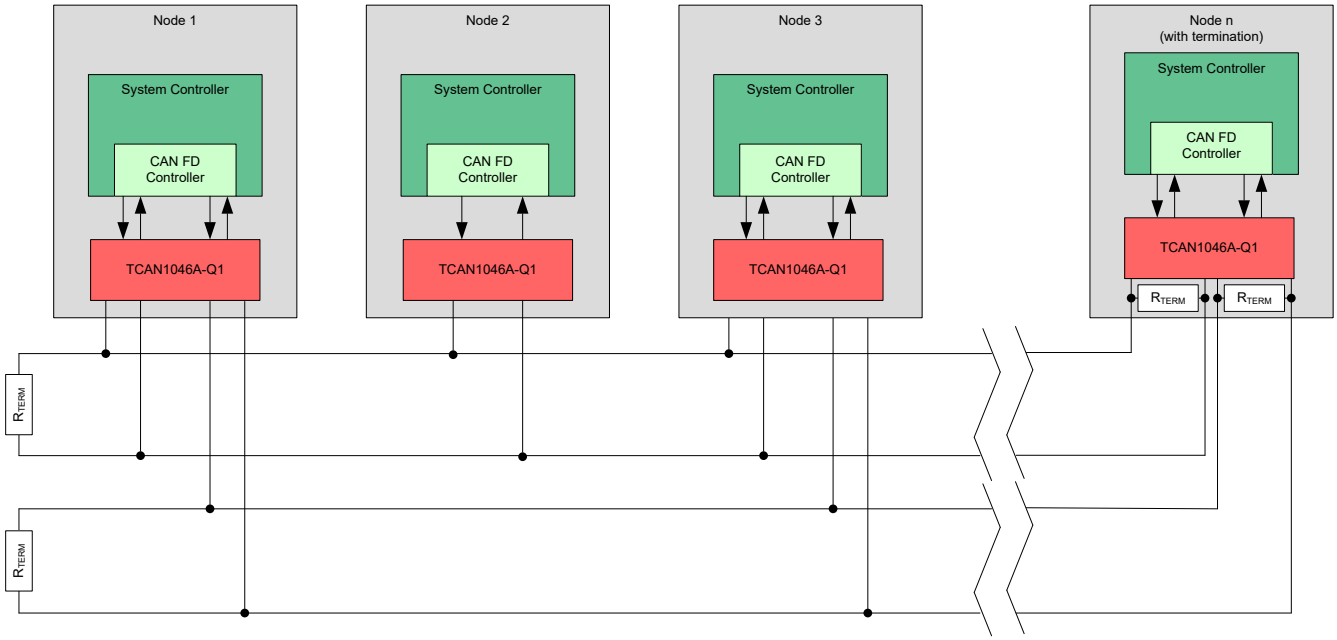
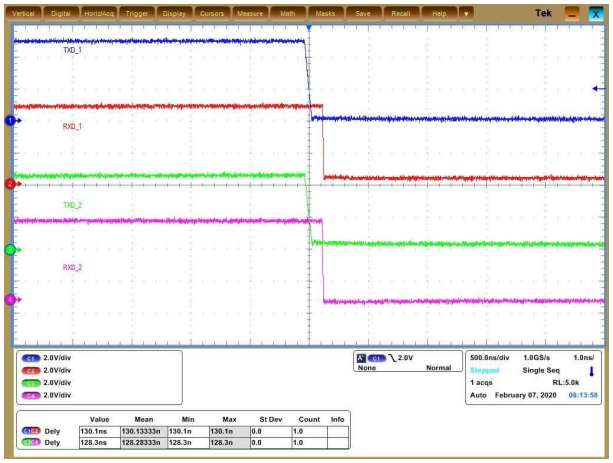


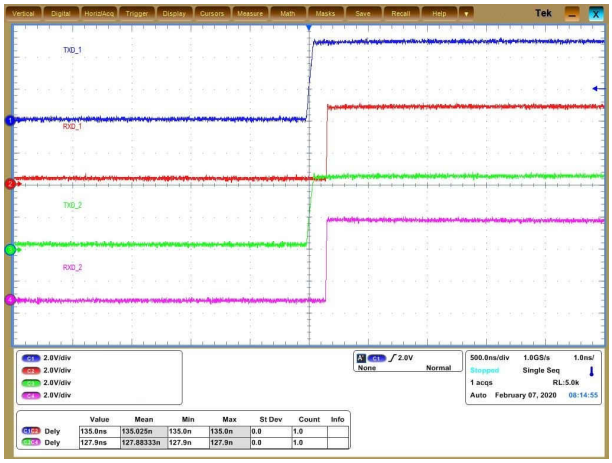

**Figure 9-3. Typical CAN Bus**

### 9.2.3 Application Curves



$V_{CC}$ = 5 V $R_L$ = 60 Ω

**Figure 9-4. $t_{PROP(LOOP1)}$ Transceiver 1 and Transceiver 2**



$V_{CC}$ = 5 V $R_L$ = 60 Ω

**Figure 9-5. $t_{PROP(LOOP2)}$ Transceiver 1 and Transceiver 2**

## 10 Power Supply Recommendations

The TCAN1046A-Q1 dual transceiver is designed to operate with a main $V_{CC1}$ and $V_{CC2}$ input voltage supply range between 4.5 V and 5.5 V. The $V_{CC}$ supply inputs must be well regulated. A decoupling capacitor, typically 100 nF, should be placed near the CAN transceiver's main $V_{CC1}$ and $V_{CC2}$ supply pins.

# 11 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high-frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

## 11.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows optional transient voltage suppression (TVS) diodes, D1 and D2, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4, C5, C6 and C8.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins $V_{CC1}$ and $V_{CC2}$ of the transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

**Note**

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R7 and R8 for channel 1, R9 and R10 for channel 2 with the center or split tap of the termination connected to ground via capacitor C3 and C7. Split termination provides common-mode filtering for the bus. See CAN Termination, CAN Bus Short Circuit Current Limiting, and Equation 2 for information on termination concepts and power ratings needed for the termination resistor(s).

## 11.2 Layout Example

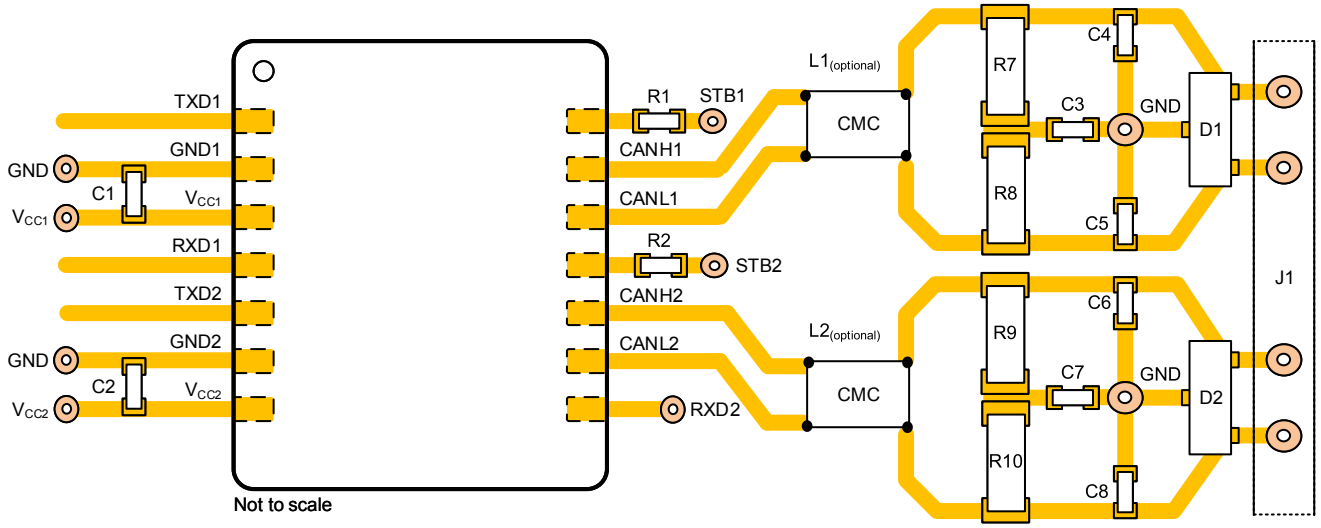



**Figure 11-1. Layout Example**

# 12 Device and Documentation Support

## 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TCAN1046ADMTRQ1 | Active | Production | VSON (DMT) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1046A |
| TCAN1046ADMTRQ1.A | Active | Production | VSON (DMT) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1046A |
| TCAN1046ADMTRQ1.B | Active | Production | VSON (DMT) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| TCAN1046ADRQ1 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 1046A |
| TCAN1046ADRQ1.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 1046A |
| TCAN1046ADRQ1.B | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

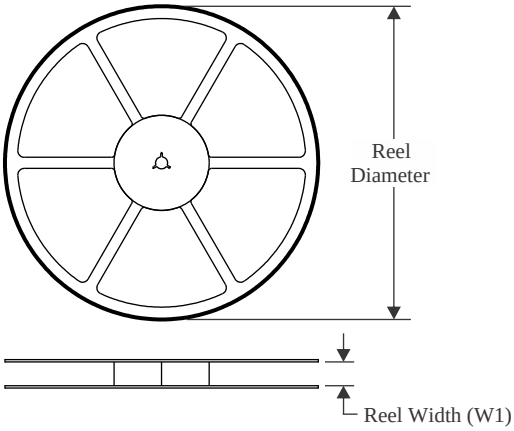
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

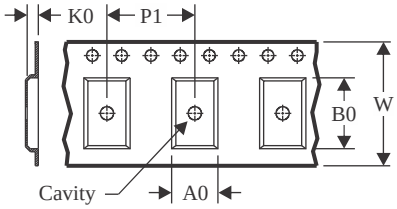
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

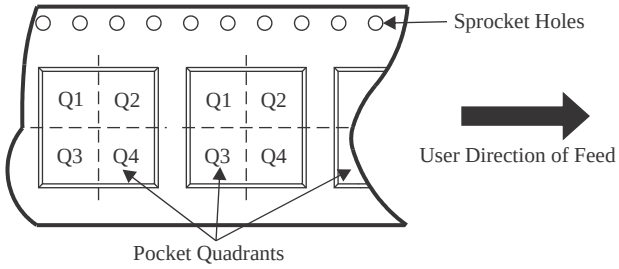



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

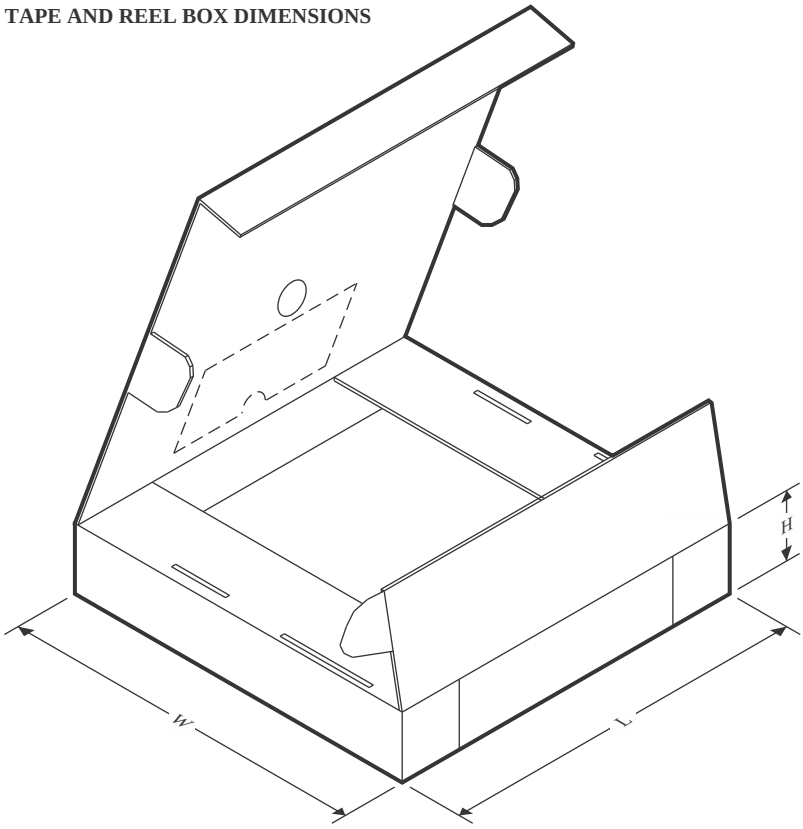
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

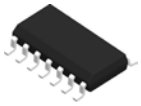
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TCAN1046ADMTRQ1 | VSON | DMT | 14 | 3000 | 330.0 | 12.4 | 3.3 | 4.8 | 1.2 | 8.0 | 12.0 | Q1 |
| TCAN1046ADRQ1 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TCAN1046ADMTRQ1 | VSON | DMT | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| TCAN1046ADRQ1 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |

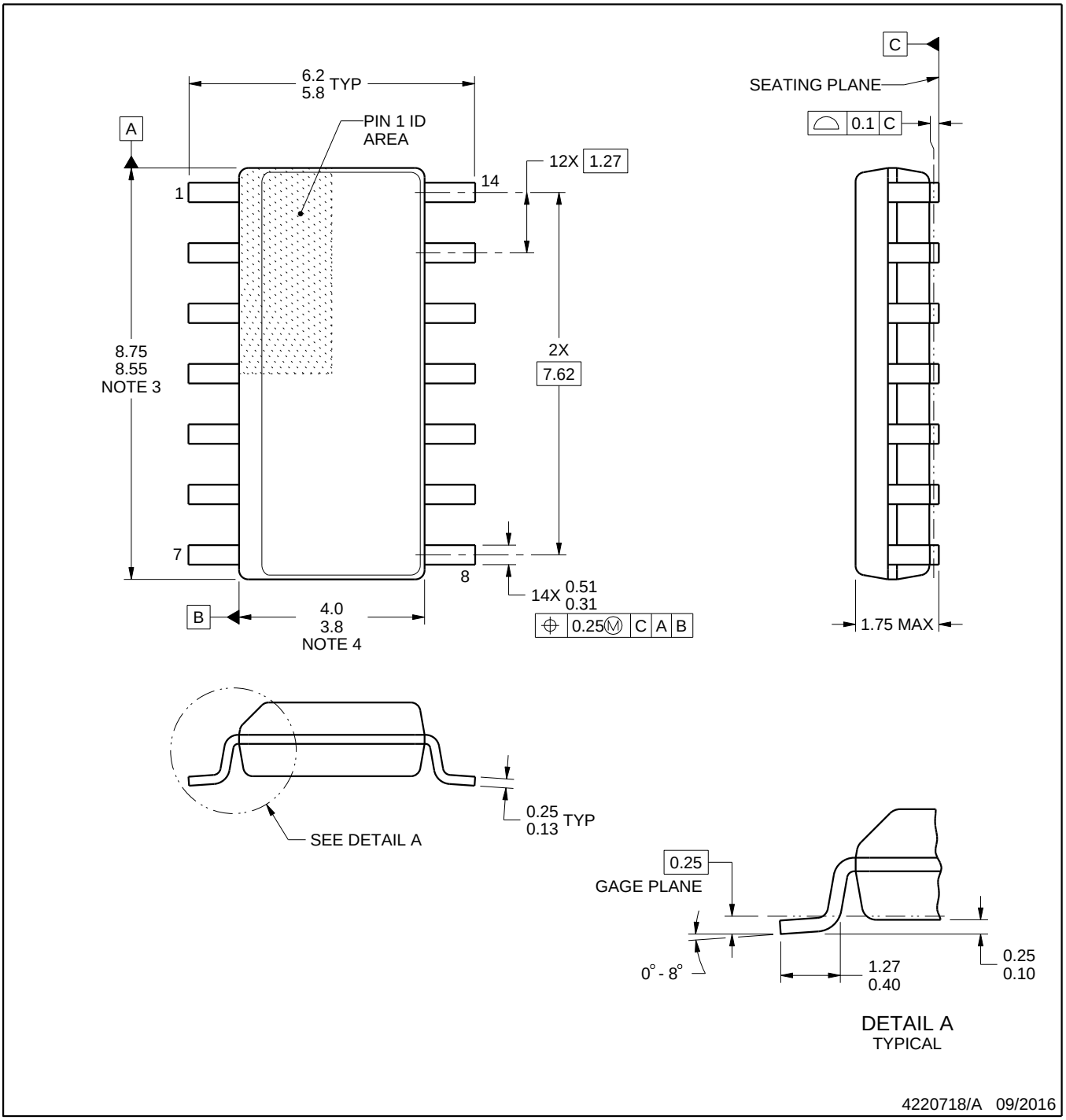


# PACKAGE OUTLINE

## D0014A

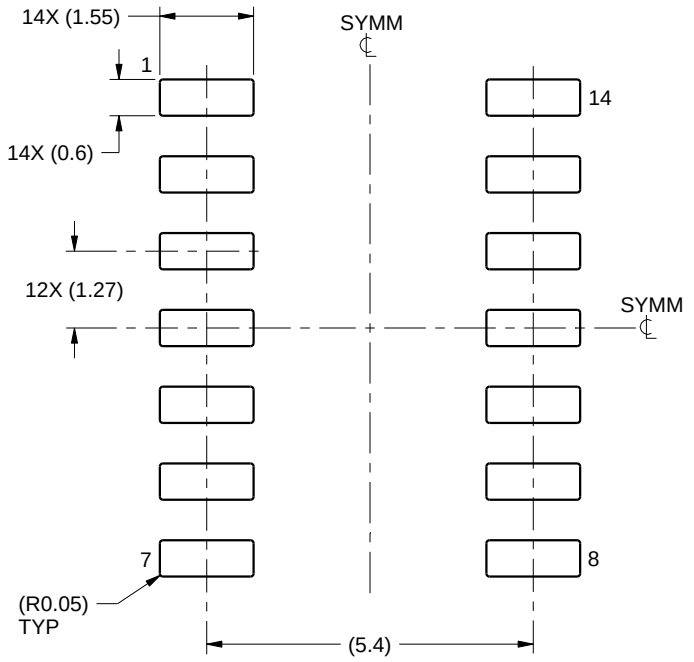
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

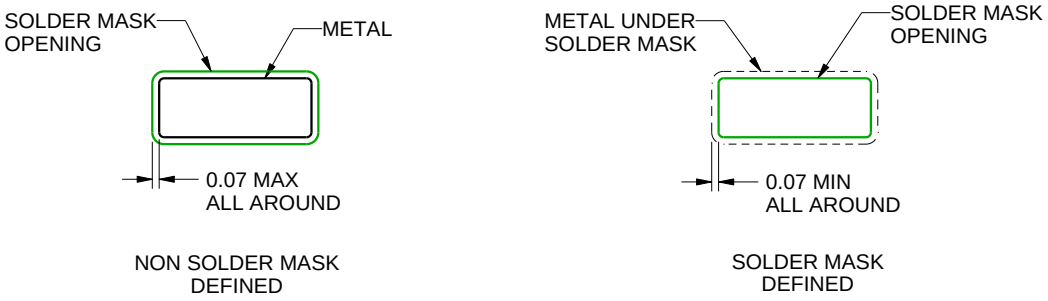



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

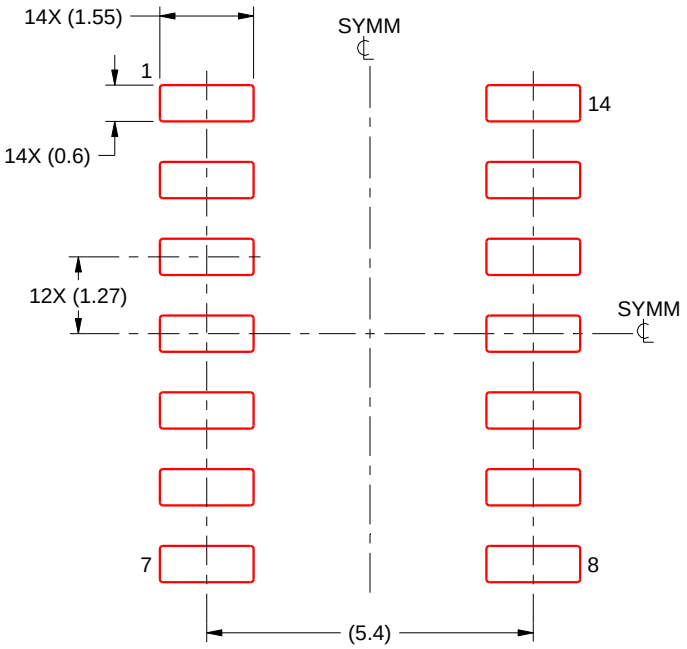
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

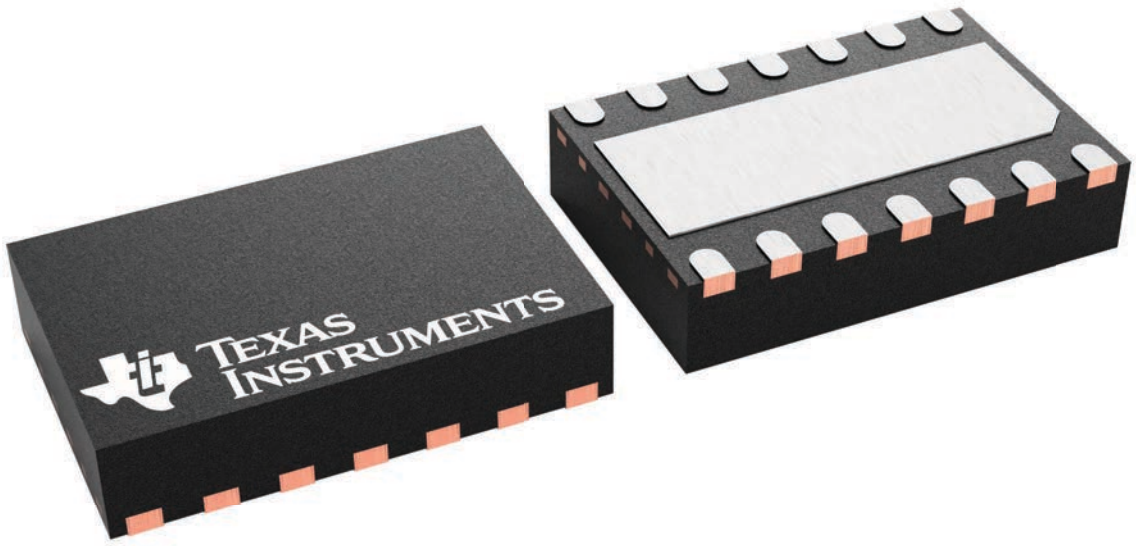
## DMT 14

## VSON - 0.9 mm max height

**3 x 4.5, 0.65 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



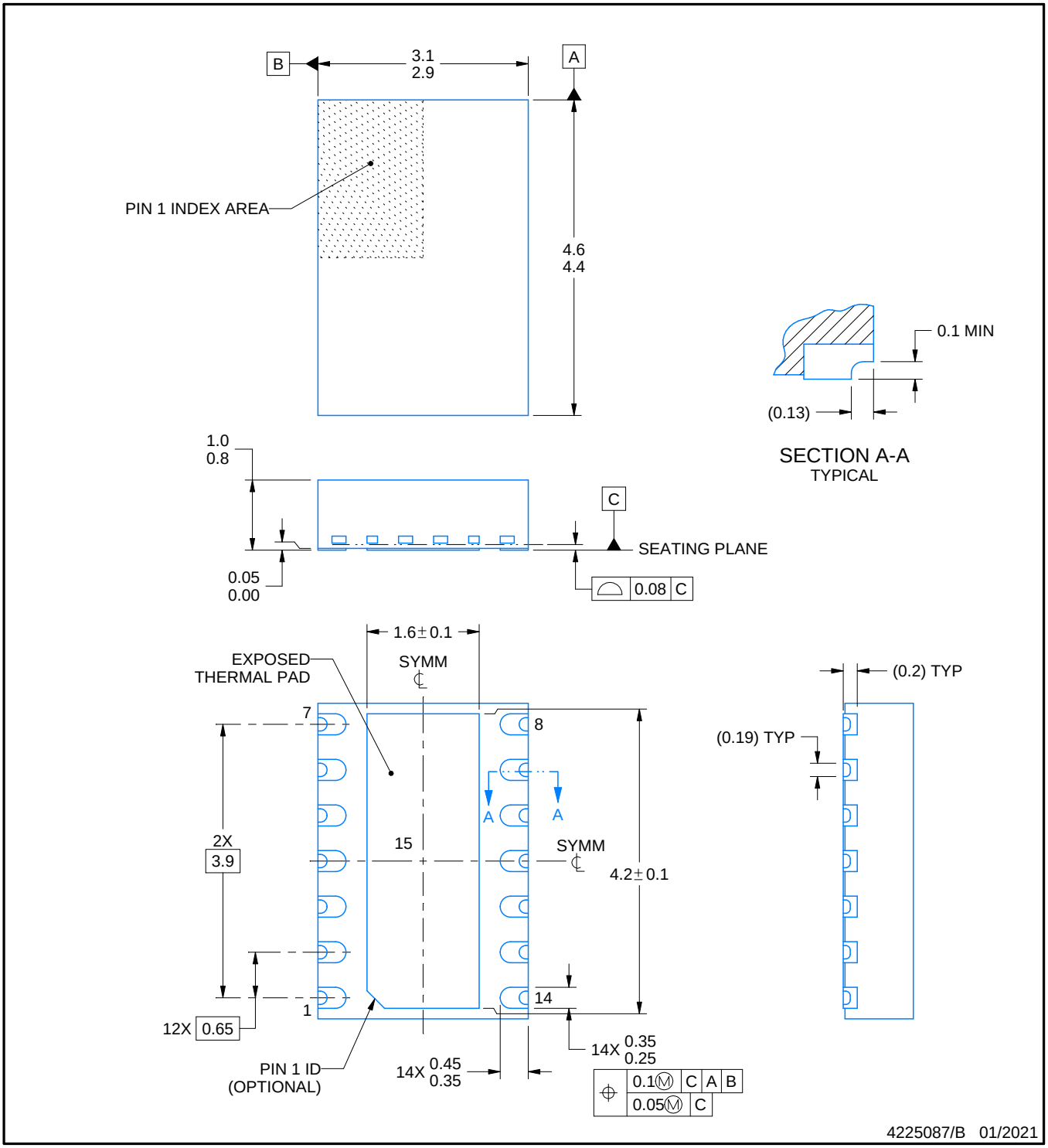

4225088/A

# DMT0014B

# PACKAGE OUTLINE

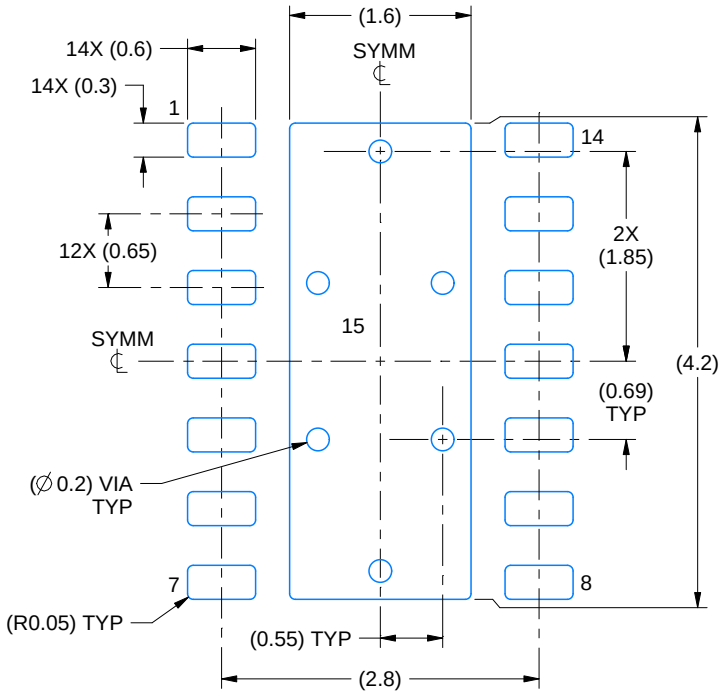
## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

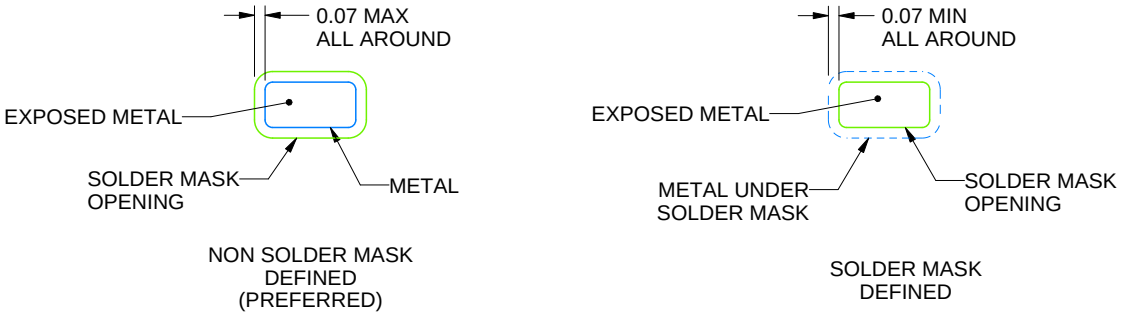



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

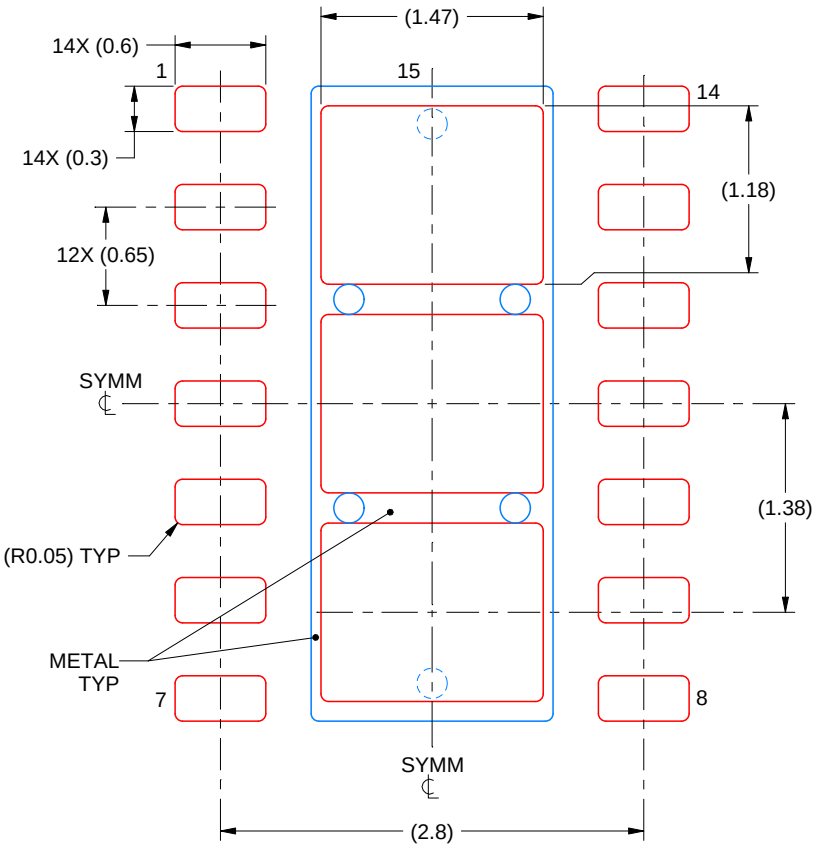



SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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