TCA9539A-Q1 Automotive Low Voltage 16-Bit I²C and SMBus Low-Power I/O Expander with Interrupt Output, Reset Pin, and Configuration Registers

1 Features

- AEC-Q100 Qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- I²C to parallel port expander
- Open-drain active-low interrupt output
- Active-low reset input
- 5V tolerant input and output ports
- Compatible with most microcontrollers
- 400kHz Fast I²C bus
- Polarity inversion register
- Internal power-on reset
- No glitch on power up
- Address by two hardware address pins for use of up to four devices
- Latched outputs for directly driving LEDs
- Latch-up performance exceeds 100mA Per JESD 78, class II
- ESD protection exceeds JESD 22
  - 2000V Human-body model (A114-A)
  - 1000V Charged-device model (C101)

2 Applications

- Automotive infotainment, advanced driver assistance systems (ADAS), automotive body electronics, HEV, EV and powertrain
- Industrial automation, factory automation, building automation, test and measurement, EPOS
- I²C GPIO expansion

3 Description

The TCA9539A-Q1 is a 24-pin device that provides 16 bits of general purpose parallel input and output (I/O) expansion for the two-line bidirectional I²C bus (or SMBus protocol). The device can operate with a power supply voltage (V_{CC}) range from 1.65V to 5.5V. The device supports 100kHz (I²C Standard mode) and 400kHz (I²C Fast mode) clock frequencies. I/O expanders such as the device provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and other similar devices.

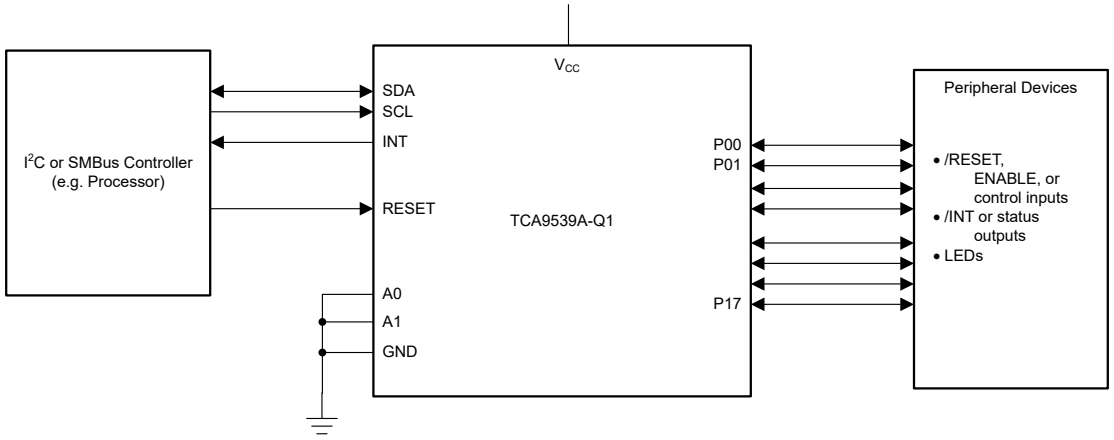
The features of the device include an interrupt that is generated on the $\overline{INT}$ pin when an input port changes state. The A0 and A1 hardware selectable address pins allow up to four devices on the same I²C bus. The device can be reset to its default state by cycling the power supply and causing a power-on reset. Also, the device has a hardware $\overline{RESET}$ pin that can be used to reset the device to its default state.

The TCA9539A-Q1 I²C I/O expander is qualified for automotive applications.

Package Information

PART NUMBER	PACKAGE TYPE(1)	PACKAGE SIZE(2)
TCA9539A-Q1	TSSOP (24)	7.8mm × 6.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

Table of Contents

4 Pin Configuration and Functions

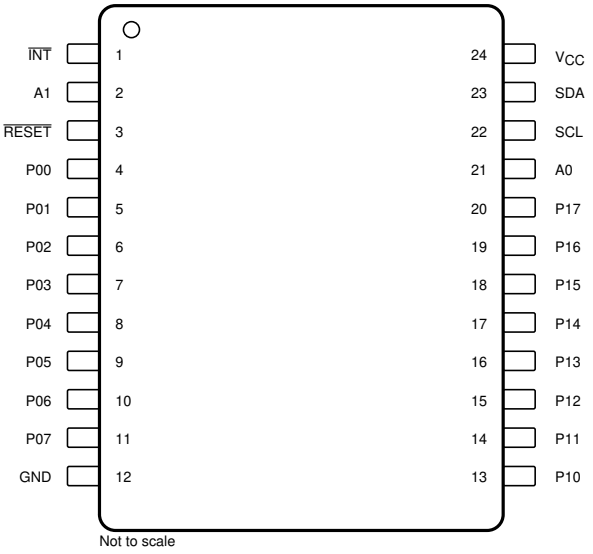


Figure 4-1. PW Package, 24-Pin TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{INT}$	O	Interrupt open-drain output. Connect to V_{CC} through a pull-up resistor
2	A1	I	Address input. Connect directly to V_{CC} or ground
3	$\overline{RESET}$	I	Active-low reset input. Connect to V_{CC} through a pull-up resistor if no active connection is used
4	P00	I/O	P-port input-output. Push-pull design structure. At power-on, P00 is configured as an input
5	P01	I/O	P-port input-output. Push-pull design structure. At power-on, P01 is configured as an input
6	P02	I/O	P-port input-output. Push-pull design structure. At power-on, P02 is configured as an input
7	P03	I/O	P-port input-output. Push-pull design structure. At power-on, P03 is configured as an input
8	P04	I/O	P-port input-output. Push-pull design structure. At power-on, P04 is configured as an input
9	P05	I/O	P-port input-output. Push-pull design structure. At power-on, P05 is configured as an input
10	P06	I/O	P-port input-output. Push-pull design structure. At power-on, P06 is configured as an input
11	P07	I/O	P-port input-output. Push-pull design structure. At power-on, P07 is configured as an input
12	GND	—	Ground
13	P10	I/O	P-port input-output. Push-pull design structure. At power-on, P10 is configured as an input
14	P11	I/O	P-port input-output. Push-pull design structure. At power-on, P11 is configured as an input
15	P12	I/O	P-port input-output. Push-pull design structure. At power-on, P12 is configured as an input
16	P13	I/O	P-port input-output. Push-pull design structure. At power-on, P13 is configured as an input
17	P14	I/O	P-port input-output. Push-pull design structure. At power-on, P14 is configured as an input
18	P15	I/O	P-port input-output. Push-pull design structure. At power-on, P15 is configured as an input
19	P16	I/O	P-port input-output. Push-pull design structure. At power-on, P16 is configured as an input
20	P17	I/O	P-port input-output. Push-pull design structure. At power-on, P17 is configured as an input
21	A0	I	Address input. Connect directly to V_{CC} or ground
22	SCL	I	Serial clock bus. Connect to V_{CC} through a pull-up resistor
23	SDA	I/O	Serial data bus. Connect to V_{CC} through a pull-up resistor
24	V_{CC}	—	Supply voltage

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6	V
V_I	Input voltage (2)		–0.5	6	V
V_O	Output voltage (2)		–0.5	6	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–20	mA
I_{IOK}	Input-output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
$T_{j(MAX)}$	Maximum junction temperature			140	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under R*ecommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			1.65	5.5	V
$V_{I/O}$	I/O ports voltage	SCL, SDA, A0, A1, $\overline{RESET}$, $\overline{INT}$ (1)		–0.5	5.5	V
		For P00–P07, P10–P17 configured as outputs		–0.5	5.5	V
		For P00–P07, P10–P17 configured as inputs(1)		–0.5	5.5	V
V_{IH}	High-level input voltage	SCL, SDA, A0, A1, $\overline{RESET}$, P07–P00, P10–P17		0.7 × V_{CC}		V
V_{IL}	Low-level input voltage	SCL, SDA, A0, A1, $\overline{RESET}$, P07–P00, P10–P17			0.3 × V_{CC}	V
I_{OH}	High-level output current	P00–P07, P10–P17			–8	mA
I_{OL}	Low-level output current	P00–P07, P10–P17	T_j ≤ 132°C		4.5	mA
I_{OL}	Low-level output current	$\overline{INT}$, SDA	T_j ≤ 132°C		6	mA
P_d	Power dissipation (2)		T_j ≤ 132°C		65	mW
T_J	Junction temperatture	Junction temperature	Junction temperature	–40	132	°C
T_{PCB}	PCB temperature	Measured 1mm away from the device	P_d ≤ 65 mW	–40	128	°C
T_A	Operating free-air temperature			–40	125	°C

(1) For voltages applied above V_{CC}, an increase in I_{CC} results.

(2) See the *Section 8.2.2.1* section on how to calculate the junction temperature.

5.4 Thermal Information

THERMAL METRIC(1)		TCA9539A-Q1 PW (TSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.3	°C/W

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics*.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP (1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18mA	1.65V to 5.5V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	V_I = V_{CC} or GND	1.65V to 5.5V		1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	V_I = V_{CC} or GND	1.65V to 5.5V	0.75	1		V
V_{OH}	P-port high-level output voltage (2)	I_{OH} = –8mA	1.65V	1.2			V
			2.3V	1.8			
			3V	2.6			
			3.6V	3.3			
			5.5V	4.7			
		I_{OH} = –10mA	1.65V	1			
			2.3V	1.7			
			3V	2.5			
			3.6V	3.2			
			5.5V	4.5			
I_{OL}	SDA	V_{OL} = 0.4V	1.65V to 5.5V	3			mA
	P port (3)	V_{OL} = 0.5V		8			
		V_{OL} = 0.7V		10			
	$\overline{INT}$	V_{OL} = 0.4V		3			

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP (1)	MAX	UNIT
I_I	SCL, SDA	$V_I = V_{CC}$ or GND		1.65V to 5.5V			±1	μA
	A0, A1, $\overline{RESET}$						±1	
I_{IH}	P port	$V_I = V_{CC}$		1.65V to 5.5V			1	
I_{IL}	P port	V_I = GND		1.65V to 5.5V			–1	
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 400kHz, no load		5.5V		22	52	
				3.6V		10	30	
				2.7V		5	19	
				1.95V		4	11	
	Standby mode	I_O = 0, I/O = inputs, f_{SCL} = 0kHz, no load	$V_I = V_{CC}$	5.5V		1.5	10	
				3.6V		1.1	5	
				2.7V		1	4.5	
				1.95V		0.4	3.5	
			V_I = GND	5.5V		1.5	20	
				3.6V		1.1	13	
				2.7V		1	9.5	
				1.95V		0.4	6.5	
C_i	SCL	$V_I = V_{CC}$ or GND		1.65V to 5.5V		3	8	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND		1.65V to 5.5V		3	9.5	pF
	P port					3.7	9.5	

(1) All typical values are at nominal supply voltage (1.8V, 2.5V, 3.3V, or 5.0V, V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to the maximum allowed I_{OL}, and each octal (P07–P00 and P17–P10) must be limited to keep at T_j ≤ 135°C. See the *Section 5.3* table for more information.
(3) The total current sourced by all I/Os must be limited to keep T_j ≤ 135°C. See the *Section 5.3* table for more information.

5.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

			MIN	MAX	UNIT
I²C BUS—STANDARD MODE					
f_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		μs
t_{scl}	I²C clock low time		4.7		μs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10pF to 400pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7		μs
t_{sts}	I²C start or repeated start condition setup		4.7		μs
t_{sth}	I²C start or repeated start condition hold		4		μs
t_{sps}	I²C stop condition setup		4		μs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	μs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	μs

5.6 I²C Interface Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

			MIN	MAX	UNIT
C_b	I²C bus capacitive load			400	pF
I²C BUS—FAST MODE					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns
t_{icf}	I²C input fall time		20 × (V_{CC} / 5.5V)	300	ns
t_{ocf}	I²C output fall time	10pF to 400pF bus	20 × (V_{CC} / 5.5V)	300	ns
t_{buf}	I²C bus free time between stop and start		1.3		µs
t_{sts}	I²C start or repeated start condition setup		0.6		µs
t_{sth}	I²C start or repeated start condition hold		0.6		µs
t_{sps}	I²C stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I²C bus capacitive load			400	pF

5.7 $\overline{\text{RESET}}$ Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-4)

		MIN	MAX	UNIT
t_W	Reset pulse duration	6		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset; For V_{CC} =2.3V – 5.5V	400		ns
	Time to reset; For V_{CC} = 1.65V – 2.3V	550		ns

5.8 Switching Characteristics

over recommended operating free-air temperature range, C_L ≤ 100pF (unless otherwise noted) (see Figure 6-2 and Figure 6-3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	µs
t_{pv}	Output data valid; For V_{CC} = 2.3V – 5.5V	SCL	P port		200	ns
	Output data valid; For V_{CC} = 1.65V – 2.3V				300	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

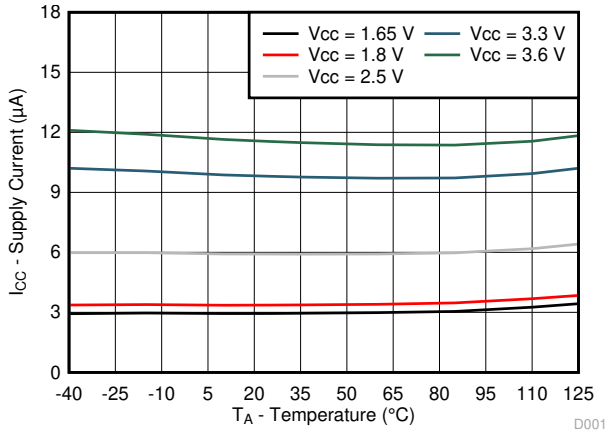


Figure 5-1. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

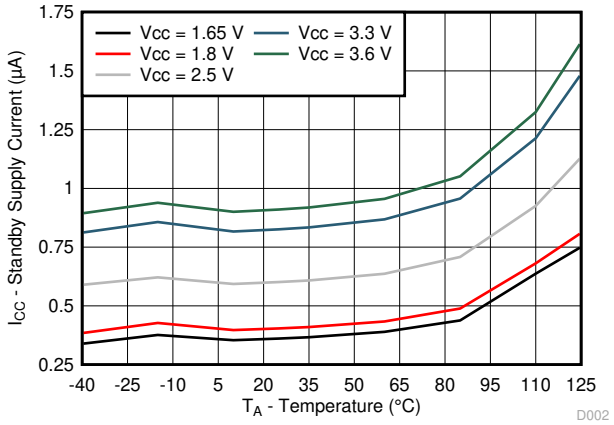


Figure 5-2. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

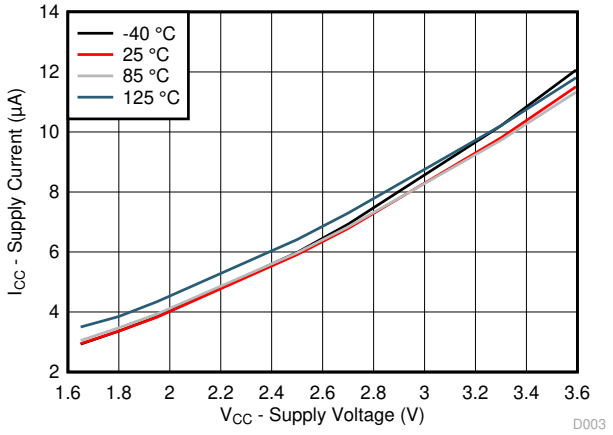
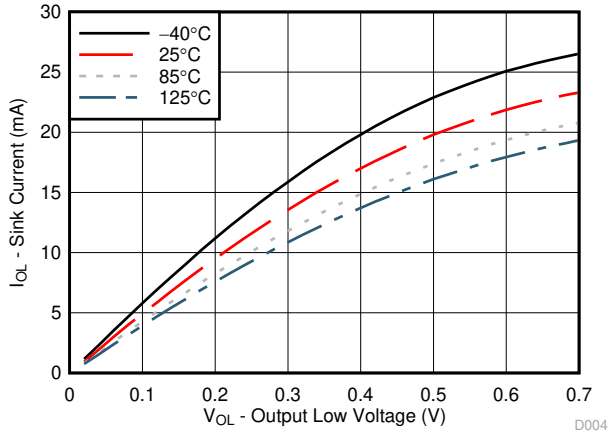
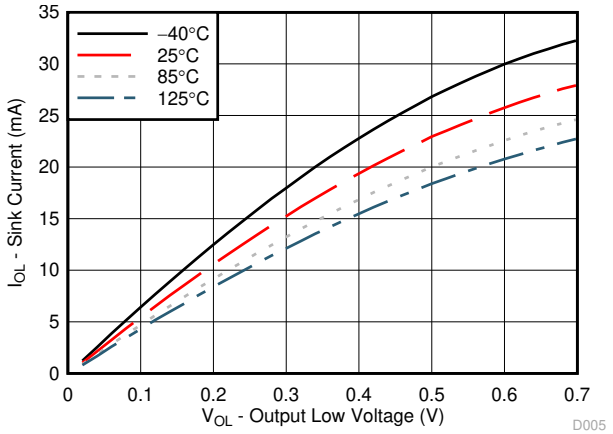


Figure 5-3. Supply Current vs Supply Voltage for Different Temperature (T_A)



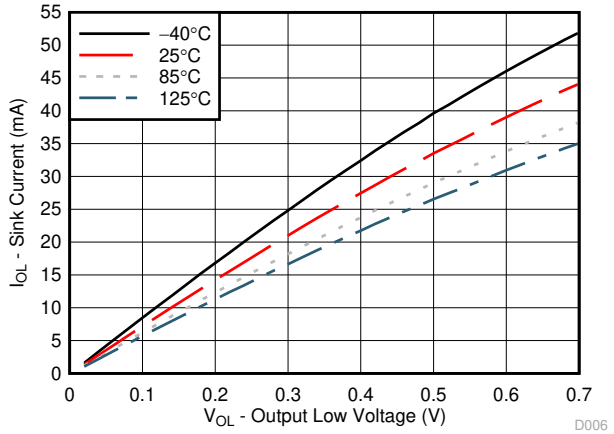
V_{CC} = 1.65V

Figure 5-4. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A)



V_{CC} = 1.8V

Figure 5-5. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A)



V_{CC} = 2.5V

Figure 5-6. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A)

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

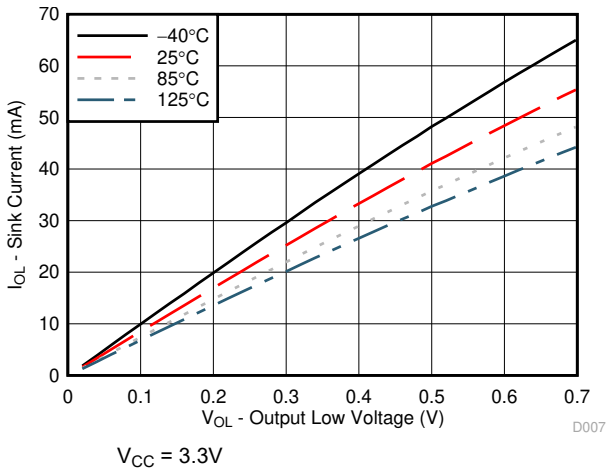


Figure 5-7. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A)

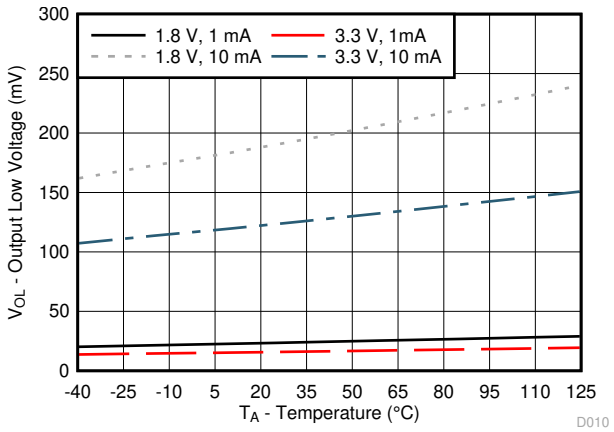


Figure 5-8. I/O Low Voltage vs Temperature for Different V_{CC} and I_{OL}

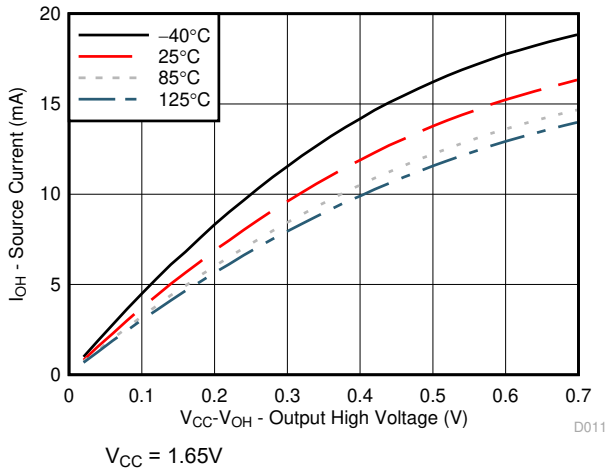


Figure 5-9. I/O Source Current vs Output High Voltage for Different Temperature (T_A)

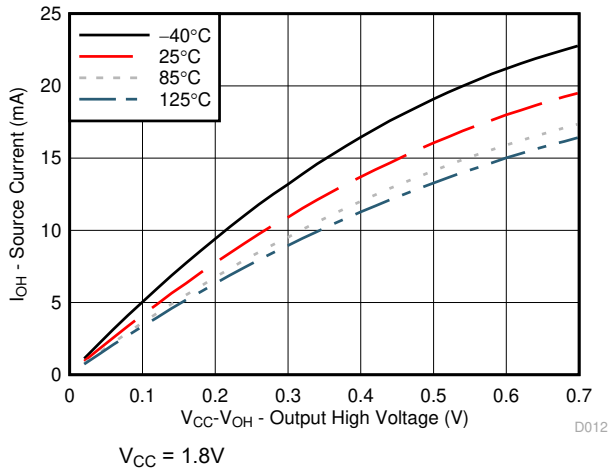
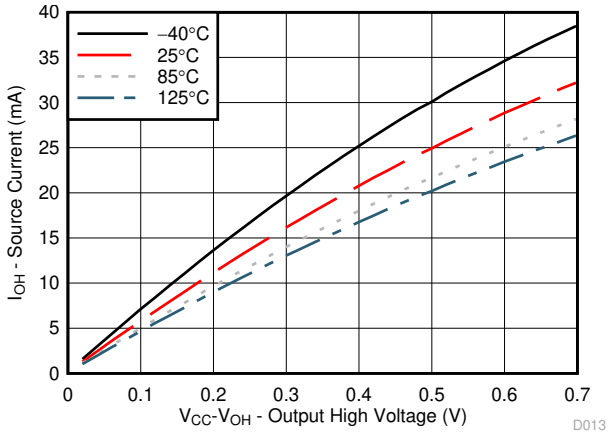


Figure 5-10. I/O Source Current vs Output High Voltage for Different Temperature (T_A)

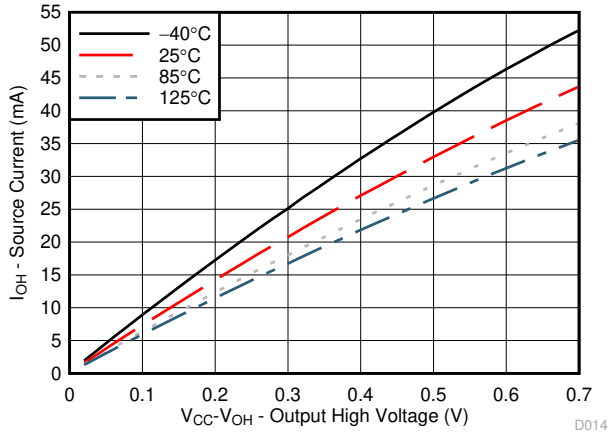
5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)



V_{CC} = 2.5V

Figure 5-11. I/O Source Current vs Output High Voltage for Different Temperature (T_A)



V_{CC} = 3.3V

Figure 5-12. I/O Source Current vs Output High Voltage for Different Temperature (T_A)

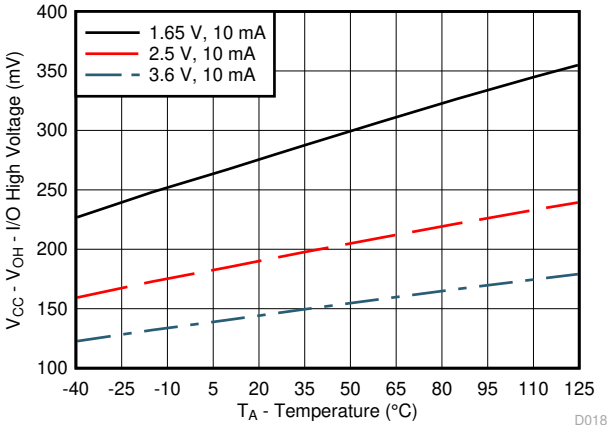
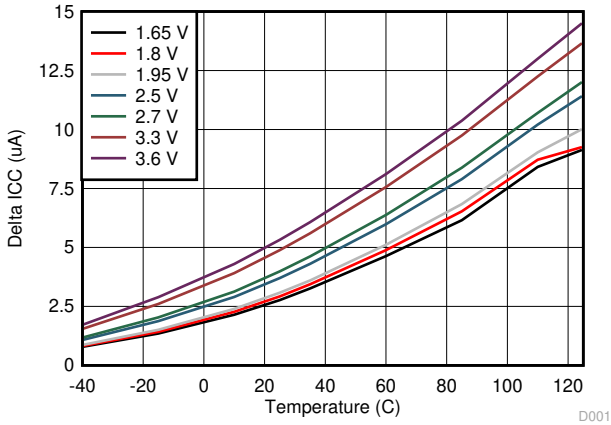


Figure 5-13. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}



(V_I = V_{CC} – 0.6V)

Figure 5-14. Δ I_{CC} vs Temperature for Different V_{CC}

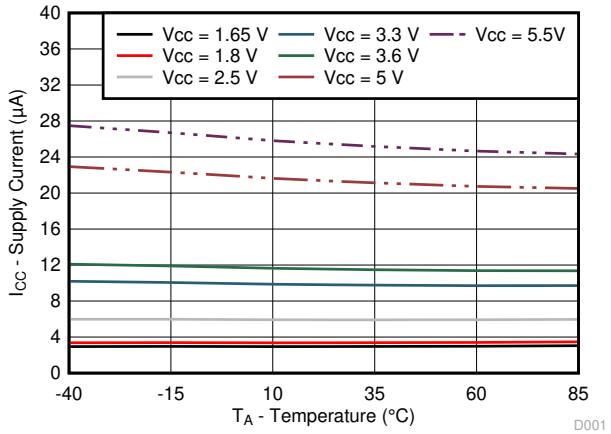


Figure 5-15. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

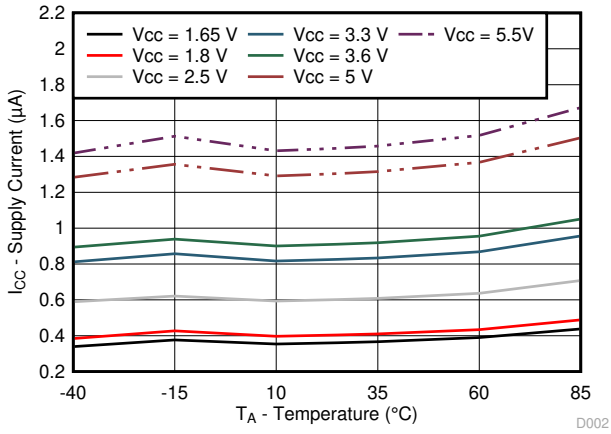


Figure 5-16. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

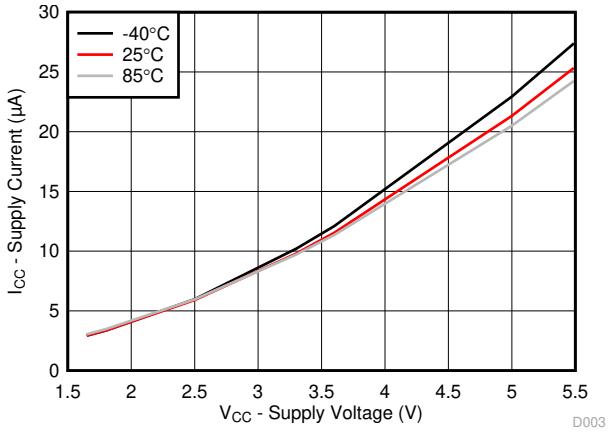


Figure 5-17. Supply Current vs Supply Voltage for Different Temperature (T_A)

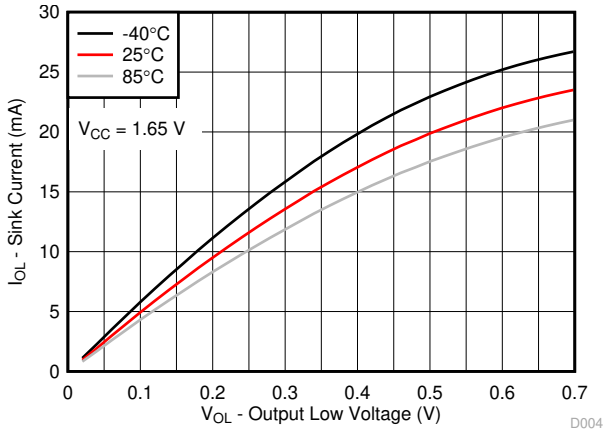


Figure 5-18. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.65V

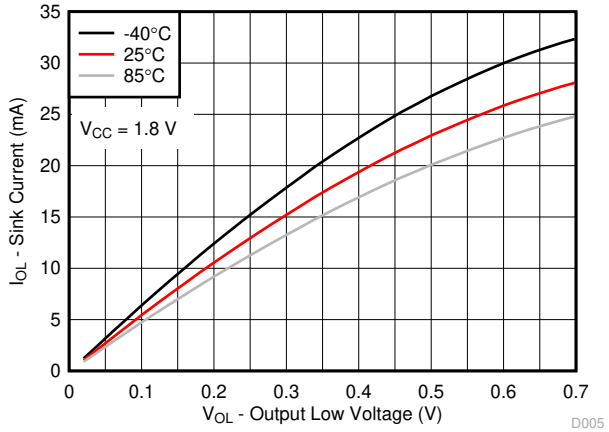


Figure 5-19. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.8V

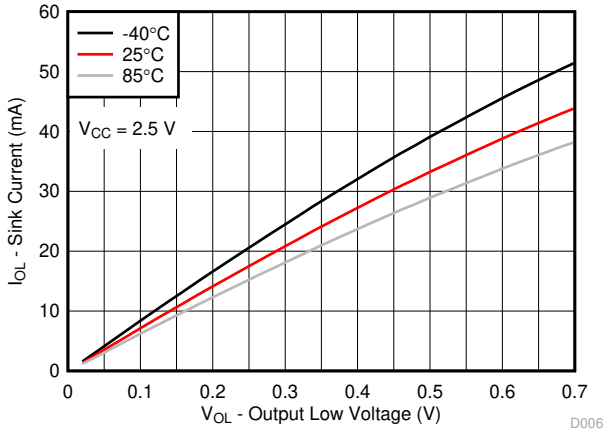


Figure 5-20. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 2.5V

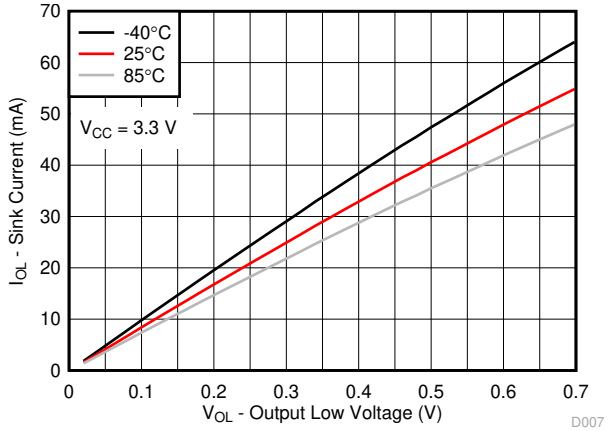


Figure 5-21. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 3.3V

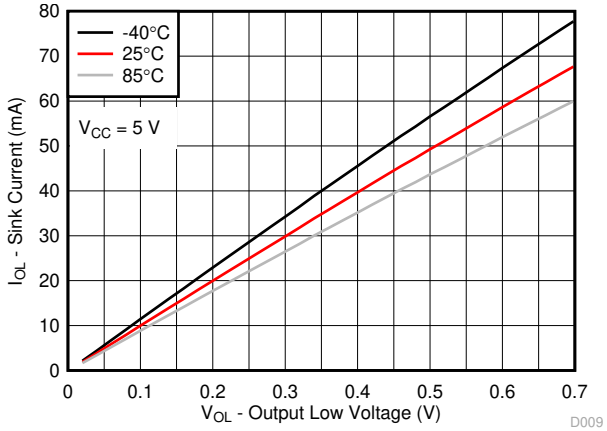


Figure 5-22. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5V

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

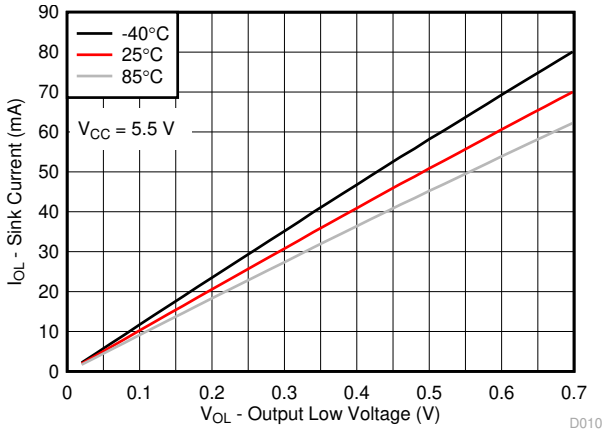


Figure 5-23. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5.5V

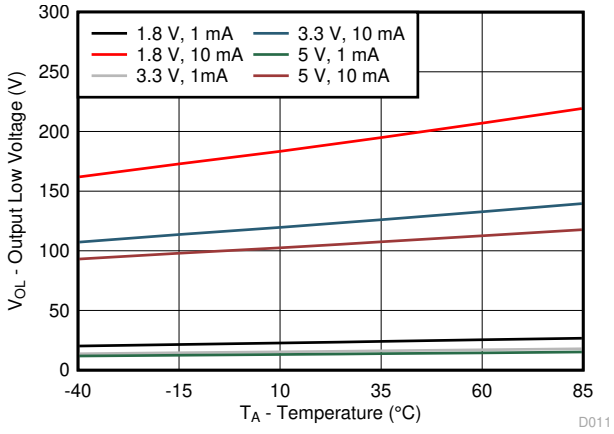


Figure 5-24. II/O Low Voltage vs Temperature for Different V_{CC} and I_{OL}

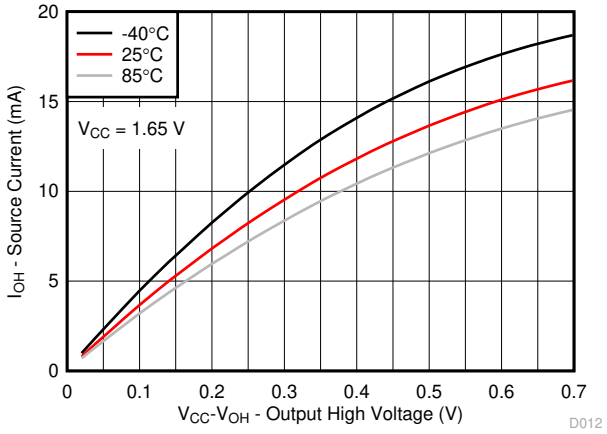


Figure 5-25. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.65V

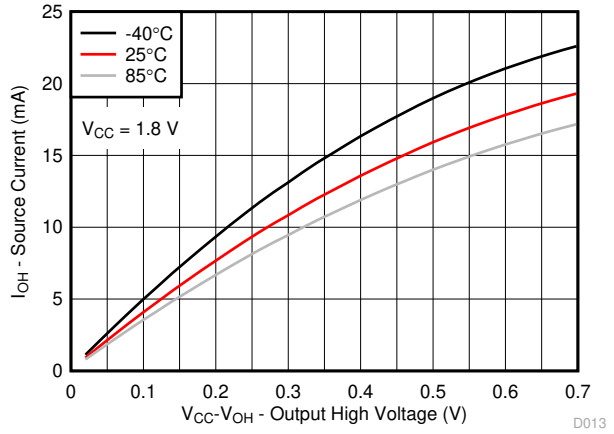


Figure 5-26. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.8V

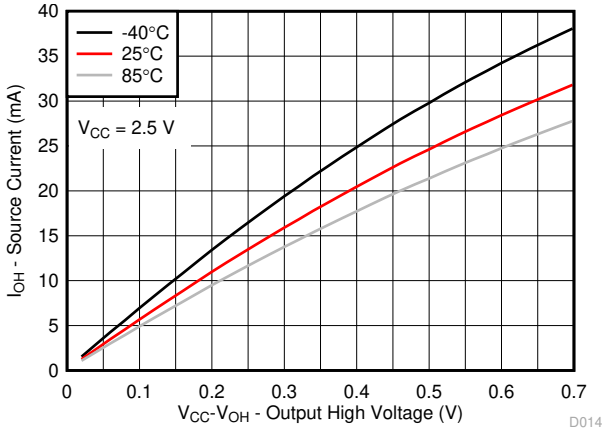


Figure 5-27. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 2.5V

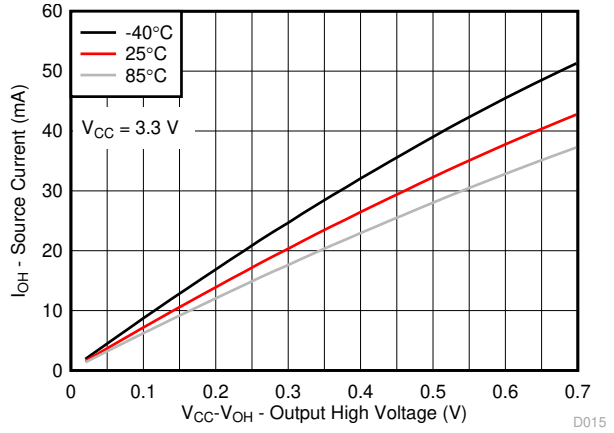


Figure 5-28. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 3.3V

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

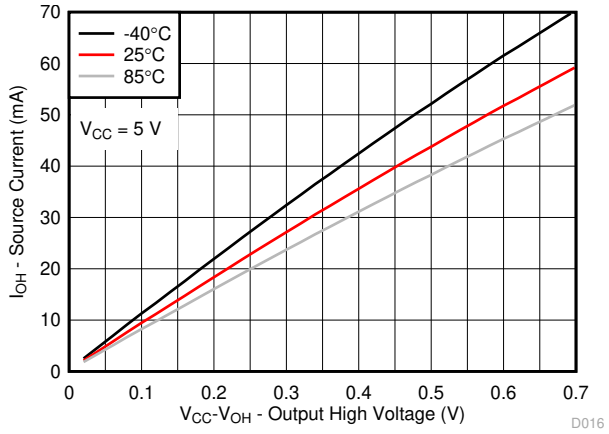


Figure 5-29. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5V

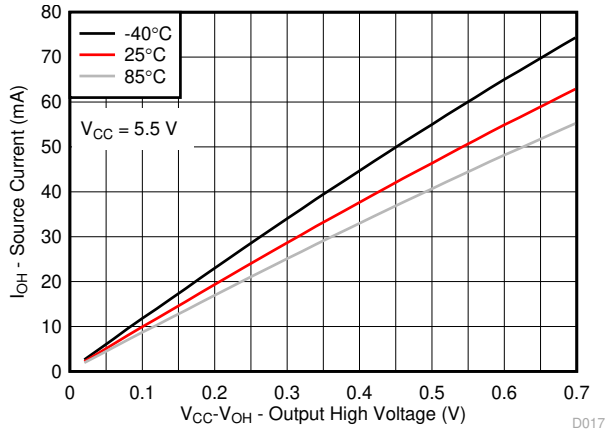


Figure 5-30. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5.5V

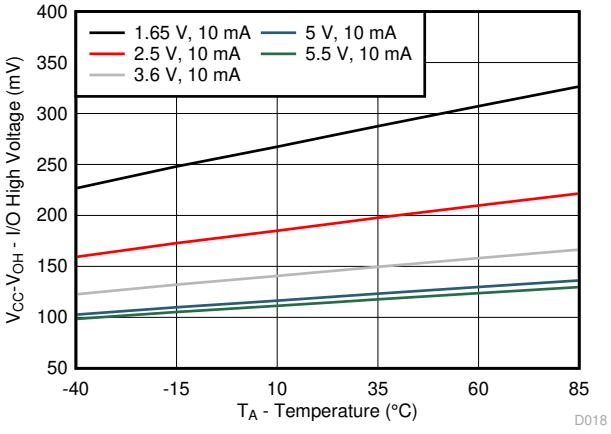


Figure 5-31. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}

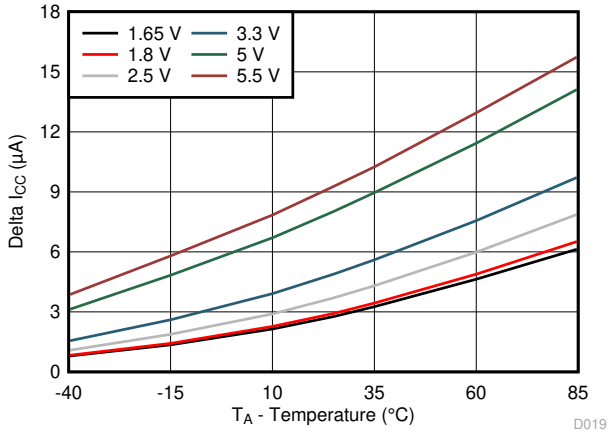
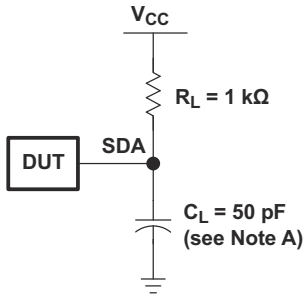
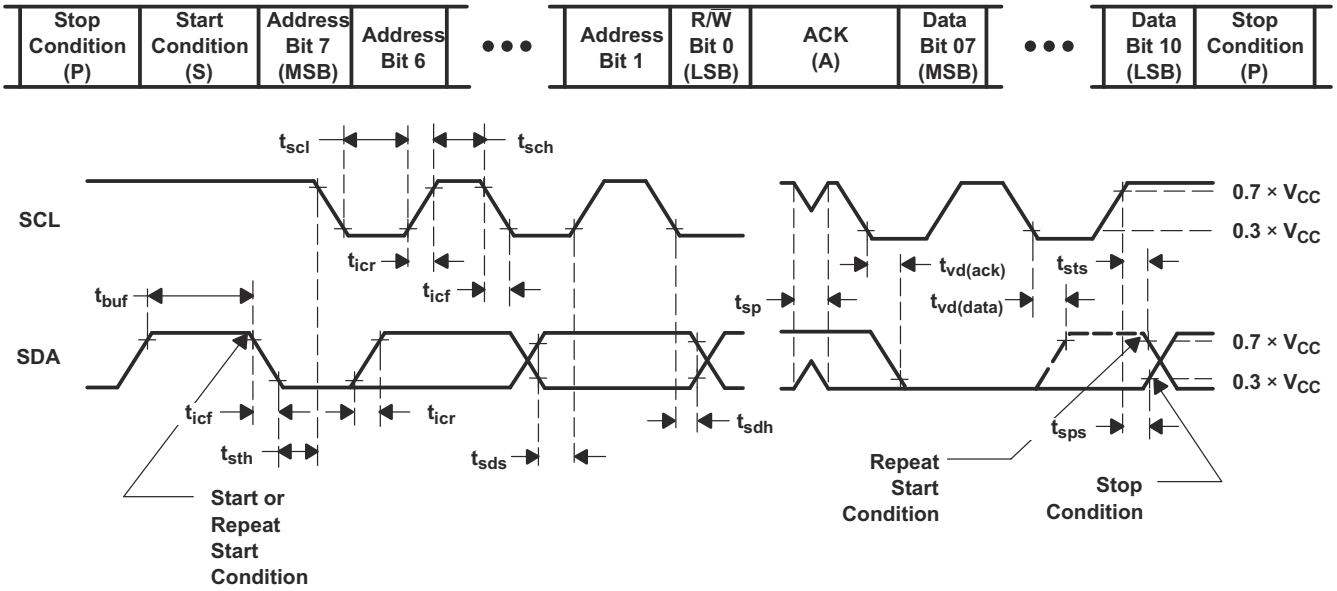


Figure 5-32. Δ I_{CC} vs Temperature for Different V_{CC} (V_I = V_{CC} – 0.6V)

6 Parameter Measurement Information



SDA Load Configuration

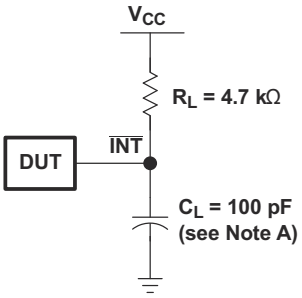


Voltage Waveforms

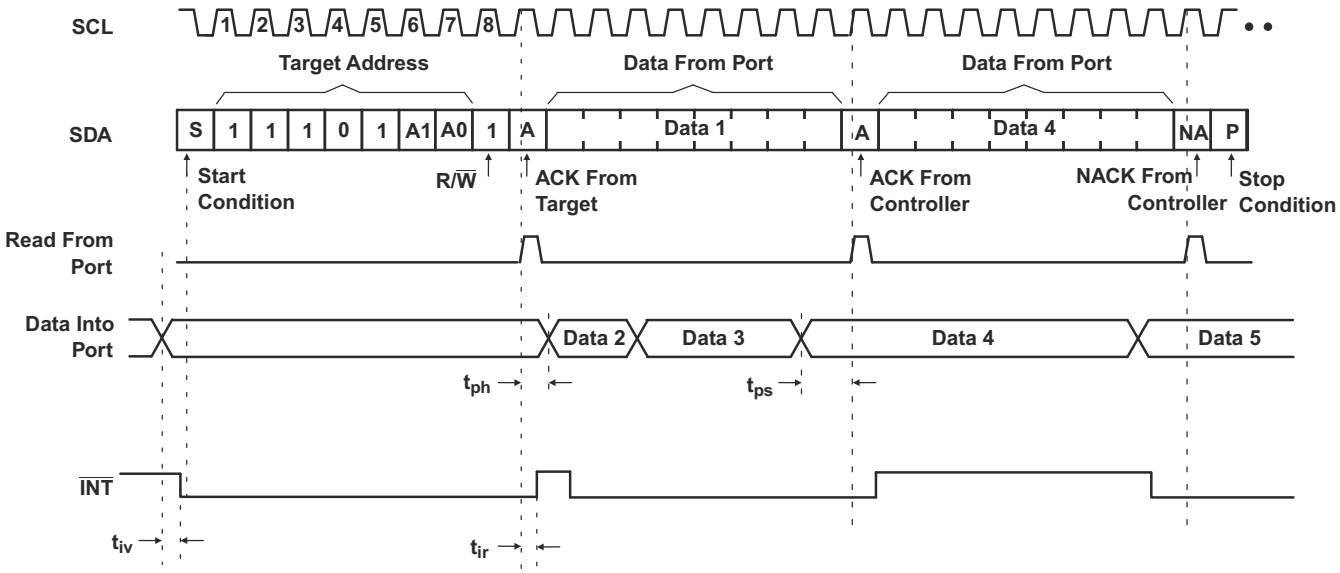
BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

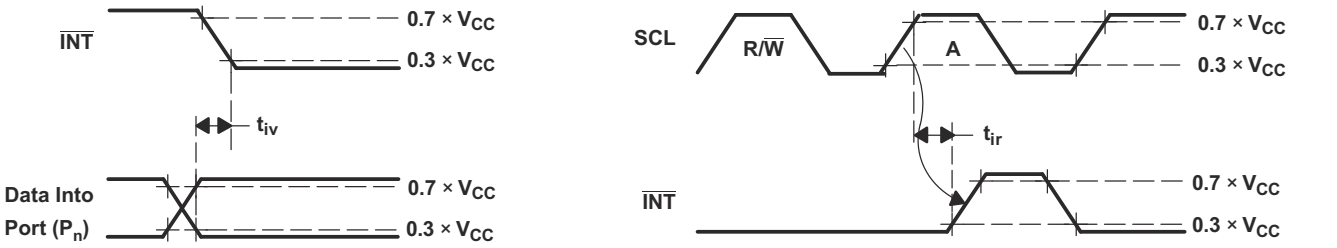
A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
C. All parameters and waveforms are not applicable to all devices.

Figure 6-1. I^2C Interface Load Circuit and Voltage Waveforms



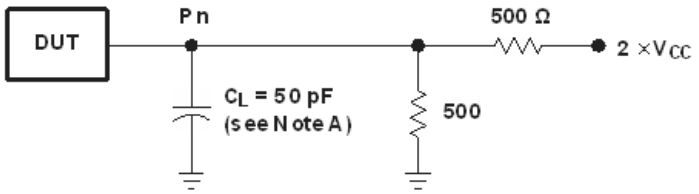
Interrupt Load Configuration



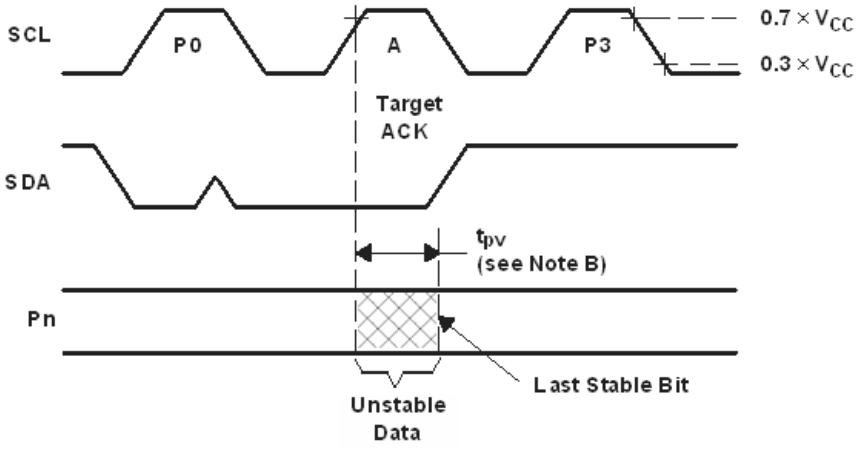


A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10Hz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
C. All parameters and waveforms are not applicable to all devices.

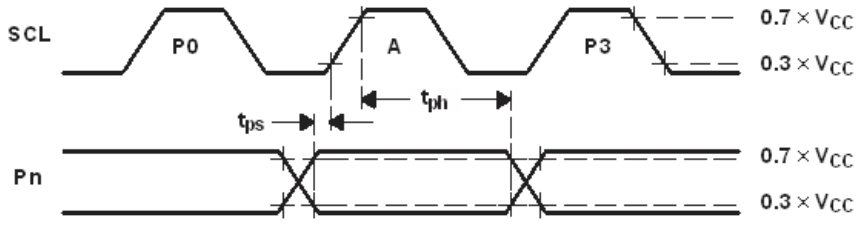
Figure 6-2. Interrupt Load Circuit and Voltage Waveforms



P-Port Load Configuration



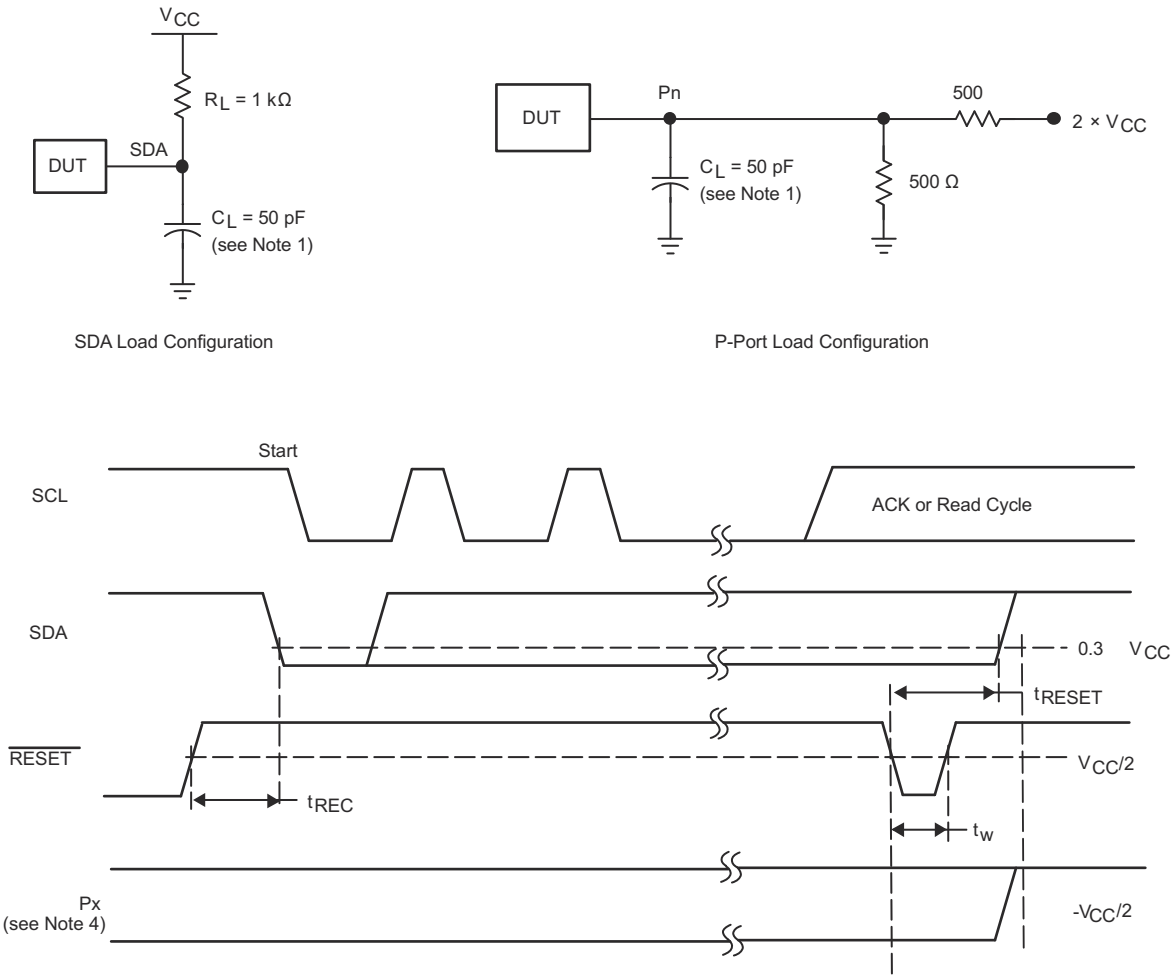
Write Mode (R/W = 0)



Read Mode (R/W = 1)

A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (P_n) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 6-3. P-Port Load Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.
E. All parameters and waveforms are not applicable to all devices.

Figure 6-4. Reset Load Circuits and Voltage Waveforms

7 Detailed Description

7.1 Overview

The TCA9539A-Q1 is a 16-bit I/O expander for the two-line bidirectional bus (I^2C) designed for 1.65V to 5.5V, V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface, serial clock (SCL) and serial data (SDA).

The TCA9539A-Q1 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system controller can enable the I/Os as either inputs or outputs by writing to the configuration register bits. The data for each input or output is kept in the corresponding Input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller.

The system controller can reset the TCA9539A-Q1 in the event of a time-out or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I^2C-SMBus state machine. Asserting $\overline{\text{RESET}}$ causes the same reset-initialization to occur without powering down the device.

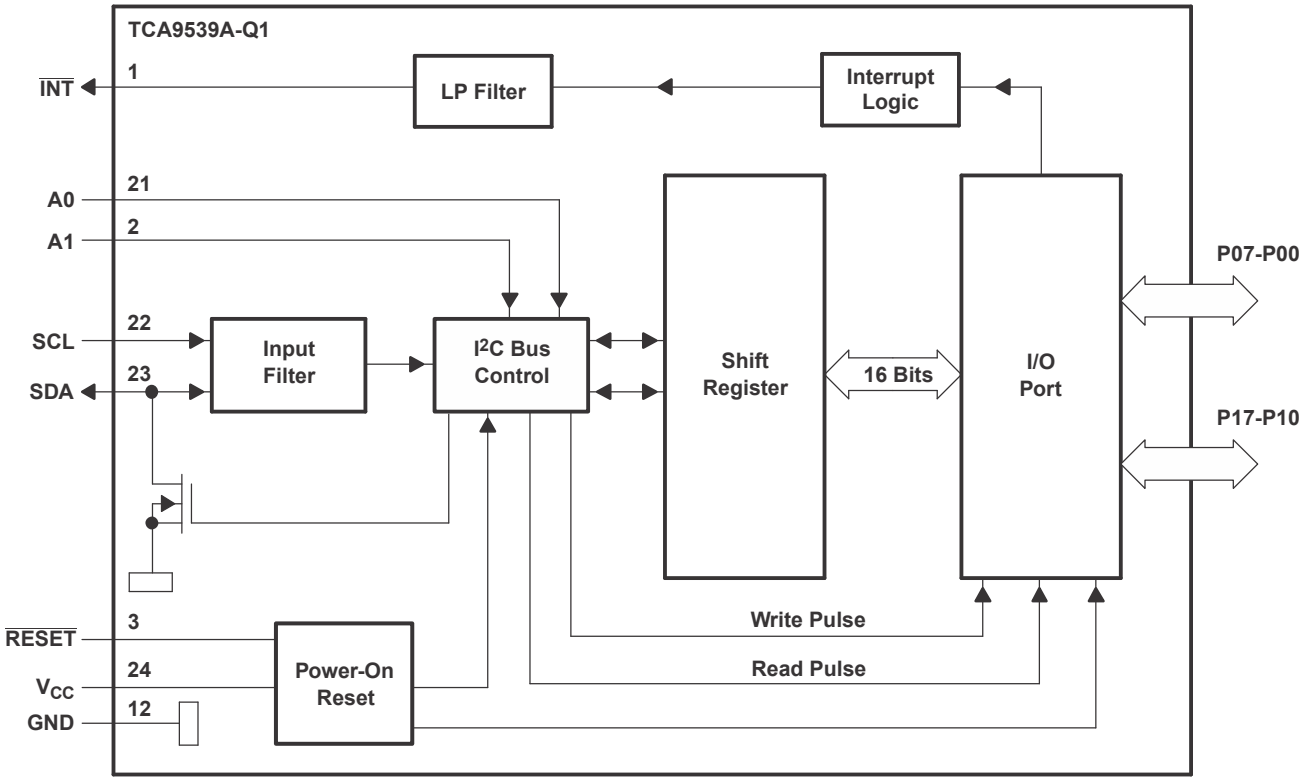
The TCA9539A-Q1 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O informs the microcontroller of incoming data on the ports without having to communicate via the I^2C bus. The TCA9539A-Q1 remains a simple target device.

The TCA9539A-Q1 is similar to the TCA9555, except for the removal of the internal I/O pull-up resistor, which reduces power consumption when the I/Os are held low, replacement of A2 with $\overline{\text{RESET}}$, and a different address range. The TCA9539A-Q1 is similar to the PCA9539 with lower voltage support (down to V_{CC} = 1.65V), and also improved power-on reset circuitry for different application scenarios.

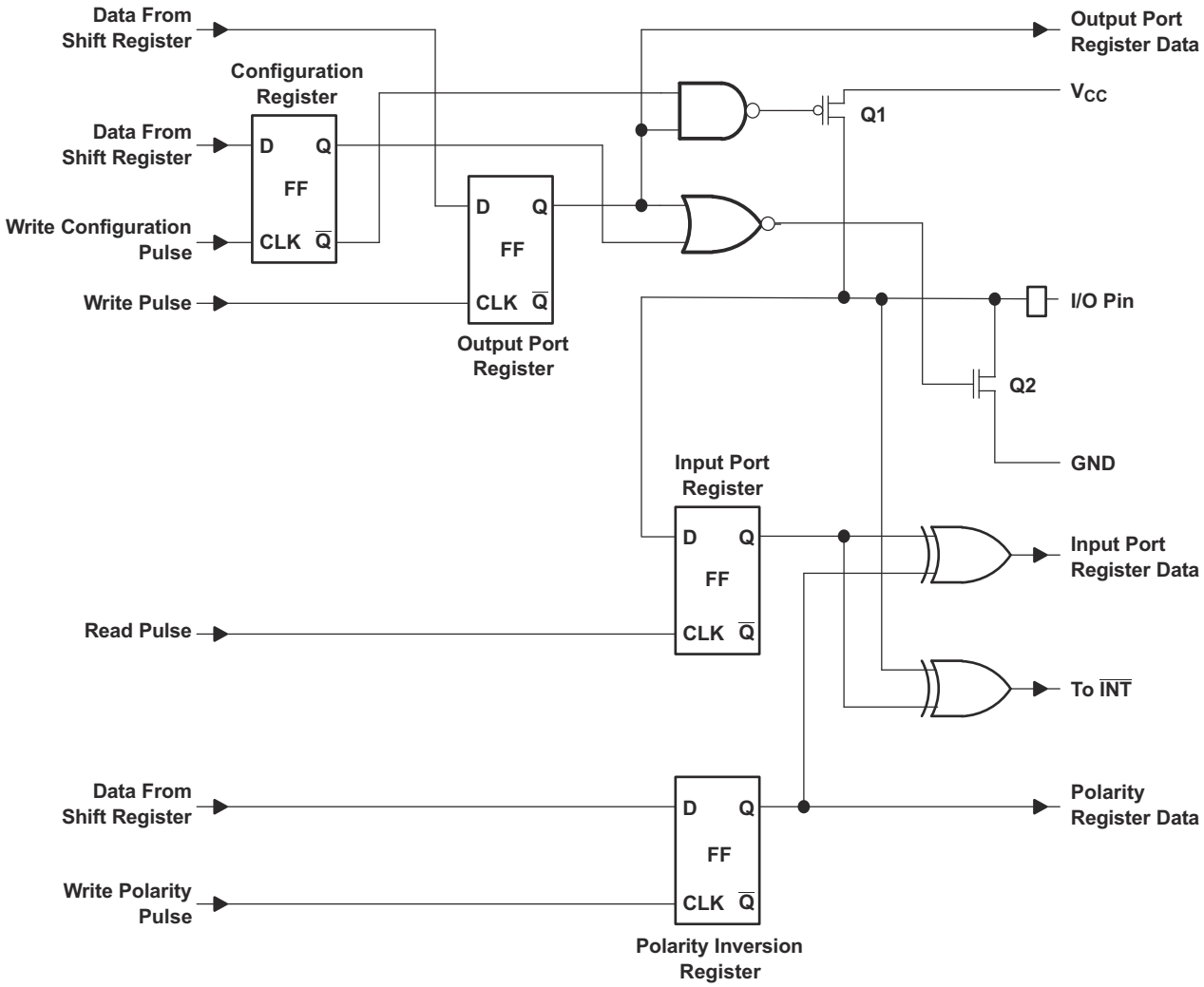
Two hardware pins (A0 and A1) are used to program and vary the fixed I^2C address and allow up to four devices to share the same I^2C bus or SMBus.

7.2 Functional Block Diagram



Pin numbers shown are for PW package.
All I/Os are set to inputs at reset.

Figure 7-1. Logic Diagram (Positive Logic)



At power-on reset, all registers return to default values.

Figure 7-2. Simplified Schematic of P-Port I/Os

7.3 Feature Description

7.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

7.3.2 $\overline{RESET}$ Input

A reset can be accomplished by holding the $\overline{RESET}$ pin low for a minimum of t_W. The TCA9539A-Q1 registers and I^2C-SMBus state machine are held in their default states until $\overline{RESET}$ is once again high. This input requires a pull-up resistor to V_{CC}, if no active connection is used.

7.3.3 Interrupt ($\overline{INT}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the $\overline{INT}$ is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa.

$\overline{INT}$ has an open-drain structure and requires a pull-up resistor to V_{CC}.

7.4 Device Functional Modes

7.4.1 Power-On Reset

When power (from 0V) is applied to V_{CC}, an internal power-on reset holds the TCA9539A-Q1 in a reset condition until V_{CC} has reached V_{PORR}. At that point, the reset condition is released and the TCA9539A-Q1 registers and I^2C-SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to V_{PORF} and then back up to the operating voltage for a power-reset cycle. See Figure 7-3.

7.5 Programming

7.5.1 I^2C Interface

The TCA9539A-Q1 has a standard bidirectional I^2C interface that is controlled by a controller device in order to be configured or read the status of this device. Each target on the I^2C bus has a specific device address to differentiate between other target devices that are on the same I^2C bus. Many target devices require configuration upon startup to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see, *Understanding the I^2C Bus*.

The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I^2C lines. For further details see, *I^2C Pull-up Resistor Calculation*. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition. See Table 7-1.

Figure 7-3 and Figure 7-4 show the general procedure for a controller to access a target device:

1. If a controller wants to send data to a target:
   - Controller-transmitter sends a START condition and addresses the target-receiver.
   - Controller-transmitter sends data to target-receiver.
   - Controller-transmitter terminates the transfer with a STOP condition.
2. If a controller wants to receive or read data from a target:
   - Controller-receiver sends a START condition and addresses the target-transmitter.
   - Controller-receiver sends the requested register to read to target-transmitter.
   - Controller-receiver receives data from the target-transmitter.

- Controller-receiver terminates the transfer with a STOP condition.

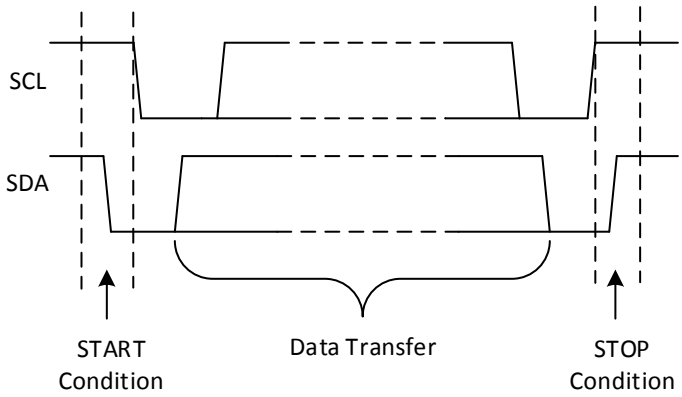


Figure 7-3. Definition of Start and Stop Conditions

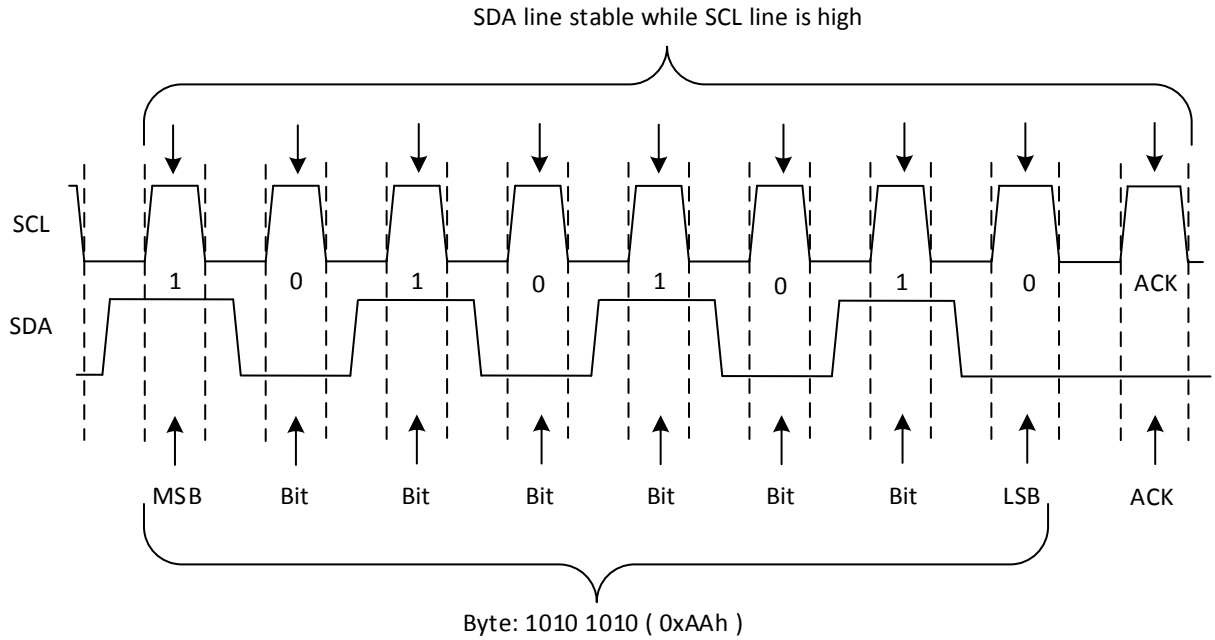


Figure 7-4. Bit Transfer

Table 7-1 shows the interface definition.

Table 7-1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C target address	H	H	H	L	H	A1	A0	R/ $\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

7.6 Register Map

7.6.1 Device Address

Figure 7-5 shows the address byte of the TCA9539A.

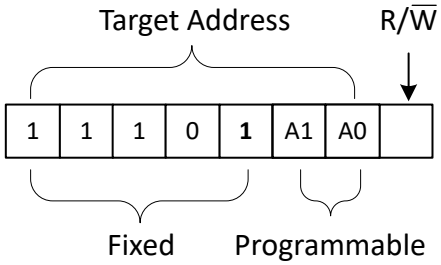


Figure 7-5. Address for Device #1 (TCA9539A)

Table 7-2 shows the address reference of the TCA9539A.

Table 7-2. Address Reference

INPUTS		I2C BUS TARGET ADDRESS
A1	A0	
L	L	116 (decimal), 74 (hexadecimal)
L	H	117 (decimal), 75 (hexadecimal)
H	L	118 (decimal), 76 (hexadecimal)
H	H	119 (decimal), 77 (hexadecimal)

Figure 7-6 shows the address reference of TCA9539B.

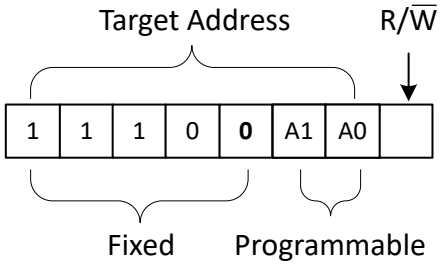


Figure 7-6. Address for Device #2 (TCA9539B)

Table 7-3 shows the address reference of the TCA9539B.

Table 7-3. Address Reference

INPUTS		I2C BUS TARGET ADDRESS
A1	A0	
L	L	112 (decimal), 70 (hexadecimal)
L	H	113 (decimal), 71 (hexadecimal)
H	L	114 (decimal), 72 (hexadecimal)
H	H	115 (decimal), 73 (hexadecimal)

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

7.6.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte (shown in Table 7-4) that is stored in the control register in the TCA9539-Q1. Three bits of this data byte state the operation (read or write) and the internal register (input, output, Polarity Inversion or Configuration) that is affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Table 7-4. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	XXXX XXXX
0	0	1	0x01	Input Port 1	Read byte	XXXX XXXX
0	1	0	0x02	Output Port 0	Read-write byte	1111 1111
0	1	1	0x03	Output Port 1	Read-write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read-write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read-write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read-write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read-write byte	1111 1111

When a command byte has been sent, the register pair that was addressed continues to be accessed by reads until a new command byte has been sent. Figure 7-7 shows the control register bits.

0	0	0	0	0	B2	B1	B0

Figure 7-7. Control Register Bits

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

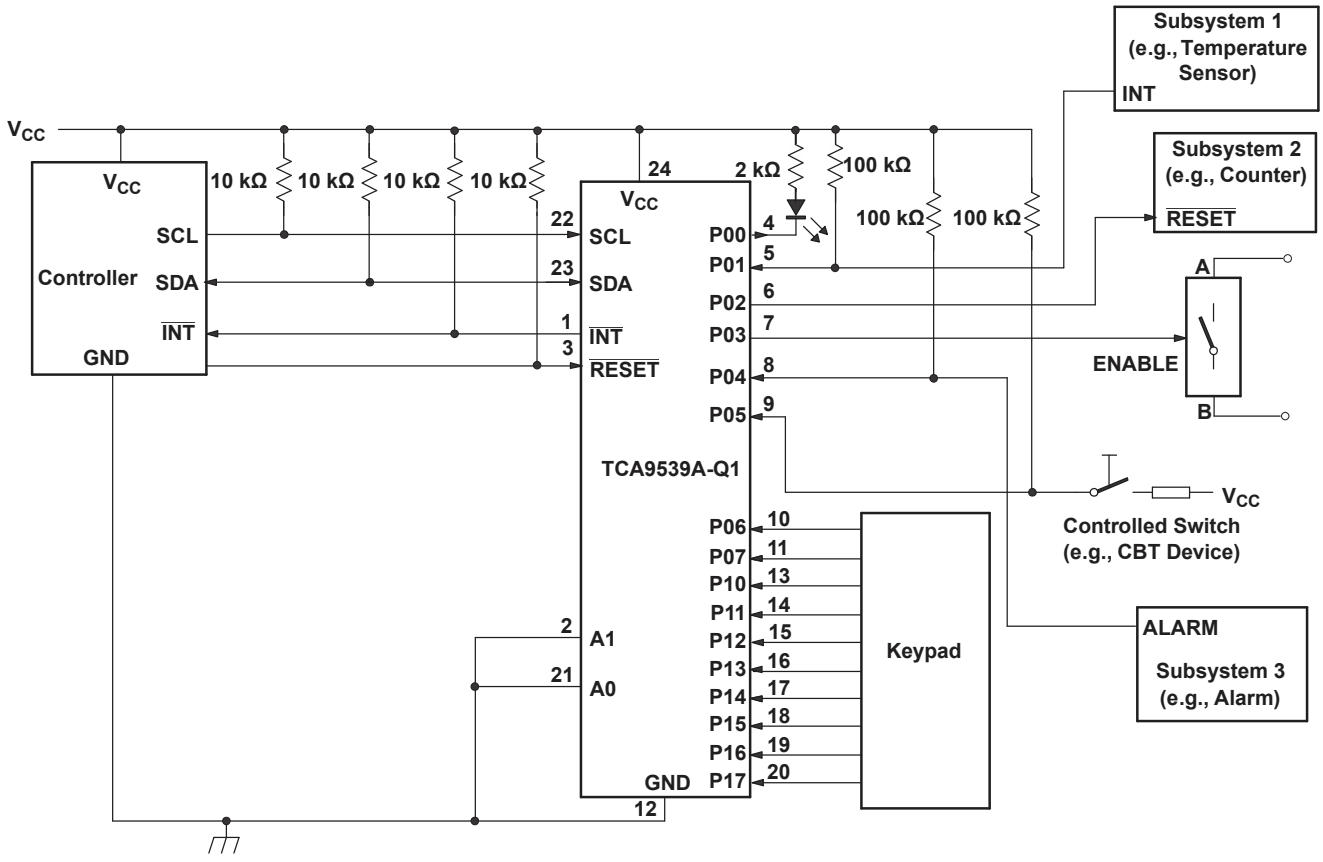
8.1 Application Information

Applications of the TCA9539A-Q1 has this device connected as a target to an I^{2}C controller (processor), and the I^{2}C bus can contain any number of other target devices. The TCA9539A-Q1 is typically in a remote location from the controller, placed close to the GPIOs to which the controller needs to monitor or control.

IO Expanders such as the TCA9539A-Q1 are typically used for controlling LEDs (for feedback or status lights), controlling enable or reset signals of other devices, and even reading the outputs of other devices or buttons.

8.2 Typical Application

Figure 8-1 shows an application in which the TCA9539A-Q1 can be used.



Device address is configured as 1110100 for this example.
P00, P02, and P03 are configured as outputs.
P01 and P04 to P17 are configured as inputs.
Pin numbers shown are for the PW package.

Figure 8-1. Application Schematic

8.2.1 Design Requirements

8.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I^2C bus. The resistor value needed for minimum pull-up is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL} as shown in Equation 1.

$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The resistor value needed for maximum pull-up is a function of the maximum rise time, t_r (300ns for fast-mode operation,
f_{SCL} = 400kHz) and bus capacitance, C_b as shown in Equation 2.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9539A-Q1, C_i for SCL or C_{io} for SDA, the capacitance of wires, connections, traces, and the capacitance of additional targets on the bus.

Table 8-1. Design Parameters

PARAMETER	VALUE
VCC	5.5V
$V_{OL(max)}$	0.4V
I_{OL}	3.0mA
$R_{p(min)}$	1.7kΩ
f_{SCL}	400kHz
C_b	200pF
t_r	150ns
$R_{p(max)}$	885Ω
Pull-up R (between $R_{p(max)}$ and $R_{p(min)}$)	1.2 ± 10%kΩ

8.2.2.1 Calculating Junction Temperature and Power Dissipation

When designing with the TCA9539A-Q1, it is important that the *Recommended Operating Conditions* not be violated. Many of the parameters of this device are rated based on junction temperature, so junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in Equation 3.

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (3)$$

θ_{JA} is the standard junction to ambient thermal resistance measurement of the package, as seen in *Section 5.4* table. P_d is the total power dissipation of the device, and the approximation is shown in Equation 4.

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (4)$$

Equation 4 is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied

by the voltage on the pin). Note that this ignores power dissipation in the $\overline{INT}$ and SDA pins, assuming these transients to be small. They can be included in the power dissipation calculation by using Equation 5 to calculate the power dissipation in $\overline{INT}$ or SDA while pulling low. This provides the maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (5)$$

Equation 5 shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the V_{OL} of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (6)$$

Equation 6 shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between V_{CC} and the output voltage).

8.2.2.2 Minimizing I_{CC} When I/Os Control LEDs

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor (see Figure 8-1). Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2V less than V_{CC}. The ΔI_{CC} parameter in the *Electrical Characteristics* table show how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC}, when the LED is off, to minimize current consumption.

Figure 8-2 shows a high-value resistor in parallel with the LED. Figure 8-3 shows V_{CC} less than the LED supply voltage by at least 1.2V. Both of these methods maintain the I/O V_{CC} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

Take care to make sure that the recommended maximum I_{OL} through the ports not be violated based upon junction temperature. See the *Recommended Operating Conditions* for more information.

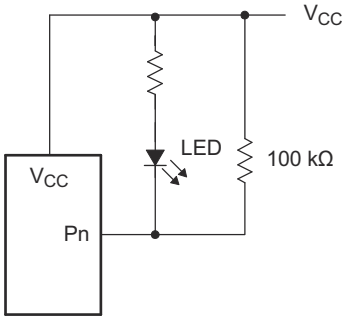


Figure 8-2. High-Value Resistor In Parallel With LED

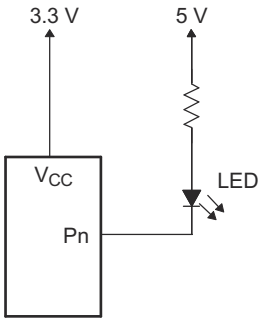
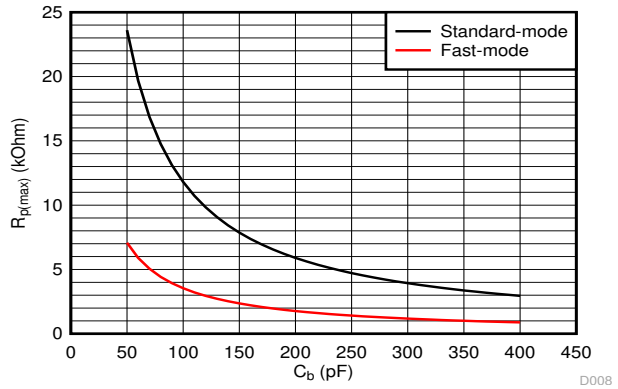


Figure 8-3. Device Supplied By Lower Voltage

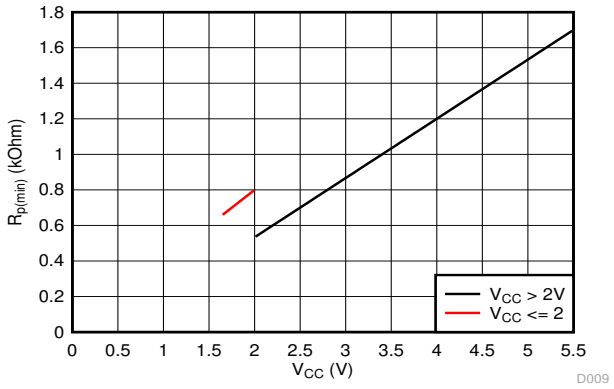
8.2.3 Application Curves



Standard-mode (f_{SCL} = 100kHz, t_r = 1µs)

Fast-mode (f_{SCL} = 400kHz, t_r = 300ns)

Figure 8-4. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 × V_{CC}, I_{OL} = 2mA when V_{CC} ≤ 2V

V_{OL} = 0.4V, I_{OL} = 3mA when V_{CC} > 2V

Figure 8-5. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

8.3 Power Supply Recommendations

8.4 Layout

8.4.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9539A-Q1, common PCB layout practices must be followed, but additional concerns related to high-speed data transfer such as matched impedance and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, the best practice is to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9539A-Q1 as possible. These best practices are shown in Figure 8-6 .

For the layout example provided in Figure 8-6, the user can fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, the user can route signals on the top and bottom layer. Dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which must attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 8-6.

8.4.2 Layout Example

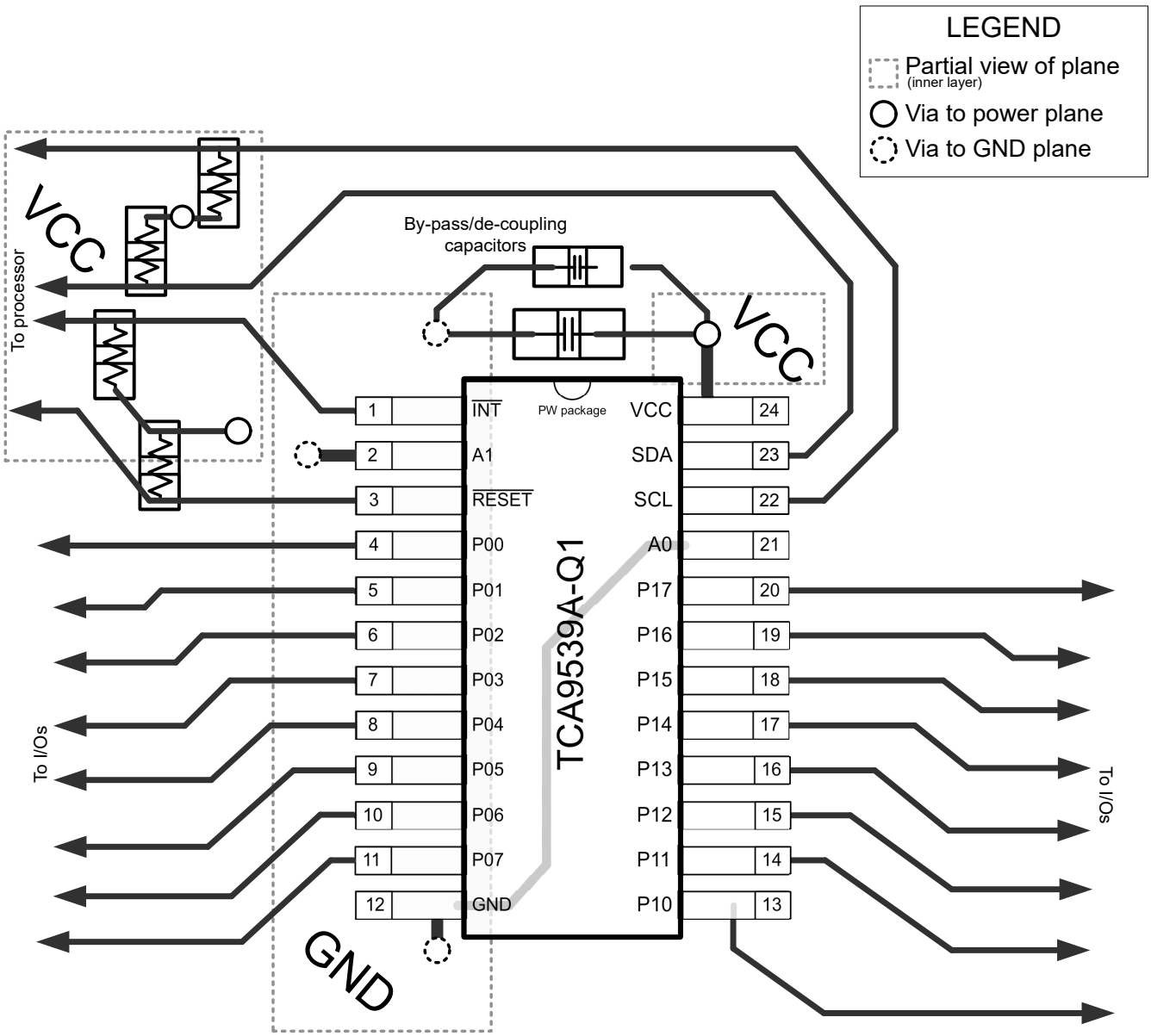


Figure 8-6. TCA9539A-Q1 Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Understanding the I2C Bus*
- Texas Instruments, *I2C Pull-up Resistor Calculation*
- Texas Instruments, *Introduction to Logic*
- Texas Instruments, *Maximum Clock Frequency of I2C Bus Using Repeaters*
- Texas Instruments, *I2C Bus Pull-Up Resistor Calculation*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA9539AQPWRQ1	Active	Production	TSSOP (PW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TCA539AQ
TCA9539BQPWRQ1	Active	Production	TSSOP (PW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TCA539BQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

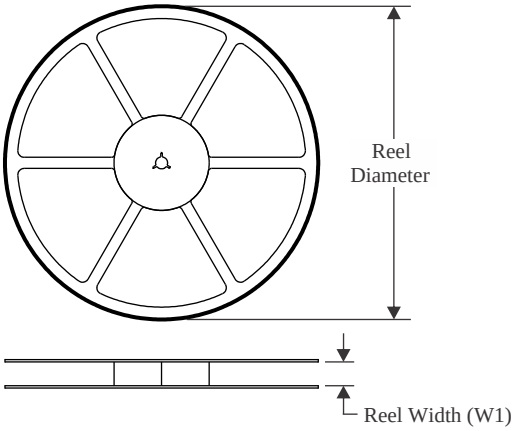
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

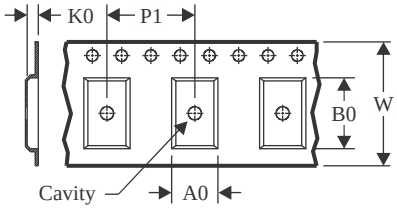
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

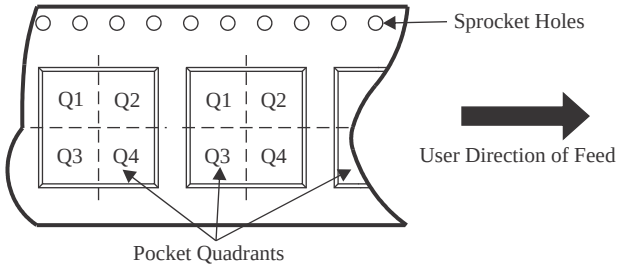


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

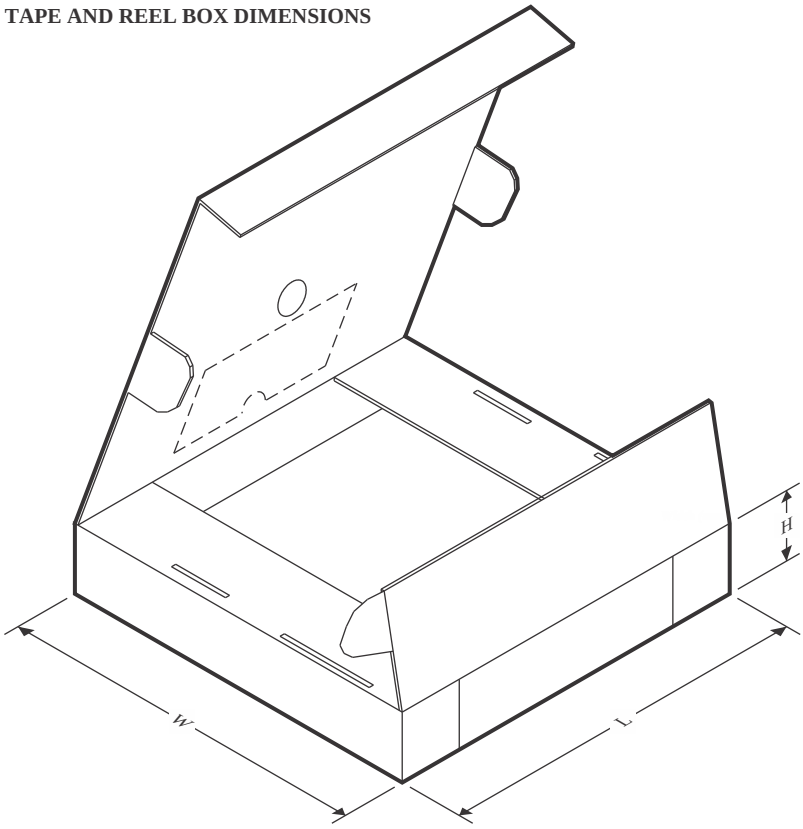
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9539AQPWRQ1	TSSOP	PW	24	3000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA9539BQPWRQ1	TSSOP	PW	24	3000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

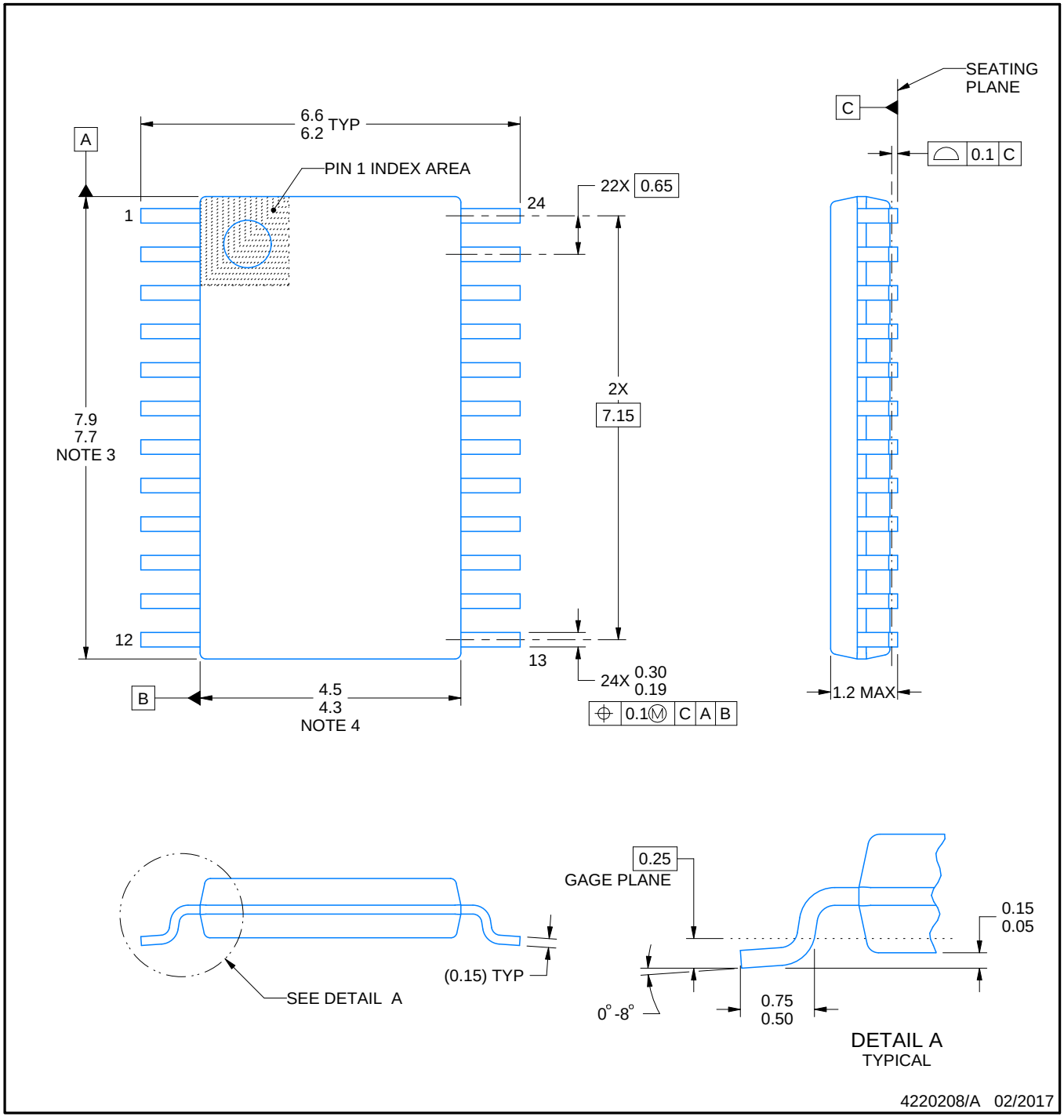
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9539AQPWRQ1	TSSOP	PW	24	3000	353.0	353.0	32.0
TCA9539BQPWRQ1	TSSOP	PW	24	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0024A

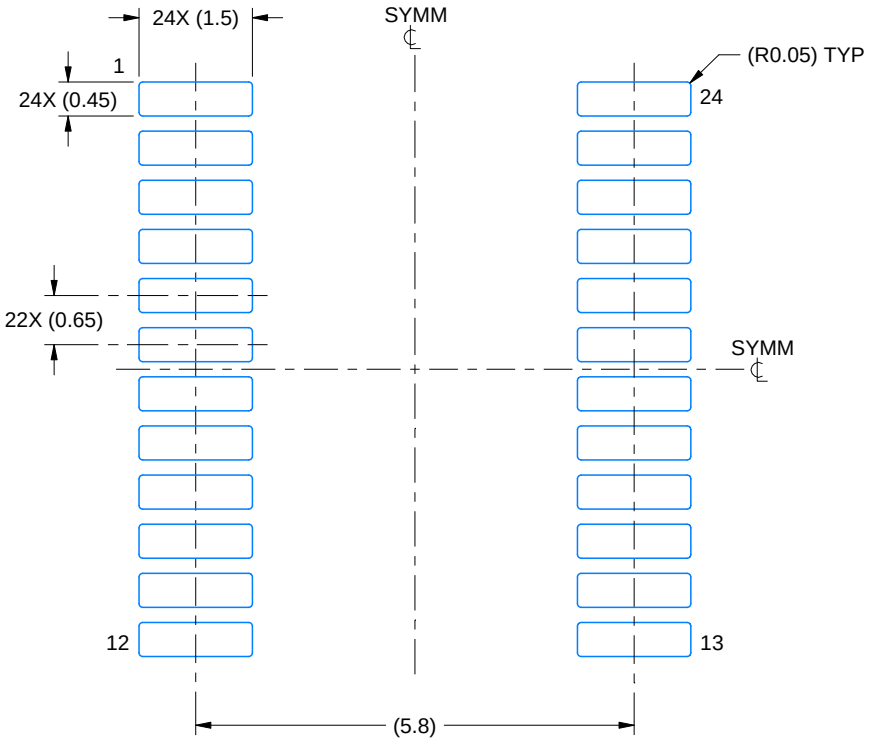
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

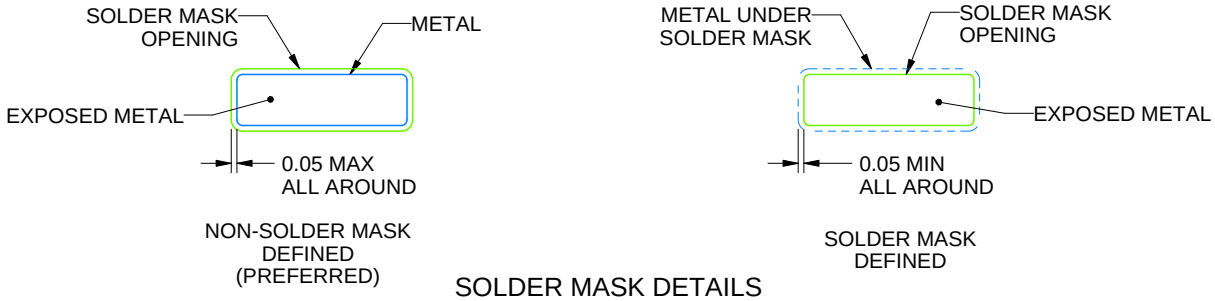


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

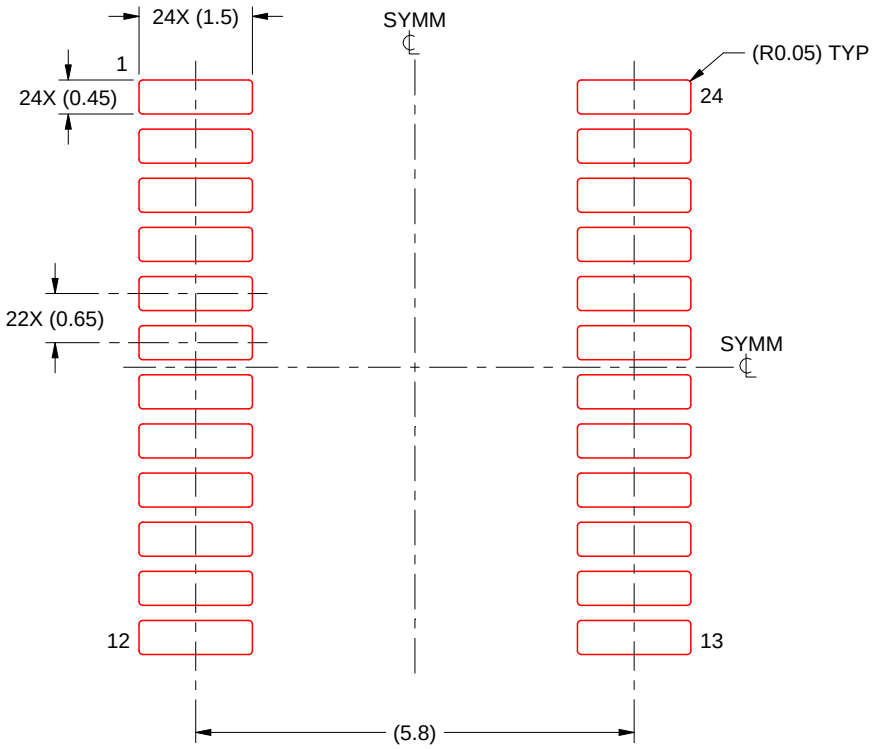


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025