TCA9517A Level-Shifting I²C Bus Repeater

1 Features

- Two-channel bidirectional buffer
- I²C Bus and SMBus compatible
- Operating supply voltage range of 0.9V to 5.5V on A-side
- Operating supply voltage range of 2.7V to 5.5V on B-side
- Voltage-level translation from 0.9V - 5.5V to 2.7V - 5.5V
- Footprint and functional replacement for PCA9515B
- Active-high repeater-enable input
- Open-drain I²C I/O
- 5.5V Tolerant I²C and enable input support mixed-mode signal operation
- Accommodates standard mode and fast mode I²C devices and multiple controllers
- High-impedance I²C pins when powered-off
- Latch-up performance exceeds 100mA Per JESD 78, class II
- ESD Protection exceeds JESD 22
  - 5500V Human-body model (A114-A)
  - 200V Machine model (A115-A)
  - 1000V Charged-device model (C101)

2 Applications

- Servers
- Routers (telecom switching equipment)
- Industrial equipment
- Products with many I²C targets and/or long PCB traces

3 Description

The TCA9517A is a bidirectional buffer with level shifting capabilities for I²C and SMBus systems. It provides bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9V) and higher voltages (2.7V to 5.5V) in mixed-mode applications. This device enables I²C and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517A buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing two buses of up to 400pF bus capacitance to be connected in an I²C application.

The TCA9517A has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.5V, even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0V).

The TCA9517A offers a higher contention level threshold, V_{ILC}, than the TCA9517, which allows connections to targets which have weaker pulldown ability.

The type of buffer design on the B-side prevents it from being used in series with devices which use static voltage offset. This is because these devices do not recognize buffered low signals as a valid low and do not propagate it as a buffered low again.

The B-side drivers operate from 2.7V to 5.5V. The output low level for this internal buffer is approximately 0.5V, but the input voltage must be 70mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released.

The A-side drivers operate from 0.9V to 5.5V and drive more current. They do not require the buffered low feature (or the static offset voltage). This means that a low signal on the B-side translates to a nearly 0V low on the A-side, which accommodates smaller voltage swings of lower-voltage logic. The output pulldown on the A-side drives a hard low, and the input level is set at 0.3 × V_{CCA} to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.9V.

The A-side of two or more TCA9517As can be connected together, allowing many topographies (See Figure 8-2 and Figure 8-3), with the A-side as the common bus. Also, the A-side can be connected directly to any other buffer with static- or dynamic-offset voltage. Multiple TCA9517As can be connected in series, A-side to B-side, with no buildup in offset voltage and with only time-of-flight delays to consider. The TCA9517A cannot be connected B-side to B-side, because of the buffered low voltage from the B-side. The B-side cannot be connected to a device with rise time accelerators.

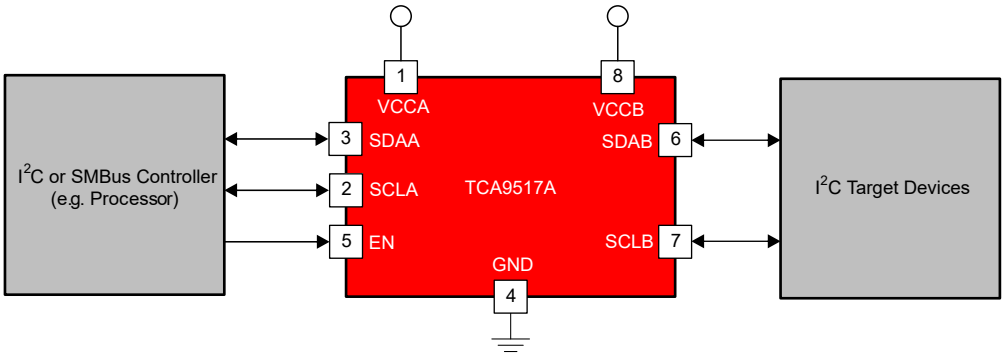
VCCA is only used to provide the 0.3 × V_{CCA} reference to the A-side input comparators and for the power-good-detect circuit. The TCA9517A logic and all I/Os are powered by the VCCB pin.

As with the standard I^2C system, pullup resistors are required to provide the logic-high levels on the buffered bus. The TCA9517A has standard open-drain configuration of the I^2C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard mode and Fast mode I^2C devices in addition to SMBus devices. Standard mode I^2C devices only specify 3mA in a generic I^2C system, where Standard mode devices and multiple controllers are possible. Under certain conditions, higher termination currents can be used.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
TCA9517A	VSSOP (8)	3mm × 3mm

(1) For more information, see Section 13.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

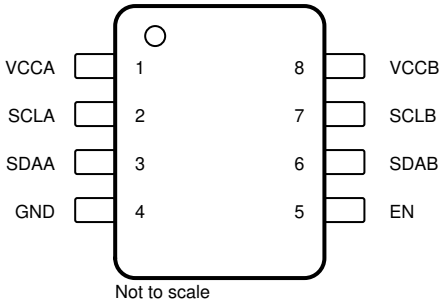


Figure 4-1. DGK Package, 8-Pin VSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCCA	Supply	A-side supply voltage (0.9V to 5.5V)
2	SCLA	Input/Output	Serial clock bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
3	SDAA	Input/Output	Serial data bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
4	GND	Ground	Ground
5	EN	Input	Active-high repeater enable input
6	SDAB	Input/Output	Serial data bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
7	SCLB	Input/Output	Serial clock bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
8	VCCB	Supply	B-side and device supply voltage (2.7V to 5.5V)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	7	V
V_{CCA}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range(2)		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±5500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.9(2)	5.5	V
V_{CCB}	Supply voltage, B-side bus		2.7	5.5	V
V_{IH}	High-level input voltage	SDAA, SCLA	0.7 × V_{CCA}	5.5	V
		SDAB, SCLB	0.7 × V_{CCB}	5.5	
		EN	0.7 × V_{CCB}	5.5	
V_{IL}	Low-level input voltage	SDAA, SCLA		0.3 × V_{CCA}	V
		SDAB, SCLB(1)		0.3 × V_{CCB}	
		EN		0.3 × V_{CCB}	
I_{OL}	Low-level output current			6	mA
T_A	Operating free-air temperature		–40	85	°C

(1) V_{IL} specification is for the first low level seen by the SDAB and SCLB lines. V_{ILc} is for the second and subsequent low levels seen by the SDAB and SCLB lines. See *Section 8.2.2.2* for V_{ILC} application information
(2) Low-level supply voltage

5.4 Thermal Information

THERMAL METRIC[1]		TCA9517A DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

V_{CCB} = 2.7V to 5.5V, GND = 0V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCB}	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18mA	2.7V to 5.5V			–1.2	V
V_{OL}	Low-level output voltage	SDAB, SCLB	I_{OL} = 100µA or 6mA, V_{ILA} = V_{ILB} = 0V	2.7V to 5.5V	0.45	0.52	0.6	V
		SDAA, SCLA	I_{OL} = 6mA			0.1	0.2	
V_{OL} – V_{ILc}	Low-level input voltage below low-level output voltage	SDAB, SCLB	ensured by design	2.7V to 5.5V		70		mV
V_{ILC}	SDA and SCL low-level input voltage contention	SDAB, SCLB		2.7V to 5.5V		0.45		V
I_{CC}	Quiescent supply current for V_{CCA}		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				1	mA
I_{CC}	Quiescent supply current		Both channels high, SDAA = SCLA = V_{CCA} and SDAB = SCLB = V_{CCB} and EN = V_{CCB}	5.5V		1.5	5	mA
			Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open			1.5	5	
			In contention, SDAA = SCLA = GND and SDAB = SCLB = GND			3	5	
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}	2.7V to 5.5V			±1	µA
			V_I = 0.2V				10	
		SDAA, SCLA	V_I = V_{CCB}				±1	
			V_I = 0.2V				10	
		EN	V_I = V_{CCB}				±1	
			V_I = 0.2V			–10	–30	
I_{OH}	High-level output leakage current	SDAB, SCLB	V_O = 3.6V	2.7V to 5.5V			10	µA
		SDAA, SCLA					10	
C_I	Input capacitance	EN	V_I = 3V or 0V	3.3V		6	10	pF
		SCLA, SCLB	V_I = 3V or 0V	3.3V		8	13	
				0V		7	11	
C_{IO}	Input/output capacitance	SDAA, SDAB	V_I = 3V or 0V	3.3V		8	13	pF
				0V		7	11	

5.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition(1)	100		ns
t_h	Hold time, EN high after Stop condition(1)	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

5.7 I²C Interface Switching Characteristics

V_{CCB} = 2.7V to 5.5V, GND = 0V, T_A = –40°C to 85°C (unless otherwise noted)(1) (4)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP(5)	MAX	UNIT
t_{PLZ}	Propagation delay		SDAB, SCLB(3) (see Figure 6-4)	SDAA, SCLA(3) (see Figure 6-4)		80	141	350	ns
			SDAA, SCLA(2) (see Figure 6-3)	SDAB, SCLB(2) (see Figure 6-3)		25	74	110	
t_{PZL}	Propagation delay		SDAB, SCLB	SDAA, SCLA	V_{CCA} ≤ 2.7V (see Figure 6-2)	30	76(6)	110	ns
					V_{CCA} ≥ 3V (see Figure 6-2)	10	86	230	
			SDAA, SCLA(2) (see Figure 6-3)	SDAB, SCLB(2) (see Figure 6-3)		60	107	230	
t_{TLH}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7V (see Figure 6-3)	10	12	15	ns
					V_{CCA} ≥ 3V (see Figure 6-3)	40	42	45	
		A side to B-side (see Figure 6-2)				110	125	140	
t_{THL}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7V (see Figure 6-3)	1	52(6)	105	ns
					V_{CCA} ≥ 3V (see Figure 6-3)	20	67	175	
		A side to B-side (see Figure 6-2)				30	48	90	

(1) Times are specified with loads of 1.35kΩ pull-up resistance and 50pF load capacitance on the B-side and 167Ω pull-up and 57pF load capacitance on the A side. Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.
(2) The proportional delay data from A to B-side is measured at 0.3V_{CCA} on the A side to 1.5V on the B-side.
(3) The t_{PLH} delay data from B to A side is measured at 0.4V on the B-side to 0.5V_{CCA} on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
(4) pull-up voltages are V_{CCA} on the A side and V_{CCB} on the B-side.
(5) Typical values were measured with V_{CCA} = V_{CCB} = 3.3V at T_A = 25°C, unless otherwise noted.
(6) Typical value measured with V_{CCA} = 2.7V at T_A = 25°C

5.8 Typical Characteristics

V_{CCA} = 0.9V, V_{CCB} = 2.7V

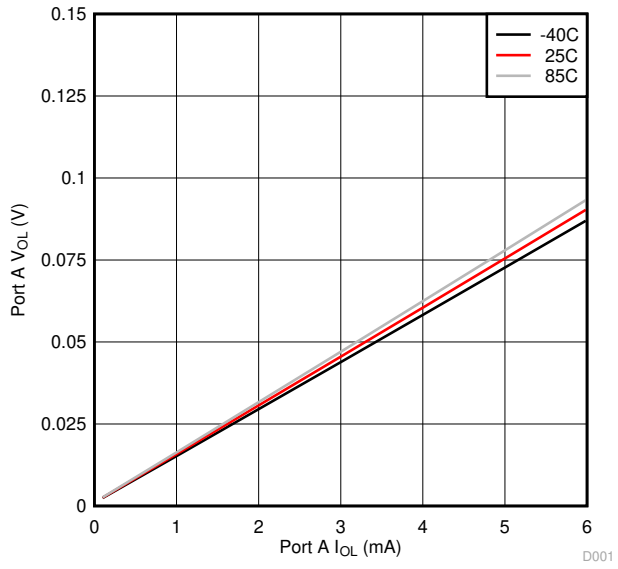


Figure 5-1. Port A V_{OL} vs I_{OL}

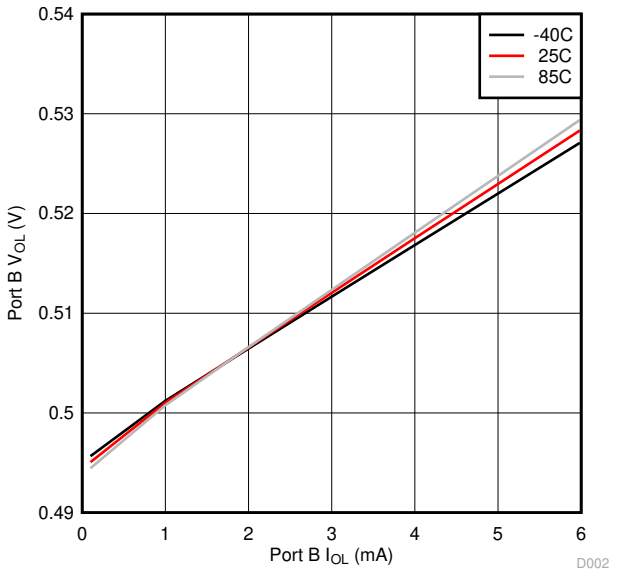
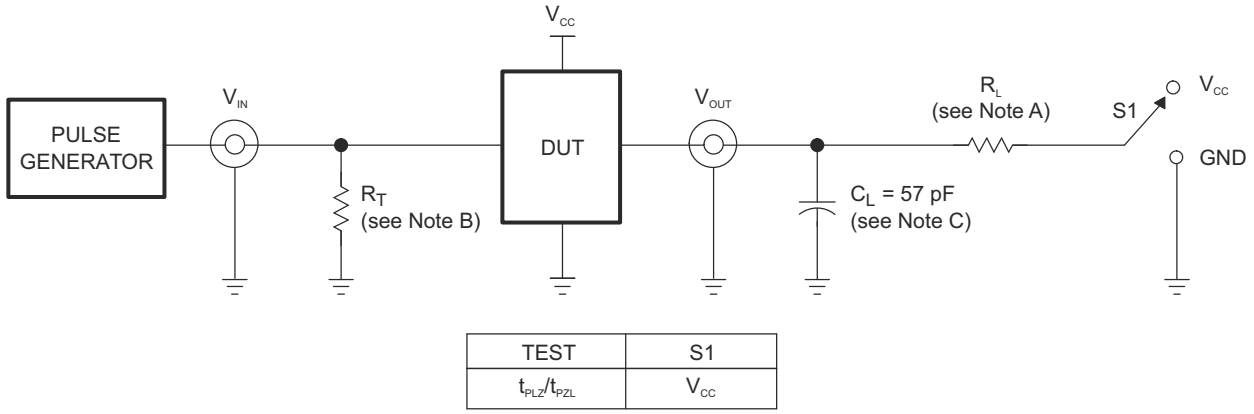


Figure 5-2. Port B V_{OL} vs I_{OL}

6 Parameter Measurement Information



TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

A. R_L = 167Ω (0.9V to 2.7V) and R_L = 450Ω (3.0V to 5.5V) on the A side and 1.35kΩ on the B-side
B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
C. C_L includes probe and jig capacitance.
D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
E. The outputs are measured one at a time, with one transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
H. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-1. Test Circuit

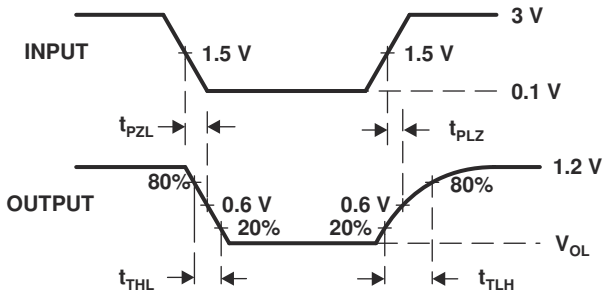


Figure 6-2. Waveform 1 – Propagation Delay and Transition Times for B-side to A-side

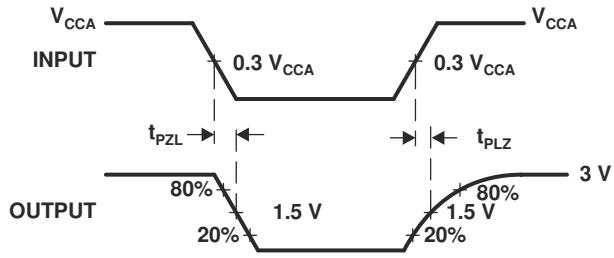


Figure 6-3. Waveform 2 – Propagation Delay and Transition Times for A-side to B-side

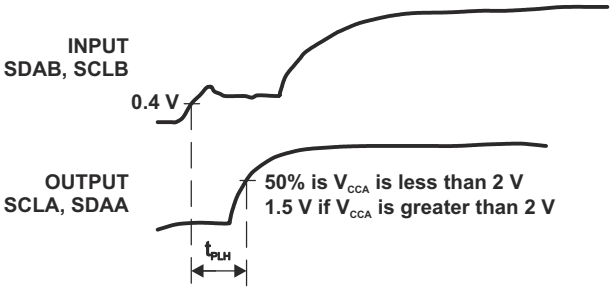


Figure 6-4. Waveform 3 – Propagation Delay for B-side to A-side

7 Detailed Description

7.1 Overview

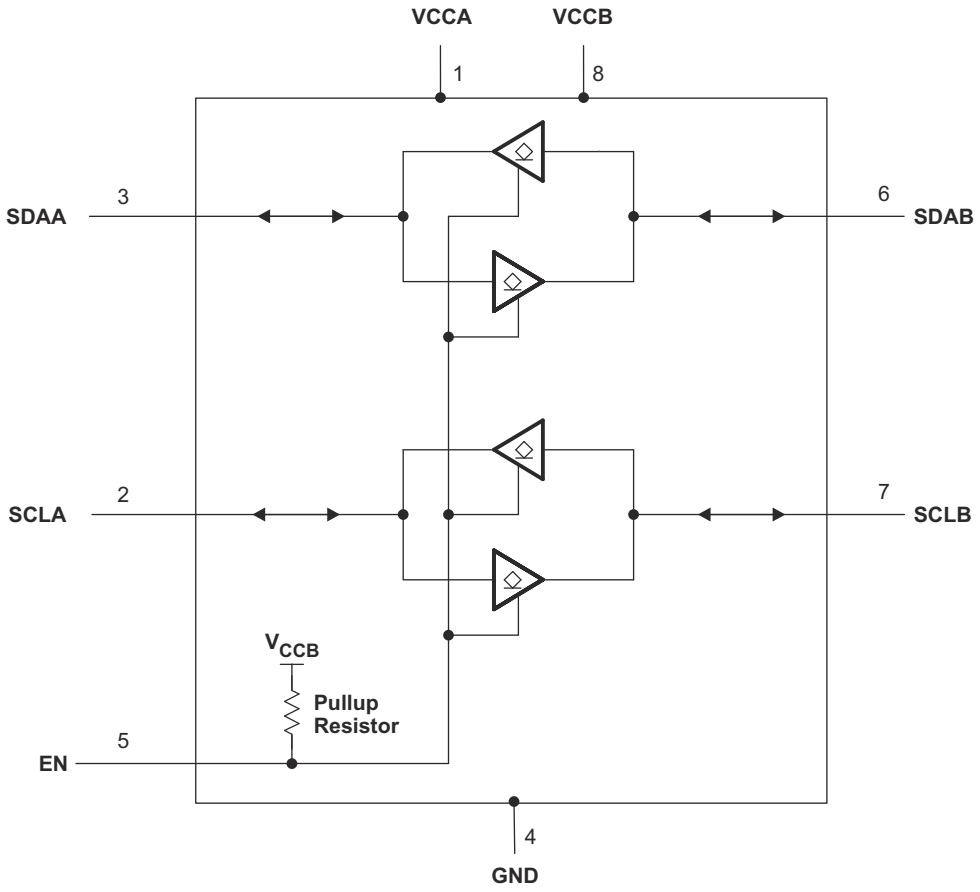
The TCA9517A is a bidirectional buffer with level shifting capabilities for I^2C and SMBus systems. It provides bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9V) and higher voltages (2.7V to 5.5V) in mixed-mode applications. This device enables I^2C and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517A buffers both the serial data (SDA) and the serial clock (SCL) signals on the I^2C bus, thus allowing two buses of up to 400pF bus capacitance to be connected in an I^2C application.

The TCA9517A has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.5V, even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0V).

The TCA9517A offers a higher contention level threshold, V_{ILC}, than the TCA9517, which allows connections to targets which have weaker pull-down ability.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Two-Channel Bidirectional Buffer

The TCA9517A is a two-channel bidirectional buffer with level-shifting capabilities

7.3.2 Active-High Repeater-Enable Input

The TCA9517A has an active-high enable (EN) input with an internal pull-up to V_{CCB}, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved target on power-up reset. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

7.3.3 V_{OL} B-Side Offset Voltage

The B-side drivers operate from 2.7V to 5.5V. The output low level for this internal buffer is approximately 0.5V, but the input voltage must be 70mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design prevents 2 B-side ports from being connected to each other.

7.3.4 Standard Mode and Fast Mode Support

The TCA9517A supports standard mode as well as fast mode I^2C. The maximum system operating frequency will depend on system design and the delays added by the repeater.

7.3.5 Clock Stretching Support

The TCA9517A can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the target and controller. This is best done by increasing the pull-up resistor value.

7.4 Device Functional Modes

Table 7-1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A typical application is shown in Figure 8-1. In this example, the system controller is running on a 3.3V I^2C bus, and the target is connected to a 1.2V I^2C bus. Both buses run at 400kHz. Controller devices can be placed on either bus.

The TCA9517A is 5V tolerant, so it does not require any additional circuitry to translate between 0.9V to 5.5V bus voltages and 2.7V to 5.5V bus voltages.

When the A side of the TCA9517A is pulled low by a driver on the I^2C bus, a comparator detects the falling edge when it goes below 0.3 × V_{CCA} and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5V. When the B-side of the TCA9517A falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 8-3 and Figure 8-4. If the bus controller in Figure 8-1 were to write to the target through the TCA9517A, waveforms shown in Figure 8-3 would be observed on the A bus. This looks like a normal I^2C transmission, except that the high level may be as low as 0.9V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the TCA9517A, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9517A. After the eighth clock pulse, the data line is pulled to the V_{OL} of the target device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9517A for a short delay, while the A-bus side rises above 0.3 × V_{CCA} and then continues high.

8.2 Typical Application

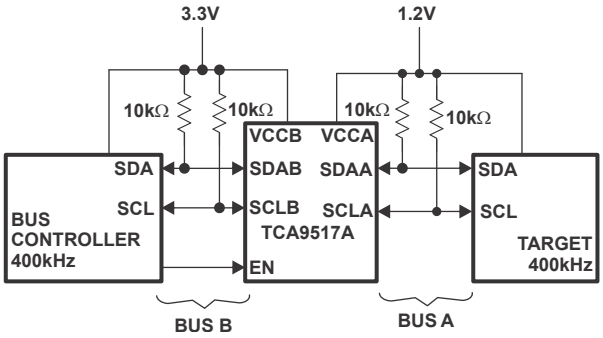


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

For the level translating application, the following should be true:

- V_{CCA} = 0.9V to 5.5V
- V_{CCB} = 2.7V to 5.5V
- B-side ports must not be connected together

8.2.2 Detailed Design Procedure

8.2.2.1 Clock Stretching Support

The TCA9517A can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the target and controller. This is best done by increasing the pull-up resistor value.

8.2.2.2 V_{ILC} and Pullup Resistor Sizing

For the TCA9517A to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the B-side must be below 0.45V.

V_{OL} of a device can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistance value. The pull-up resistance on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

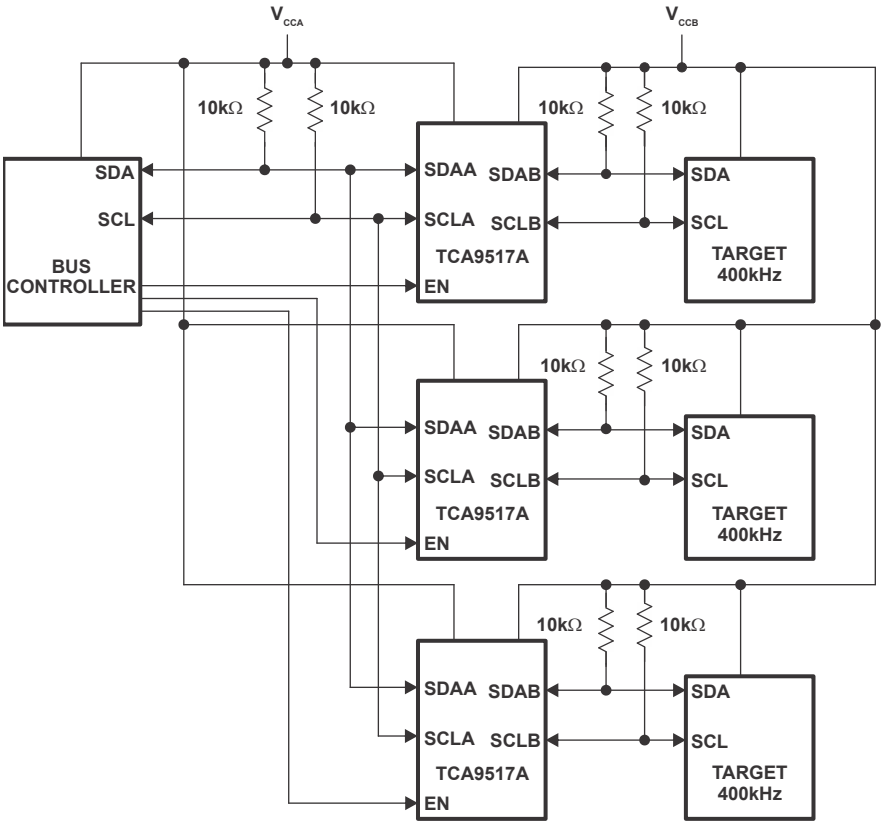


Figure 8-2. Typical Star Application

Multiple A sides of TCA9517As can be connected in a star configuration, allowing all nodes to communicate with each other.

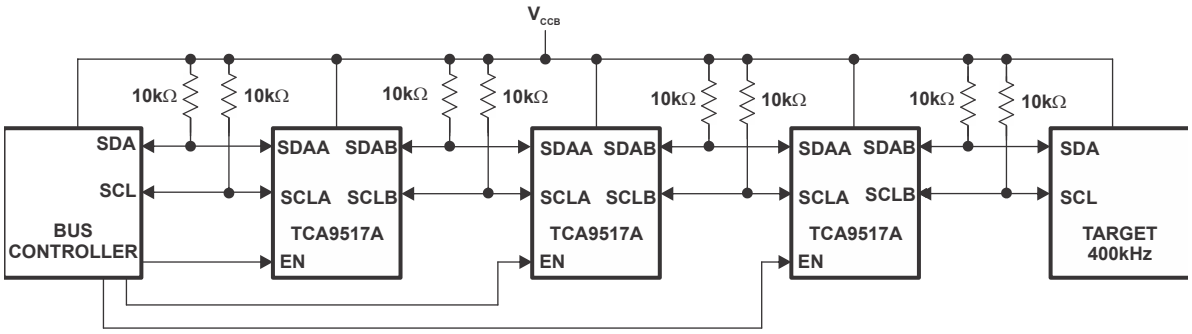


Figure 8-3. Typical Series Application

To further extend the I^2C bus for long traces/cables, multiple TCA9517As can be connected in series as long as the A-side is connected to the B-side. I^2C bus target devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

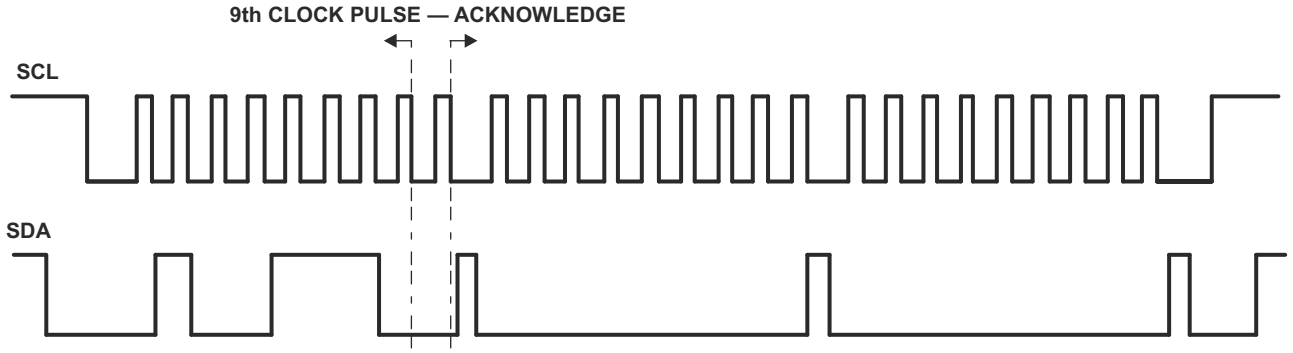


Figure 8-4. Bus A (0.9V to 5.5V Bus) Waveform

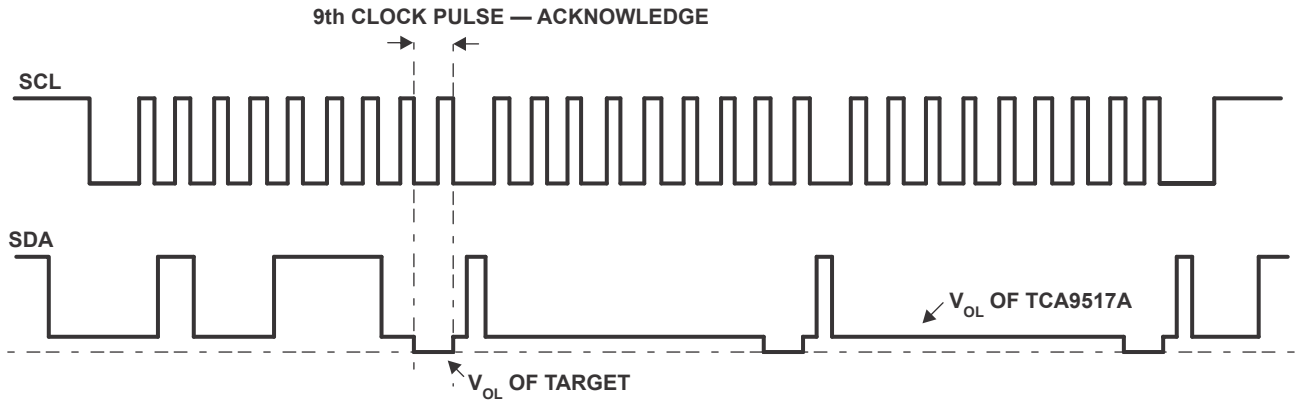


Figure 8-5. Bus B (2.7V to 5.5V Bus) Waveform

8.2.3 Application Curve

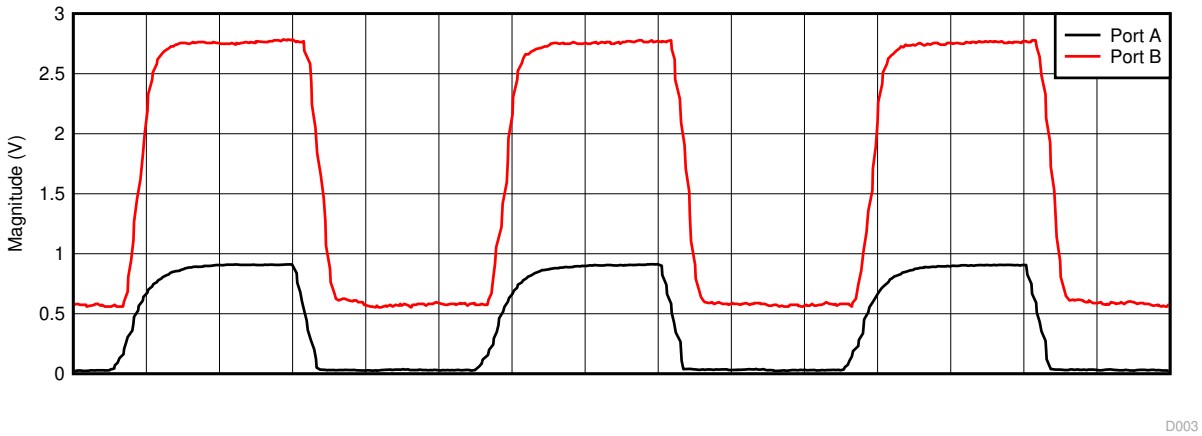


Figure 8-6. Voltage Translation at 400kHz, V_{CCA} = 0.9V, V_{CCB} = 2.7V

9 Power Supply Recommendations

V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9517A includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5V and the V_{CCA} is above 0.8V. After power up and with the EN high, a low level on the A-side (below 0.3 × V_{CCA}) turns the corresponding B-side driver (either SDA or SCL) on and drives the B-side down to approximately 0.5V. When the A-side rises above 0.3 × V_{CCA}, the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the B-side falls first and goes below 0.3 × V_{CCB}, the A-side driver is turned on and the A-side pulls down to 0V. The B-side pull-down is not enabled unless the B-side voltage goes below 0.4V. If the B-side low voltage does not go below 0.5V, the A-side driver turns off when the B-side voltage is above 0.7 × V_{CCB}. If the B-side low voltage goes below 0.4V, the B-side pull-down driver is enabled, and the B-side is able to rise to only 0.5V until the A-side rises above 0.3 × V_{CCA}.

TI recommends using a decoupling capacitor and placing it close to the VCCA and VCCB pins of a value of about 100nF.

10 Layout

10.1 Layout Guidelines

There are no special layout procedures required for the TCA9517A. It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

10.2 Layout Example

Figure 10-1 shows an example layout of the DGK package.

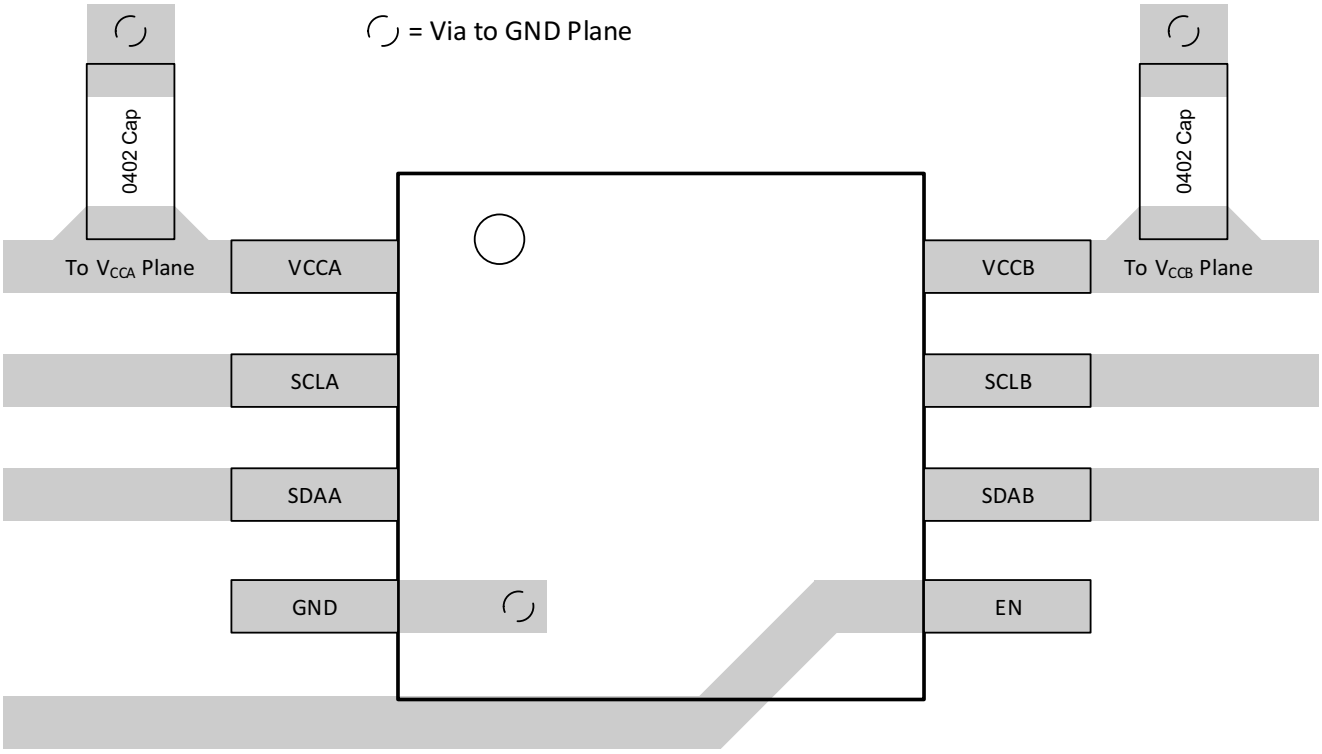


Figure 10-1. TCA9517A Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2024) to Revision E (October 2025)	Page
• Updated the *Package Information* table	1
• Updated Tape and Reel Information	20

Changes from Revision C (December 2018) to Revision D (September 2024)	Page
• Updated Tape and Reel Information	20
• Updated Mechanical Data	22

Changes from Revision B (June 2015) to Revision C (December 2018)	Page
• Changed the appearance of the DGK pin out image	4
• Deleted $V_{CCA} < V_{CCB}$ from the *Design Requirements* list	13

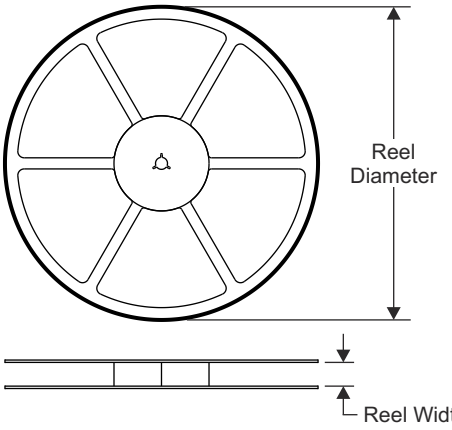
Changes from Revision A (April 2013) to Revision B (June 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

13 Mechanical, Packaging, and Orderable Information

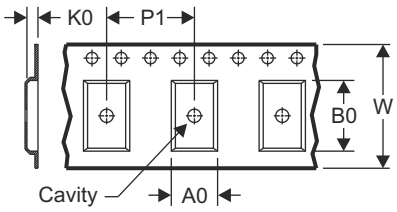
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Tape and Reel Information

REEL DIMENSIONS

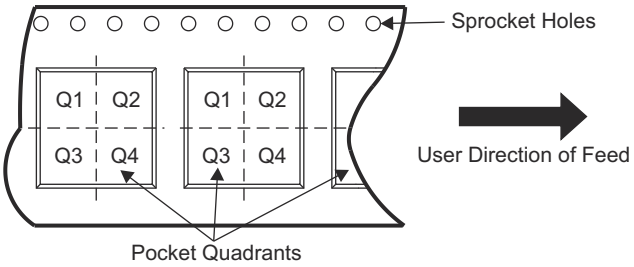


TAPE DIMENSIONS



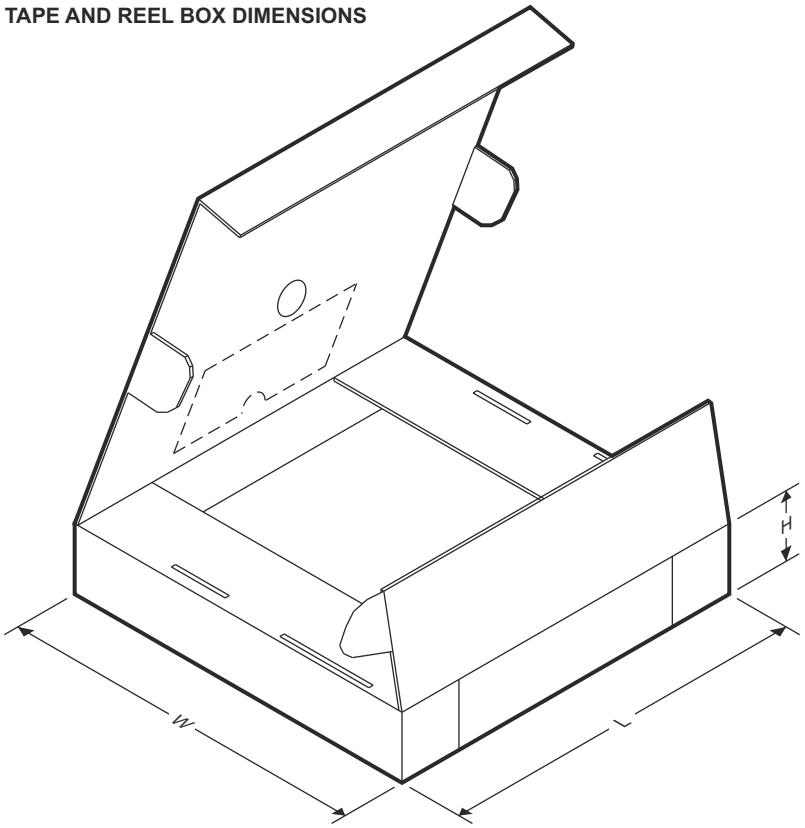
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9509MRVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q1
TCA9509RVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q3
TCA9509DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

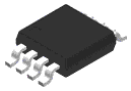
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9509MRVHR	X2QFN	RVH	8	5000	183.0	183.0	20.0
TCA9509RVHR	X2QFN	RVH	8	5000	202.0	201.0	28.0
TCA9509DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0

13.2 Mechanical Data

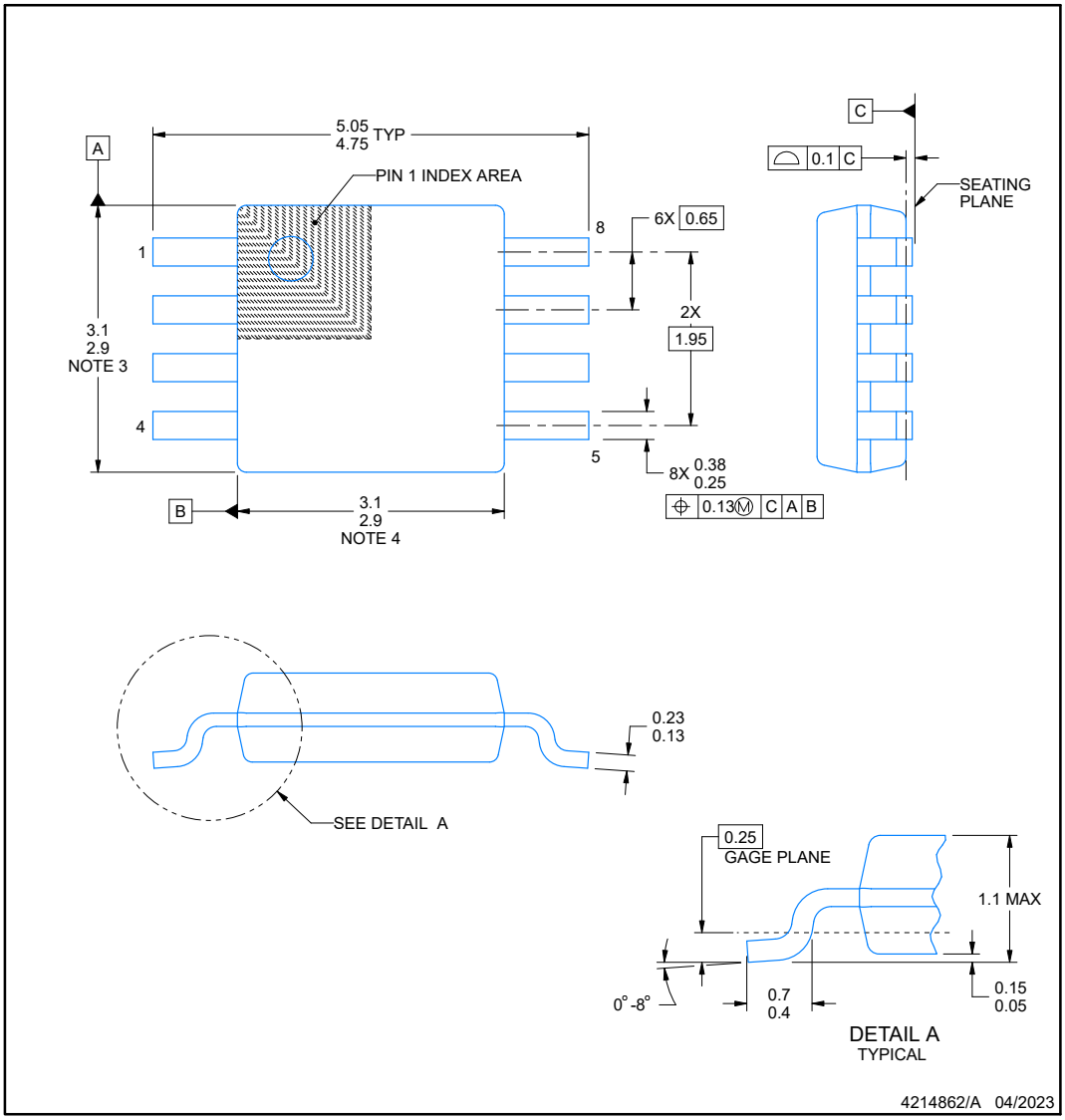
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

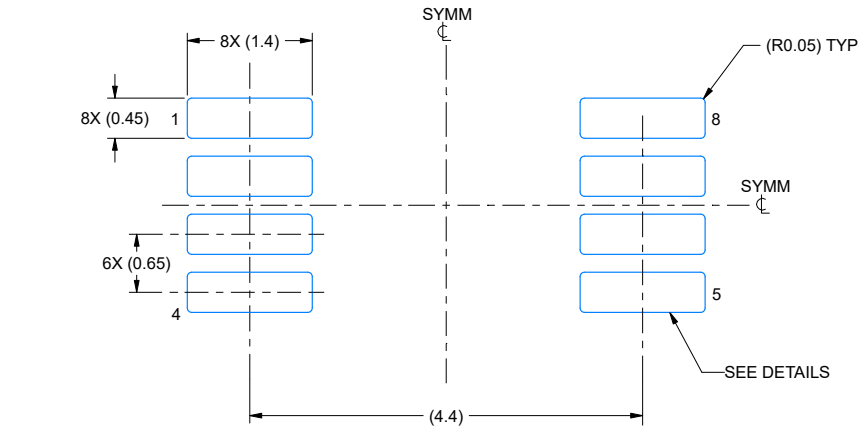
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

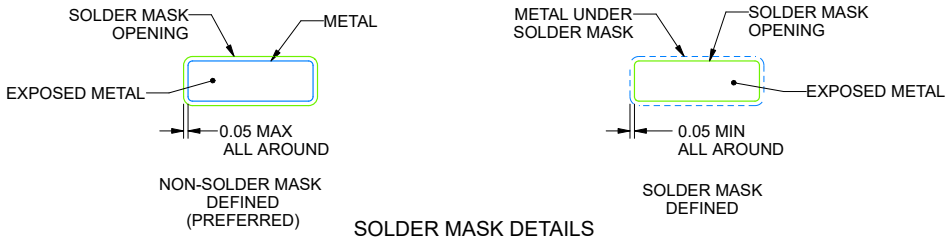
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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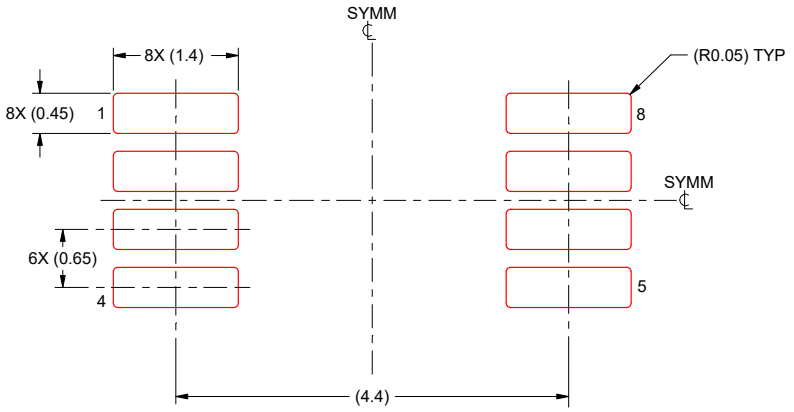
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A ™ **VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA9517ADGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BSK
TCA9517ADGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BSK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

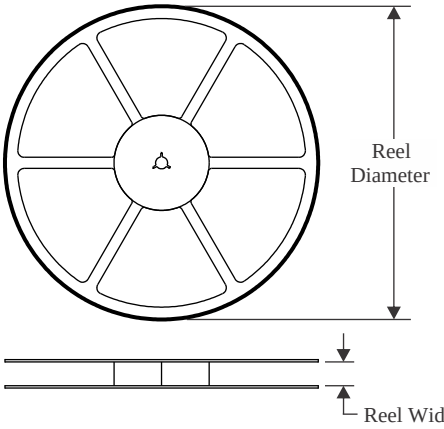
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

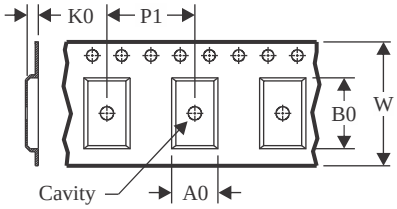
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



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B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
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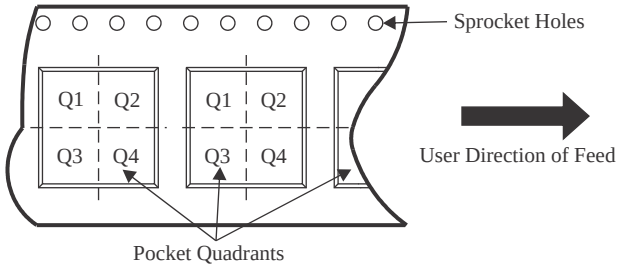
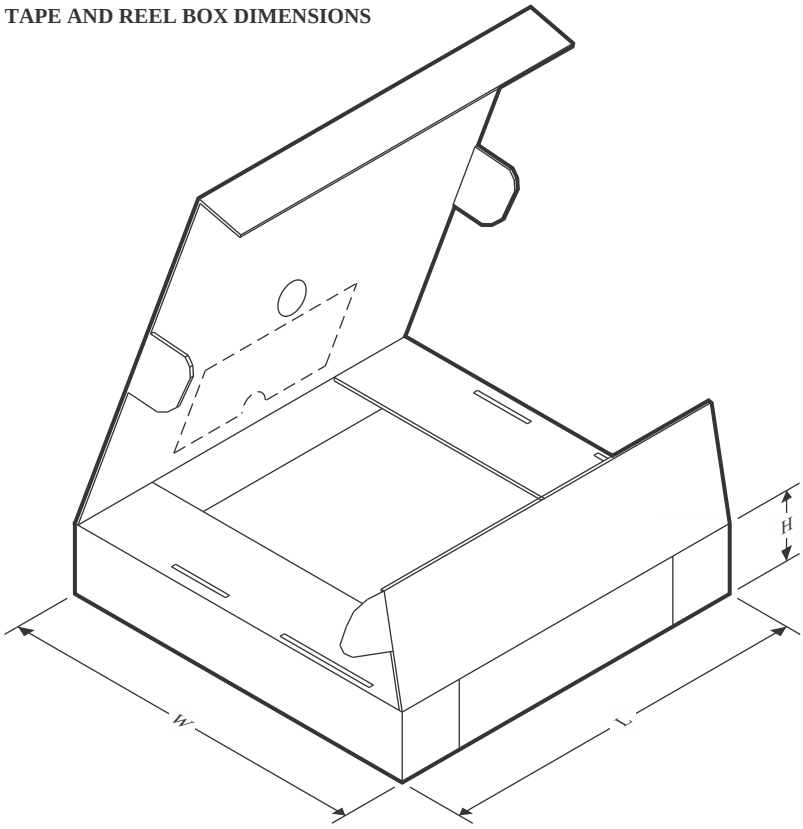
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9517ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TCA9517ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

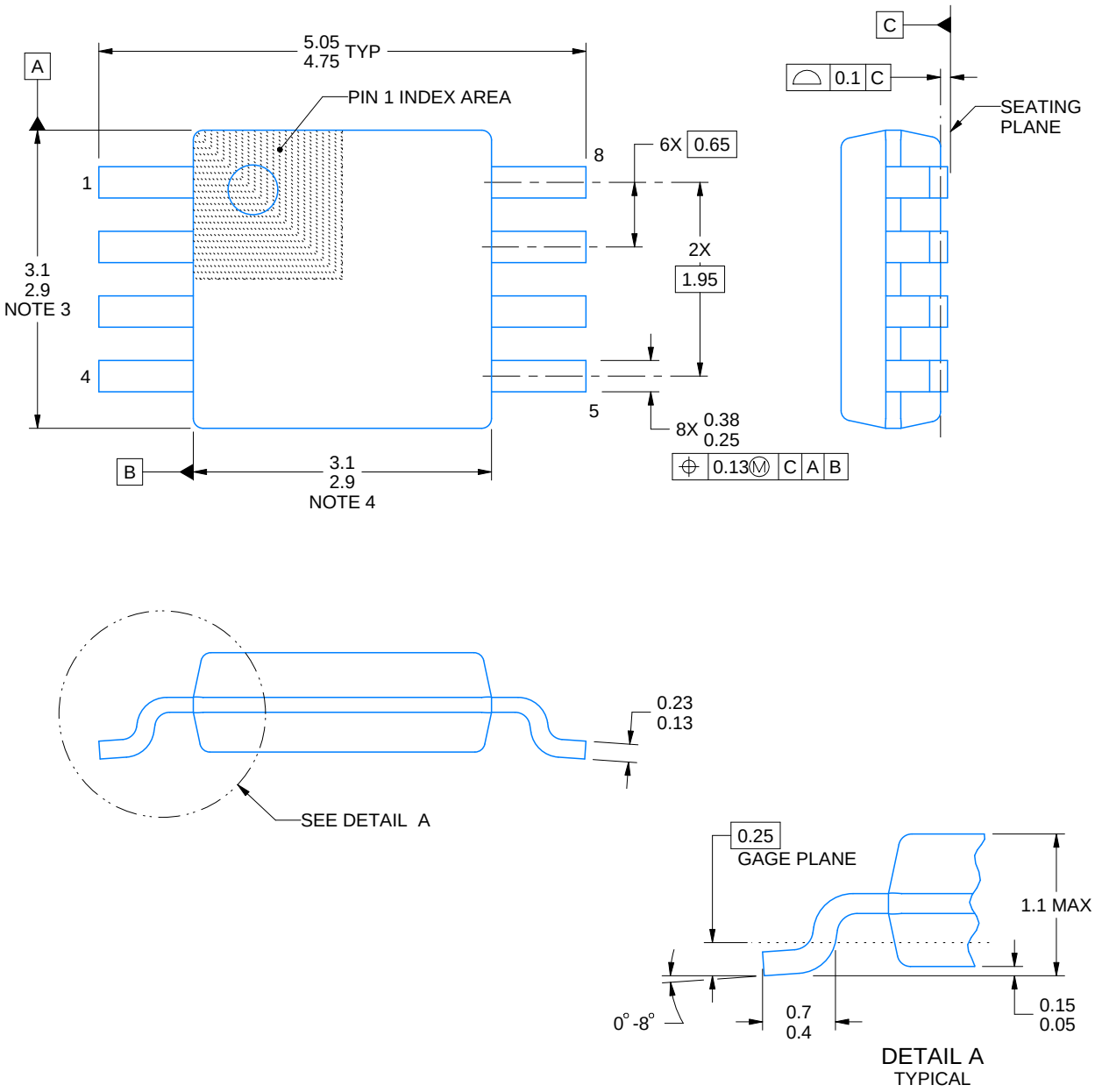
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9517ADGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TCA9517ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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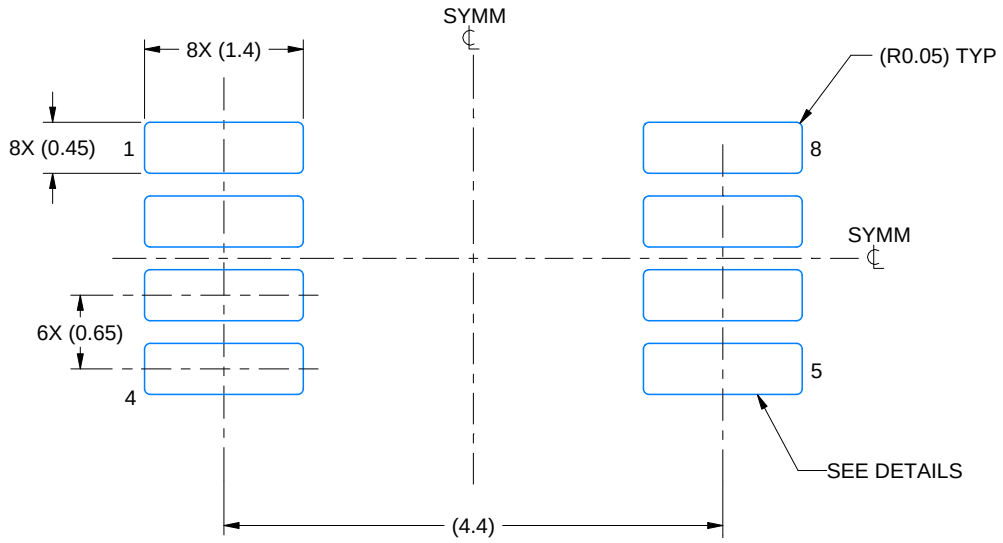
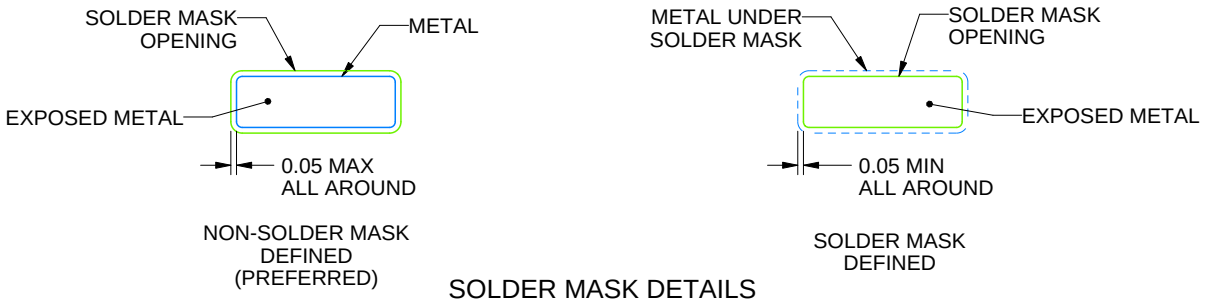


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

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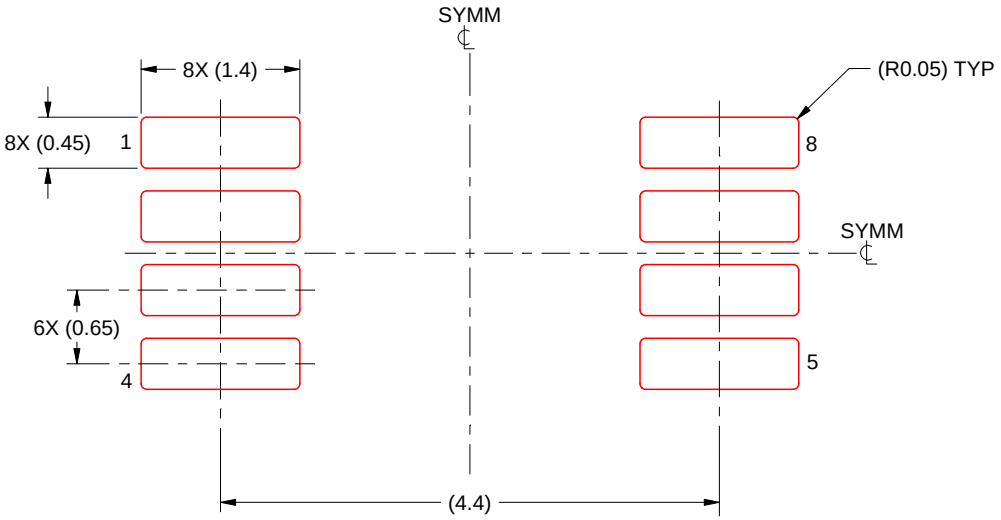

SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

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Last updated 10/2025