TAS6754-Q1 1L Modulation, 2MHz Digital Input 4-Channel Automotive Class-D Audio Amplifier with Current Sense and Real-time Load Diagnostics

1 Features

- AEC-Q100 qualified for Automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
- General operation
  - 4.5V to 19V supply voltage, 40V load dump
  - Low latency path reducing group delay by >70% at 48kHz
  - Support for 1.8V and 3.3V I/O's
  - I^2C control with 8 address options
- 1L Modulation
  - Requires only one inductor per channel saving four inductors vs a traditional design
  - Lower system component cost for inductors
  - Smaller PCB footprint
- Audio Performance
  - THD+N 0.03% (4Ω, 1W, 1kHz)
  - Output noise: 35μV_{RMS} at 14.4V, A-weighting
  - Efficiency > 87% @ 4×25W, 4Ω, 14.4V
- Output current sensing by channel via I^2S or TDM
  - No external circuitry needed
- Real-time load diagnostics
  - Monitor output conditions while playing audio
  - Open load and shorted load detection
- DC and AC Standby load diagnostics
- Audio inputs
  - 2-4 channel via I^2S or 4-16 channel via TDM
  - Input sample rates: 44.1, 48, 96, 192kHz
- Audio outputs
  - 4 channel bridge-tied load (BTL)
  - 2MHz output switching frequency
  - 4×30W (4Ω, 14.4V, 1kHz, 10% THD+N)
  - 4×50W (2Ω, 14.4V, 1kHz, 10% THD+N)
- Advanced spread-spectrum and selectable phase offset
- Protection and Monitoring
  - Cycle-by-cycle current limiting
  - Output short protection
  - Clip detection with configurable thresholds
  - Thermal foldback and PVDD foldback
  - I^2C temperature and supply voltage readout
  - Configurable overtemperature warning and individual channel shutdown
  - DC offset, undervoltage and overvoltage

2 Applications

- Automotive head unit
- Automotive external amplifier
- Acoustic vehicle alerting system (AVAS)

3 Description

The TAS6754-Q1 is a four-channel digital-input Class-D audio amplifier that implements 1L modulation only requiring one inductor per BTL channel reducing system size and cost by removing four inductors compared to a traditional design. Additionally, 1L modulation lowers switching losses compared to traditional Class-D modulation schemes.

The TAS6754-Q1 integrates DC and AC Load Diagnostics to determine the status of the connected loads. During audio playback this status can be monitored through output current sense which is available for each channel and reports the measurement to a host processor through TDM with minimal delay. The device monitors the output load condition while playing audio through real-time load diagnostics independent of the host and audio input.

The TAS6754-Q1 device features an additional low latency signal path for each channel, providing up to 70% faster signal processing at 48kHz which enables time-sensitive Active Noise Cancellation (ANC), Road Noise Cancellation (RNC) applications.

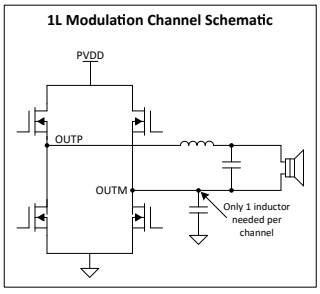
The device supports global temperature, channel temperature and PVDD values via I^2C readout for easy system level thermal management.

The device is offered in a 56 pin HSSOP package with the exposed thermal pad up.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TAS6754-Q1	HSSOP (56)	18.42mm × 10.35mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Channel Schematic

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4 Pin Configuration and Functions

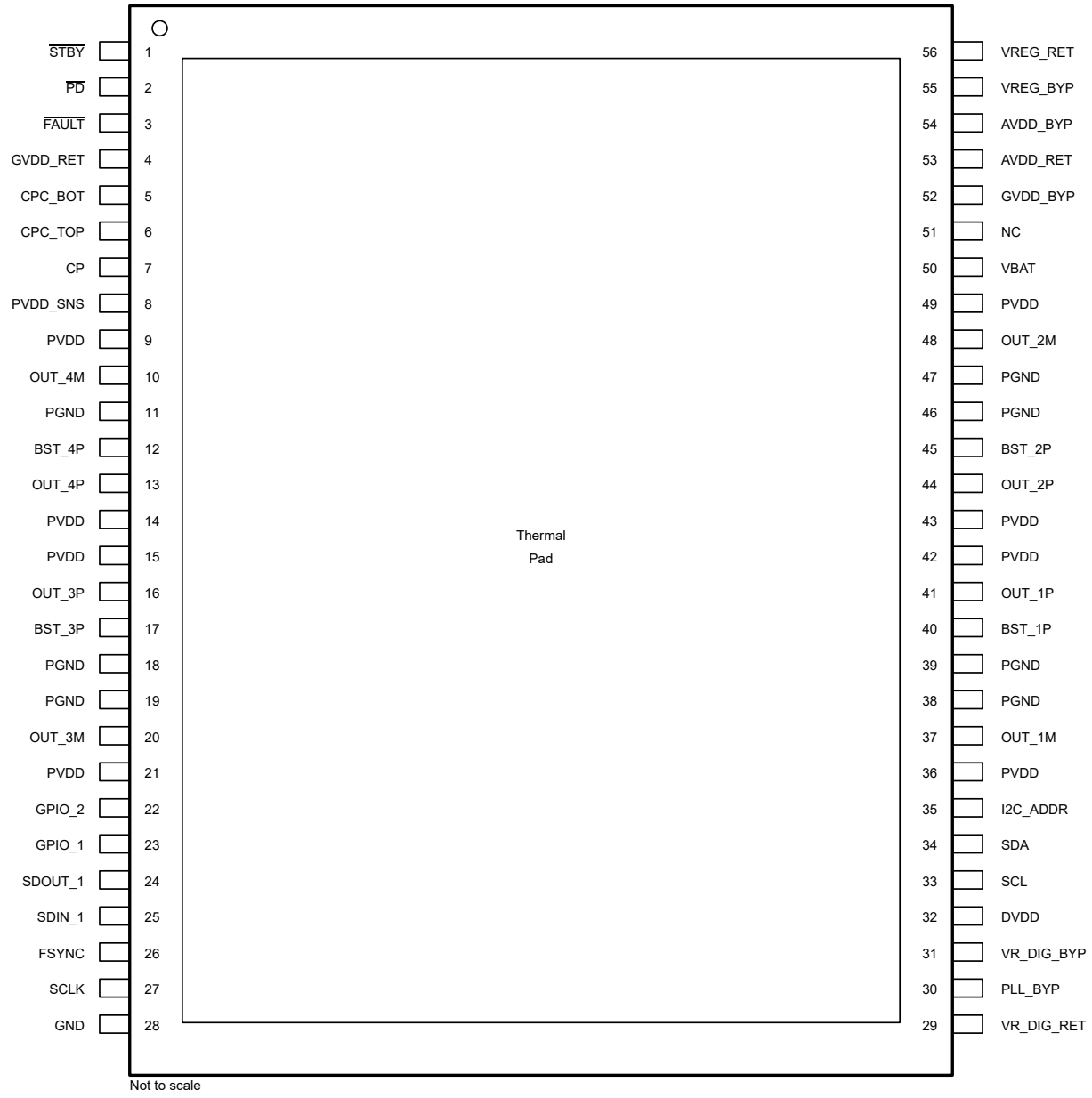


Figure 4-1. DKQ Package, 56-Pin HSSOP with exposed Thermal Pad Up, Top View

Table 4-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
AVDD_BYP	54	PWR	Voltage regulator bypass. Connect 1µF capacitor from AVDD_BYP to AVDD_RET
AVDD_RET	53	PWR	AVDD bypass capacitor return
BST_1P	40	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_2P	45	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_3P	17	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_4P	12	PWR	Bootstrap capacitor connection pins for high-side gate driver
CP	7	PWR	Top of main storage capacitor for charge pump. Connect 330nF capacitor from pin to PVDD
CPC_BOT	5	PWR	Bottom of flying capacitor for charge pump. Connect 100nF capacitor from pin to CPC_TOP pin

Table 4-1. Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
CPC_TOP	6	PWR	Top of flying capacitor for charge pump. Connect 100nF capacitor from pin to CPC_BOT pin
DVDD	32	PWR	DVDD supply input
$\overline{\text{FAULT}}$	3	DO	Reports a fault (active low, open drain), 100kΩ internal pull-up resistor
FSYNC	26	DI	Audio frame clock input
GND	28	GND	Ground
GPIO_1	23	DI/O	General purpose IO, function set by register programming
GPIO_2	22	DI/O	General purpose IO, function set by register programming
GVDD_BYP	52	PWR	Gate drive voltage regulator derived from VBAT input pin. Connect 2.2µF capacitor to GVDD_RET
GVDD_RET	4	PWR	GVDD bypass capacitor return
I2C_ADDR	35	DI	I^2C address pin
NC	51	NC	No internal connection. Leave unconnected or connect to ground.
OUT_1M	37	PWR	Negative output for the channel
OUT_1P	41	PWR	Positive output for the channel
OUT_2M	48	PWR	Negative output for the channel
OUT_2P	44	PWR	Positive output for the channel
OUT_3M	20	PWR	Negative output for the channel
OUT_3P	16	PWR	Positive output for the channel
OUT_4M	10	PWR	Negative output for the channel
OUT_4P	13	PWR	Positive output for the channel
$\overline{\text{PD}}$	2	DI	Shuts down the device for minimal power draw (active low), 110kΩ internal pull-down resistor
PGND	11,18,19,38,39,46,47	GND	Ground
PLL_BYP	30	PWR	PLL supply bypass, derived from DVDD input
PVDD	9,14,15,21,36,42,43, 49	PWR	PVDD voltage input (can be connected to battery)
PVDD_SNS	8	PWR	PVDD input for sensitive internal circuits. Keep at the same voltage level as PVDD
SCL	33	DI	I^2C clock input
SCLK	27	DI	Audio input serial clock
SDA	34	DI/O	I^2C data input and output
SDIN_1	25	DI	TDM data input and audio I^2S data input for channels 1 and 2
SDOUT_1	24	DO	I^2S / TDM data output
$\overline{\text{STBY}}$	1	DI	Enables low power DEEP SLEEP state (active low), 110kΩ internal pull-down resistor
VBAT	50	PWR	Battery voltage input
VR_DIG_BYP	31	PWR	DSP core regulator output. Connect 1uF to GND.
VR_DIG_RET	29	PWR	VR_DIG bypass capacitor return
VREG_BYP	55	PWR	5V Internal voltage regulator
VREG_RET	56	PWR	VREG bypass capacitor return
Thermal Pad	-	GND	Provides electrical and thermal connection for the device. Heatsink must be connected to GND.

(1) DI = digital input, DO = digital output, DI/O = digital input/output, GND = ground, NC = no connect, NO = negative output, PO = positive output, PWR = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
PVDD, VBAT	DC supply-voltage range relative to GND		-0.3	30	V
V_{MAX}	Transient supply voltage - PVDD, VBAT	t ≤ 400 ms exposure	-1	40	V
V_{RAMP}	Supply-voltage ramp rate - PVDD, VBAT			75	V/ms
DVDD	DC supply voltage range relative to GND		-0.3	3.9	V
I_{MAX}	Maximum current per pin - PVDD, VBAT, GND, OUT_xP, OUT_xM			±9	A
I_{MAX_PULSED}	Pulsed supply current per PVDD pin (one shot)	t < 100 ms		±12	A
I_{MAX_Peak}	Maximum peak current per pin - OUT_xP, Out_xM	t < 100 ms		±12	A
V_{LOGIC}	Input voltage for logic pins - SCL, SDA, $\overline{FAULT}$, $\overline{STBY}$, GPIOx		–0.3	DVDD + 0.5	V
V_{GND}	Maximum voltage between GND pins			±0.3	
T_J	Maximum operating junction temperature range		–55	175	°C
T_{stg}	Storage temperature range		–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
PVDD	Output FET Supply Voltage Range	Relative to GND	4.5	14.4	19	V
VBAT	Battery Supply Voltage Input	Relative to GND	4.5	14.4	19	V
DVDD	DC Logic supply	Relative to GND	1.62		3.6	V
T_A	Ambient temperature		–40		125	°C
T_J	Junction temperature	An adequate thermal design is required	–40		175	
R_L	Nominal speaker load impedance	BTL Mode	2	4		Ω
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
C_{Bypass}	External capacitance on bypass pins	Pin 30, 31, 32, 54, 55		1		µF
C_{GVDD}	External capacitance on GVDD pins	Pin 52		2.2		µF
L_O	OUTP output filter inductance - I_{SD}	Minimum output filter inductance at I_{SD} current levels. Applies to short to ground or short to power protection.	1			µH

5.3 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±3500	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.4 Thermal Information

THERMAL METRIC[1]		TAS6754-Q1[2]	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) JEDEC Standard, 4-Layer PCB.

5.5 Electrical Characteristics

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = 14.4V, VBAT = 14.4V, DVDD = 1.8V, R_L = 4Ω, P_{out} = 1W/ch, f_{out} = 1kHz, F_{sw} = 2.048MHz, AES17 Filter, reconstruction filter inductor used: 3.3µH-VCMT053T-3R3MN5 and 1µF, default I^2C settings + start-up script, see application diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{DVDD}	DVDD supply current	All channels playing, -60dB Signal		22	28	mA
		All channels playing, -60dB Signal, DVDD = 3.3V		22		
I_{PVDD_IDLE}	PVDD idle current	All channels playing, no audio input, F_{SW} = 2.048MHz		47	60	mA
I_{VBAT_IDLE}	VBAT idle current	All channels playing, no audio input, F_{SW} = 2.048MHz		115	130	mA
$I_{PVDD\_Shutdown}$	PVDD shutdown current	$\overline{PD}$ active, DVDD = 0V		4	5	µA
$I_{VBAT\_Shutdown}$	VBAT shutdown current	$\overline{PD}$ active, DVDD = 0V		5	7	µA
$I_{TOTAL\_Shutdown}$	PVDD+VBAT shutdown current	$\overline{PD}$ active, DVDD = 0V			12	µA
$I_{DVDD\_Shutdown}$	DVDD shutdown current	$\overline{PD}$ active, DVDD = 1.8V		1	3	µA
		$\overline{PD}$ active, DVDD = 3.3V		1	3	
OUTPUT POWER						
P_{O_BTL}	Output power per channel, BTL	4Ω, PVDD = 14.4V, THD+N = 1%,T_C = 75°C	21	23		W
		4Ω, PVDD = 14.4V, THD+N = 10%,T_C = 75°C	26	30		
		4Ω, PVDD = 18V, THD+N = 1%,T_C = 75°C	33	37		
		4Ω, PVDD = 18V, THD+N = 10%,T_C = 75°C	41	46		
		2Ω, PVDD = 14.4V, THD+N = 1%,T_C = 75°C	37	40		
		2Ω, PVDD = 14.4V, THD+N = 10%,T_C = 75°C	44	50		
EFF_P	Power efficiency	4 channels operating, 25W output power per channel, R_L = 4Ω, PVDD = 14.4V, T_C = 25°C; (includes output filter losses)		87		%
AUDIO PERFORMANCE						
V_n	Output noise voltage	Zero input, A-weighting, Gain = -5dB to match PVDD of 14.4V		35		µV
G	Gain	Peak output voltage at full scale digital input		28		V/FS
THD+N	Total harmonic distortion + noise			0.03		%
		20Hz to 20kHz		0.08		%
F_{BW}	Frequency response	20Hz to 20kHz, without LC filter impact or integrated compensation		0.5		dB
G_{MUTE}	Output attenuation	Assert $\overline{MUTE}$ and compare to amp playing 1W audio into 4Ω		100		dB
Crosstalk	Channel crosstalk	PVDD = 14.4Vdc, f = 1kHz		-90	-80	dB
PSRR	Power-supply rejection ratio	PVDD = 14.4Vdc + 1V_{RMS}, f = 1kHz		-75		dB
DIGITAL INPUT PINS						
V_{IH}	Input logic level high		70			%DVDD
V_{IL}	Input logic level low				30	
I_{IH}	Input logic current	V_I = DVDD			15	µA
I_{IL}		V_I = 0			-15	
DIGITAL OUTPUT PINS						
V_{OH}	Output voltage for logic level high	I = ±1mA	90			%DVDD
V_{OL}	Output voltage for logic level low				10	
V_{OH}	Output voltage for logic level high	DVDD = 3.3V, I = ±2mA	90			%DVDD
V_{OL}	Output voltage for logic level low	DVDD = 3.3V, I = ±2mA			10	%DVDD
BYPASS VOLTAGES						
V_{GVDD}	Gate drive bypass pin voltage			5		V
V_{AVDD_BYP} , V_{VREG_BYP}	Analog bypass pins voltage			5		V
V_{DVDD_BYP}, V_{PLL_BYP}, V_{VR_DIG}	Digital bypass pins voltage			1.5		V
OVERVOLTAGE (OV) PROTECTION						
$PVDD_{OV\_SET}$	PVDD overvoltage shutdown set		19.1	20	21	V
$PVDD_{OV\_HYS}$	PVDD overvoltage recovery hysteresis			0.5		V

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = 14.4V, VBAT = 14.4V, DVDD = 1.8V, R_L = 4Ω, P_{out} = 1W/ch, f_{out} = 1kHz, F_{sw} = 2.048MHz, AES17 Filter, reconstruction filter inductor used: 3.3µH-VCMT053T-3R3MN5 and 1µF, default I^2C settings + start-up script, see application diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VBAT_{OV\_SET}$	VBAT overvoltage shutdown set		19.1	20	22	V
$VBAT_{OV\_HYS}$	VBAT overvoltage recovery hysteresis			0.5		V
UNDERVOLTAGE (UV) PROTECTION						
$PVDD_{UV\_SET}$	PVDD undervoltage shutdown set		3.5	4	4.5	V
$PVDD_{UV\_HYS}$	PVDD undervoltage recovery hysteresis			0.5		V
$VBAT_{UV\_SET}$	VBAT undervoltage shutdown set		3.5	4	4.5	V
$VBAT_{UV\_HYS}$	VBAT undervoltage recovery hysteresis			0.5		V
$DVDD_{UV\_SET}$	DVDD undervoltage shutdown set		1.4		1.59	V
POWER-ON RESET (POR)						
V_{POR_SET}	DVDD power on reset set	Increasing DVDD	0.9		1.51	V
V_{POR_HYS}	DVDD power on reset recovery hysteresis			0.2		V
V_{POR_OFF}	DVDD power off threshold	Decreasing DVDD	0.5		1.3	V
OVERTEMPERATURE (OT) PROTECTION and Temperature Sensing						
OTSD(i)	Per channel over-temperature shutdown			175		°C
OTW	Global junction over-temperature warning			135		°C
OTSD	Global junction over-temperature shutdown			155		°C
OT_{HYS_Global}	Over-temperature recovery hysteresis			15		°C
OT_{HYS_Local}	Over-temperature recovery hysteresis			15		°C
LOAD OVERCURRENT PROTECTION						
I_{LIM}	Overcurrent cycle-by-cycle limit	OC Level 1	2.5	3.5		A
		OC Level 2	3.3	4.3		
		OC Level 3	4.6	5.6		
		OC Level 4	6.3	6.7		
I_{SD}	Overcurrent shutdown	OC Level 1, Any short to supply, ground, or other channels		5		A
		OC Level 2, Any short to supply, ground, or other channels		6		
		OC Level 3, Any short to supply, ground, or other channels		8		
		OC Level 4, Any short to supply, ground, or other channels		9		
CLICK AND POP						
V_{CP_Multi}	Output click and pop voltage	ITU-R 2k filter, Hi-Z to PLAY, PLAY to Hi-Z, Multistep turn on, PVDD = 14.4V		5		mV
DC OFFSET						
V_{OFFSET}	Output offset voltage	T_C = 50°C		2	5	mV
DC DETECT						
DC_{FAULT}	Output DC fault protection		1.4	2	2.5	V
LOAD DIAGNOSTICS						
S2P	Maximum resistance to detect a short from OUT pin(s) to PVDD		2000			Ω
S2G	Maximum resistance to detect a short from OUT pin(s) to ground		200			Ω
SL	Shorted load detection tolerance	Other channels in Hi-Z		±0.5		Ω
OL	Open Load (OL) Detection Threshold	Other channels in Hi-Z		40		Ω

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = 14.4V, VBAT = 14.4V, DVDD = 1.8V, R_L = 4Ω, P_{out} = 1W/ch, f_{out} = 1kHz, F_{sw} = 2.048MHz, AES17 Filter, reconstruction filter inductor used: 3.3µH-VCMT053T-3R3MN5 and 1µF, default I^2C settings + start-up script, see application diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC_{IMP}	AC impedance accuracy	f = 18.75kHz, R_L = 4Ω, Impedance at output pins		±0.75		Ω
f_{AC}	AC diagnostic test frequency	Default		18.75		kHz
I²C ADDRESS PIN						
t_{I2C_ADDR}	Time delay needed for I^2C address set-up			300		µs
I²C CONTROL PORT						
t_{BUS}	Bus free time between start and stop conditions		1.3			µs
t_{h1}	Hold Time, SCL to SDA		0			ns
t_{h2}	Hold Time, start condition to SCL		0.6			µs
t_{START}	I2C Startup Time After DVDD Power On Reset				12	ms
t_{RISE}	Rise Time, SCL and SDA				300	ns
t_{FALL}	Fall Time, SCL and SDA				300	ns
t_{SU1}	Setup, SDA to SCL		100			ns
t_{SU2}	Setup, SCL to Start Condition		0.6			µs
t_{SU3}	Setup, SCL to Stop Condition		0.6			µs
$t_{W(H)}$	Required Pulse Duration SCL "High"		0.6			µs
$t_{W(L)}$	Required Pulse Duration SCL "Low"		1.3			µs
SERIAL AUDIO PORT						
D_{SCLK}	Allowable input clock duty cycle		45%	50%	55%	
f_S	Supported input sample rates		44.1		192	kHz
f_{SCLK}	Supported SCLK frequencies		32		512	xFS
f_{SCLK_Max}	Maximum frequency				24.576	MHz
t_{SCY}	SCLK pulse cycle time		40			ns
t_{SCL}	SCLK pulse-with LOW		16			ns
t_{SCH}	SCLK pulse-with HIGH		16			ns
t_{SF}	SCLK rising edge to FSYNC edge		8			ns
t_{FS}	FSYNC edge to SCLK rising edge		8			ns
t_{DS}	DATA set-up time		8			ns
c_i	Input capacitance, pins SCLK, FSYNC, SDIN_1, SDOUT_1, GPIO_x				10	pF
t_{DH}	DATA hold time		8			ns
$T_{Audio}LA$	Audio path latency from input to output measured in FSYNC sample count	FSYNC = 44.1kHz or 48kHz			22	samples
		FSYNC = 96kHz			23	
		FSYNC = 192kHz			24	
$T_{LLP}LA$	Low latency path latency from input to output measured in FSYNC sample count	FSYNC = 44.1kHz or 48kHz			6	samples
		FSYNC = 96kHz			7	

5.6 Typical Characteristics

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = 14.4V, VBAT = 14.4V, DVDD = 1.8V, R_L = 4Ω, P_{out} = 1W/ch, f_{out} = 1kHz, F_{sw} = 2.048MHz, AES17 Filter, reconstruction filter as described in Parameter Measurement Information, default I^2C settings + start-up script, see application diagram

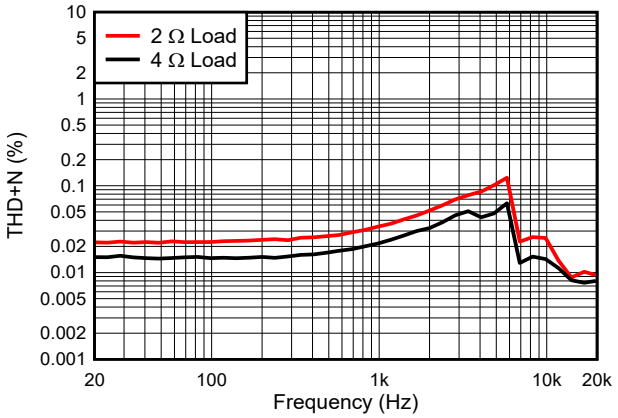


Figure 5-1. THD+N vs Frequency

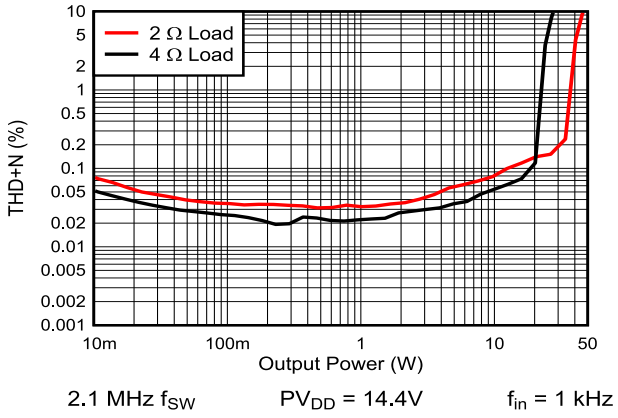


Figure 5-2. THD+N vs Power

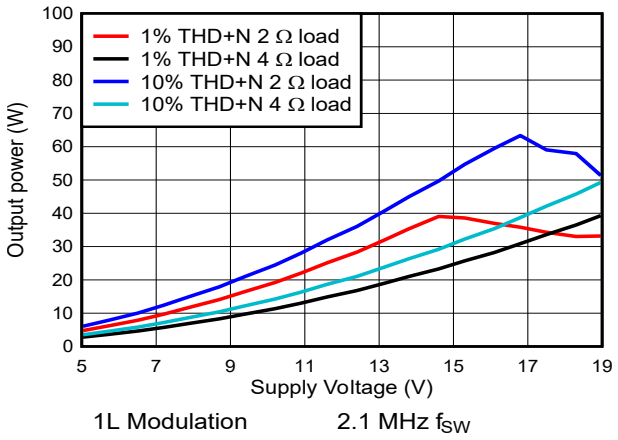


Figure 5-3. Output Power vs Supply Voltage

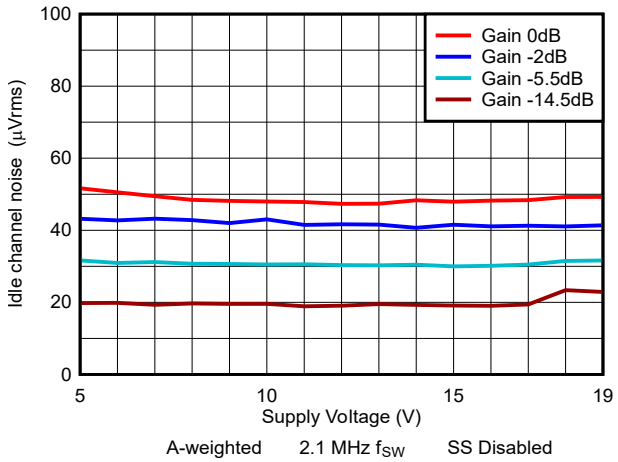


Figure 5-4. Noise vs Supply Voltage

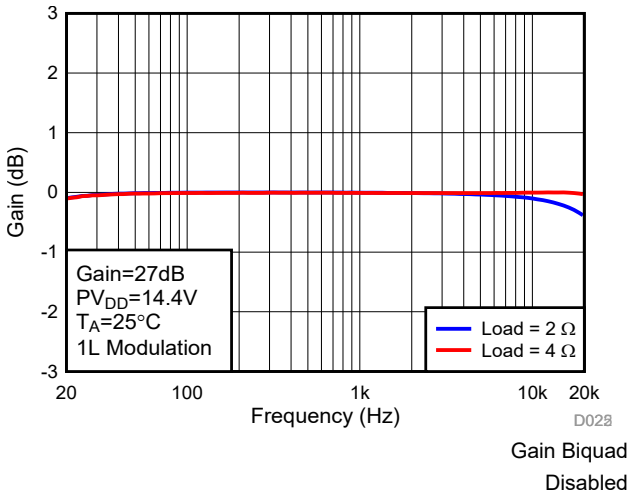


Figure 5-5. Frequency Response

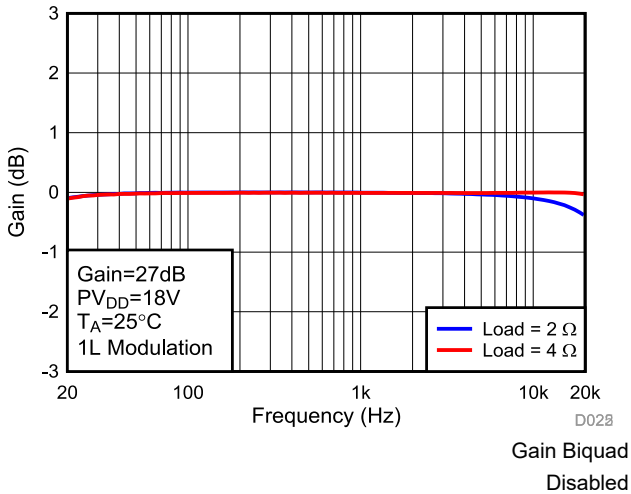
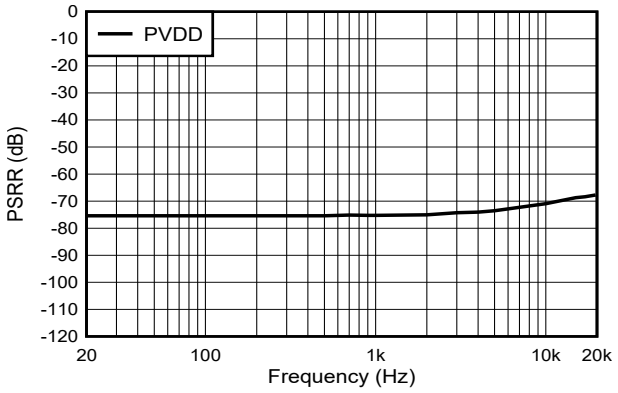


Figure 5-6. Frequency Response - PVDD = 18V

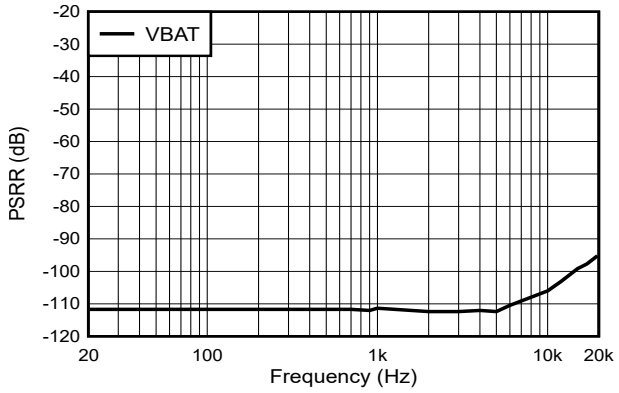
5.6 Typical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = 14.4V, VBAT = 14.4V, DVDD = 1.8V, R_L = 4Ω, P_{out} = 1W/ch, f_{out} = 1kHz, F_{sw} = 2.048MHz, AES17 Filter, reconstruction filter as described in Parameter Measurement Information, default I^2C settings + start-up script, see application diagram



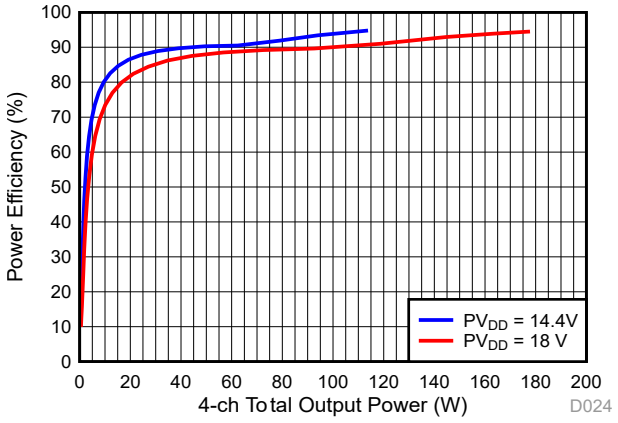
Po = Idle PVDD = 14.4VDC + 1VRMS

Figure 5-7. PVDD PSRR vs Frequency



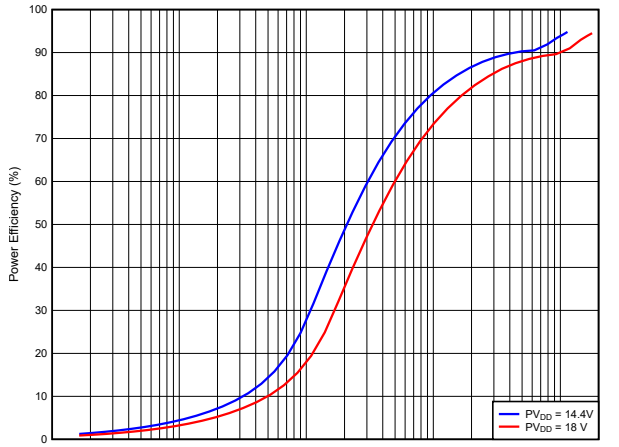
Po = Idle VBAT = 14.4VDC + 1VRMS

Figure 5-8. VBAT PSRR vs Frequency



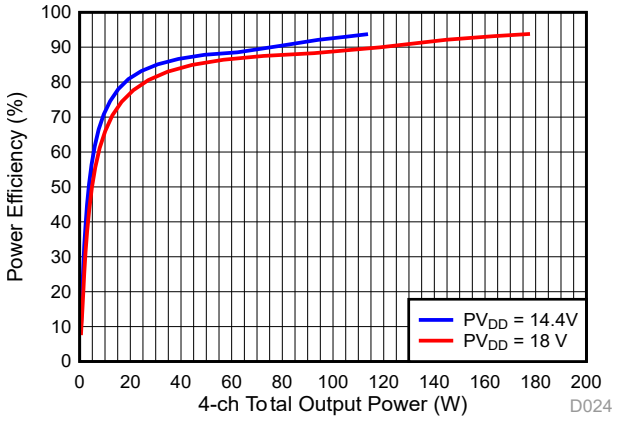
PVDD Only 2.1MHz 4Ω Load

Figure 5-9. Efficiency vs Output Power - 4Ω, PVDD



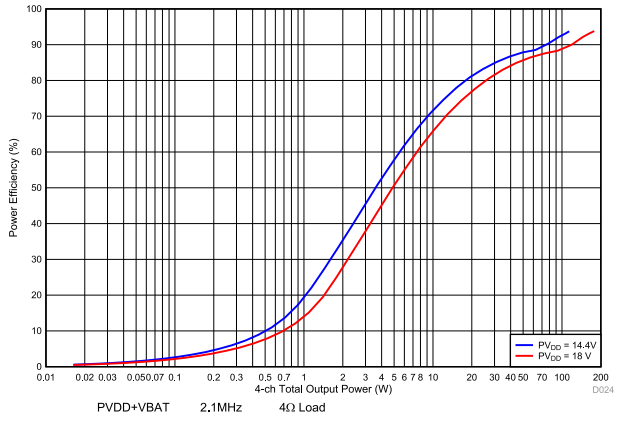
PVDD Only 2.1MHz 4Ω Load

Figure 5-10. Efficiency vs Output Power - 4Ω, PVDD (Zoomed)



PVDD+VBAT 2.1MHz 4Ω Load

Figure 5-11. Total Efficiency vs Output Power - 4Ω



PVDD+VBAT 2.1MHz 4Ω Load

Figure 5-12. Total Efficiency vs Output Power - 4Ω (Zoomed)

5.6 Typical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = 14.4V, VBAT = 14.4V, DVDD = 1.8V, R_L = 4Ω, P_{out} = 1W/ch, f_{out} = 1kHz, F_{sw} = 2.048MHz, AES17 Filter, reconstruction filter as described in Parameter Measurement Information, default I^2C settings + start-up script, see application diagram

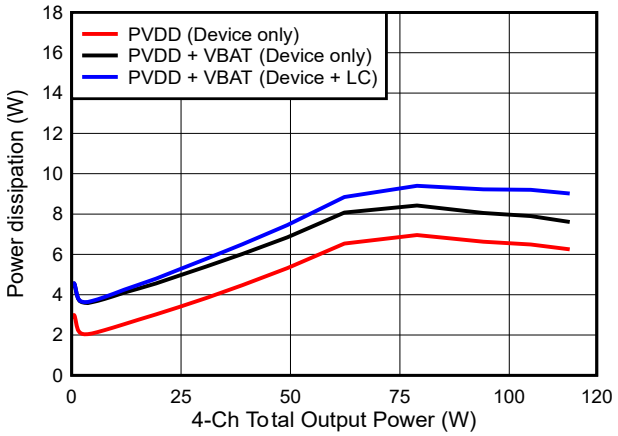


Figure 5-13. Power Dissipation vs Output Power - 4Ω

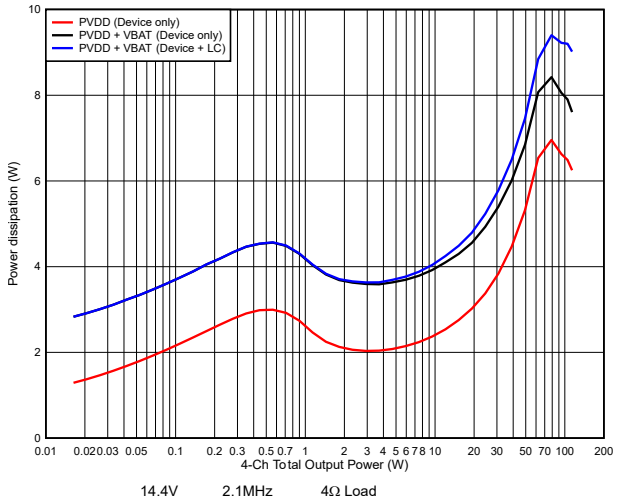


Figure 5-14. Power Dissipation vs Output Power - 4Ω (Zoomed)

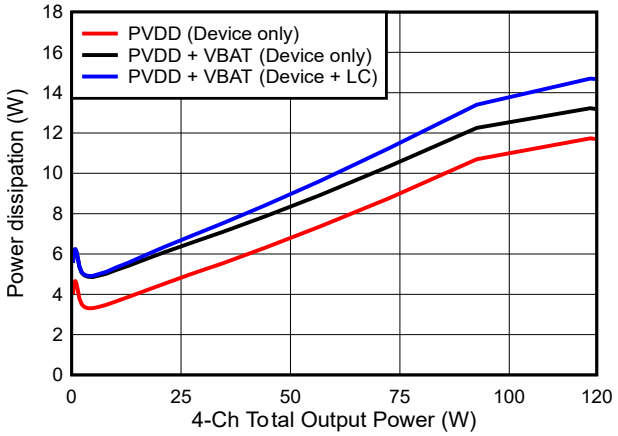


Figure 5-15. Power Dissipation vs Output Power - 4Ω, PVDD = 18V

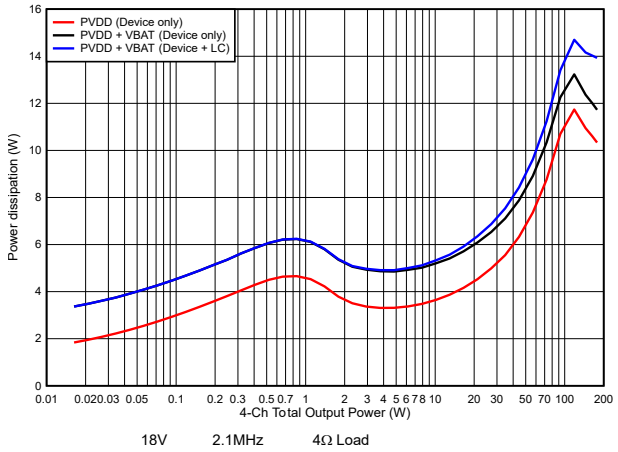


Figure 5-16. Power Dissipation vs Output Power - 4Ω, PVDD = 18V (Zoomed)

5.6 Typical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = 14.4V, VBAT = 14.4V, DVDD = 1.8V, R_L = 4Ω, P_{out} = 1W/ch, f_{out} = 1kHz, F_{sw} = 2.048MHz, AES17 Filter, reconstruction filter as described in Parameter Measurement Information, default I^2C settings + start-up script, see application diagram

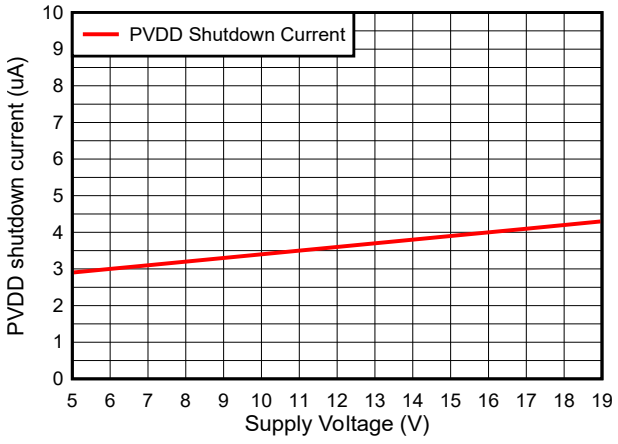


Figure 5-17. Shutdown Current vs Voltage, PVDD

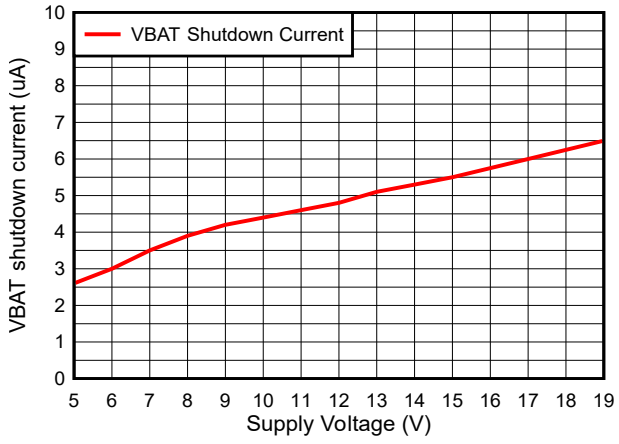


Figure 5-18. Shutdown Current vs Voltage, VBAT

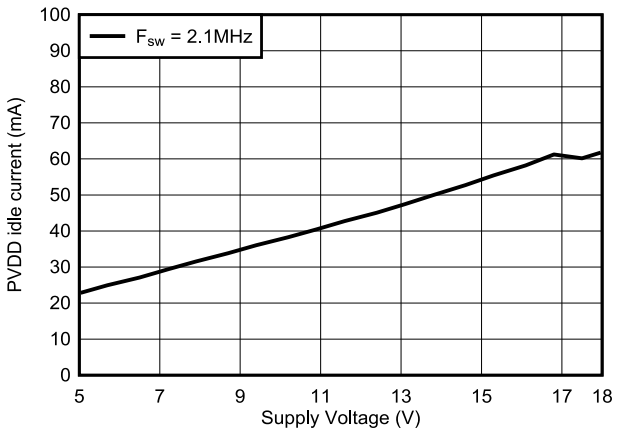


Figure 5-19. PVDD Idle Current vs Voltage

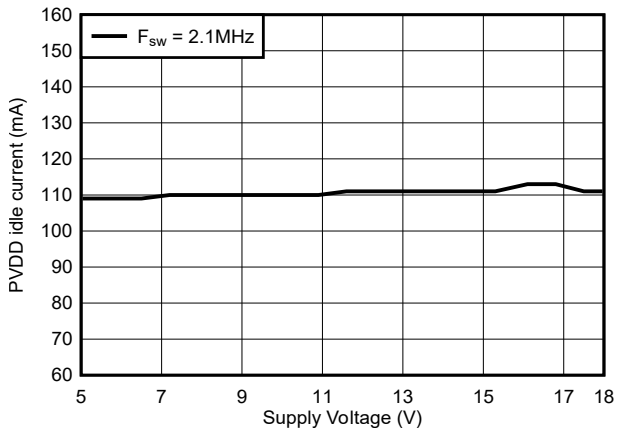


Figure 5-20. VBAT Idle Current vs Voltage

6 Parameter Measurement Information

For measurements, the LC reconstruction filter Cyntec VCMT053T-3R3MN5 3.3µH inductor + 1µF capacitor is used.

When enabling Real-Time Load Diagnostics with the integrated pilot tone, an analog balanced input filter must be used to avoid misleading measurement results. An elliptic high pass filter as provided by the APx500 series with a cutoff frequency of 20Hz and a low-pass filter such as AES17 (20kHz) are recommended. If the test equipment does not support this filter type, TI recommends to turn off the Real-Time Load Diagnostics for accurate performance measurements.

7 Detailed Description

7.1 Overview

The TAS6754-Q1 is a four-channel digital input Class-D audio amplifier, specifically tailored for use in the automotive industry. The device is designed for vehicle battery operation up to 19V with up to 40V load dump support. The ultra-efficient Class-D technology with advanced 1L modulation allows for lower switching losses, and a smaller PCB area. The device realizes a high-fidelity audio sound system design with smaller size, lower weight and advanced functionality.

The core design blocks are:

- Serial audio port
- PLL and Clock management
- Dual Core Audio DSP subsystem
- Pulse width modulator (PWM) with output stage feedback
- Gate drive
- Power FETs
- Current Sense
- Diagnostics including Real-Time Load Diagnostics
- Protection
- Power supply
- I^2C serial communication bus
- Sensing

7.2 Functional Block Diagram

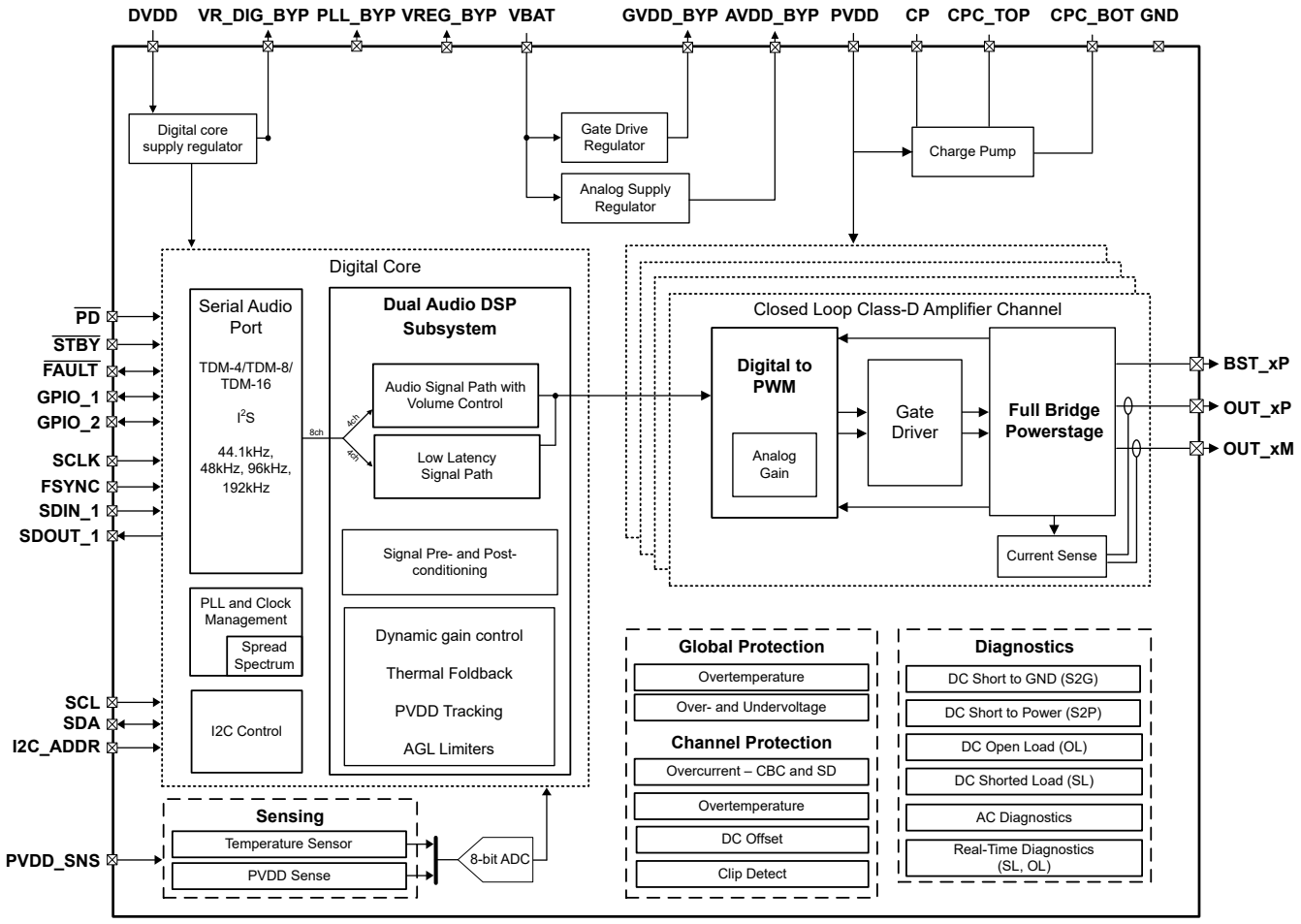


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Power Supply

The device has three power supply inputs, DVDD, VBAT and PVDD, which are described as follows:

DVDD This is a 1.8V or 3.3V supply that is connected at the DVDD pin and provides power to the digital circuitry.

VBAT This pin is a higher voltage supply that can be connected to the vehicle battery or the regulated voltage rail in a boosted system within the recommended limits. For best performance, this rail is 10V or higher. See the *Recommended Operating Conditions* table for the maximum supply voltage. This supply rail is used for higher voltage analog circuits but not the output FETs.

PVDD This pin is a high current supply that can either be connected to the vehicle battery or to another voltage rail in a boosted system. The PVDD pin supplies the power to the output FETs and can be within the *Recommended Operating Conditions*, even if that is below the VBAT supply, to allow for dynamic voltage systems.

Several on-chip regulators are included generating the voltages necessary for the internal circuitry. The external pins are provided only for bypass capacitors to filter the supply and are not be used to power other circuits.

The device can withstand fortuitous open ground and power conditions within the absolute maximum ratings for the device. Fortuitous open ground usually occurs when a speaker wire is shorted to ground, allowing for a second ground path through the body diode in the output FETs.

7.3.1.1 Power-Supply Sequence

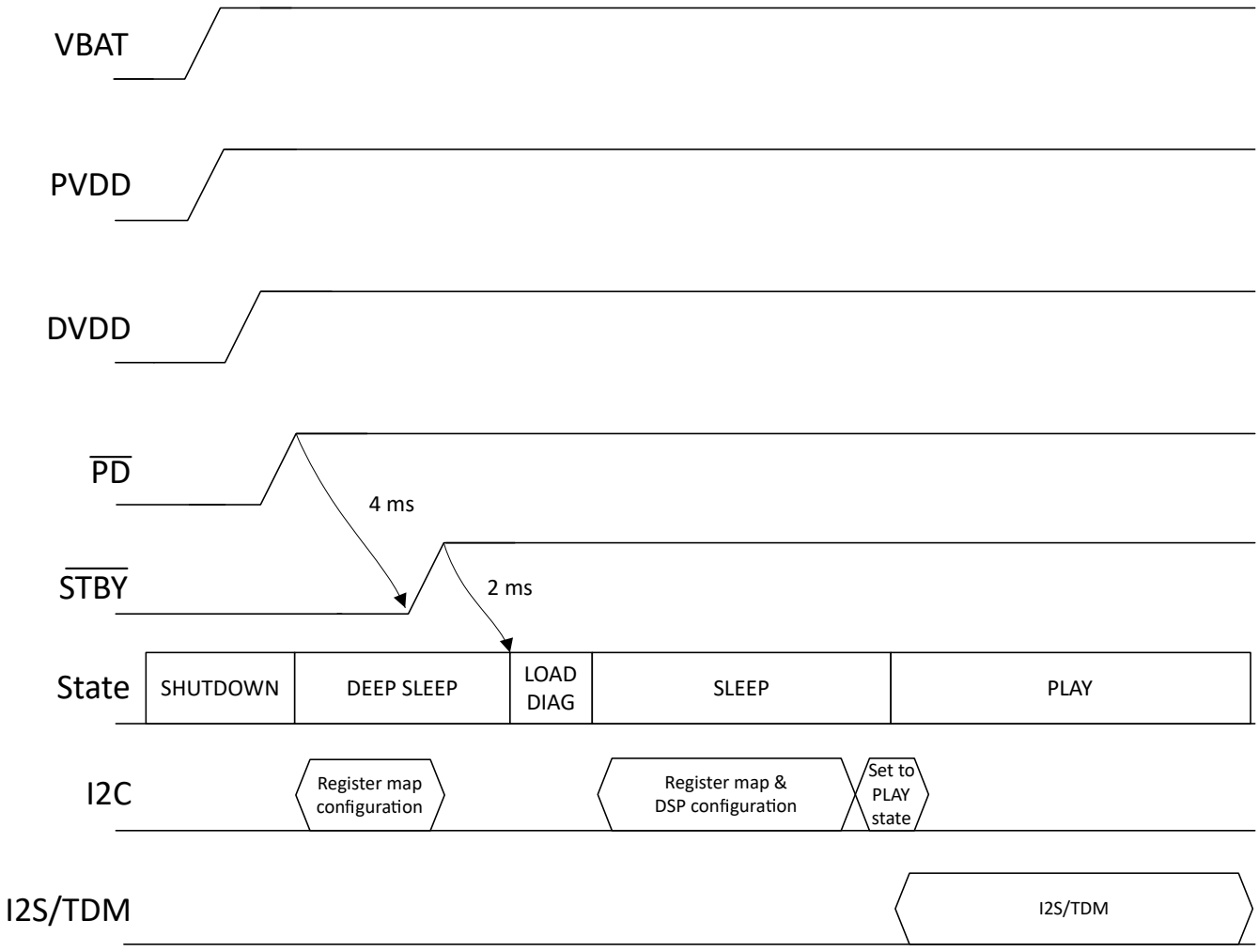
In a typical system, the VBAT and PVDD supplies are both connected to the vehicle battery and power up at the same time.

7.3.1.1.1 Power-Up Sequence

At power-up, the $\overline{\text{PD}}$ pin is recommended to be kept low until all three power supply rails (VBAT, PVDD, DVDD) are within the *Recommended Operating Conditions*.

When all power rails are applied and ready, releasing the $\overline{\text{PD}}$ pin powers up the internal digital circuitry. After releasing the $\overline{\text{PD}}$ pin a minimum 4ms wait time is recommended before releasing the $\overline{\text{STBY}}$ pin. Releasing the $\overline{\text{STBY}}$ pin powers up the internal analog circuitry. If this sequence is not possible and $\overline{\text{PD}}$ as well as $\overline{\text{STBY}}$ have to be released at the same time, the following state transition can take up to 6ms in which the device powers up the analog circuitry and maintains a proper internal boot procedure.

Any time a power fault happens after the analog circuitry is powered up (VBAT ready and $\overline{\text{STBY}}$ released), TAS6754-Q1 leaves PLAY or other states and go back to the Auto Recovery (AUTOREC) State, until the power fault disappears.



Applying DVDD before VBAT will leads to a reported “VBAT Undervoltage Fault” which needs to be cleared

Figure 7-2. TAS6754-Q1 Power-Up Sequence

7.3.1.1.2 Power-Down Sequence

To power-down the device, first set the $\overline{\text{STBY}}$ pin or $\overline{\text{PD}}$ pin low for at least 10ms before removing PVDD, VBAT or DVDD. After 10ms, the power supplies can be removed. Removing PVDD and VBAT first is recommended before removing the DVDD supply.

7.3.1.2 Device Initialization and Power-On-Reset (POR)

The device initializes when either the system first powers up, the $\overline{\text{PD}}$ pin is pulled high, or when the DVDD voltage falls below the POR threshold and then comes back to normal condition.

During device initialization all I^2C registers are set to default values.

The I^2C device address is determined from the I2C_ADDR pin. See I^2C Address Selection for details.

7.3.2 Serial Audio Port

The Serial Audio Interface can receive data in left-justified, I^2S or DSP mode formats. In addition, time-division multiplexing (TDM) can be implemented to enable multichannel operation with support up to TDM16.

The pins SDIN_1 and SDOUT_1 are available for the data transfer, while any of the GPIO pins can be assigned to become SDIN_2 and SDOUT_2 if required. Refer to GPIO Pins for more details.

7.3.2.1 Left-Justified Timing

Left-Justified timing uses the FSYNC pin to define when the data is being transmitted for the left channel or the right channel. The MSB of the left channel is valid on the rising edge of the serial clock (SCLK) following the rising edge of the audio frame clock (FSYNC). Similarly, the MSB of the right channel is valid on the rising edge of SCLK clock following the falling edge of FSYNC. A channel offset can be configured and is identical across all channels.

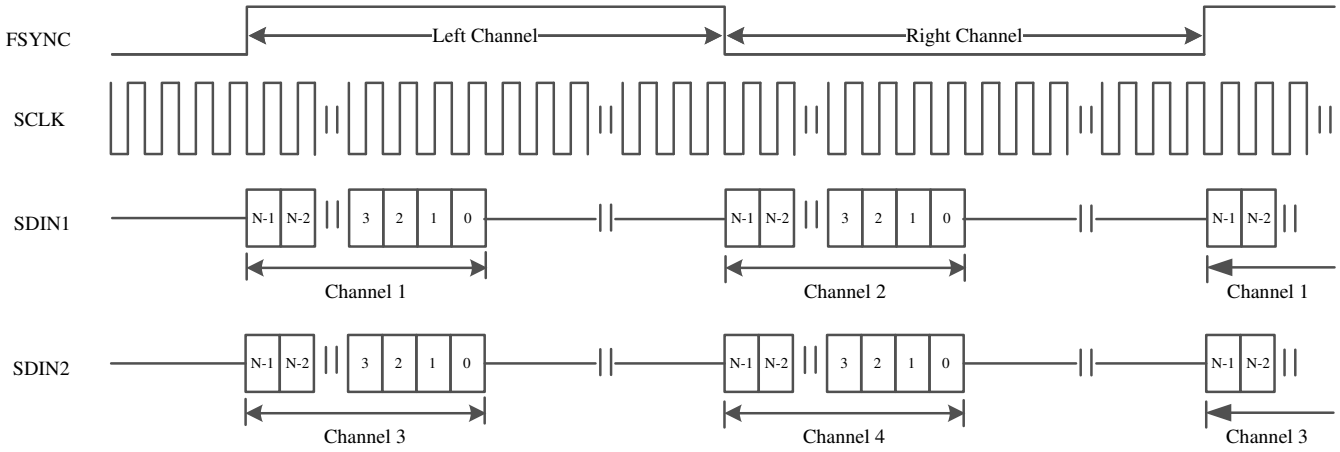


Figure 7-3. Timing Diagram for Left-Justified Timing

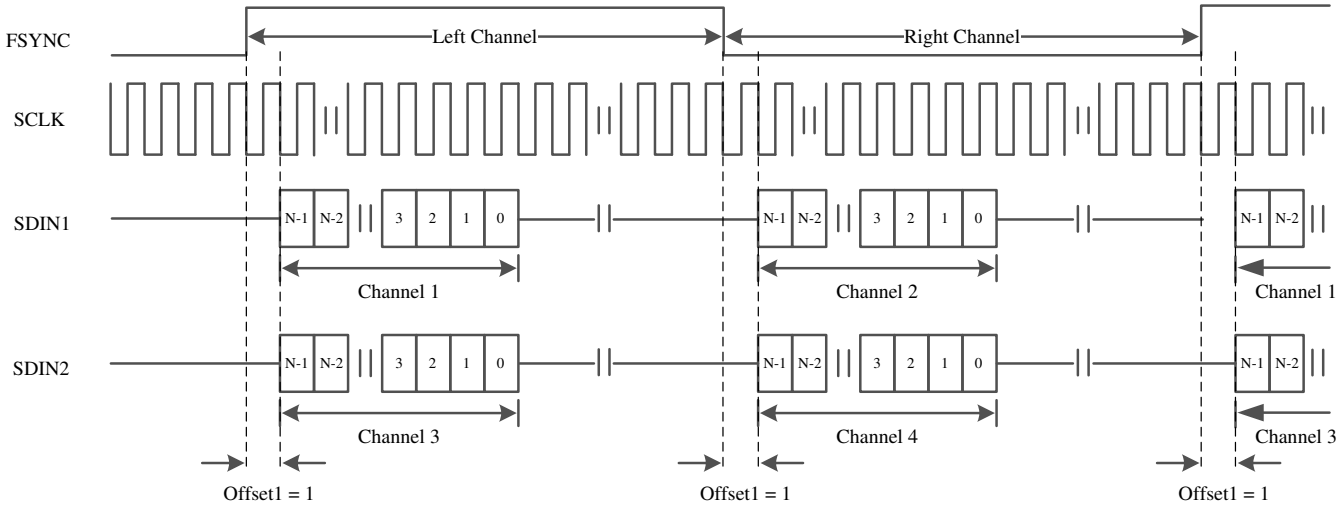


Figure 7-4. Timing Diagram for Left-Justified Timing with Offset 1 = 1

7.3.2.2 I²S Mode

I²S mode uses the FSYNC pin to define when the data is being transmitted for the left channel and when the data is being transmitted for the right channel. In I²S mode, the MSB of the left channel is valid on the second rising edge of the serial clock (SCLK) after the falling edge of the audio frame clock (FSYNC). Similarly the MSB of the right channel is valid on the second rising edge of SCLK after the rising edge of FSYNC. A channel offset can be configured and is identical for across channels.

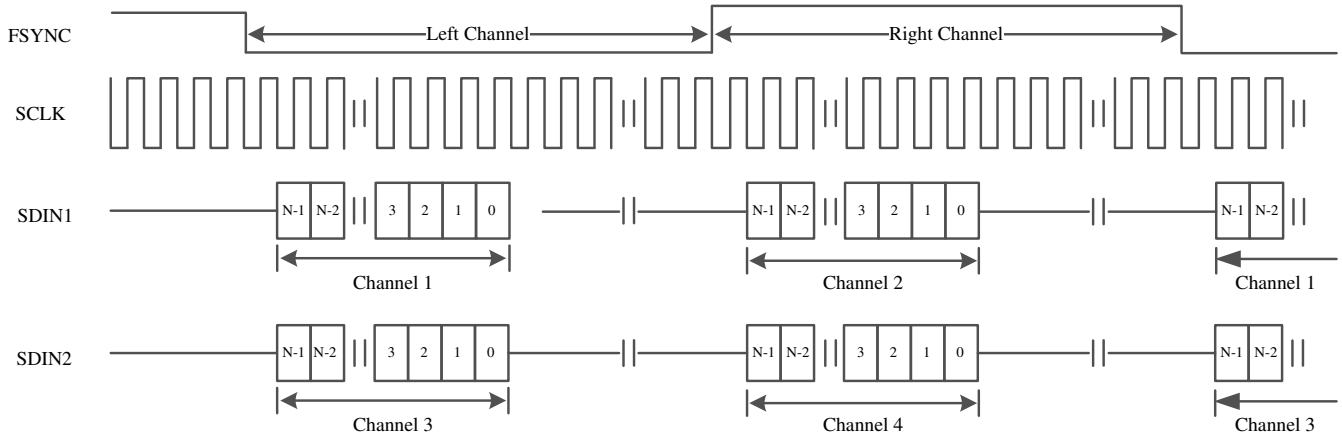


Figure 7-5. Timing Diagram for I2S Mode

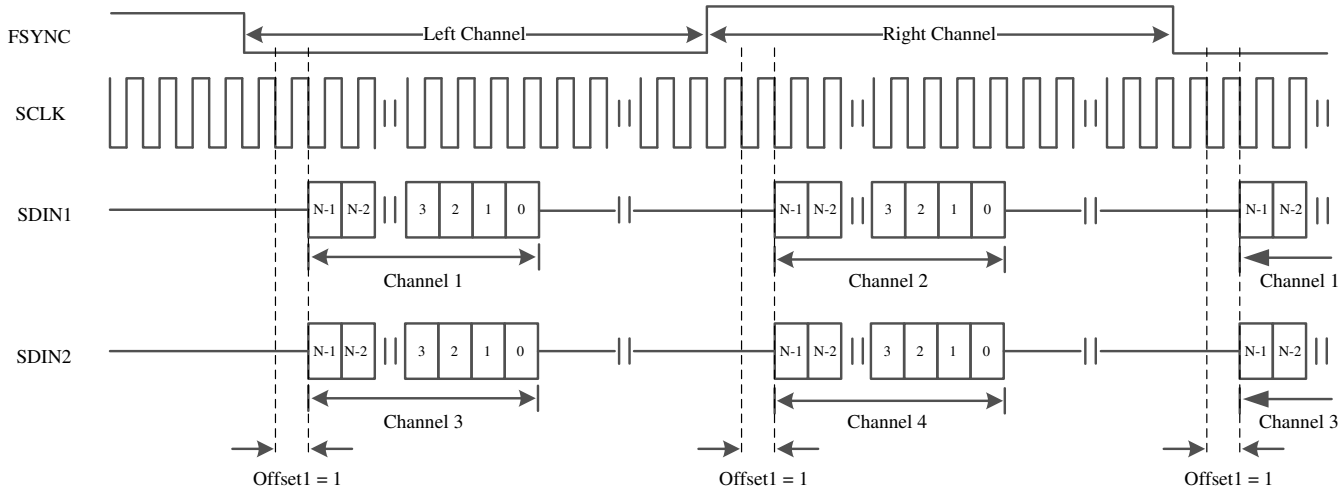


Figure 7-6. Timing Diagram for I2S Mode with Offset = 1

7.3.2.3 DSP Mode

DSP mode uses the FSYNC pin to define the start of the audio data, but not to differentiate between channels. The rising edge of the audio frame clock (FSYNC) starts the data transfer with the left channel data first and is immediately followed by the right channel data. Each data bit is valid on the rising edge of the serial clock (SCLK). A 10-bit channel offset can be configured and is identical across all channels.

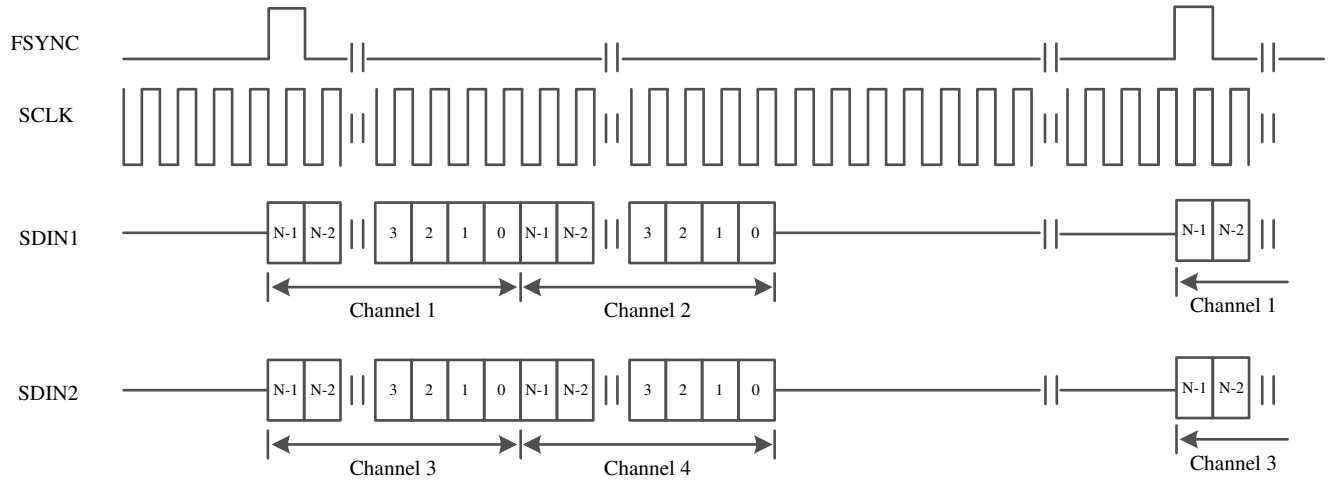


Figure 7-7. Timing Diagram for DSP Mode

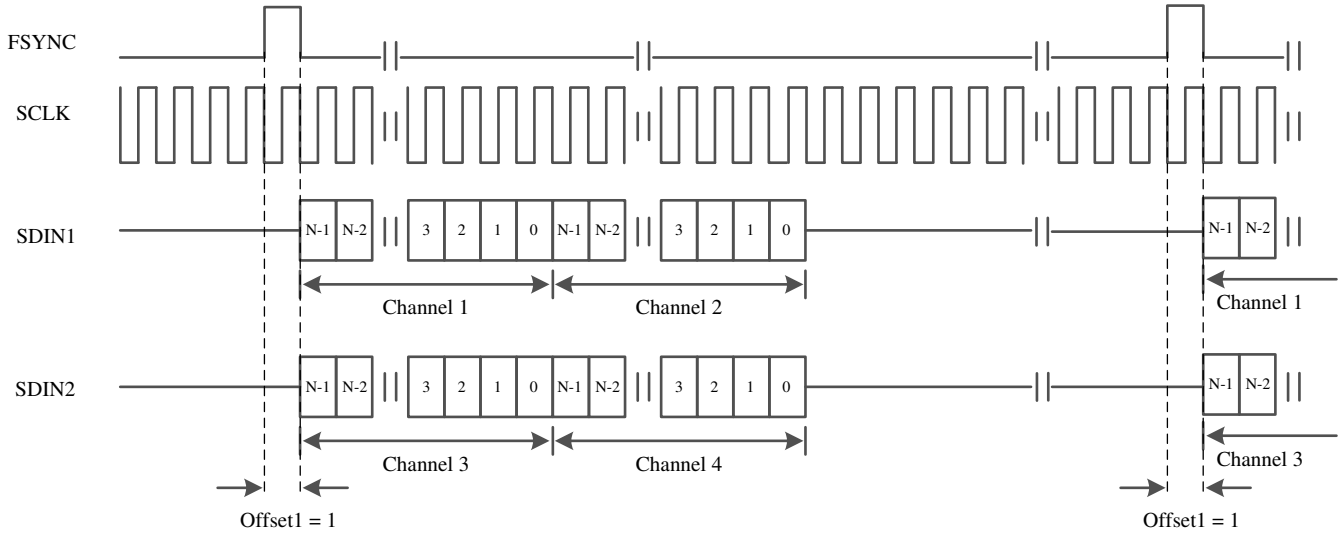


Figure 7-8. Timing Diagram for DSP Mode with Offset = 1

7.3.2.4 TDM Mode

TDM mode supports 4, 8, or 16 channels of audio data through SDIN. The data can be received through a single pin or split across SDIN_1 and SDIN_2. The data format follows the DSP Mode.

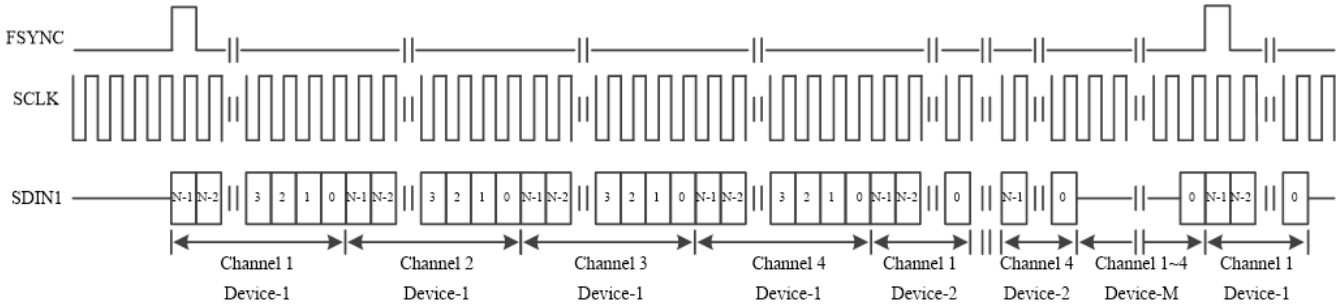


Figure 7-9. Timing Diagram for TDM Mode

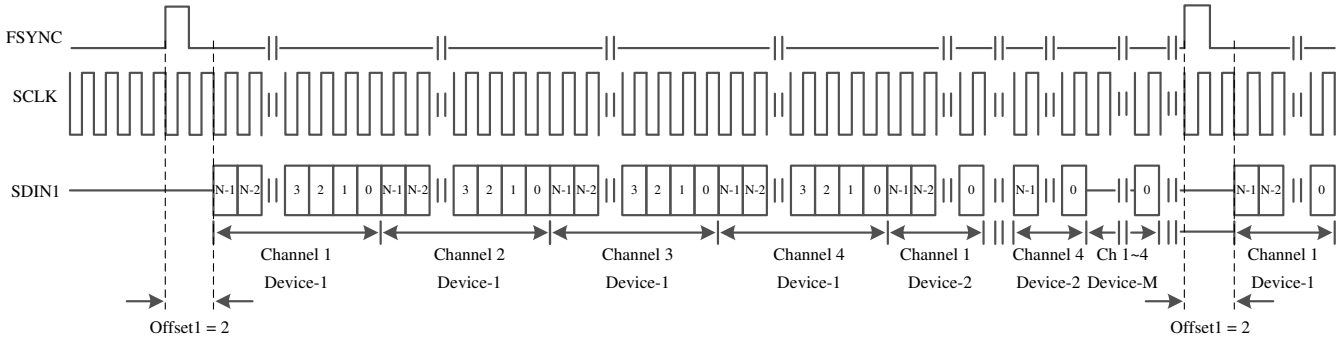


Figure 7-10. Timing Diagram for TDM mode with Audio Channels Offset1 = 2

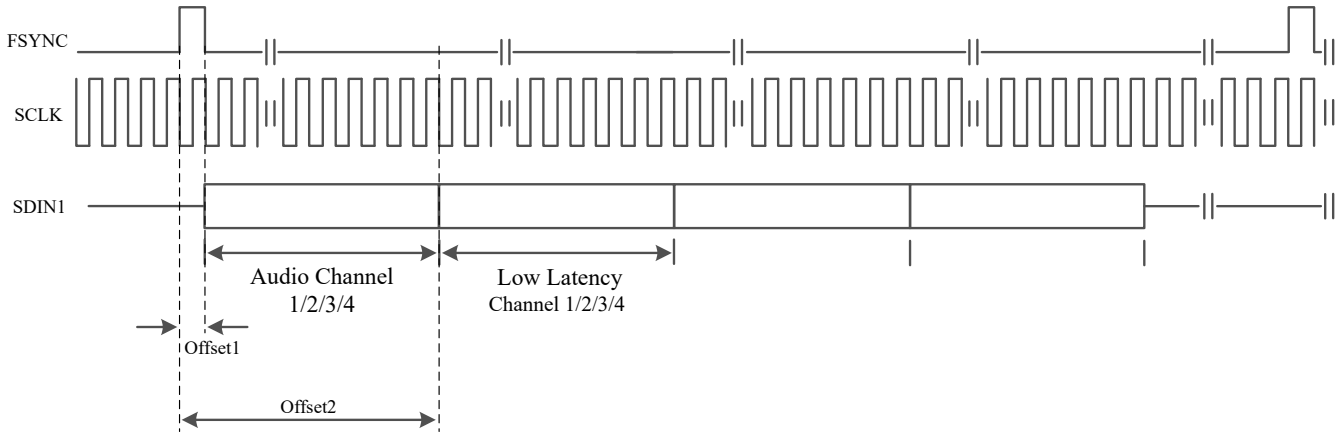


Figure 7-11. Timing Diagram for TDM mode with Audio Channels Offset1, Low Latency Channels Offset2

7.3.2.5 SDOUT - Data Output

TAS6754-Q1 can transmit selected data in either I²S mode or TDM mode. The audio input serial clock (SCLK) and audio frame clock (FSYNC) is reused, and the outgoing data has the same sampling frequency and maximum audio frame size as the audio input signal.

7.3.2.6 Device Clocking

The TAS6754-Q1 has a flexible clocking system. Internally, the device requires several additional clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

Figure 7-12 shows the basic data flow and clock distribution.

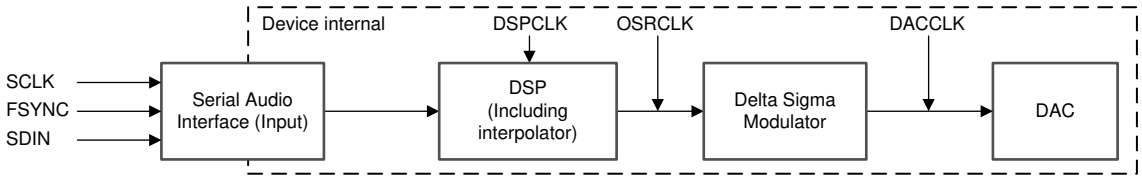


Figure 7-12. Audio Flow with Respective Clocks

The Serial Audio Interface typically has 3 connection pins which are listed as follows:

- SCLK (Audio Serial Clock)
- FSYNC (Frame Sync in TDM or Left/Right in I²S)
- SDIN (Input Data). In TDM mode, a single SDIN is used while I²S requires two SDIN pins to provide audio data for 4 channels
- Optional: SDOUT for outgoing data transmission. Up to two SDOUT pins can be configured

The device has an internal PLL which uses SCLK as reference clock and creates the higher rate clocks required by the DSP and the DAC clock.

The TAS6754-Q1 has an audio sampling rate detection circuit that automatically senses the sampling frequency. Common audio sampling frequencies of 44.1kHz – 48kHz, 88.2kHz – 96kHz and 192kHz are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

7.3.2.6.1 Clock Rates

The serial audio interface port is a 3-wire serial port with the signals SCLK, FSYNC and SDIN_1 as well as an optional SDIN_2 in I²S Mode.

SCLK is the serial audio bit clock used to clock the serial data present on SDIN_x into the serial shift register of the audio interface. Serial data is clocked into the TAS6754-Q1 device with SCLK.

The FSYNC pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

SDIN_1 is the TDM data input. In I²S mode, SDIN_1 is the data input for channels 1 and 2 and a GPIO pin needs to be configured as SDIN_2 to receive the data input for channels 3 and 4.

Table 7-1. Audio Data Formats, Bit Depths and Clock Rates

Format	Data Bits	Maximum FSYNC Frequency (kHz)	SCLK Rate (f_s)
I²S / LJ	32, 24, 20, 16	44.1 to 192	x64, x32
TDM	32, 24, 20, 16	44.1 / 48	x128, x256, x512
		96	x128, x256
		192	x128

7.3.2.6.2 Clock Halt Auto-recovery

Certain host processors halt the audio clock when no audio is playing. When the clock is halted, the device puts all channels into the Hi-Z state and issues a latched error report. The transition to Hi-Z occurs gracefully by holding the last received sample from the audio interface and ramping down the volume. This behavior can be

changed. The latched error report clears once read. After audio clock recovery, the device automatically returns to the previous state.

7.3.2.6.3 Sample Rate on the Fly Change

TAS6754-Q1 supports an on-the-fly change of the FSYNC rate. When changing FSYNC, for example from 48kHz to 96kHz, the host processor needs to put the FSYNC/SCLK to halt state for at least 30ms before changing to the new sample rate. During this halt state a clock error is reported. See Clock Halt Auto-recovery section for further details.

7.3.2.7 Clock Error Handling

After Power-On-Reset (POR) the device assumes that a clock error exists, but does not assert the clock error flag until the clock error detection result is valid.

If any input clock changes are detected, the auto detect system immediately requests the device to mute gracefully by holding the last received sample from the audio interface, while the auto detect continues to monitor and identify a new stable condition.

7.3.3 Digital Audio Processing

TAS6754-Q1 offers advanced digital audio processing capabilities including:

- High-Pass Filter / DC Blocking
- Digital Volume Control
- PVDD Foldback / AGL
- Thermal Foldback
- Gain Compensation Biquads
- Real-Time Load Diagnostics
- Clip Detect
- Low Latency Path

The availability of specific features is dependent on the selected sampling frequency. Higher sampling frequencies reduce the available processing time of the integrated DSP and limit the amount of functions that can operate in parallel. Attention is needed to maintain that the total processing need of the enabled functions does not exceed the available amount of processing time at all sampling frequencies.

7.3.3.1 PVDD Foldback

PVDD Foldback applies a smooth compression to the audio signal to maintain a consistent dynamic range while the supply voltage (PVDD) varies. This feature helps to prevent unexpected output clipping and distortion in systems where the audio signal exceeds the supply headroom and can also be described as Automatic Gain Limiter (AGL).

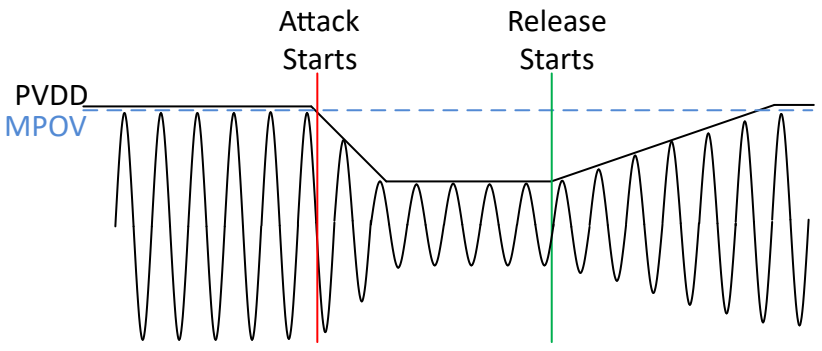


Figure 7-13. PVDD Foldback Example

7.3.3.2 High-Pass Filter

To protect speakers connected to the TAS6754-Q1, a DC blocking high pass filter is built into the audio processing path.

7.3.3.3 Analog Gain

TAS6754-Q1 allows the user to set the analog gain for each channel pair and in increments of 0.5dB.

A gain setting of 0dB corresponds with a peak output voltage of 28V/FS at full scale digital input. TI recommends to select the lowest possible gain for the expected PVDD operation to optimize output noise and dynamic range performance.

Only change the Analog Gain setting while affected channels are in DEEP SLEEP or SLEEP state.

As the device enters PLAY State, the device gradually ramps the analog gain to the desired value in steps of 0.5dB.

7.3.3.4 Digital Volume Control

The output channels have a digital-volume control with a range from -103dB to 0dB with 0.5dB steps.

7.3.3.4.1 Auto Mute

When detecting a consecutive stream of zero samples at the audio input, the device can automatically set channels into mute. In this mode, the device continues to monitor the input signal, and, depending on the configuration, unmute either individual channels or all channels at the same time when a valid non-zero signal arrives.

7.3.3.5 Gain Compensation Biquads

The modulator and output LC filter of the Class-D amplifier can have an undesired influence on frequency response linearity causing frequency drop/peaking. To help compensate for this effect and achieve a flat response, TAS6754-Q1 offers integrated and channel-based gain compensation biquads.

The biquad is configurable by channel and is disabled by default. To enable the desired tuning, the respective coefficients need to be written to the DSP memory.

7.3.3.6 Low Latency Signal Path

For time-sensitive audio signals that require a minimal processing delay, such as active noise cancellation (ANC) or road noise cancellation (RNC), TAS6754-Q1 offers a low latency signal path. At 48kHz sampling frequency, this path reduces the signal delay by more than 70% between the input and output of the amplifier by minimizing the internal signal processing.

The low latency signal path is established in parallel to the regular audio signal path. When both signal paths are provided with input data, the two signals - audio and low latency - for each channel are internally mixed together right before the output amplification stage of the channel. Both signals are added together and the combined signal amplitude must not exceed the available gain range nor the voltage headroom to avoid distortion. Note that the low latency signals pass through the device with less delay than the regular audio path signals.

The low latency signal path is only available at a sampling frequency of 48kHz or 96kHz.

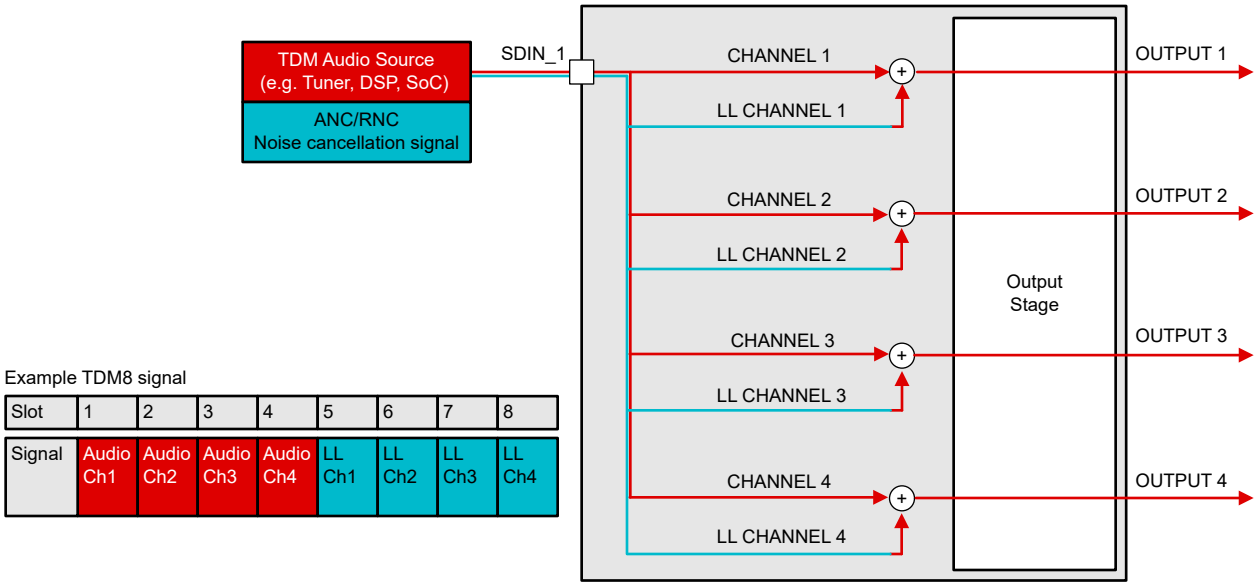


Figure 7-14. Low Latency and Audio Signal Path

7.3.3.7 Full Feature Low Latency Path

In addition to the Low Latency Signal Path the TAS6754-Q1 integrates a Full Feature Low Latency Path. Using the Full Feature Low Latency Path the time-sensitive audio signals, such as active noise cancellation (ANC) or road noise cancellation (RNC), can be premixed and do not need to be separated from the non-time-sensitive audio data. The premixed audio data is processed through the DSP and then amplified at the output stage with a lower group delay.

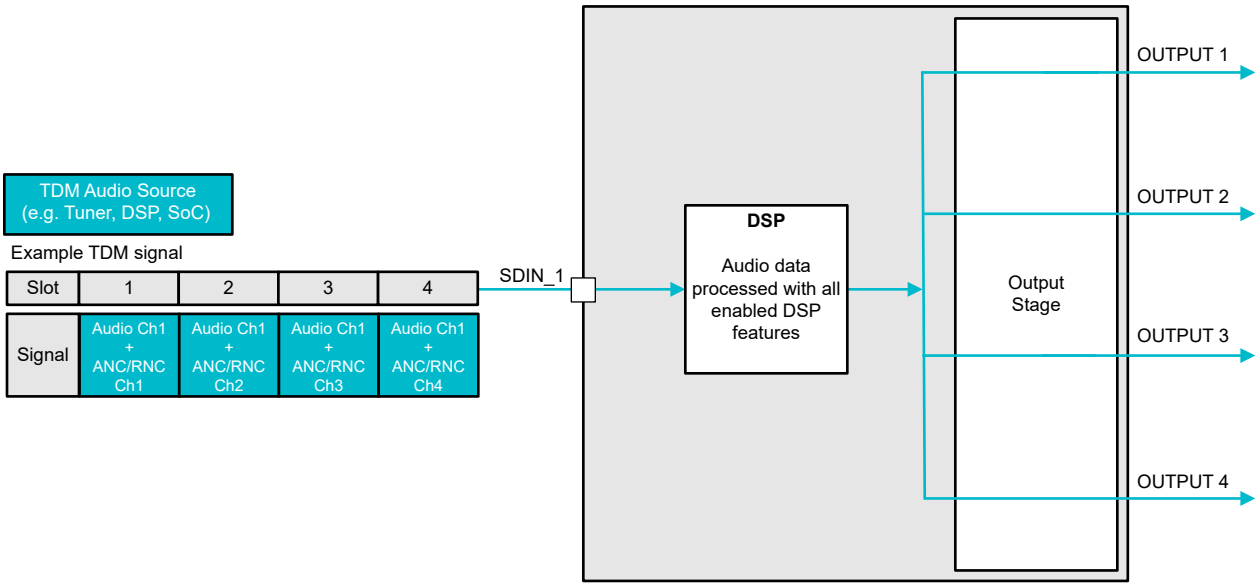


Figure 7-15. Full Feature Low Latency and Audio Signal Path

7.3.4 Class-D operation and Spread Spectrum Control

7.3.4.1 1L Modulation

TAS6754-Q1 supports 1L modulation. With 1L modulation, the OUT_xP side switches from 0 volts to the supply voltage at the switching frequency (Fsw). The OUT_xM side switches from 0 volts to the supply voltage at the

audio frequency. Since the OUT_xM side of the channel switches at a lower frequency, no inductor is required on this side of the BTL channel.

7.3.4.2 High-Frequency Pulse-Width Modulator (PWM)

The PWM modulator converts the input audio data into a switched signal of varying duty cycle. The PWM modulator is an advanced design with high bandwidth, low noise, low distortion, and excellent stability.

TAS6754-Q1 has configurable output PWM phase control to manage conducted and radiated emissions. This feature allows the channel output PWM phase offset to be changed relative to other channels.

7.3.4.3 Spread Spectrum Control

TAS6754-Q1 applies spread spectrum control to the modulator's clock signal. Controlling the spectrum of the clock signal translates into an optimized behavior of higher frequency signal components which are visible during EMI testing. Spread spectrum modulation is a PWM modulation technique that reduces the peaks seen in EMI measurements by varying the output PWM frequency, resulting in a wider spectrum but lower level.

7.3.4.4 Gate Drive

The gate driver accepts the low-voltage PWM signal and level shifts it to drive a high-current, full-bridge, power-FET stage.

The device uses proprietary techniques to optimize EMI and audio performance. The gate driver power supply voltage, GVDD, is internally generated and a decoupling capacitor must be connected.

The full H-bridge output stages use only NMOS transistors. Therefore, bootstrap capacitors are required for the proper operation of the high side NMOS transistors for the OUT-xP sides. A 1µF ceramic capacitor of quality X7R or better, rated appropriately for the applied voltages (including load dump voltages), must be connected from each output to the corresponding bootstrap input. The bootstrap capacitors connected between the BST pins and the corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high, keeping the high- side MOSFETs turned on.

The high-side FET gate driver of the OUT_xM side is supplied by a charge pump (CP) supply for all four channels. A 330nF ceramic capacitor of quality X7R or better, rated appropriately for the applied voltages (including load dump voltages), must be connected from the CP pin to PVDD. Additionally, a similarly rated 100nF ceramic capacitor must be connected from the CPC_TOP pin to the CPC_BOT pin.

7.3.4.5 Power FETs

The BTL output channel comprises four N-channel FETs for high efficiency and maximum power transfer to the load. These FETs are designed to handle the fast switching frequency and large voltage transients during operation within the *Recommended Operating Conditions*.

7.3.5 Load Diagnostics

The device incorporates both DC and AC load diagnostics which are used to determine the status of the load. The DC-diagnostics are turned on by default.

7.3.5.1 DC Load Diagnostics

The DC load diagnostics are used to verify if the load is connected properly.

To support system level start up requirements of a fast time to audio:

- The diagnostics are available as soon as the device leaves the DEEP SLEEP mode and supplies are within the recommended operating range.
- The diagnostics do not rely on external audio input signals or clock and sync frequencies to be available.

DC Diagnostics complete successfully and allow a channel to enter MUTE or PLAY mode if the following tests pass on the output pins:

- No Short-to-Ground
- No Short-to-Power

- No Shorted Load
- No Open Load

7.3.5.1.1 Automatic DC Load Diagnostics at Device Initialization

The TAS6754-Q1 supports automatic and autonomous DC load diagnostics at device start-up. When leaving DEEP SLEEP state and under the condition that all power supplies are within the recommended operating range, the device transitions into SLEEP state and automatically starts DC load diagnostics on all four channels.

Neither I^2C configuration nor any audio signals are necessary for the TAS6754-Q1 to perform short-to-power (S2P), short-to-ground (S2G), open-load (OL), and shorted-load (SL) tests based on default configuration. Systems can benefit from this autonomous operation because of the possibility to run the load diagnostics while bringing up the digital part of the audio chain.

7.3.5.1.2 Automatic DC load diagnostics during Hi-Z or PLAY

When a fault occurs while a channel is in Hi-Z or PLAY state, the device places the channel in either FAULT state or Auto Recovery State. After the fault is resolved or cleared, the device automatically runs DC load diagnostics on the affected channel and recover to previous Hi-Z respective PLAY state unless a different state was requested through I^2C .

7.3.5.1.3 Manual start of DC load diagnostics

Manual DC load diagnostics can be enabled in any state after all power supplies are within the recommended operating range and after the device has transitioned to SLEEP state for the first time. DC diagnostics can be enabled manually by setting the I^2C control state register to LOAD DIAG state to run on any or all channels. If either the $\overline{\text{STBY}}$ pin or a GPIO pin function set the device to SLEEP or DEEP SLEEP state, manual DC Load diagnostics cannot be run. This doesn't apply when the device is set to SLEEP or DEEP SLEEP state through I^2C control, in which manual DC Load diagnostics are available.

7.3.5.1.4 Short-to-Ground

The Short-to-Ground (S2G) tests triggers a fault condition if there is a conductive path from output pin OUT_(i)M or OUT_(i)P of the tested channel (i) to GND with an impedance below that specified in the Electrical Characteristics section.

7.3.5.1.5 Short-to-Power

The Short-to-Power (S2P) tests triggers a fault condition if there is a conductive path from output pin OUT_(i)M or OUT_(i)P of the tested channel (i) to a power rail with an impedance below that specified in the Electrical Characteristics section.

7.3.5.1.6 Shorted-Load and Open-Load

The Shorted-Load (SL) test triggers a fault condition if the conductive path between the OUT_(i)M pin and OUT_(i)P pin of the tested channel (i) has an impedance below the threshold set. The SL test has a configurable threshold depending on the expected load to be connected. Because the speakers and cable impedance connected to each channel can be different, each channel can be assigned a unique threshold value.

The Open-Load (OL) test triggers a fault condition if the conductive path between the OUT_(i)M pin and OUT_(i)P pin of the tested channel (i) has an impedance higher than that specified in the Electrical Characteristics section.

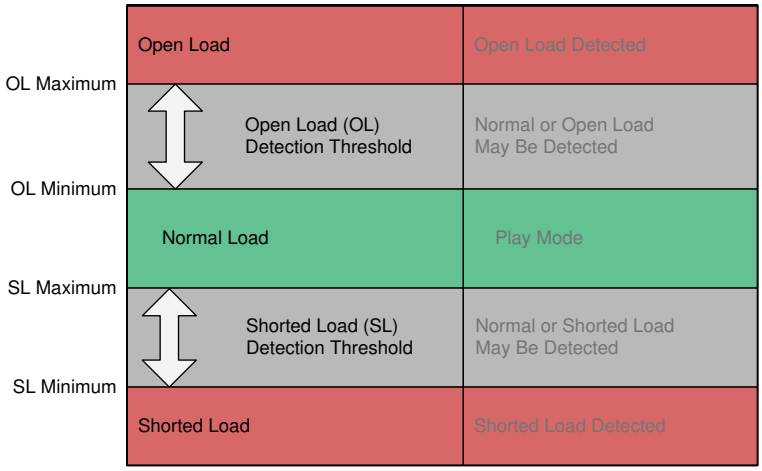


Figure 7-16. DC Load Diagnostic Reporting Thresholds

7.3.5.2 Line Output Diagnostics

The device also includes an optional test to detect a line output load (LO). A line output load is a high-impedance load that is above the open load (OL) threshold such that the DC-load diagnostics report an OL condition. If the line output detection bit is set high, when an OL condition is detected during the DC Diagnostic test, the system tests if a line output load is present.

7.3.5.3 AC Load Diagnostics

The AC load diagnostic is used to determine the proper connection of a capacitive coupled speaker or tweeter when used with a passive crossover. The AC load diagnostic is controlled through I^2C. The TAS6754-Q1 provides a required signal source to determine the AC impedance and reports the tweeter detection result back to I^2C registers. The I^2C selected test frequency creates current flow through the desired speaker for proper detection. AC Load Diagnostics can operate without the TDM/I^2S clocks being present.

Note

If a fault occurs during AC diagnostics, the AC diagnostics is stopped. AC Diagnostics is not allowed to be performed again until the DC Diagnostics are performed. This is to make sure the fault is not a potential hazard during AC diagnostics.

7.3.5.3.1 Operating Principal

The AC Load Diagnostic circuit of TAS6754-Q1 provides an internally generated stimulus to the load; captures the response of the load; provides real and imaginary parts of the captured complex load impedance; and offers a magnitude estimator and tweeter detection comparator.

7.3.5.3.2 Stimulus

The device drives a low level, 10mA output current through the load which does not create any significant sound pressure levels from the speaker.

7.3.5.3.3 Load Impedance

The load impedance as seen by the device is simply the ratio of the voltage across the output pins and the current flowing through the load.

Typically the load has a frequency dependent magnitude and causes current and voltage to have a phase shift. The TAS6754-Q1 internally captures the load impedance as a complex value consisting of a real and imaginary part. Expressing a load impedance in magnitude and phase or in real and imaginary part is mathematically equivalent. Both forms can be transformed into each other without loss of information. After AC load diagnostics

have finished, the real and imaginary parts of the complex impedance are available by channel for readout in I^2C registers.

7.3.5.3.4 Tweeter Detection

In most cases, using the TAS6754-Q1 built-in magnitude estimator and tweeter detection report is sufficient to perform the desired tweeter detection test. If a tweeter is properly connected in the system, the magnitude of the load impedance is close to the nominal impedance of the speaker, for example 4Ω.

7.3.5.4 Real-Time Load Diagnostics

Real-Time Load Diagnostics (RTLDG) allows the detection of shorted load (SL) and open load (OL) conditions during audio operation of the amplifier. To monitor the load impedance while in PLAY state the TAS6754-Q1 uses the devices integrated current sense to measure the output impedance by channel and compare the results with configurable thresholds. An internally generated pilot tone maintains the continuous detection of the output impedance, regardless if an external audio input signal is present.

7.3.5.5 DC Resistance Measurement

The TAS6754-Q1 supports a DC Resistance Measurement of the loads connected to each channel that can be read back to the system processor via I^2C. To read out the DC resistance of the load connected to each channel, DC load diagnostics must be completed.

7.3.6 Protection and Monitoring

7.3.6.1 Overcurrent Limit (Cycle-By-Cycle)

Under normal operation, during high level music playback, dynamic load currents can possibly rise beyond the maximum load current, I_{LIM} , of the device. In these cases, the device dynamically limits the current into the load and operation continues without disruption and prevents undesired shutdown for transient music events.

7.3.6.2 Overcurrent Shutdown

If the output load current reaches I_{SD}, such as during an output short to GND, then an Overcurrent Shutdown (OCSD) event occurs, limiting the peak current and shutting down the affected channel. The time to shutdown the channel varies depending on the severity of the short condition.

The channel is placed into the FAULT state with the output stage in Hi-Z.

Based on the configuration, a fault signal is generated, which by default generates an active low signal at the $\overline{\text{FAULT}}$ pin.

7.3.6.3 Current Sense

TAS6754-Q1 can measure the output current of each channel simultaneously. This functionality is completely integrated and requires no external components.

The channel output current measurement is performed at the rate of the sampling frequency F_s. The measured current amplitude is provided through SDOUT. For more details on the data transmission configuration see SDOUT. Note that the current measurement and the data transmission are two separate functions and both require proper setup before the data can be made available.

7.3.6.4 DC Detect

This circuit detects the DC offset continuously of the amplifier during normal operation. If the DC offset exceeds the DC_{FAULT} threshold, that channel triggers a DC Fault Event and is placed in the FAULT state and the output stage is set to high impedance.

Based on the configuration, a fault signal is generated, which by default generates an active low signal at the $\overline{\text{FAULT}}$ Pin.

TI recommends to leave DC Detect enabled at all times to prevent speaker damage from excessive DC bias output.

7.3.6.5 Digital Clip Detect

The DSP monitors the audio signal of each channel individually and compares the magnitude of the audio signal at the input to the interpolation filters to a configurable threshold. If the audio signal exceeds the threshold, a Clip Detect Warning Event is triggered.

TAS6754-Q1 supports Pseudo-Analog Clip Detect (PACD). With PACD the DSP processing mimics an analog Clip Detect approach by taking the analog gain and supply voltage into account when determining if the output is clipping against a set clipping threshold..

7.3.6.6 Charge Pump

The TAS6754-Q1 has built-in protections on the charge pump pins (CP, CPC_TOP, and CPC_BOT). When the device detects a fault condition on the charge pins the charge pump skips a clock cycle. This is considered one fault cycle. The device tries again on the next incoming clock cycle. If a fault condition is detected two times consecutively or three times in total, the charge pump starts to ignore the incoming clock and go into a Charge Pump Fault condition with the output stage in Hi-Z and charge pump shutdown.

Based on the configuration, a fault signal is generated, which by default generates an active low signal at the $\overline{\text{FAULT}}$ pin.

7.3.6.7 Temperature Protection and Monitoring

The device monitors temperature with five temperature sensors. Every output channel has a temperature sensor in close proximity to the center of the output channels output stage to monitor the temperature of each channel separately. An additional temperature sensor is located in a global position on the die, this better represents the actual die junction temperature. Based on these sensors, warning and fault signals can be generated. A Thermal Gain Foldback scheme is available that autonomously regulates audio gain and consequently limits die temperature.

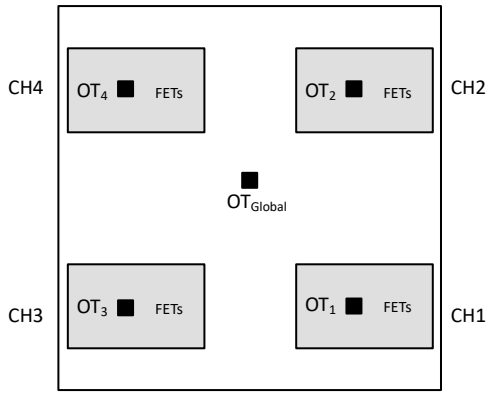


Figure 7-17. Abstract Temperature Sensor Locations Within the Device

7.3.6.7.1 Overtemperature Shutdown

The temperature thresholds for global OTSD and for overtemperature shutdowns generated by the output channels, OTSD(i) are set to fixed values. Refer to Section 5.5 for the nominal temperature and recovery hysteresis values.

Global OTSD: If the global junction temperature rises above the OTSD threshold, all channels are placed into a protective shutdown state and an Overtemperature Shutdown (OTSD) Event is created.

Channel-specific OTSD: If the junction temperature of a channel rises above the OTSD threshold, the affected channel is put into a protective state and an Overtemperature Shutdown (OTSD) Event is created.

The tolerance of the warning levels and OTSD temperatures track each other.

By default, a fault signal generates an active low signal on the $\overline{\text{FAULT}}$ Pin when an OTSD event occurs.

7.3.6.7.2 Overtemperature Warning

The temperature threshold for global Overtemperature Warning (OTW) is fixed to the level shown in the *Electrical Characteristics*. Each output channel has an independent temperature sensor.

During operation, if the device heats up and crosses the threshold, a global Overtemperature Warning Event is generated. Similarly, if the temperature at a channel raises above the threshold an Overtemperature Warning Event for that channel is generated. While the device continues to operate, the OTW information enables higher level software to make decisions to optimize thermal system performance.

As described in the Overtemperature Warning Event, the report can either be polled via I^2C register or a hardware signal can be generated by assigning a GPIO Pin for Warning Signals and enabling the OTW report routing.

7.3.6.7.3 Thermal Gain Foldback

Thermal Gain Foldback (TGFB) is a power limiting feature to protect the TAS6754-Q1 from excessive die temperature while maintaining audio output.

The main purpose of foldback power limiting is to keep the output stage within safe power dissipation limit to avoid unexpected Overtemperature Shutdown. The feature provides a smooth audio response and allows for uninterrupted music playback when temperature limits are crossed. That means the TAS6754-Q1 does not simply shut down, but continues to operate with considerable music output power while avoiding the trigger of OTSD.

The DSP of TAS6754-Q1 monitors the die temperature continuously in real-time for safe operation. The device can warn the host if the die temperature is approaching the OTW limits. TAS6754-Q1 still functions until the temperature reaches the OTSD threshold, at which either individual channels or the amplifier is shut down.

If the channel die temperature rises above the configured foldback level, the thermal gain foldback circuit initially activates. The device starts to reduce the gain in steps of 0.25dB per sample and thereby output power. This attack rate can be configured. The configured max attenuations are individual to the level and do not stack between levels.

When the temperature decreases below the foldback level, the attenuation is held for a configurable number of samples before the attenuation begins releasing at the gain step rate of 0.1dB per sample. This release rate of the TGFB can be programmed.

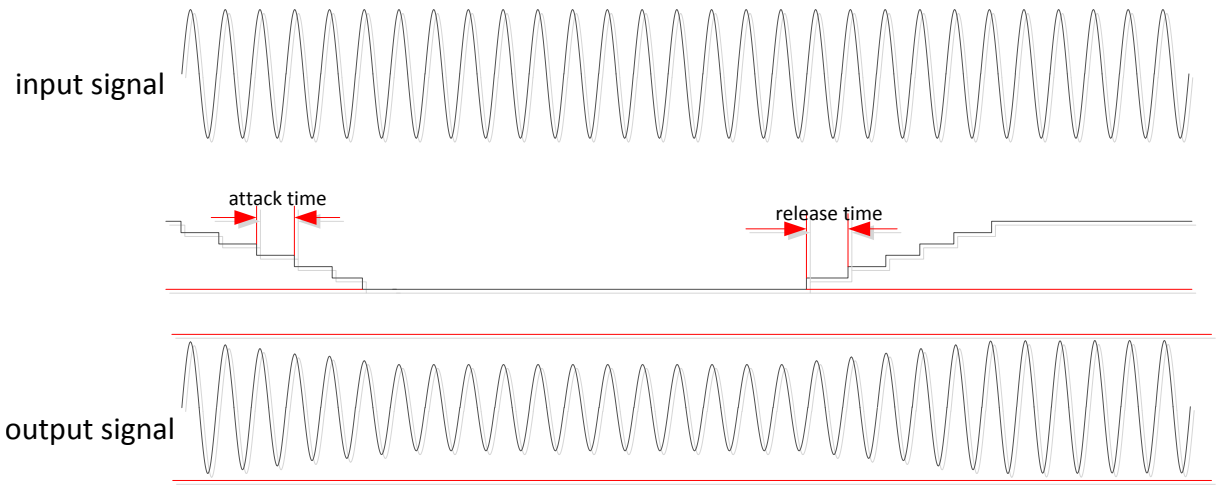


Figure 7-18. Thermal Foldback Attack and Release

7.3.6.8 Power Failures

The power supplies VBAT, PVDD, DVDD, and charge pump are monitored for undervoltage and overvoltage events as described in Power Fault Events. This automatically engages shutdown and protects the device. VBAT and PVDD safe operating voltage ranges can be found in the *Recommended Operating Conditions* table.

The device shutdowns if DVDD supply falls below V_{POR_OFF}. The DVDD POR fault event is described in DVDD Power-On-Reset .

7.3.7 Hardware Control Pins

7.3.7.1 $\overline{\text{FAULT}}$ Pin

By default the $\overline{\text{FAULT}}$ pin reports fault events and is active low under any of the following conditions:

- Overtemperature shutdown (OTSD) - Latching and non-latching
- Overcurrent Limit and Shutdown events - Latching
- DC Detect - Latching

Register bits are available to mask fault categories from reporting to the $\overline{\text{FAULT}}$ pin. These bits only mask the setting of the pin and do not affect the register reporting or protection of the device. Additional fault events can be assigned to be reported by the $\overline{\text{FAULT}}$ pin. These include:

- Power Faults - Latching and non-latching
- DC Load Diagnostic faults
- Real-time Load Diagnostic reports - Latching and non-latching
- Clock Errors - Latching
- Charge Pump faults - Latching and non-latching
- Warning events

This pin is an open-drain output with an internal 110 kΩ pull-up resistor to DVDD.

7.3.7.2 $\overline{\text{PD}}$ Pin

The $\overline{\text{PD}}$ pin is active low. When asserted the device goes into shutdown and current draw is limited to a minimum. During shutdown all internal blocks are powered off and registers initialize to default values during the next start-up.

This pin has a 110kΩ internal pull-down resistor.

7.3.7.3 $\overline{\text{STBY}}$ Pin

The $\overline{\text{STBY}}$ pin is active low. When asserted, the $\overline{\text{STBY}}$ pin sets the device into DEEP SLEEP state. In this mode the device has a reduced current while the output pins are placed into a Hi-Z state. All internal analog bias are disabled. In DEEP SLEEP and while DVDD is present, the I^2C bus is active and the internal registers are active.

This pin has a 110kΩ internal pull-down resistor.

7.3.7.4 GPIO Pins

TAS6754-Q1 offers two configurable GPIO pins. The pins can be configured as input or outputs. The pins must be configured through I^2C before becoming operational after Device Initialization and Power-On-Reset (POR).

7.3.7.4.1 General Purpose Input

A General Purpose Input (GPI) pin can be configured by assigning a function to the pin through I^2C in the related register.

7.3.7.4.2 General Purpose Output

A General Purpose Output (GPO) pin can be configured by writing the value of the intended output function to the GPO pin configuration register through I^2C. lists the GPO configuration register address for all GPIO pins.

7.3.7.5 Advanced GPIO functions

7.3.7.5.1 Clock Synchronization

TAS6754-Q1 supports multiple options for clock synchronization to improve system EMI behavior and control supply peak current conditions.

7.3.7.5.1.1 External SYNC signal (GPIO sync)

Multiple TAS6754-Q1 synchronize the clocks by using an externally provided sync signal.

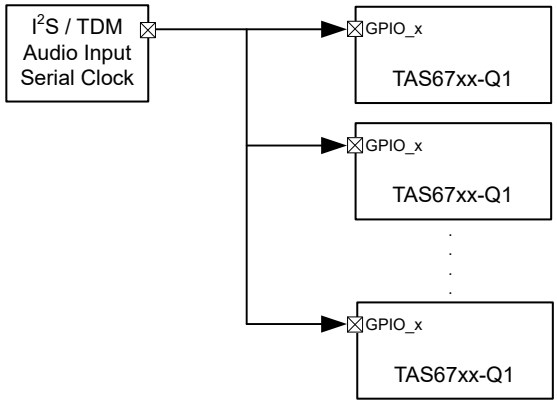


Figure 7-19. External SYNC signal architecture

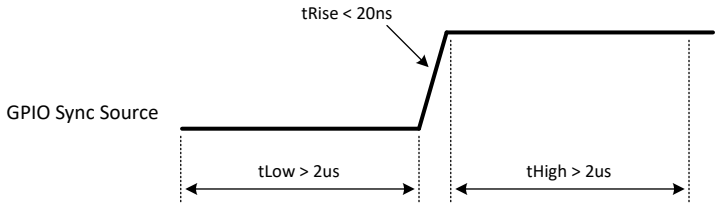


Figure 7-20. GPIO Sync source signal

7.3.7.5.1.2 Synchronization through the audio serial clock (SCLK)

Multiple TAS6754-Q1 synchronize clocks through the Audio Serial Clock (SCLK).

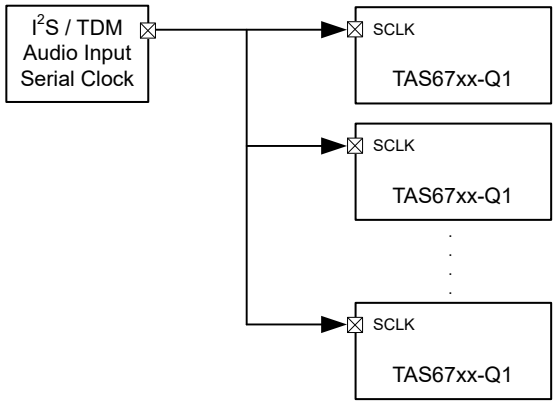


Figure 7-21. Audio serial clock (SCLK) Synchronization architecture

7.3.7.5.1.3 TAS6754-Q1 as clock source for external devices

This synchronization option allows the TAS6754-Q1 to share the devices clock with external system components such as a DC-DC regulator. In this mode the device shares internal ramp clock through the selected GPIO pin. If Spread Spectrum is enabled, the clock output is affected and share the spread signal frequency with the

connected component. Refer to the technical documentation of the connected system components to maintain correct sequencing for clock synchronization and avoiding unexpected system behavior.

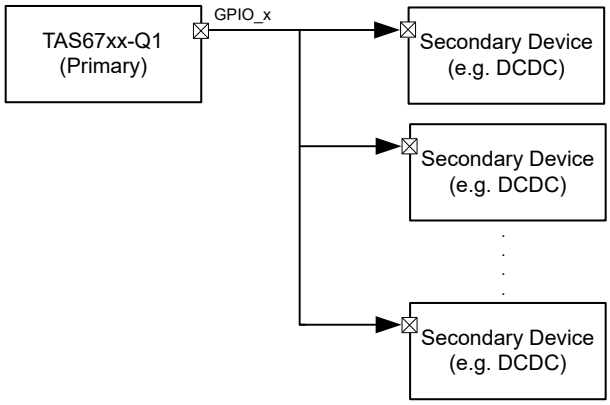


Figure 7-22. Clock source for external devices architecture

7.4 Device Functional Modes

7.4.1 Internal Reporting Signals

To support software driver development, the TAS6754-Q1 allows the flexible configuration of internal fault and warning signals. These signals, where applicable, can be configured based on current device status registers or events stored in memory registers. These signals can be configured and routed to the available GPIO pins for signaling purposes.

7.4.1.1 Fault Signal

Automotive systems have a high demand on gathering device information in case of unexpected conditions. of TAS6754-Q1 allow for a flexible configuration of fault information necessary for higher level system software to effectively control the system.

The Fault Signal can be configured to be active in response to the following Fault Events:

- Power Fault (latched or non-latched)
- Overtemperature Shutdown (latched or non-latched)
- DC Load Diagnostic events
- Overcurrent limiting and shutdown (latched)
- DC Detect (latched)
- Channels entering the FAULT state
- Real-Time Load Diagnostics faults (latched)
- Clock error (latched)
- Charge Pump Fault (latched)

The Fault Signal, by default, gets routed to the $\overline{\text{FAULT}}$ to create a HW signal. The Fault Signal can optionally be routed to additional GPIO pins.

There are two report bits for Fault signals:

- GLOBAL FAULT - Reports any active fault in device, regardless of fault signal configuration
- FAULT SIGNAL - Reports active fault signals that are configured accordingly in the fault signal configuration registers

7.4.1.2 Warning Signal

The Warning Signal can be configured to be active in response to the following Warning Events:

- Power Fault (latched or non-latched)
- Overtemperature Shutdown (latched or non-latched)
- Overtemperature Warning (latched or non-latched)
- DC Load Diagnostic events
- Overcurrent limiting (latched or non-latched)
- Clip Detect (latched or non-latched)
- Real-Time Load Diagnostics faults (latched)
- Clock error (latched)

The Warning Signal is by default not routed to a pin. TAS6754-Q1 can be configured to route warning signals to GPIO pins to create a HW signal.

- GLOBAL WARNING - Reports any active warning in device, regardless of warning signal configuration with the exception of Clock Fault events.
- WARNING SIGNAL - Reports active warning signals that are configured accordingly in the warning signal configuration registers

7.4.2 Device States and Flags

7.4.2.1 Audio Channel States

Every audio channel has a set of states that carefully control the set up and shut down procedure of an audio path from source to load. These states are listed in Table 7-2.

Table 7-2. Audio Channel States

STATE NAME	OUTPUT FETS	DSP	OSCILLATOR	I²C	LEVEL
SHUTDOWN	Hi-Z	Stopped	Stopped	High impedance	Device
DEEP SLEEP	Hi-Z	Stopped	Active	Active	Device
LOAD DIAG	Hi-Z	Stopped	Active	Active	Channel
SLEEP	Hi-Z	Stopped	Active	Active	Channel
HI-Z	Hi-Z	Active	Active	Active	Channel
PLAY	Switching with audio	Active	Active	Active	Channel
FAULT	Hi-Z	Stopped	Active	Active	Channel
AUTOREC	Hi-Z	Stopped	Active	Active	Channel

7.4.2.1.1 SHUTDOWN State

The device remains in shutdown when the $\overline{PD}$ pin is pulled low. All internal regulators are disabled for minimal power consumption.

Releasing the $\overline{PD}$ pin starts the device and resets all registers to the default value. SHUTDOWN is maintained on a device level with no deviation for individual channels.

7.4.2.1.2 DEEP SLEEP State

DEEP SLEEP puts the device in a standby state. In DEEP SLEEP, the I²C communication and registers as well as the 1.5V LDO for the digital core are active. All other regulators remain deactivated to save energy.

DEEP SLEEP is an appropriate state to configure the device through I²C before powering up. Unlike SHUTDOWN state, entering or exiting DEEP SLEEP state maintains the register map and DSP memory.

Note

The DSP is deactivated in DEEP SLEEP.

7.4.2.1.3 LOAD DIAG State

Diagnostic mode engages the DC Diagnostic circuitry to test for Short to Power, Short to Ground, Shorted Load and Open Load without activating the output power stage. These tests must be completed without fault before the Output FETs can be activated. For a more detailed description see DC Load Diagnostics.

The DC diagnostics are available as soon as the device supplies are within the *Recommended Operating Conditions*. The DC diagnostics do not rely on external audio input signals or clock and sync frequencies to be available.

LOAD DIAG can be set on a channel level. Channels transition to SLEEP state mode after successfully passing the diagnostic tests.

7.4.2.1.4 SLEEP State

SLEEP state activates further functional blocks in comparison to the DEEP SLEEP state, including the internal LDO for analog circuitry and gate driver. The supply for the Digital-to-PWM conversion remains deactivated.

SLEEP can be set on a channel level. Each channel transitions to Hi-Z state by setting the State Control register to either Hi-Z or PLAY under the condition that no clock error is present.

7.4.2.1.5 Hi-Z State

In Hi-Z state the output driver is set to a high impedance state while all other blocks are fully functional.

The channel transitions to PLAY state by setting the State Control register to PLAY.

7.4.2.1.6 PLAY State

In PLAY state the device is fully operational. The output stages are active, switching and amplify the input signal.

Real-Time Load Diagnostics can be activated to monitor the connected load for shorts or open conditions.

7.4.2.1.7 FAULT State

FAULT state is a device-internally generated mode that cannot be manually set by the user.

If one or more channels of the device are in PLAY state and encounter a fault, the device needs to take protective actions and shutdown one or more audio channels. The output FETs of only the affected channels are turned off and the output pins become high impedance. The reported state for affected channels is 'FAULT'.

Possible reasons for individual channels to enter this state are:

- Overcurrent Shutdown
- Load Current fault
- DC Diag fault
- Real-Time Load Diagnostic fault
- Channel over temperature shutdown, if configured to no auto-recovery

Possible reason for all channels to enter this state is:

- Global over temperature shutdown, if configured to no auto-recovery
- Charge Pump fault

7.4.2.1.8 Auto Recovery (AUTOREC) State

AUTOREC is a device-internally generated state that cannot be manually set by the user.

If one or more channels of the device are in PLAY state and encounter a fault, the device needs to take protective actions and shutdown one or more audio channels. The output FETs of the affected channels are turned off and the output pins become high impedance. Once the cause for the protective shutdown is no longer present, the device auto-recovers and resumes back to PLAY. The reported state for affected channels is 'AUTOREC'.

Possible reason for individual channels to enter this state is:

- Channel over temperature shutdown, OTSD(i), if configured to auto-recovery

Possible reasons for all channels to enter this state are:

- Power failures
- Clock Error
- Global over temperature shutdown, OTSD, if configured to auto-recovery

7.4.3 Fault Events

7.4.3.1 Power Fault Events

Power fault events are by default masked from pin reporting. This can be enabled. See $\overline{\text{FAULT}}$ for more details.

7.4.3.1.1 DVDD Power-On-Reset (POR)

When DVDD falls below V_{POR_OFF}, the device shuts down. All channels are set to SLEEP State, the DSP is disabled and I^2C communication terminates. When DVDD rises above V_{POR_SET} or when the device is first powered and DVDD rises above V_{POR_SET} the device initiates a Power-On-Reset routine. During this routine all registers and device states are set to default values.

7.4.3.1.2 DVDD Undervoltage Fault

The DVDD undervoltage (UV) protection detects low voltages on the DVDD pin. In the event of a UV condition, the device moves all channels from PLAY/HI-Z to Auto Recovery (AUTOREC) state, disable the DSP, and update the I^2C report registers.

7.4.3.1.3 VBAT Overvoltage Fault

When the VBAT supply rail rises above nominal range, a VBAT Overvoltage Fault event is created and the device enters into Auto Recovery (AUTOREC) State. Once VBAT falls back down into nominal range, the fault event is cleared.

7.4.3.1.4 VBAT Undervoltage Fault

When the VBAT supply rail falls below nominal range, a VBAT Undervoltage Fault event is created and the device enters into Auto Recovery (AUTOREC) state. Once VBAT rises back up into nominal range, the fault event is cleared.

7.4.3.1.5 PVDD Overvoltage Fault

When the PVDD supply rail rises above nominal range, a PVDD Overvoltage Fault event is created and the device enters into Auto Recovery (AUTOREC) state. Once PVDD falls back down into nominal range, the fault event is cleared.

7.4.3.1.6 PVDD Undervoltage Fault

When the PVDD supply rail falls below nominal range, a PVDD Undervoltage Fault event is created and the device enters into Auto Recovery (AUTOREC) state. Once PVDD rises back up into nominal range, the fault event is cleared.

7.4.3.2 Overtemperature Shutdown (OTSD) Event

Section Overtemperature Shutdown describes the circumstances under which the device creates an OTSD event as well as the configurable recovery behavior.

7.4.3.3 Overcurrent Limit Fault Event

Section Overcurrent Limit (Cycle-By-Cycle) describes the circumstances under which the device creates an Overcurrent Limit Fault event. This is a transient event that only lasts for a limited time.

7.4.3.4 Overcurrent Shutdown Event

Section Overcurrent Protection describes the circumstances under which the device creates an OCSD event.

As Overcurrent Shutdown (OCSD) Event is a transient event and is not reported in a status register. The latched OCSD events are reported in Channel Overcurrent and DC Detection Fault Memory Register. Affected channels are placed in FAULT state.

7.4.3.5 DC Fault Event

Section DC Detect describes the circumstances under which the device creates an DC Fault event.

A DC Fault Event is a transient event and is not reported in a status register. The latched DC Fault events are reported in Channel Overcurrent and DC Detection Fault Memory Register. Affected channels are placed in FAULT state.

7.4.3.6 Clock Error Event

The Clock Rates section describes the supported Audio Data Formats, Bit Depths, and Clock Rates. If these conditions are violated or the clock is halted, the device reports a Clock Error Fault event and the device gracefully transitions to the AUTOREC state. After audio clock recovery, the device automatically returns to the previous state.

A Clock Error Event is a transient event and is not reported in a status register.

7.4.3.7 Charge Pump Fault Event

Section Charge Pump describes the circumstances under which the device creates an charge pump fault event as well as the recovery behavior.

7.4.4 Warning Events

7.4.4.1 Overtemperature Warning Event

Section Overtemperature Warning describes the circumstances under which the device creates a Overtemperature Warning event.

7.4.4.2 Overcurrent Limit Warning Event

Section Overcurrent Limit (Cycle -By-Cycle) describes the circumstances under which the device creates an Overcurrent Limit Warning event. This is a transient event that only lasts for a limited time.

7.4.4.3 Clip Detect Warning Event

Section Clip Detect describes the circumstances under which the device creates a Clip Detect Warning event.

7.5 Programming

7.5.1 I²C Serial Communication Bus

The device communicates with the system processor through the I²C serial communication bus as an I²C target-only device and supports 100kHz and 400kHz data transfer rates for random and sequential write and read operation. The processor can poll the device through I²C to determine the operating status, configure settings, or run diagnostics.

The TAS6754-Q1 register map and DSP memory span multiple pages and books. The user changes from page to page before writing individual registers or DSP memory. Changing from page to page is accomplished via register 0 on each page. This register value selects the page address, from 0 to 255. All registers listed in the TAS6754-Q1 Data sheet belong to Page 0.

For a complete list and description of all I²C controls, see the Register Maps section.

7.5.2 I²C Address Selection

TAS6754-Q1 supports eight I²C addresses, thus up to eight devices can be used together in a system with no additional bus switching hardware.

The pull-up or pull-down resistor connected between the device I2C_ADDR pin and the DVDD-rail (pull-up) or GND (pull-down) determines the I²C address during power up. The I2C address latches after a POR event and is locked until the next POR event.

Table 7-3. I²C Addresses

I2C_ADDR Pin Pull-Up resistor	I2C_ADDR Pin Pull-Down resistor	I²C Write	I²C Read
-	0	0xE0	0xE1
-	1 kΩ	0xE2	0xE3
-	4.7 kΩ	0xE4	0xE5
-	24 kΩ	0xE6	0xE7
24 kΩ	-	0xE8	0xE9
4.7 kΩ	-	0xEA	0xEB
1 kΩ	-	0xEC	0xED
0	-	0xEE	0xEF

7.5.3 I²C Bus Protocol

The I²C bus uses two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8- bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the controller device driving a start condition on the bus and ends with the controller device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. The controller generates the 7-bit target address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The device holds SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When this occurs, the controller transmits the next byte of the sequence. Each device is addressed by a unique 7-bit target address plus a R/W bit (1 byte). All compatible devices share the same

signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. The number of bytes that can be transmitted between start and stop conditions is unlimited. When the last word transfers, the controller generates a stop condition to release the bus.

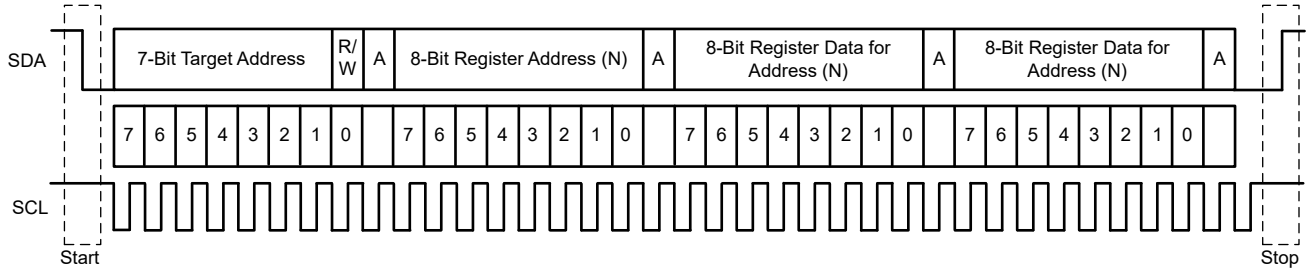


Figure 7-23. Typical I²C Sequence

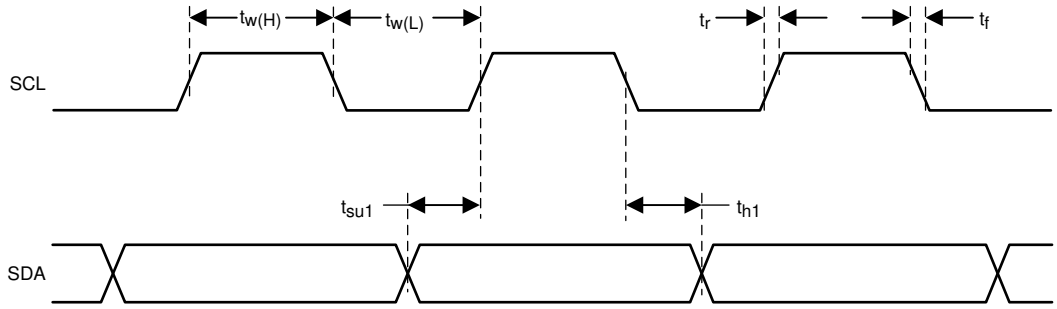


Figure 7-24. SCL and SDA Timing

7.5.4 Random Write

As shown in Figure 7-25 , a single-byte data-write transfer begins with the controller device transmitting a start condition, followed by the I²C device address, and then read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the controller transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the controller device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the controller device transmits a stop condition to complete the single-byte data-write transfer.

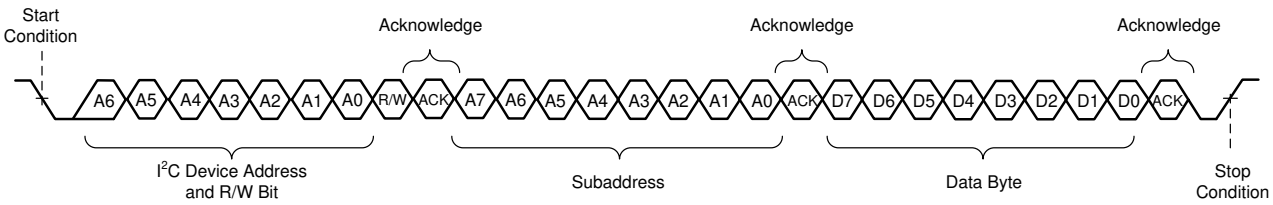


Figure 7-25. Random Write Transfer

7.5.5 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the controller to the device as shown in Figure 7-26. After receiving each data byte, the device responds with an acknowledge bit and the I²C subaddress is automatically incremented by one.

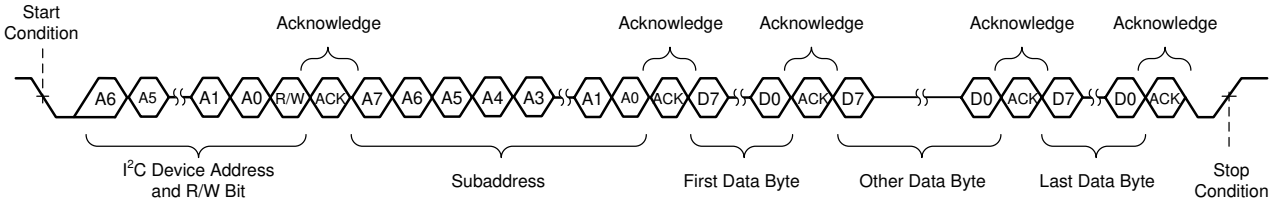


Figure 7-26. Sequential Write Transfer

7.5.6 Random Read

As shown in Figure 7-27, a single-byte data-read transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the controller device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

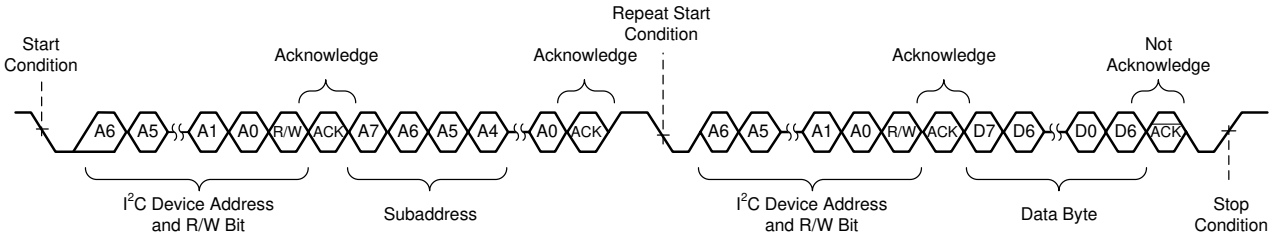


Figure 7-27. Random Read Transfer

7.5.7 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the controller device as shown in Figure 7-28. Except for the last data byte, the controller device responds with an acknowledge bit after receiving each data byte and automatically increments the I²C subaddress by one. After receiving the last data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the transfer.

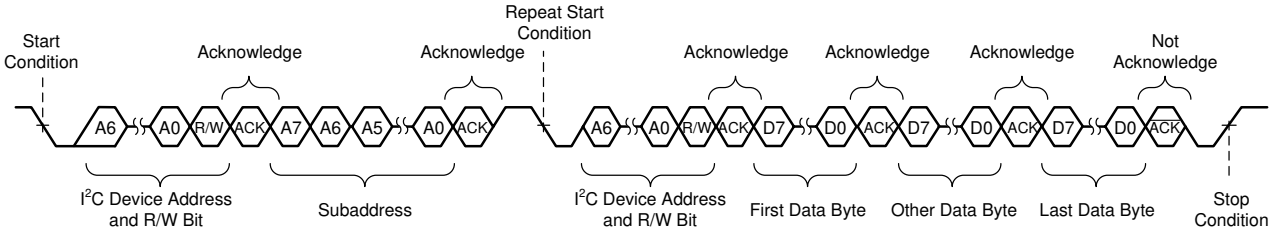


Figure 7-28. Sequential Read Transfer

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TAS6754-Q1 is a four-channel digital input Class-D audio-amplifier design with integrated real time Current Feedback and DSP for use in automotive head units and external amplifier modules. The TAS6754-Q1 incorporates the necessary functionality to perform in demanding automotive OEM applications.

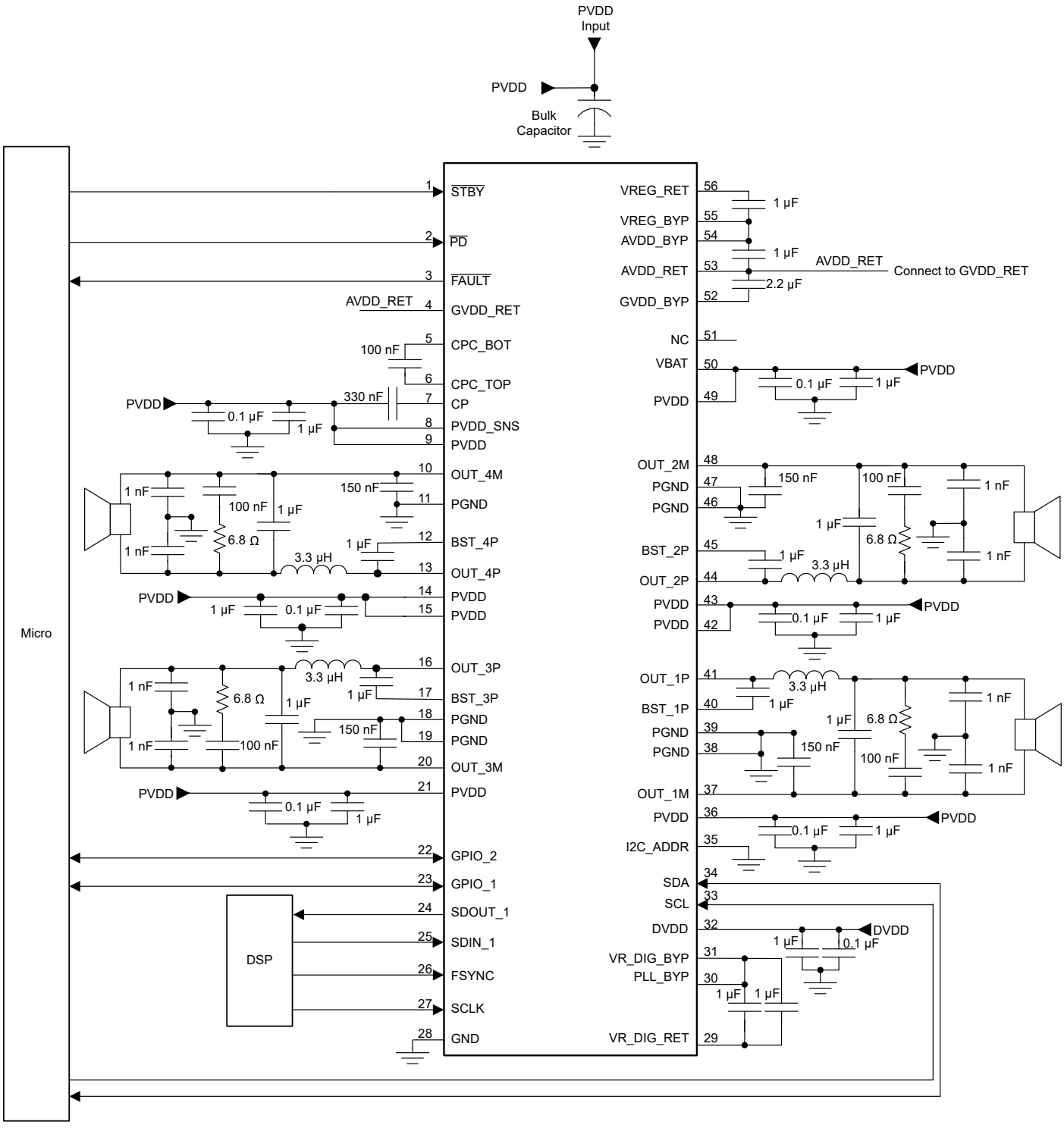
8.1.1 Reconstruction Filter Design

The amplifier outputs are driven by high-current LDMOS transistors in an H-bridge configuration. The OUTP transistors are either fully off or fully on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. An LC demodulation filter is used to recover the audio signal. The filter attenuates the high-frequency components of the output signals that are out of the audio band. The design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to meet the system THD+N requirements, carefully consider the selection of the inductors used in the output filter.

8.2 Typical Application

8.2.1 BTL Application

Figure 8-1 shows the schematic for a typical 4 channel application.


PVDD
Input
PVDD
Bulk
Capacitor
Micro
DSP
1 STBY
2 PD
3 FAULT
AVDD_RET 4 GVDD_RET
5 CPC_BOT
6 CPC_TOP
7 CP
8 PVDD_SNS
9 PVDD
10 OUT_4M
11 PGND
12 BST_4P
13 OUT_4P
14 PVDD
15 PVDD
16 OUT_3P
17 BST_3P
18 PGND
19 PGND
20 OUT_3M
21 PVDD
22 GPIO_2
23 GPIO_1
24 SDOUT_1
25 SDIN_1
26 FSYNC
27 SCLK
28 GND
VREG_RET 56
VREG_BYP 55
AVDD_BYP 54
AVDD_RET 53
GVDD_BYP 52
NC 51
VBAT 50
PVDD 49
OUT_2M 48
PGND 47
PGND 46
BST_2P 45
OUT_2P 44
PVDD 43
PVDD 42
OUT_1P 41
BST_1P 40
PGND 39
PGND 38
OUT_1M 37
PVDD 36
I2C_ADDR 35
SDA 34
SCL 33
DVDD 32
VR_DIG_BYP 31
PLL_BYP 30
VR_DIG_RET 29
1 µF
2.2 µF
AVDD_RET
Connect to GVDD_RET
0.1 µF
330 nF
100 nF
150 nF
1 nF
6.8 Ω
3.3 µH
DVDD

8.2.2 Power Supply Recommendations

The TAS6754-Q1 requires three power supplies. The PVDD supply is the high-current supply in the recommended supply range. The VBAT supply is lower current supply that must be in the recommended supply range. The PVDD and VBAT pins can be connected to the same supply. When using a higher voltage, TI recommends to use automotive battery voltage for VBAT for improved efficiency. The DVDD supply is the 1.8Vdc or 3.3Vdc logic supply and must be maintained in the tolerance as shown in the *Recommended Operating Conditions* in the device data sheet.

8.2.3 Power Supply Decoupling

The power supply decoupling has multiple functions. The large electrolytic capacitor is used to reduce the PVDD voltage ripple due to the audio frequencies. The 1µF MLCC on each group of PVDD pins is to reduce the PVDD voltage ripple at the PWM switching frequency and the 100nF is for EMI reduction. The large electrolytic capacitor value is dependent on the regulation capabilities of the boost converter used. If a battery is used with long wires, a larger value is needed to reduce the voltage ripple in the audio band to meet the output power requirements.

8.3 Layout

8.3.1 Layout Guidelines

The TAS6754-Q1 has two output channels on each side of the device, to achieve the best thermal performance. See Typical Application for a typical application schematic. Figure 8-2 shows a reference low EMI layout.

8.3.1.1 Electrical Connection of Thermal pad and Heat Sink

For the DKQ package, the heat sink connected to the thermal pad of the device is connected to GND. The heat slug must not be connected to any other electrical node.

8.3.1.2 EMI Considerations

Automotive-level EMI performance depends on both careful integrated circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design. The design has minimal parasitic inductances because of the short leads on the package which reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase. The design also incorporates circuitry that optimizes output transitions that cause EMI.

For optimizing the EMI a solid ground layer plane is recommended. While the TAS6754-Q1 EVM layout is a good starting point, the EVM layout is not recommended for EMC testing. Further board level optimizations are suggested to maintain that the EMI requirements are passed. A first reference is seen in Figure 8-2

8.3.1.3 General Guidelines

Refer to Section 8.3.2 for the following guidelines:

- PVDD decoupling capacitors, **A**. The 100nF capacitors are placed on the same layer and very close to the device, with the ground return close to the PGND pins. The 1µF capacitors can be placed on the back of the PCB.
- Traces that carry large currents incorporate multiple vias, **B**, to reduce the series impedance of these traces.
- A ground plane, **C**, on the same side as the device pins, helps reduce EMI by providing a very-low loop impedance for the high-frequency switching current. This plane has many vias between the ground planes on other layers.
- The ground connections for the capacitors in the LC filter, **D**, have a direct path back to the device and also the ground return for each channel is the shared. This direct path allows for improved common mode EMI rejection. This is on the same layer of the PCB as the TAS6754-Q1.
- OUT_xP inductor, OUT_xP to OUT_xM capacitor, and the OUT_xM to GND capacitor, **E**, need to have minimum loop size, starting from the device's OUT pin to GND pins. These are the switching related PCB traces. The loop size directly influences the electric field coupling.
- Heat sink mounting screws, **F**, are close to the device to keep the loop short from the package to ground, providing a low impedance trace for the high frequency noise coupled into the heat sink back to the PCB.

- Decoupling capacitors, **G**, at PLL_BYP, VR_DIG_BYP, VR_DIG_RET, AVDD_BYP, AVDD_RET, VREG_BYP, VREG_RET, GVDD_BYP, DVDD, are placed on the same layer with device, without affecting the return path from the LC filter, **D**.
- PVDD supply trace, **H**, is suggested to be placed on an internal layer, and symmetrical to the channels on both sides of the device.
- Device output trace, **I**, is suggested to be placed on an internal layer, and symmetrical on both sides of the device.

8.3.2 Layout Example

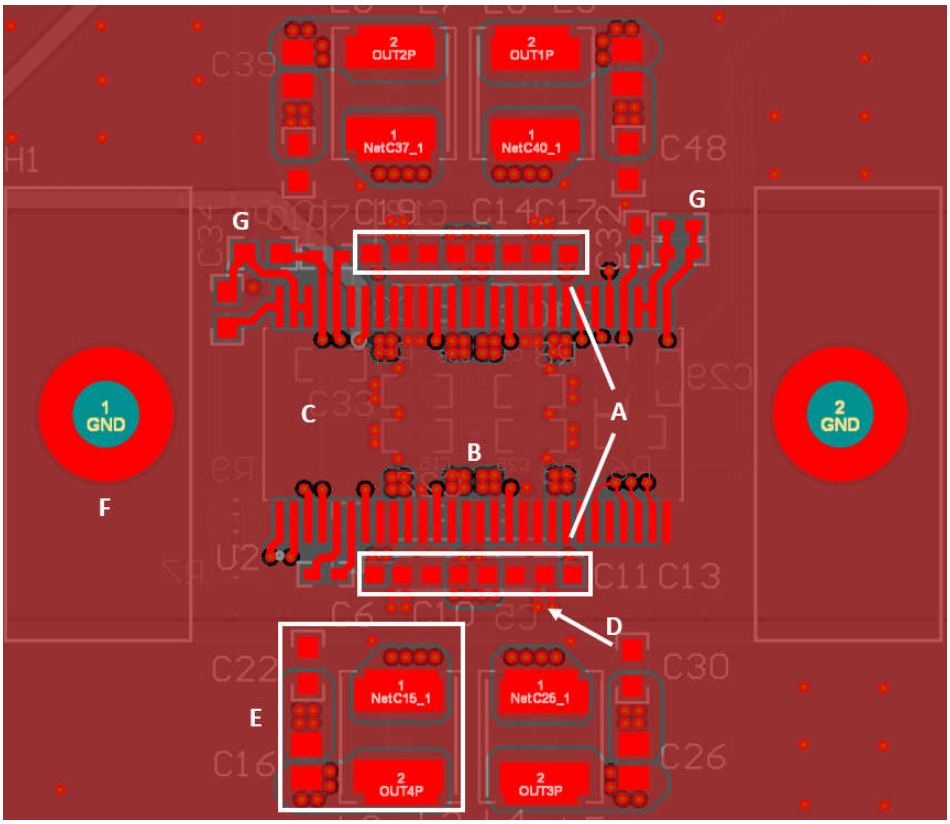


Figure 8-2. TAS6754-Q1 Layout Top Example

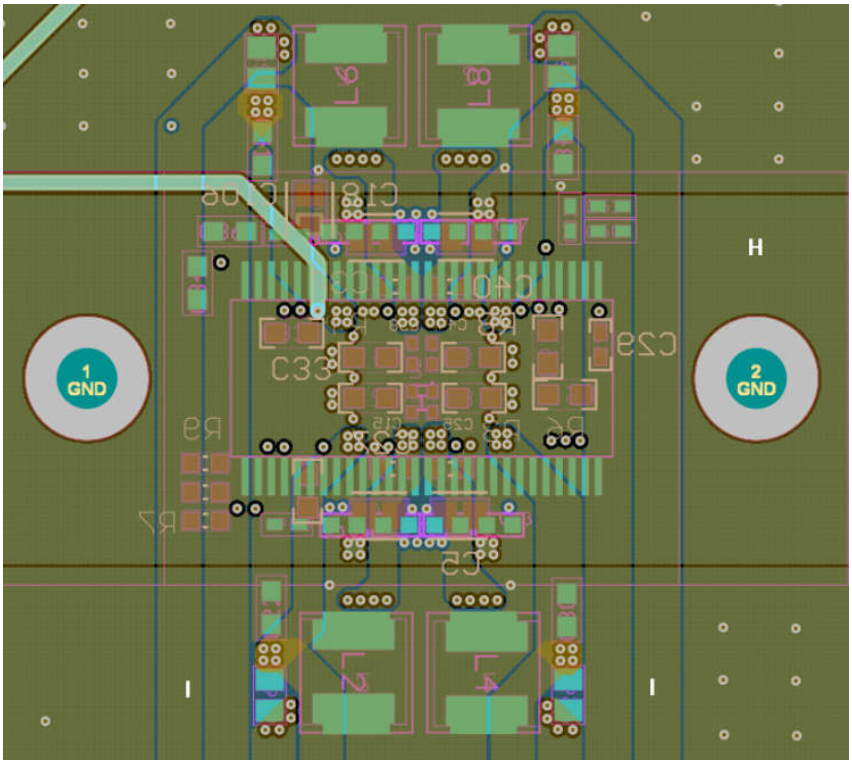


Figure 8-3. TAS6754-Q1 Example PVDD and Output Traces

8.3.3 Thermal Considerations

The thermally enhanced PowerPAD package has an exposed pad up for connection to a heat sink. The output power of any amplifier is determined by the thermal performance of the amplifier as well as limitations placed on the amplifier by the system, such as the ambient operating temperature. The heat sink absorbs heat from the TAS6754-Q1 and transfers the heat to the air. With proper thermal management this process can reach equilibrium and heat can be continually transferred from the device. Heat sinks can be smaller than that of classic linear amplifier design because of the excellent efficiency of class-D amplifiers. This device is intended for use with a heat sink, therefore, $R_{\theta JC}$ is used as the thermal resistance from junction to the exposed metal package. This resistance dominates the thermal management, so other thermal transfers is not considered. The thermal resistance of $R_{\theta JA}$ (junction to ambient) is required to determine the full thermal design. The thermal resistance is comprised of the following components:

- $R_{\theta JC}$ of the TAS6754-Q1
- Thermal resistance of the thermal interface material
- Thermal resistance of the heat sink

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- TAS6754-Q1 Technical Reference Manual
- TAS6754Q1EVM Evaluation Module Users Guide
- PurePath™ Console 3 Graphical Development Suite

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2024) to Revision A (March 2025)	Page
• Changed document status from *Advanced Information* to *Production Data*.	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTAS6754QDKQRQ1	Active	Preproduction	HSSOP (DKQ) | 56	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTAS6754QDKQRQ1.A	Active	Preproduction	HSSOP (DKQ) | 56	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TAS6754QDKQRQ1	Active	Production	HSSOP (DKQ) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6754
TAS6754QDKQRQ1.A	Active	Production	HSSOP (DKQ) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6754

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

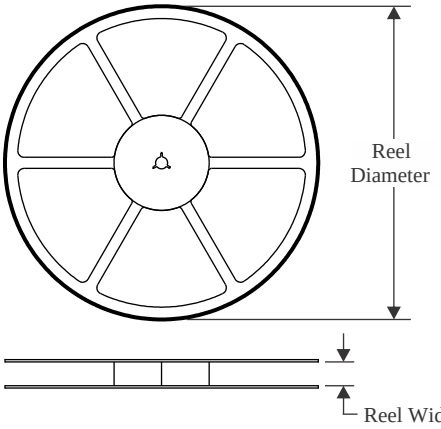
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

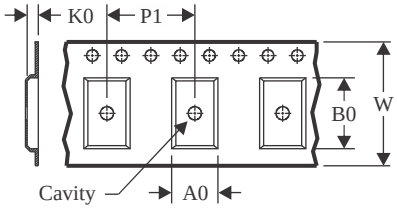
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

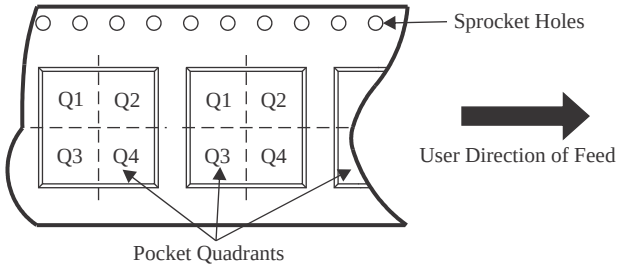


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

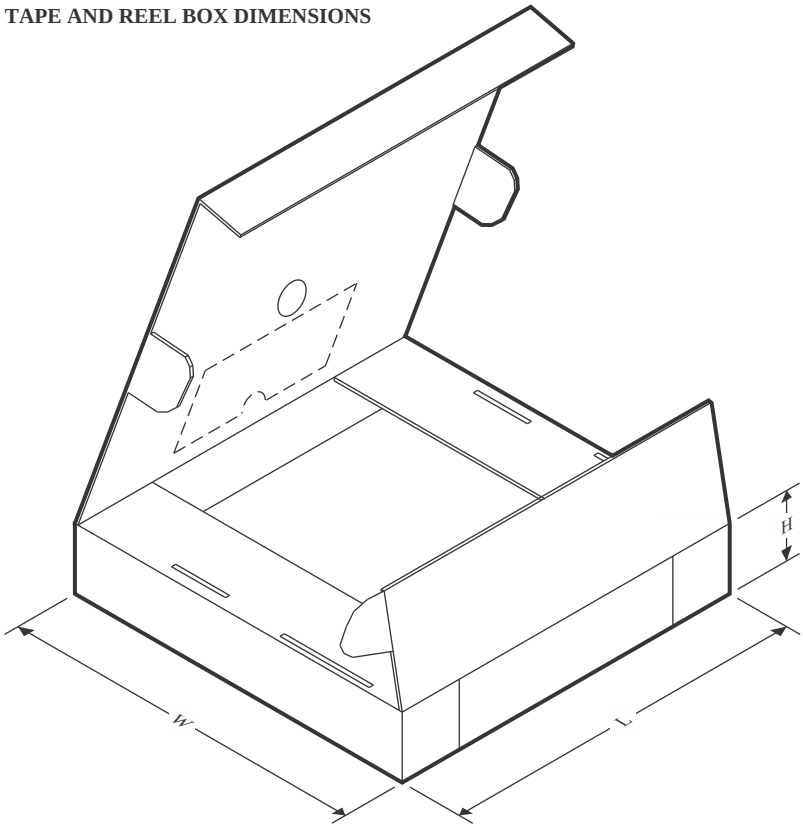
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS6754QDKQRQ1	HSSOP	DKQ	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

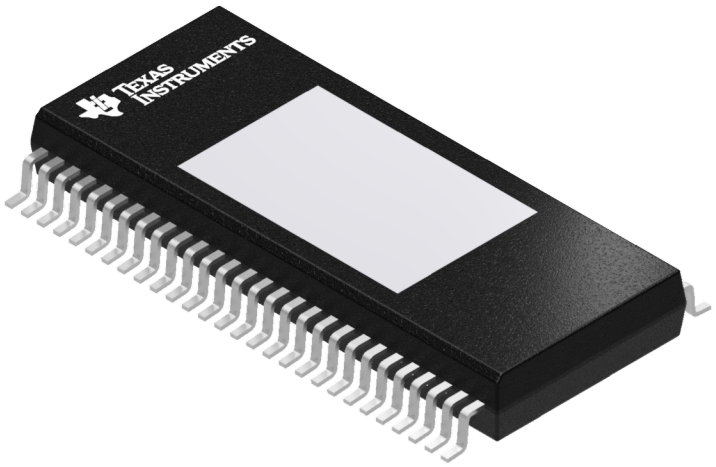


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS6754QDKQRQ1	HSSOP	DKQ	56	1000	356.0	356.0	53.0

DKQ 56 PowerPAD™ SSOP - 2.34 mm max height

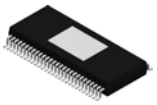
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

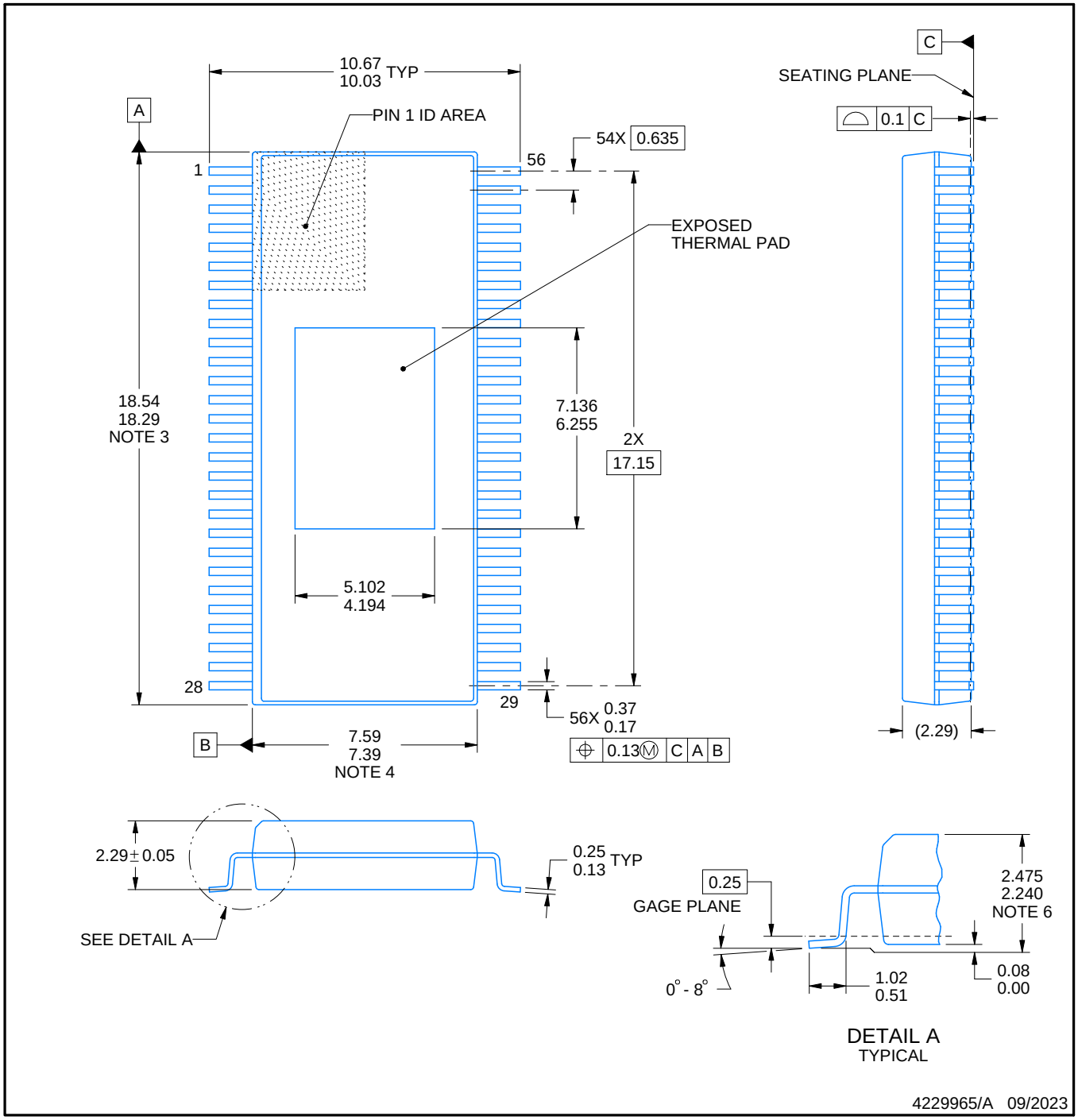
PACKAGE OUTLINE

DKQ0056D



PowerPAD™ HSSOP - 2.475 mm max height

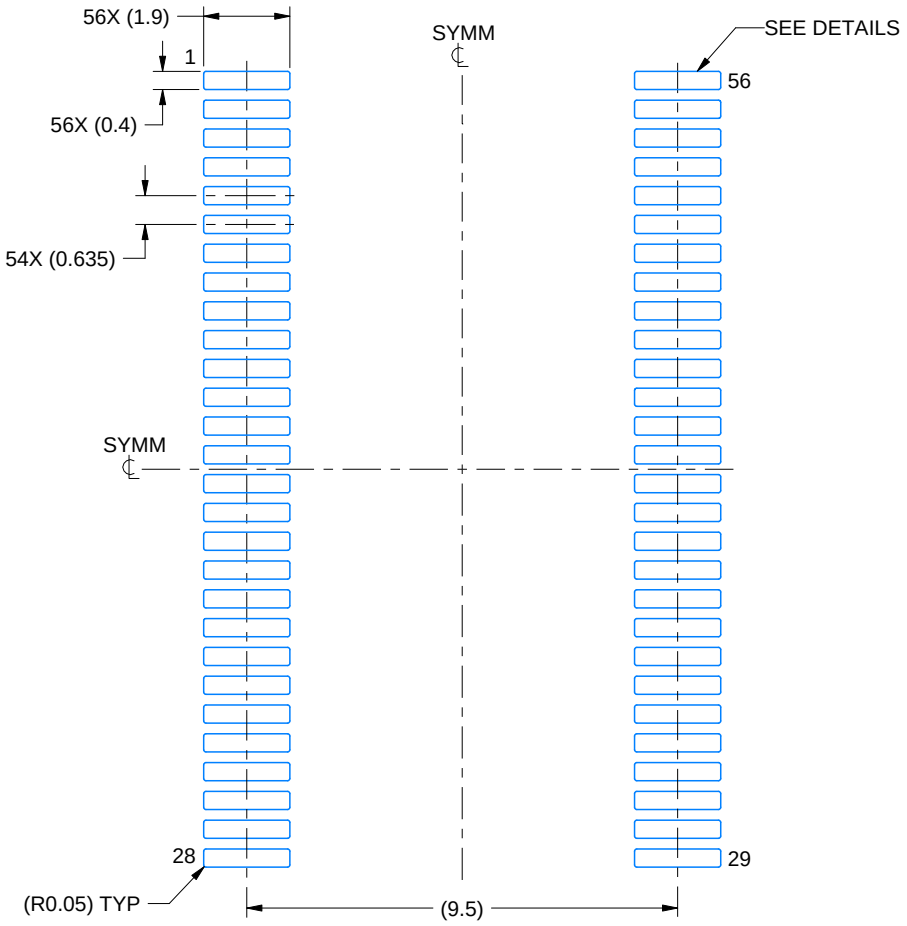
PLASTIC SMALL OUTLINE



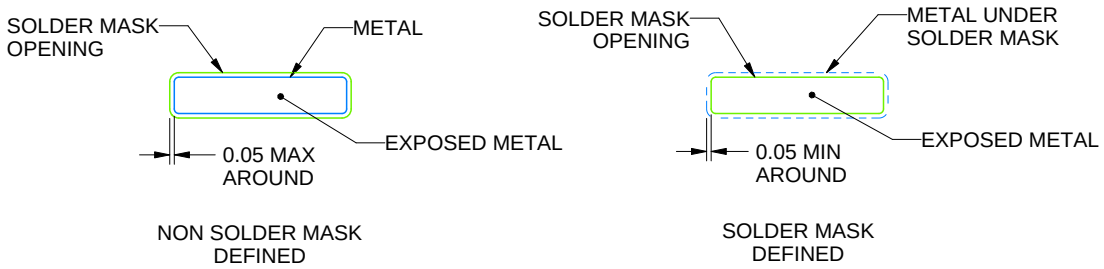
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. For clamped heatsink design, refer to overall package height above the seating plane as 2.325 +/- 0.075 and molded body thickness dimension.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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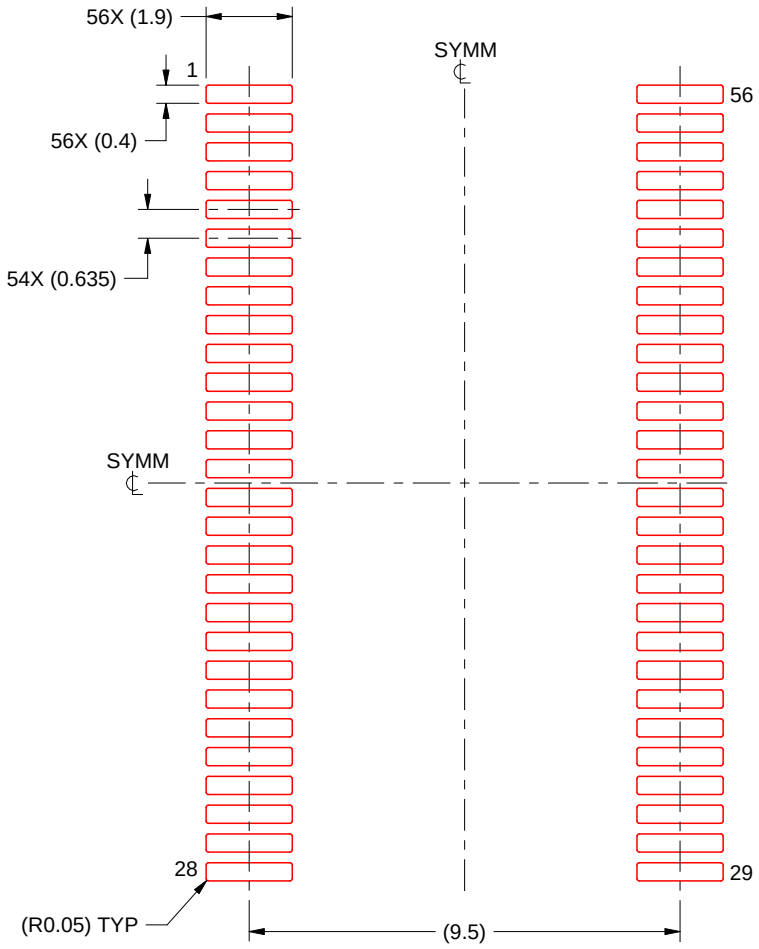
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE:6X

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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