TAS2781 24-V Class-D Amplifier with Real Time Integrated Speaker Protection and Audio Processing

1 Features

Key Features
- Integrated DSP for audio processing
- 24-V Supply for class-d output stage
- Y-Bridge multi-level supply architecture
- Hybrid-pro external boost control algorithm
- Ultrasonic output support up to 40 kHz

Output power:
- 25 W, 1% THD+N (4 Ω, 18 V)
- 30 W Maximum output power, 10% THD+N

Efficiency (1% THDN) and power consumption
- 82% at 1W, 4 Ω, PVDDH = 12 V, PVDDL = 3.8 V
- 83% at 1W, 8 Ω, PVDDH = 18 V, PVDDL = 5 V
- 84% at 1W, 4 Ω, PVDDH = 18 V, PVDDL = 5 V
- 90% at 15W, 4 Ω, PVDDH = 18 V, PVDDL = 5 V
- 93% at 15W , 8 Ω, PVDDH = 18 V, PVDDL = 5 V
- <0.5 µA in Hardware Shutdown Mode

Power supplies and management:
- AVDD: 1.8 V
- IOVDD: 1.8 V/ 3.3 V
- PVDDL: 2.7 V to 5.5 V
- PVDDH: 3 V to 24 V

Interfaces and Control:
- SDOUT for echo cancellation
- I²S/TDM: 8 channels of 32 bits up to 192 KSPS
- I²C with fast mode+ or SPI
- Inter-chip communication bus
- 16 kHz to 192 kHz sample rates

Advanced DSP audio processing:
- Real-time IV-sense for speaker protection
- Dynamic range compressor
- Brownout protection with power limiter
- Multi-channel balancing communication

Protection and EMI:
- Over power and low battery protection
- PVDDH/ PVDDL supply tracking limiters
- Thermal and over current protections
- Thermal foldback
- Post filter feedback and slew rate control

2 Applications

- Laptop and Desktop Computers
- Smart Speakers
- Tablets and Handhelds
- Wireless Speakers

3 Description

The TAS2781 is a mono, digital input Class-D audio amplifier optimized for efficiently driving high peak power into loudspeakers. The Class-D amplifier is capable of delivering 25 W of continuous power into a 4 Ω load with less than 1% THD+N at a supply voltage of 18 V. The broad voltage input range and the high output power makes this amplifier versatile enough to work with battery or line powered systems.

An on-chip DSP supports Texas Instruments Smart Amp speaker protection algorithm. The integrated speaker voltage and current sense provides for real-time monitoring of loudspeakers.

Y-Bridge power architecture improves amplifier efficiency by internally selecting the supplies for optimal headroom. Brownout prevention scheme with adjustable threshold allows reducing the gain in signal path when the supply drops.

The Hybrid-Pro algorithm allows user to optimize efficiency and improve battery life by controlling the external power supply.

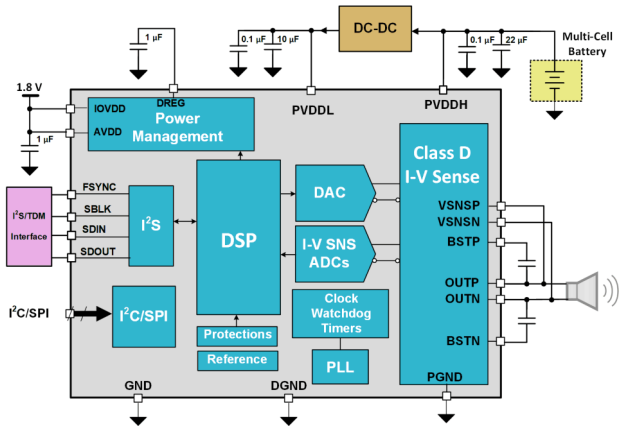
Up to eight TAS2781 devices can share a common bus via I²S/TDM and I²C/SPI interfaces.

The TAS2781 is available in a 30 pin HR-QFN package for a compact PCB footprint.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS2781	HR QFN	4 mm x 3.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2022) to Revision B (July 2023)	Page
• Updated PVDD to 24 V with -20° C temp condition footnote in *Absolute Maximum Ratings* and *Recommended Operating Conditions*	4
• Clarifications to edge rate register description	34
• PFFB feature recommendation for ferrite bead filters	68
• Startup configuration script added to fix power-up pop issue	72

Changes from Revision * (July 2022) to Revision A (November 2022)	Page
• Change device status from "Advanced Information" to "Production Data."	1

5 Pin Configuration and Functions

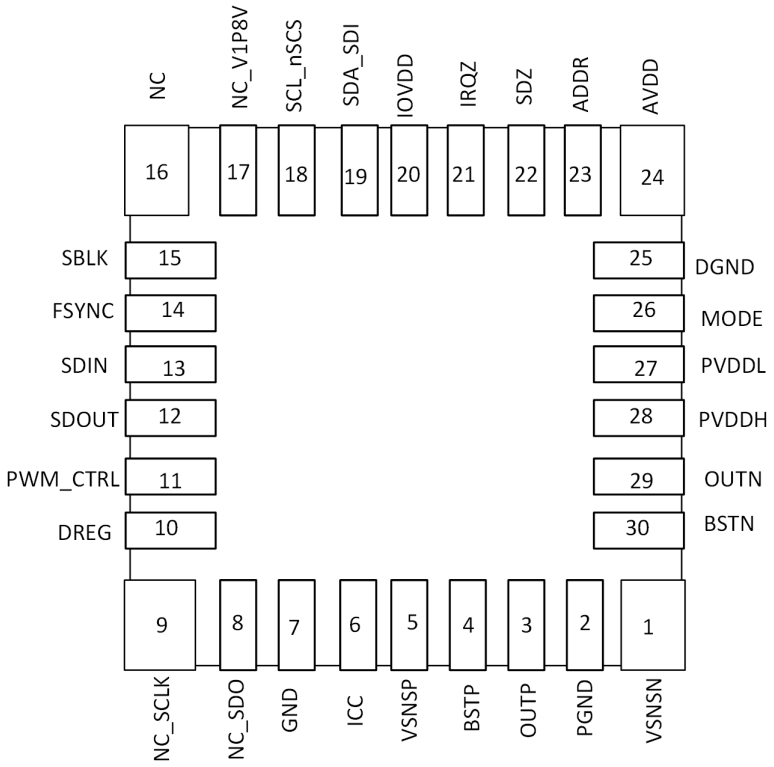


Figure 5-1. Package 30-Pin HR-QFN Bottom View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADDR	23	I	Address detect pin. Resistor value at this pin selects the I^2C address. See Section 8.3.2.
AVDD	24	P	Analog power input. Connect to 1.8 V supply and decouple to GND with capacitor.
BSTN	30	P	Class-D negative bootstrap. Connect a capacitor between BSTN and OUTN.
BSTP	4	P	Class-D positive bootstrap. Connect a capacitor between BSTP and OUTP.
DGND	25	P	Device substrate ground. Connect to PCB ground plane. Avoid any common routing inductance between this pin and GND pin.
DREG	10	P	Digital core voltage regulator output. Bypass to GND with a capacitor. Do not connect to external load.
FSYNC	14	I	Frame Synchronization Clock.
GND	7	P	Analog ground. Connect to PCB ground plane.
ICC	6	IO	Inter-chip communication pin used to transmit gain alignment. Connect to GND if not used.
IOVDD	20	P	Digital IO Supply. Connect to 1.8 V or 3.3 V IO supply and decouple with a capacitor to GND.
IRQZ	21	O	Open drain, active low interrupt pin. Pull up to IOVDD with resistor if optional internal pull up is not used.
MODE	26	I	External configuration defines the mode of operation.
NC	16	-	Tied to GND.
NC_SCLK	9	I	I^2C Mode: NC = Tied to GND, SPI Mode: Clock pin.
NC_SDO	8	O	I^2C Mode: NC = Tied to GND, SPI Mode: Serial data output pin.

Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
NC_V1P8V	17	P	NC_V1P8V = Tied to GND when ICC is not used and when SPI interface is not required, NC_V1P8V = Tied to 1.8 V supply when ICC is used and when SPI interface is required,
OUTN	29	O	Class-D negative output.
OUTP	3	O	Class-D positive output.
PGND	2	P	Class-D ground. Connect to PCB ground plane.
PVDDH	28	P	Class-D power supply input. Decouple with a capacitor.
PVDDL	27	P	Single-cell battery supply input. Decouple with a capacitor.
PWM_CTRL	11	O	Control pin for external boost converter.
SBCLK	15	I	TDM Serial Bit Clock.
SCL_nSCS	18	I	I^2C Mode: Clock pin; pull up to IOVDD with a resistor. SPI Mode: Active low chip select pin.
SDA_SDI	19	IO	I^2C Mode: Data Pin; pull up to IOVDD with a resistor. SPI Mode: Serial data input pin.
SDIN	13	I	TDM Serial Data Input.
SDOUT	12	IO	TDM Serial Data Output.
SDZ	22	I	Active low hardware shutdown.
VSNSN	1	I	Voltage Sense negative input. Connect to Class-D negative output or after a ferrite bead filter.
VSNSP	5	I	Voltage Sense positive input. Connect to Class-D positive output or after a ferrite bead filter.

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Supply Voltage	AVDD	-0.3	2	V
	IOVDD	-0.3	5	V
	NC_V1P8V	-0.3	2	V
	PVDDH	-0.3	26	V
	PVDDL	-0.3	6	V
	PVDDH - PVDDL	-0.3	22	V
Internal Supply Voltage	DREG	-0.3	1.5	V
IO Voltage(1)	SBLK, FSYNK, SDIN, SDOUT, IRQZ, SDA_SDI, SCL_nSCS, PWM_CTRL, SDZ	-0.3	5	V
IO Voltage(1)	NC_SCLK, NC_SDO, ICC, ADDR	-0.3	2	V
Operating free-air temperature, T_A ; Device is functional and reliable, some performance characteristics may be degraded.	PVDD is 23 V or below	-40	85	°C
	PVDD higher than 23 V	-20	85	°C
Performance free-air temperature, T_P ; All performance characteristics are met.		-20	70	°C
Operating junction temperature, T_J	PVDD is 23 V or below	-40	150	°C
	PVDD higher than 23 V	-20	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) All digital inputs and IOs are failsafe.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
AVDD	Supply voltage		1.65	1.8	1.95	V
IOVDD	Supply voltage		3	3.3	3.6	V
			1.65	1.8	1.95	
NC_V1P8V	Supply voltage for ICC Pin		1.65	1.8	1.95	V
PVDDH(2)	Supply voltage (functional)(1)	Min operating free-air and Min operating junction temperature of -20°C	3		24	V
		Min operating free-air and Min operating junction temperature of -40°C	3		23	
	Supply voltage (performance)	Min operating free-air and Min operating junction temperature of -20°C	4.5		24	
		Min operating free-air and Min operating junction temperature of -40°C	4.5		23	
PVDDL	Supply voltage (functional)(1)		2.7		5.5	V
	Supply voltage (performance with Y-bridge disabled)		3.5		5.5	
	Supply voltage (performance with Y-bridge enabled)		2.7		5.5	
R_{SPK}	Speaker impedance		3.2			Ω
L_{SPK}	Speaker inductance		5			µH

(1) Device will remain functional but performance may degrade.
(2) PVDDH supply voltage should be greater than PVDDL-0.7 V.

6.4 Thermal Information

THERMAL METRIC(1)		HR_QFN 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25 °C, PVDDH = 18 V, PVDDL= 3.8 V, AVDD = 1.8 V, IOVDD =1.8 V, R_L = 4Ω + 15µH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1, Measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT and OUTPUT						
V_{IH}	High-level digital input logic voltage threshold	SBLK, FSYNC, SDIN, SCL_nSCS, SDA_SDI	0.7xIOVDD			V
V_{IL}	Low-level digital input logic voltage threshold	SBLK, FSYNC, SDIN, SCL_nSCS, SDA_SDI			0.3 x IOVDD	V
$V_{IH(SDZ)}$	High-level digital input logic voltage threshold	SDZ	0.7xAVDD			V

T_A = 25 °C, PVDDH = 18 V, PVDDL= 3.8 V, AVDD = 1.8 V, IOVDD =1.8 V, R_L = 4Ω + 15µH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1, Measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL(SDZ)}$	Low-level digital input logic voltage threshold	SDZ			0.3 x AVDD	V
$V_{IH(1P8V)}$	High-level digital input logic voltage threshold	ICC, NC_SCLK	0.7xNC_V1P8V			V
$V_{IL(1P8V)}$	Low-level digital input logic voltage threshold	ICC, NC_SCLK			0.3 x NC_V1P8V	V
V_{OH}	High-level digital output voltage	SDOUT; I_{OH} = 100 µA.	IOVDD–0.2 V			V
V_{OL}	Low-level digital output voltage	SDOUT; I_{OH} = 100 µA.			0.2	V
$V_{OL(I^2C)}$	Low-level digital output voltage	SDA_SDI; I_{OL} = -1 mA.			0.2 x IOVDD	V
$V_{OH(1P8V)}$	High-level digital output voltage	NC_SDO	0.8xNC_V1P8V			V
$V_{OL(1P8V)}$	Low-level digital output voltage	NC_SDO			0.2xNC_V1P8V	V
I_{IH}	Input logic-high leakage for digital inputs	All digital pins; Input = Supply Rail.	–1		1	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins; Input = GND.	–1		1	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pull down resistance for IO pins when asserted on			18		kΩ
R_{OS}	OUT to VSNS resistors	Load disconnected		10		kΩ
IO	Output Current Strength	Measured at 0.4 V below supply and 0.4 V above GND.		8		mA
AMPLIFIER PERFORMANCE						
P_{OUT}	Peak Output Power	THD+N = 10 %, PWR_MODE0(1), PWR_MODE1(2)		30		W
	Maximum Continuous Output Power	THD+N = 1 %, PVDDL = 5 V, PWR_MODE0, PWR_MODE1		25		
	System Efficiency	P_{OUT} = 1W, PVDDL = 5 V, PWR_MODE1		84		%
		P_{OUT} = 1 W, PVDDL = 5 V, PWR_MODE0		79		
		P_{OUT} = 3 W, PVDDL = 5 V, PWR_MODE0 and PWR_MODE1		85		
		P_{OUT} = 8 W, PVDDL = 5 V, PWR_MODE0 and PWR_MODE1		88		
THD+N	Total Harmonic Distortion and Noise	P_{OUT} = 1 W, f_{in} = 1 kHz		-84		dB
		P_{OUT} = 1 W, f_{in} = 6.667 kHz		-84		
IMD	Inter-Modulation Distortion	ITU-R, 19 kHz / 20 kHz, 1:1: 12.5 W		-83		dB
V_N	Idle Channel Noise	A-Weighted, 20 Hz - 20 kHz, PWR_MODE0		42		µV
		A-Weighted, 20 Hz - 20 kHz, PWR_MODE2 (3)		34		
		A-Weghted, 20 Hz - 20 kHz, PWR_MODE1		32		
	Idle Channel Noise with Ultrasonic Chirp (100 us duty cycle, 25 ms period)	A-Weghted, 20 Hz - 20 kHz, PWR_MODE3 (4), 1 V_{Peak}, Register 0x73 set to E0h		34		
F_{PWM}	Class-D PWM Switching Frequency	Average frequency in Spread Spectrum Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=0		384		
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 44.1 kHz and 88.2 kHz		352.8		
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 48 kHz and 96 kHz		384		
V_{OS}	Output Offset Voltage	Idle Mode	-1.3	±0.3	1.3	mV

T_A = 25 °C, PVDDH = 18 V, PVDDL= 3.8 V, AVDD = 1.8 V, IOVDD =1.8 V, R_L = 4Ω + 15µH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1, Measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DNR	Dynamic Range	A-Weighted, -60 dBFS		110		dB
		A-Weighted, -60 dBFS, PWR_MODE2		109		
		A-Weighted, -60 dBFS, PWR_MODE0		109		
SNR	Signal to Noise Ratio	A-Weighted, Referenced to 1 % THD+N Output Level		110		dB
		A-Weighted, Referenced to 1 % THD+N Output Level, PWR_MODE2(1)		110		
		A-Weighted, Referenced to 1 % THD+N Output Level, PWR_MODE0		109		
K_{CP}	Click and Pop Performance	Idle mode, into and out of Shutdown mode, A-weighted		0.8		mV
	Full Scale Output Voltage	f_s ≤ 48 kHz		21		dBV
	Minimum Programmable Gain	f_s ≤ 48 kHz		11		dBV
	Maximum Programmable Gain	f_s ≤ 48 kHz		21		
	Programmable Output Level Step Size			0.5		dB
	Mute attenuation	Device in Software Shutdown or Muted in normal operation		108		dB
	Chip to Chip Group Delay		-1		1	µs
	PVDDH Power Supply Rejection Ratio	PVDDH = 18 V + 200 mV_{pp}, f_{ripple} = 217 Hz		118		dB
		PVDDH = 18 V + 200 mV_{pp}, f_{ripple} = 1 kHz		110		
		PVDDH = 18 V + 200 mV_{pp}, f_{ripple} = 20 kHz		98		
	PVDDL Power Supply Rejection Ratio	PVDDL = 5 V + 200 mV_{pp}, f_{ripple} = 217 Hz		114		dB
		PVDDL = 5 V + 200 mV_{pp}, f_{ripple} = 1 kHz		109		
		PVDDL = 5 V + 200 mV_{pp}, f_{ripple} = 20 kHz		93		
	AVDD Power Supply Rejection Ratio	AVDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		105		dB
		AVDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 1 kHz		103		
		AVDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		88		
	Power Supply Inter-modulation	PVDDH, 217 Hz, 100-mVpp, Input f = 1 kHz @ 400 mW		-120		dB
		PVDDL,217 Hz, 100-mVpp, Input f = 1 kHz @ 400 mW		-120		
		AVDD, 217 Hz, 100-mVpp, Input f = 1 kHz @ 400 mW		-80		
		IOVDD 217 Hz, 100-mVpp, Input f = 1 kHz @ 400 mW		-117		
	Turn ON Time from Release of Software Shutdown	No Volume Ramping		1.13		ms
		Volume Ramping		6.73		
	Turn OFF Time From Assertion of Software Shutdown to Amp Hi-Z	No Volume Ramping		0.56		ms
		Volume Ramping		6		
	Out of Hardware Shutdown to first I^2C command		1			ms
	SDZ timeout	Exiting HW Shutdown	2	6	23.8	ms
	Turn OFF Time when Software Shutdow	f_s = 48 ksps, DVC_RMP_RT[3:2] = 3h (disabled). Multiply by 48/f_s for differet sampling rate.		1		ms
		f_s = 48 ksps, DVC_RMP_RT[3:2] = 0h (enabled). Multiply by 48/f_s for different sampling rate.		12.5		
DIE TEMPERATURE SENSOR						
	Resolution			8		bits
	Minimum Temperature Measurement Range			-40		°C
	Maximum Temperature Measurement Range			150		°C
	Die Temperature Resolution			1		°C
	Die Temperature Accuracy		-5		5	°C
VOLTAGE MONITOR						

T_A = 25 °C, PVDDH = 18 V, PVDDL= 3.8 V, AVDD = 1.8 V, IOVDD =1.8 V, R_L = 4Ω + 15µH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1, Measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			12		bits
	PVDDH Measurement Range	Minimum Level		2		V
		Maximum Level		23		
	PVDDH Resolution			22.5		mV
	PVDDH Accuracy	2 V ≤ PVDDHV ≤ 23 V		±60		mV
	PVDDL Measurement Range	Minimum Level		2.3		V
		Maximum Level		6		
	PVDDL Resolution			20		mV
	PVDDL Accuracy	2.3 V≤ PVDDL ≤ 6 V		±20		mV
TDM SERIAL AUDIO PORT						
	Minimum PCM Sample Rates and FSYNC Input Frequency			14.7		kHz
	Maximum PCM Sample Rates and FSYNC Input Frequency			192		
	Minimum SBCLK Input Frequency	I^2S/TDM Operation		0.512		MHz
	Maximum SBCLK Input Frequency	I^2S/TDM Operation		24.576		
	SBCLK Maximum Input Jitter	RMS Jitter below 40 kHz that can be tolerated without performance degradation			0.5	ns
		RMS Jitter above 40 kHz that can be tolerated without performance degradation			1	
	Minimum SBCLK Cycles per FSYNC in I^2S and TDM Modes	Other Values: 24, 32, 48, 64, 96, 125, 128, 192, 250, 256, 384, 500		16		Cycles
	Maximum SBCLK Cycles per FSYNC in I^2S and TDM Modes	Other Values: 24, 32, 48, 64, 96, 125, 128, 192, 250, 256, 384, 500		512		
PCM PLAYBACK CHARACTERISTICS f_s ≤ 48 kHz						
f_s	Minimum Sample Rate			14.7		kHz
	Maximum Sample Rate			48		
	Passband Frequency Meeting Ripple			0.454		f_s
	Passband Ripple	20 Hz to LPF cutoff frequency	-0.5		0.5	dB
	Stop Band Attenuation	≥ 0.55 f_s		60		dB
		≥ 1 f_s		65		
	Group Delay (Including Noise Gate)	DC to 0.454 f_s, DC blocker disabled, Class-H disabled		31		1/f_s
		DC to 0.454 f_s, DC blocker disabled, Class-H enabled		221		
PCM PLAYBACK CHARACTERISTICS f_s > 48 kHz						
fs	Minimum Sample Rates			88.2		kHz
	Maximum Sample Rate			192		
	Frequency for Passband Ripple	f_s = 96 kHz		0.437		f_s
	Passband 3db Frequency	f_s = 96 kHz		0.459		f_s
	Passband Ripple	DC to LPF cutoff frequency	-0.5		0.5	dB
	Stop Band Attenuation	≥ 0.56 f_s		60		dB
		≥ 1 f_s		65		
	Group Delay (Including Noise Gate)	DC to 0.375 f_s, DC blocker disabled, Class-H disabled		51		1/f_s
		DC to 0.375 f_s, DC blocker disabled, Class-H enabled		242		
SPEAKER CURRENT SENSE						
	Resolution			16		bits

T_A = 25 °C, PVDDH = 18 V, PVDDL= 3.8 V, AVDD = 1.8 V, IOVDD =1.8 V, R_L = 4Ω + 15µH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1, Measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DNR	Dynamic Range	Un-weighted, relative to 0 dBFS		70		dB
THD+N	Total Harmonic Distortion and Noise	Pout = 15 W		-61		dB
	Full Scale Input Current	Measured at -6 dBFS. Re-scaled at 0 dBFS.		5		A
	Differential Mode Gain	Pout = 1W, using a 40Hz - 40dBFS pilot tone	0.98		1.02	
	Frequency Response	20 Hz - 20 kHz	-0.1		0.1	dB
	Group Delay			22		$1/f_s$
SPEAKER VOLTAGE SENSE						
	Resolution			16		bits
DNR	Dynamic Range	Un-weighted, relative 0 dBFS		73		dB
THD+N	Total Harmonic Distortion and Noise	Pout = 15 W		-68		dB
	Full Scale Input Voltage			16		V_{PK}
	Differential Mode Gain	Pout = 1W, using a 40Hz - 40dBFS pilot tone	0.98		1.02	
	Frequency Response	20 Hz - 20 kHz	-0.1		0.1	dB
	Group Delay			22		$1/f_s$
SPEAKER VOLTAGE/CURRENT SENSE RATIO						
	Gain Linearity	Pout ≥ 40 mW to 0.1% THD+N, using a 40 Hz -40 dBFS pilot tone, PWR_MODE0	-1		1	%
	Gain Linearity	Pout ≥ 80 mW to 0.1% THD+N, using a 40 Hz -40 dBFS pilot tone, PWR_MODE1	-1		1	%
	Gain error over temperature	-20 °C to 70 °C, Pout = 1 W		±0.6		%
	Phase Error between V and I			300		ns
PROTECTION CIRCUITRY						
	Brownout Prevention Latency to First Attack	BOP_SRC=1		400		µs
	Thermal Shutdown Temperature			145		°C
	Thermal Shutdown Retry	OTE_RETRY=1		1.5		s
	Output Over Current Limit on PVDDH	Output to Output, Output to GND or Output to PVDDH Short	5.5	6.7		A
	Output Over Current Limit on PVDDL	Output to Output, Output to GND or Output to PVDDL Short	2	2.6		A
	PVDDL Undervoltage Lockout Threshold	UVLO is asserted		2		V
		UVLO is de-asserted		2.16		
	AVDD Undervoltage Lockout Threshold	UVLO is asserted		1.45		V
		UVLO is de-asserted		1.51		
	IOVDD Undervoltage Lockout Threshold	UVLO is asserted		1.13		V
		UVLO is de-asserted		1.25		
	PVDDL Internal LDO Undervoltage Lockout Threshold	UVLO is asserted		4.1		V
CLASS-H CONTROLLER						
	Look Ahead Time	Sampling Rates 48 kHz and 96 kHz			4.8	ms
BEEP PIN GENERATOR						
f_{IN}	SDZ Pin	Input PWM signal frequency	25.6		192	kHz
f_{IN}	NC_SCLK Pin	Input PWM signal frequency	1.6		12	kHz
TYPICAL CURRENT CONSUMPTION						
	Hardware Shutdown	SDZ = 0, PVDDH		0.05		µA
		SDZ = 0, PVDDL		0.01		
		SDZ = 0, AVDD		0.14		
		SDZ = 0, IOVDD		0.005		

T_A = 25 °C, PVDDH = 18 V, PVDDL= 3.8 V, AVDD = 1.8 V, IOVDD =1.8 V, R_L = 4Ω + 15µH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1, Measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Software Shutdown	All Clocks Stopped, PVDDH		0.05		µA
		All Clocks Stopped, PVDDL		0.5		
		All Clocks Stopped, AVDD		10		
		All Clocks Stopped, IOVDD		0.52		
	Noise Gate Mode	f_s = 48 kHz, PVDDH		0.012		mA
		f_s = 48 kHz, PVDDL		0.13		
		f_s = 48 kHz, AVDD		8.2		
		f_s = 48 kHz, IOVDD		0.01		
	Idle Mode - PWR_MODE1	f_s = 48 kHz, PVDDH		0.04		mA
		f_s = 48 kHz, PVDDL		2.2		
		f_s = 48 kHz, AVDD, IV Sense = Enabled		15.5		
		f_s = 48 kHz, AVDD, IV Sense = Disabled		11.8		
		f_s = 48 kHz, IOVDD		0.02		
	Idle Mode - PWR_MODE2	f_s = 48 kHz, PVDDH		3		mA
		f_s = 48 kHz, AVDD, IV Sense = Enabled		15.5		
		f_s = 48 kHz, AVDD, IV Sense = Disabled		11.8		
		f_s = 48 kHz, IOVDD		0.02		
	Idle Mode - PWR_MODE0	f_s = 48 kHz, PVDDH		2.3		mA
		f_s = 48 kHz, PVDDL		2.1		
		f_s = 48 kHz, AVDD, IV Sense = Enabled		15.5		
		f_s = 48 kHz, AVDD, IV Sense = Disabled		11.8		
		f_s = 48 kHz, IOVDD		0.02		

(1) **PWR_MODE0**: CDS_MODE=10, PVDDL_MODE=0
(2) **PWR_MODE1**: CDS_MODE=00, PVDDL_MODE=0
(3) **PWR_MODE2**: CDS_MODE=11, PVDDL_MODE=1
(4) **PWR_MODE3**: CDS_MODE=01, PVDDL_MODE=0

6.6 I²C Timing Requirements

T_A = 25 °C, IOVDD = 1.8 V (unless otherwise noted)

		MIN	MAX	UNIT
Standard-Mode				
f_{SCL}	SCL clock frequency	0	100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4		µs
t_{LOW}	LOW period of the SCL clock	4.7		µs
t_{HIGH}	HIGH period of the SCL clock	4		µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7		µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices		3.45	µs
$t_{SU;DAT}$	Data set-up time	250		ns
t_r	SDA and SCL rise time		1000	ns
t_f	SDA and SCL fall time		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4		µs
t_{BUF}	Bus free time between a STOP and START condition	4.7		µs
C_b	Capacitive load for each bus line		400	pF
Fast-Mode				
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6		µs
t_{LOW}	LOW period of the SCL clock	1.3		µs
t_{HIGH}	HIGH period of the SCL clock	0.6		µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6		µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0	0.9	µs
$t_{SU;DAT}$	Data set-up time	100		ns
t_r	SDA and SCL rise time	20 + 0.1 × C_b[pF]	300	ns
t_f	SDA and SCL fall time	20 + 0.1 × C_b[pF]	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6		µs
t_{BUF}	Bus free time between a STOP and START condition	1.3		µs
C_b	Capacitive load for each bus line (10pF to 400pF)		400	pF
Fast-Mode Plus				
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.26		µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0		µs
$t_{SU;DAT}$	Data set-up time	50		ns
t_r	SDA and SCL Rise Time		120	ns
t_f	SDA and SCL Fall Time		120	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
C_b	Capacitive load for each bus line		550	pF

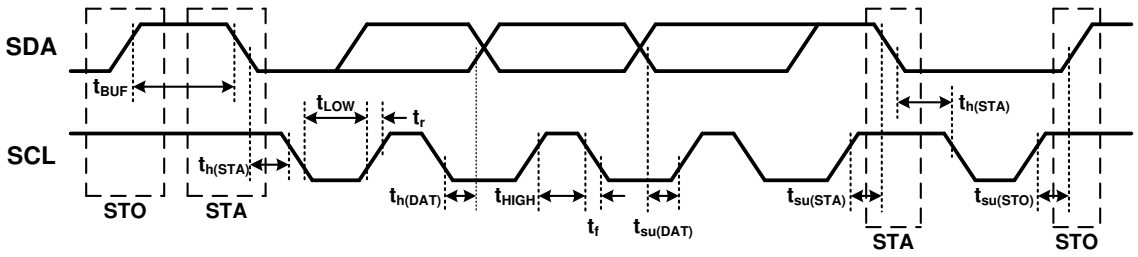


Figure 6-1. I²C Timing Diagram

6.7 TDM Port Timing Requirements

T_A = 25 °C, IOVDD = NC_V1P8V = 1.8 V, 20 pF load on all outputs(unless otherwise noted)

			MIN	MAX	UNIT
t_H(SBCLK)	SBCLK high period		20		ns
t_L(SBCLK)	SBCLK low period		20		ns
t_{SU}(FSYNC)	FSYNC setup time		8		ns
t_{HLD}(FSYNC)	FSYNC hold time		8		ns
t_{SU}(SDIN/ICC)	SDIN/ICC setup time		8		ns
t_{HLD}(SDIN/ICC)	SDIN/ICC hold time		8		ns
t_d(SBCLK_SDOUT/ICC)	SBCLK to SDOUT/ICC delay	50% of SBCLK to 50% of SDOUT/ICC, IOVDD = 1.8 V		30	ns
t_r(SBCLK)	SBCLK rise time	10 % - 90 % Rise Time		8	ns
t_f(SBCLK)	SBCLK fall time	90 % - 10 % Fall Time		8	ns

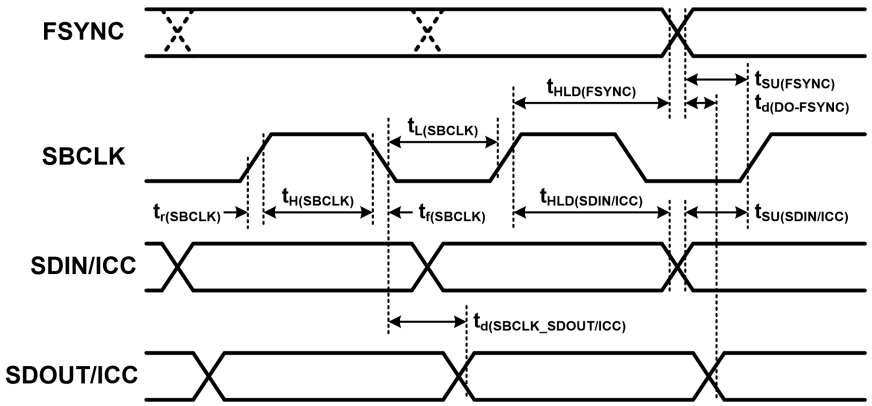


Figure 6-2. TDM and ICC Timing Diagram

6.8 SPI Timing Requirements

T_A = 25 °C, NC_V1P8V = IOVDD = 1.8 V

		MIN	NOM	MAX	UNIT
t_{HI_nSCS}	nSCS Minimum High Time efore Active Low	200			ns
t_{SU_nSCS}	nSCS Input Setup Time	60			ns
t_{H_nSCS}	nSCS Input Hold Tie	60			ns
t_{CLK}	SCLK Period	60			ns
t_{CLKH}	SCL Pulse Width High	30			ns
t_{CLKL}	SCLK Pulse Width Low	30			ns
t_{SU_SDI}	SDI Input Data Setup Time	10.5			ns
t_{H_SDI}	SDI Input Data Hold Time	8			ns
t_{D_SDO}	SDO Data Output Delay			25	ns
t_{DIS_nSCS}	nSCS Disable Delay			25	ns

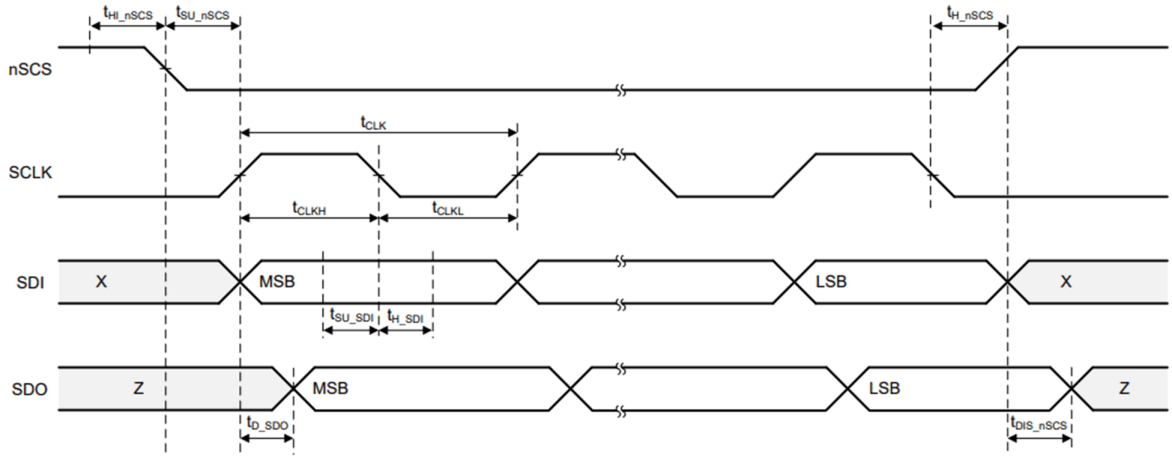
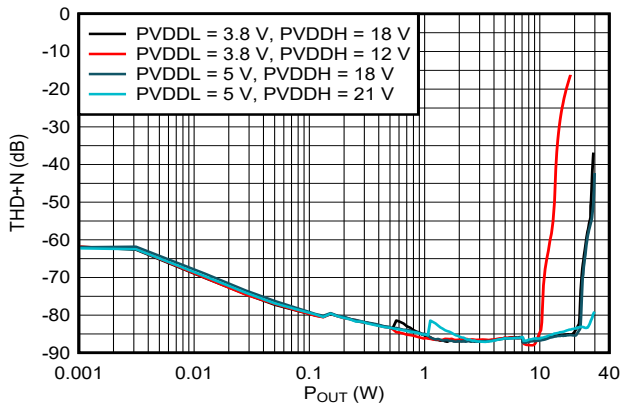


Figure 6-3. SPI Timing Diagram

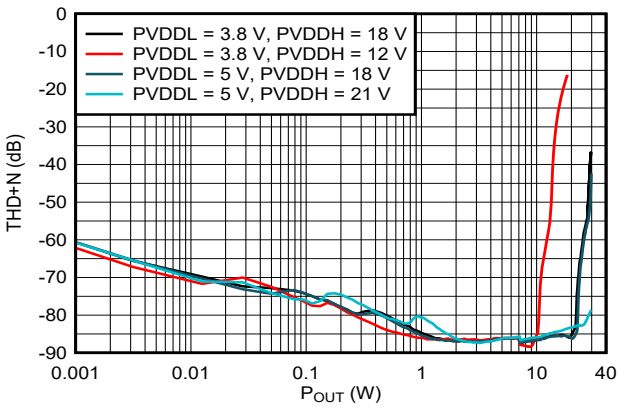
6.9 Typical Characteristics

At T_A = 25 ^{0}C, AVDD = 1.8 V, IOVDD = 1.8 V, f_s = 48 kHz, Class-D Switching Frequency = 384 kHz, input signal f_{IN} = 1kHz - Sine, Load = 4 Ω +15 µH, unless otherwise noted.



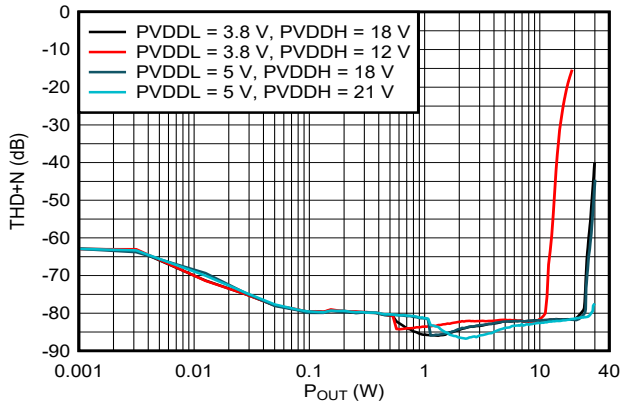
PWR_MODE1

Figure 6-4. THD+N vs Output Power



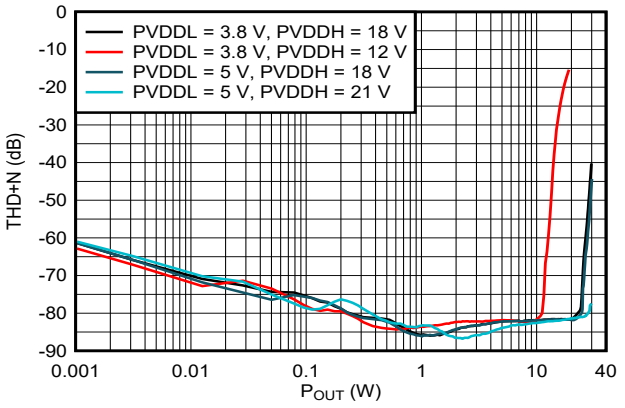
PWR_MODE0

Figure 6-5. THD+N vs Output Power



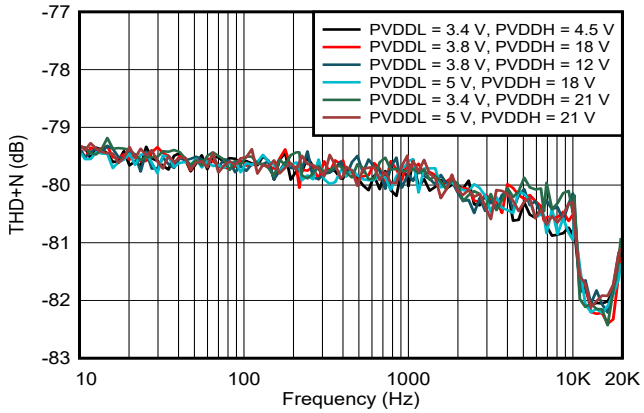
f_{IN}= 6.667 kHz PWR_MODE1

Figure 6-6. THD+N vs Output Power



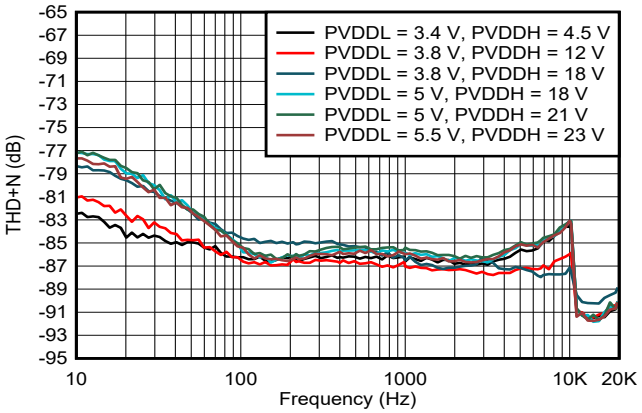
f_{IN}= 6.667 kHz PWR_MODE0

Figure 6-7. THD+N vs Output Power



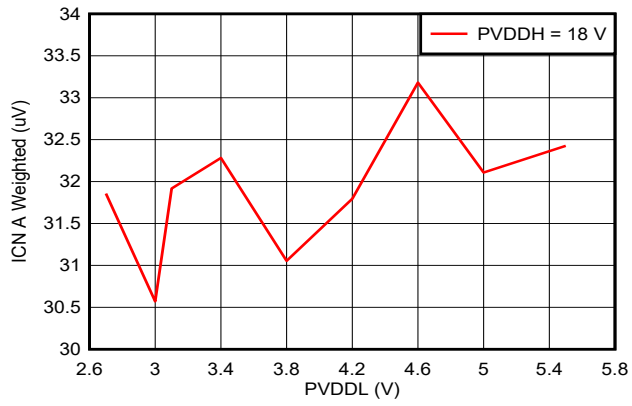
P_{OUT} = 0.1 W PWR_MODE1

Figure 6-8. THD+N vs Frequency



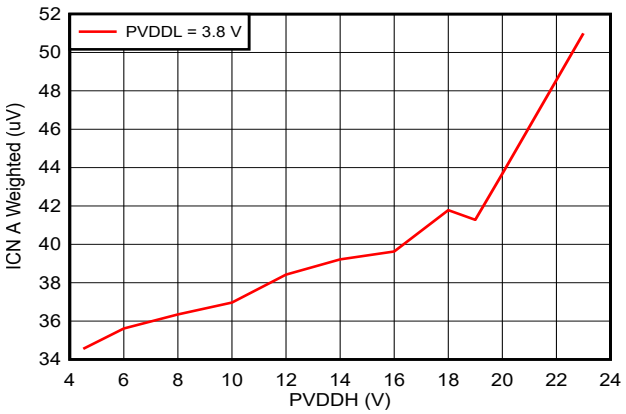
P_{OUT} = 1 W PWR_MODE1

Figure 6-9. THD+N vs Frequency



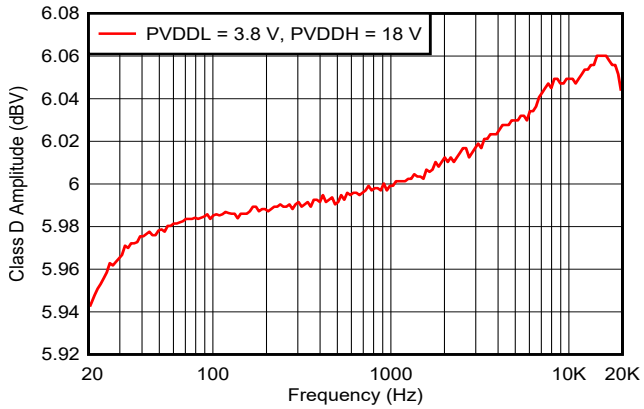
PWR_MODE1

Figure 6-10. ICN vs PVDDL



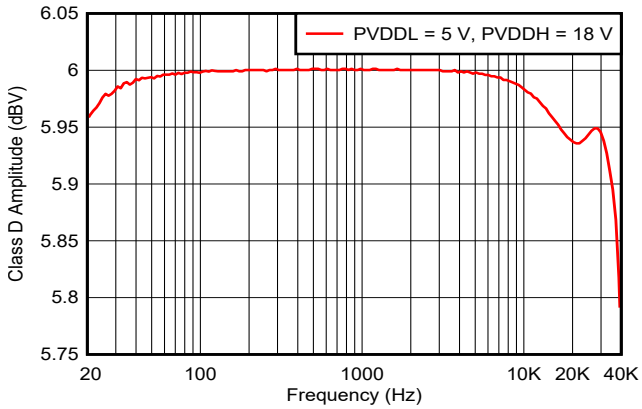
PWR_MODE0

Figure 6-11. ICN vs PVDDH



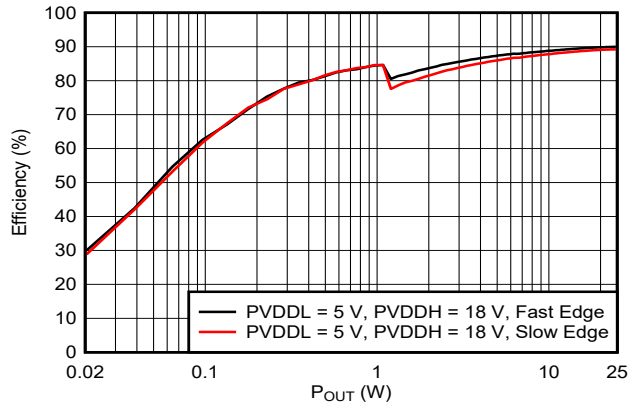
P_{OUT} = 1 W PWR_MODE1

Figure 6-12. Class-D Amplitude vs Frequency



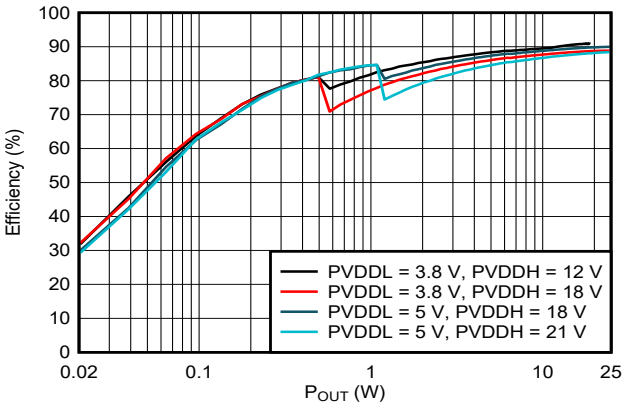
P_{OUT} = 1 W f_s = 96 kHz PWR_MODE3

Figure 6-13. Class-D Amplitude vs Frequency



PWR_MODE1

Figure 6-14. Efficiency vs Output Power



PWR_MODE1

Figure 6-15. Efficiency vs Output Power

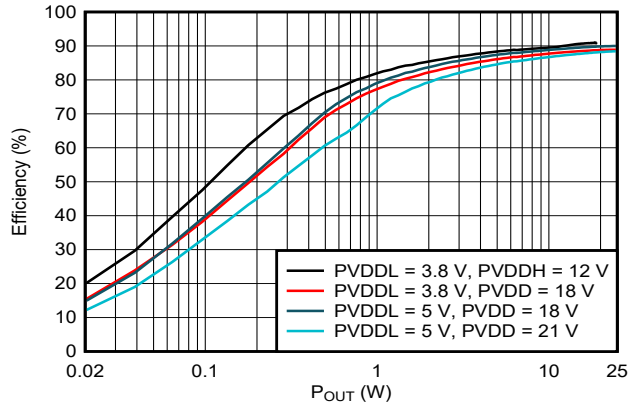


Figure 6-16. Efficiency vs Output Power

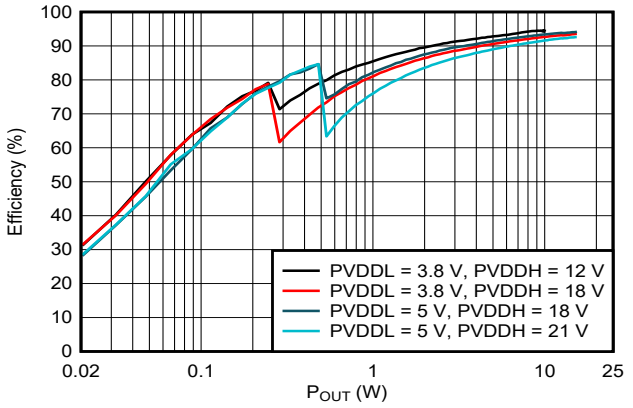


Figure 6-17. Efficiency vs Output Power

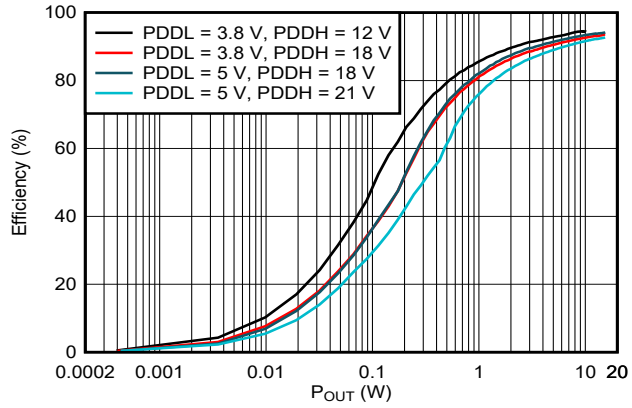


Figure 6-18. Efficiency vs Output Power

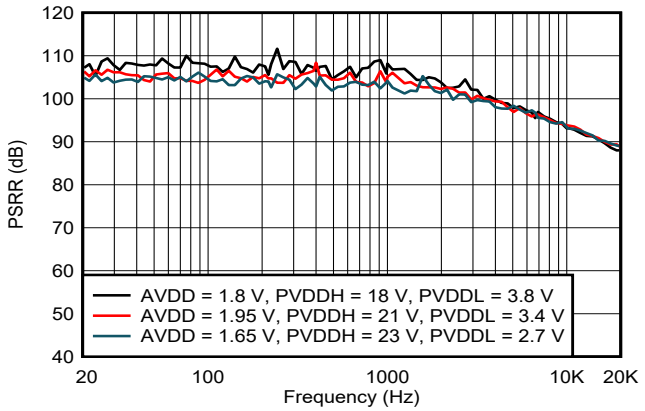


Figure 6-19. AVDD PSRR vs Frequency

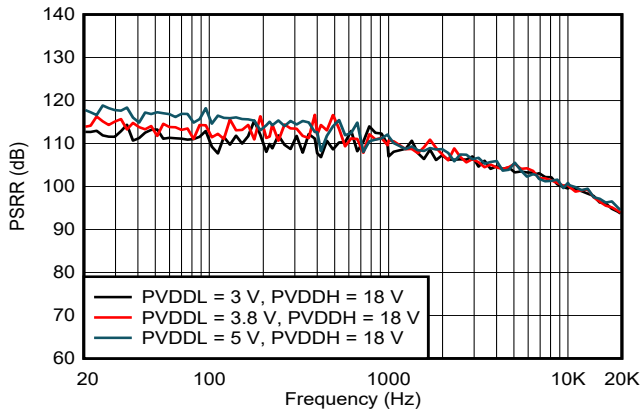


Figure 6-20. PVDDL PSRR vs Frequency

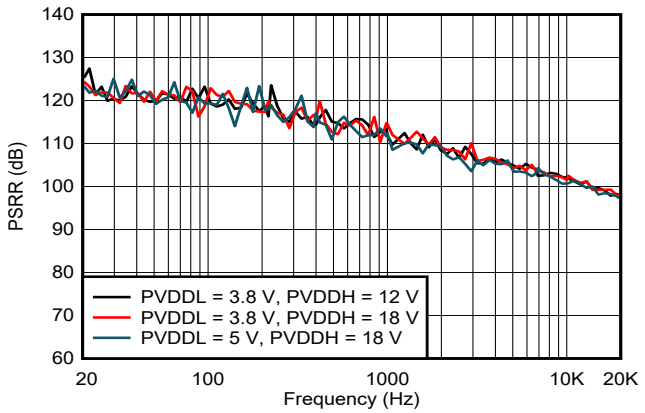


Figure 6-21. PVDDH PSRR vs Frequency

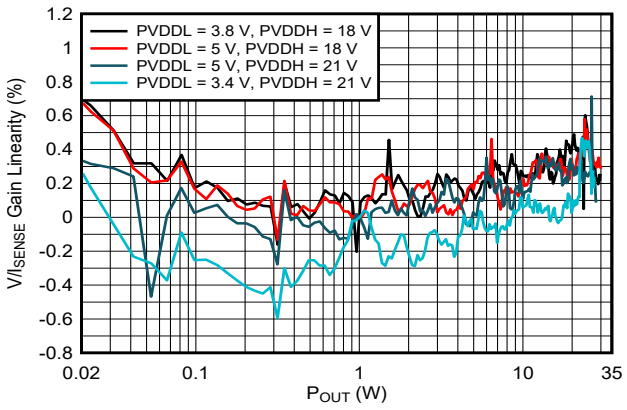


Figure 6-22. V/I Gain Linearity vs Output Power

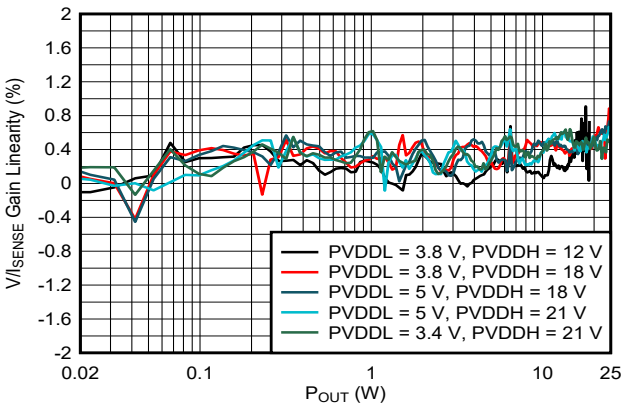


Figure 6-23. V/I Gain Linearity vs Output Power

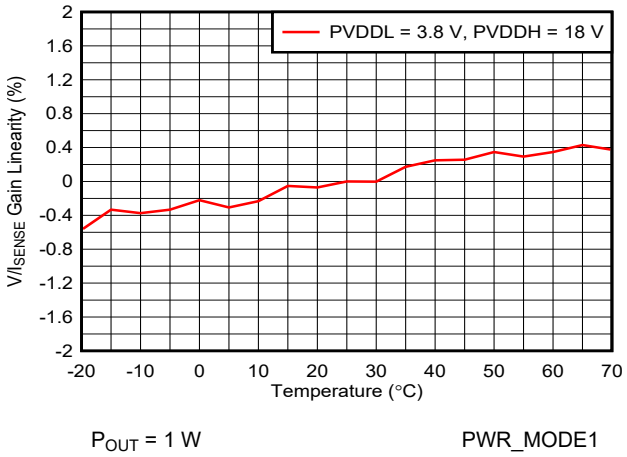


Figure 6-24. V/I Gain Linearity vs Temperature

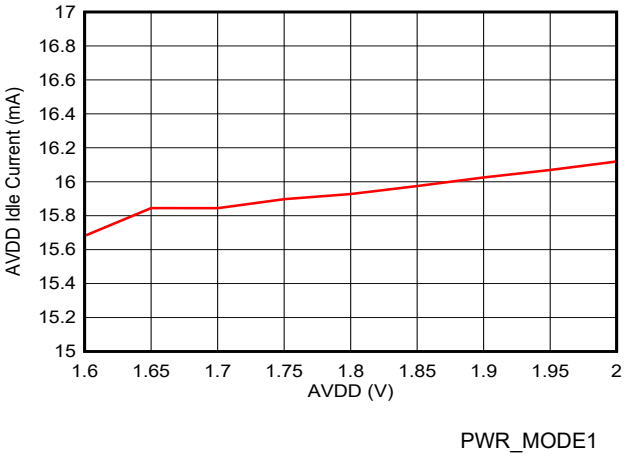


Figure 6-25. AVDD Idle Current vs AVDD

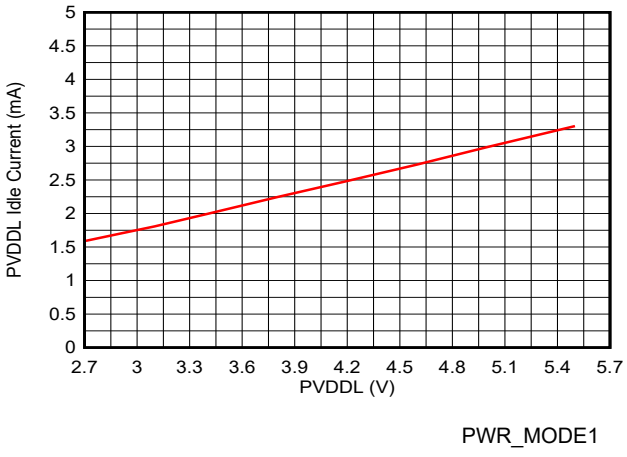


Figure 6-26. PVDDL Idle Current vs PVDDL

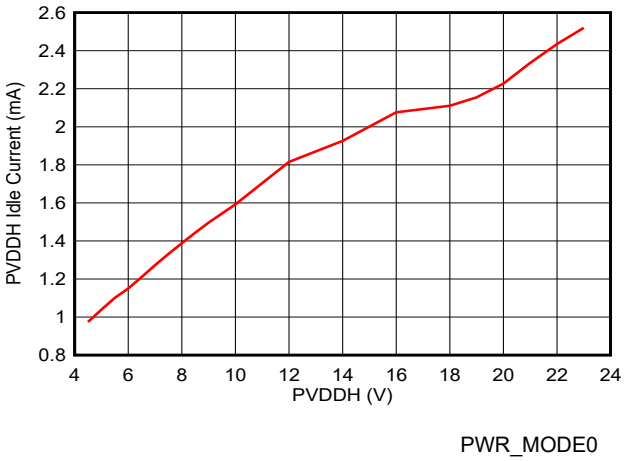


Figure 6-27. PVDDH Idle Current vs PVDDH

7 Parameter Measurement Information

The typical characteristics for the device are measured using the Bench Evaluation Module (EVM) and an Audio Precision Analyzer. A PSIA interface is used to allow the I²S interface to be driven directly into the Audio Precision Analyzer.

In some measurements (THD+N, ICN, DNR, and so forth), Class-D output terminals are connected to the Audio Precision Analyzer analog inputs through a Differential-to-Single Ended (D2S) filter as shown below. The D2S filter contains a second order passive pole at 120 kHz and an instrumenation amplifier. The D2S filter ensures the TAS2781 high performance Class-D amplifier has its outputs filtered and buffered before processed. This prevents measurement errors due to loading effects of AUX-00XX filter on the Class-D outputs.

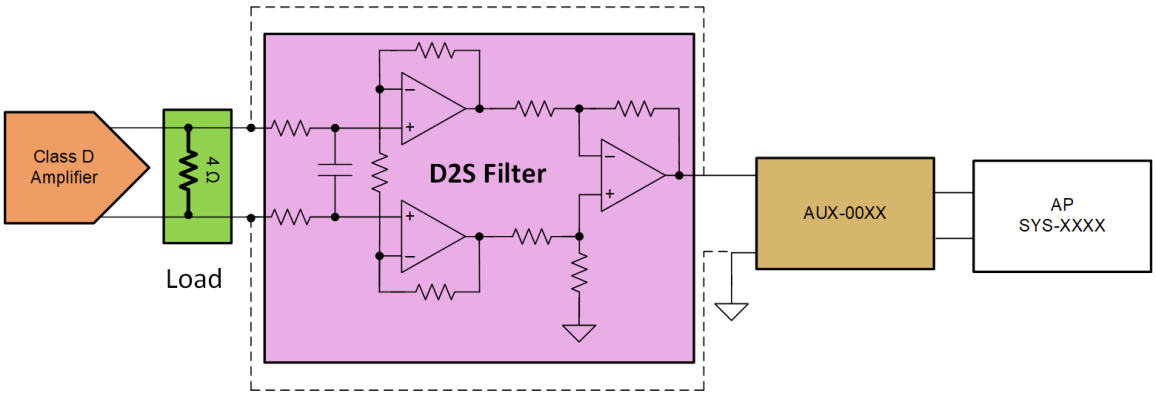


Figure 7-1. Differential to Single Ended (D2S) Filter

8 Detailed Description

8.1 Overview

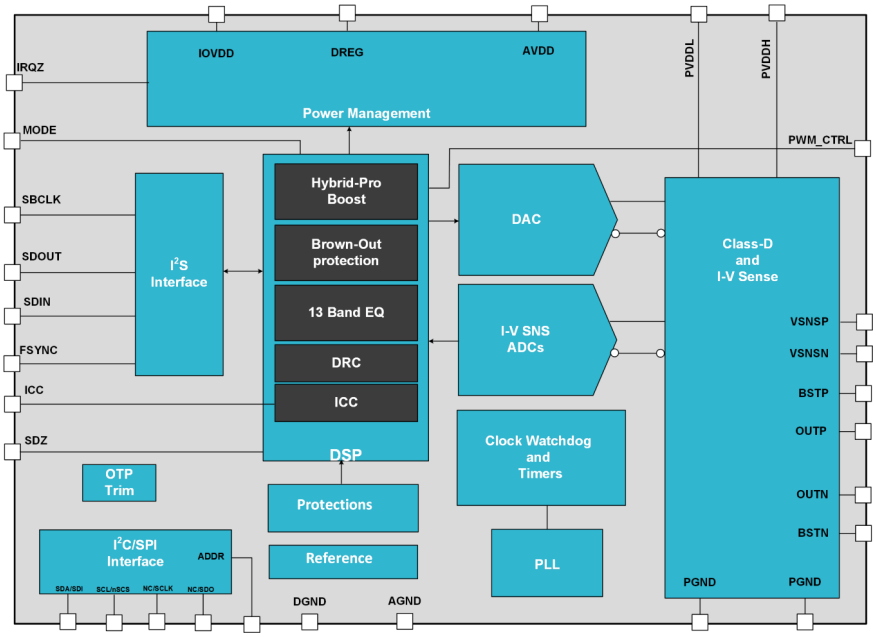
The TAS2781 is a mono digital input Class-D amplifier optimized for applications where efficient battery operation and small solution size are critical. It integrates speaker IV (current/voltage) sensing and battery tracking limiting with brown out prevention. The device operates using TDM/I²S and I²C (or SPI) interfaces.

The TAS2781 provides a Hybrid-Pro algorithm for controlling an external boost converter to extend battery life.

Table 8-1. Full Scales

Input/Output Signal	Full Scale Value
Class-D Output	21 dBV
Voltage Monitor	23 V
Current Sense	5 A
Voltage Sense	16 Vpk

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 MODE Selection

TAS2781 has two modes of operation selected based on the setting of the pin 26 (MODE) - see table below.

Table 8-2. TAS2781 Control Interface

Amplifier Mode	Control Interface	Pin 26 (MODE)
Smart Amp	I²C	Connected to GND
Smart Amp	SPI	470 Ω to GND

8.3.2 Device Address Selection

The TAS2781 operates using a TDM/I²S interface. Audio input and output are provided via the FSYNC, SBCLK, SDIN and SDOUT pins using formats including I²S, Left Justified and TDM. Configuration and status are provided using the I²C protocol (MODE pin tied to GND) or SPI protocol MODE pin connected to GND through a 470 Ohms).

The table below illustrates how to configure the device for I²C address. The peripheral addresses are shown left shifted by one bit with the R/W bit set to 0 (for example, {ADDR[6:0],1b0}). Resistors with tolerance better than 5% must be used for setting the address configuration.

Table 8-3. I²C Address Selection

I²C Address	0x70	0x72	0x74	0x76	0x78	0x7A	0x7C	0x7E
ADDR PIN	Short to GND	470 Ω to GND	470 Ω to AVDD	2.2 kΩ to GND	2.2 kΩ to AVDD	10 kΩ to GND	10 kΩ to AVDD	Short to AVDD

The TAS2781 has a global 7-bit I²C address 0x80. When bit I2C_GLB_EN of register from is set high the device will respond to I²C commands at this address regardless of the ADDR pin settings. This is used to speed up device configuration when using multiple TAS2781 devices and programming similar settings across all devices. The I²C ACK / NACK cannot be used during the multi-device writes since multiple devices are responding to the I²C command. The I²C CRC function should be used to ensure each device properly received the I²C commands. At the completion of writing multiple devices using the global address, the CRC at *I2C_CKSUM* register should be checked on each device using the local address for a proper value. The global I²C address can be disabled using *I2C_GBL_EN* register bit. The I²C address is detected by automatically sampling the

ADDR pin when SDZ pin is released. Additionally, the address may be re-detected by setting *I2C_AD_DET* register bit high after power up and the ADDR pin will be re-sampled.

8.3.3 SPI Interface

TAS2781 features an 1.8 V SPI interface when pin 26 (MODE) is connected to GND through a 470 Ω resistor.

Pin 17 (NC_V1P8) of the device needs to be tied to an 1.8 V supply.

The host controller should use the mode with CPHA = 1 and CPOL = 0. The TAS2781 SPI logic block is sampling SPI input data on falling edge of SPI clock and transmiting SPI output data on rising edge of SPI clock.

8.3.4 Register Organization

Device configuration and coefficients are stored using a page and book scheme. Each page contains 128 bytes and each book contains 256 pages. All device configuration registers are stored in book 0 which is the default setting at power up and after a software reset. The book and page can be set by the *BOOK[7:0]* bits of register from and *PAGE[7:0]* bits of register from .

Note

Programming register bits from book 0x00, pages 0x04, 0x05, 0x06, 0x08 and 0x0A needs to be done in groups of four registers (32 bit format), each byte corresponding to an 8 bit register and with less significant byte corresponding to the highest register address. For instance , when programming the limiter maximum threshold in registers from , the MSBs will be in register 0x10 and the LSBs in register 0x13.

8.4 Device Functional Modes

8.4.1 TDM Serial Audio Port

The TAS2781 provides a flexible TDM serial audio port. The port can be configured to support a variety of formats including stereo I^2S, Left Justified and TDM. Mono audio playback is available via the SDIN pin. The SDOUT pin is used to transmit sample streams including PVDDL voltage, PVDDH voltage, die temperature, status, audio for echo cancelation.

By default, the TAS2781 will automatically detect the PCM playback sample rate (*AUTO_RATE= 0*). This can be disabled and manually configured by setting the *AUTO_RATE* bit of register in to high.

The TDM serial audio port valid SBCLK to FSYNC ratios are presented in register in . The device will automatically detect the number of time slots and it does not need to be programmed.

The *SAMP_RATE[2:0]* and *SBLK_FS_RATIO[5:0]* register bits are used to configure the PCM audio sample rate when *AUTO_RATE* register bit is high (auto detection of TDM sample rate is disabled). The TAS2781 employs a robust clock fault detection engine that will automatically volume ramp down the playback path if FSYNC does not match the configured sample rate (if *AUTO_RATE* = 1) or the ratio of SBCLK to FSYNC is not supported (minimizing any audible artifacts). Once the clocks are detected to be valid in both frequency and ratio, the device will automatically volume ramp the playback path back to the configured volume and resume playback.

When using the auto rate detection the sampling rate and SBCLK to FSYNC ratio detected on the TDM bus is reported back on the read-only bits *FS_RATIO[5:0]* and *FS_RATE[2:0]* of registers in] and in .

A frame begins with the transition of FSYNC from either high to low or low to high (set by the *FRAME_START* register bit). FSYNC and SDIN are sampled by SBCLK using either the rising or falling edge (set by the *RX_EDGE* register bit). The *RX_OFF[4:0]* register bits define the number of SBCLK cycles from the transition of FSYNC until the beginning of time slot 0. This is typically set to a value of 0 for Left Justified format and 1 for an I^2S format.

The *RX_SLEN[1:0]* register bits set the length of the RX time slot to 16, 24 or 32 (default) bits. The length of the audio sample word within the time slot is configured by the *RX_WLEN[1:0]* register bits. The RX port will left justify the audio sample within the time slot by default, but this can be changed to right justification via the *RX_JSTF* register bit. The TAS2781 supports mono and stereo down mix playback ([L+R]/2). By default the device will playback mono from the time slot equal to the I^2C base address offset (set by the ADDR pin) for

playback. The *RX_SCFG[1:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX_SLOT_R[3:0]* and *RX_SLOT_L[3:0]* register bits.

If time slot selection places reception either partially or fully beyond the frame boundary, the receiver will return a null sample equivalent to a digitally muted sample.

The TDM port can transmit a number of sample streams on the SDOUT pin: speaker voltage sense, speaker current sense, interrupts and status, PVDDH voltage and die temperature.

Either the rising or falling edge of SBCLK can be used to transmit data on the SDOUT pin. This can be configured by setting the *TX_EDGE* register bit. The *TX_OFF[2:0]* register bits define the number SBCLK cycles between the start of a frame and the beginning of time slot 0. This would typically be programmed to 0 for Left Justified format and 1 for I^2S format. The TDM TX can either transmit logic 0 or Hi-Z depending on the setting of the *TX_FILL* register bit. An optional bus keeper will weakly hold the state of SDOUT pin when all devices are driving Hi-Z. Since only one bus keeper is required on SDOUT, this feature can be disabled via the *TX_KEEPEN* register bit. The bus keeper can be configured to hold the bus for only 1 LSB or Always (permanent) using *TX_KEEPLN* register bit. Additionally, the keeper LSB can be driven for a full cycle or half of cycle using *TX_KEEPCY* register bit.

TX_FILL is used in mono system where there is only one amplifier on I^2S bus. All the slots unused by the amplifier will be filled with zeros when *TX_FILL* is set to low. The TX bits mentioned are in the register in .

The *SDOUT_HIZ* registers from page 0x01 are useful when multiple devices are on the same I^2S bus. Each device does not know configuration of slots in the other devices on the bus. It is required at the system level to program the *SDOUT_HIZ* registers appropriately, in such way that the settings are done correctly and do not create any contention both internally and externally.

The current and voltage values are transmitted at the full 16-bit measured values by default. The *IVMON_EN[1:0]* bits of register from can be used to transmit only the 8 MSB bits in one slot or 12 MSB bits values across multiple slots. The special 12-bit mode is used when only 24-bit I^2S/TDM data can be processed by the host processor. The device should be configured with the voltage-sense slot and current-sense slot off by 1 slot and will consume 3 consecutive 8-bit slots. In this mode the device will transmit the first 12 MSB bits followed by the second 12 MSB bits specified by the preceding slot.

If time slot selections place transmission beyond the frame boundary, the transmitter will truncate transmission at the frame boundary.

The time slots for SAR measurements (PVDDL, PVDDH and temperature) are set using *SAR_DATA_SLOT[5:0]* register bits. To enable sample stream register bit *SAR_DATA_TX* must be set high. The slot length is selected by bit *SAR_DATA_SL* of register from .

For TDM final processed audio slot, enable and length settings use *AUDIO_SLOT[5:0]*, *AUDIO_TX* and *AUDIO_SLEN* register bits.

Information about status of slots can be find in *STATUS_SLOT[5:0]* register bits. *STATUS_TX* register bit set high enables the status transmit.

8.4.2 Playback Signal Path

8.4.2.1 Digital Signal Processor

An on-chip, low latency DSP supports Texas Instrument Smart Amp speaker protection algorithms to maximize loudness while maintaining safe speaker conditions.

The DSP also features Band EQ, stereo balancing, ultrasound and external boost controller for Class-H amplifier operation.

8.4.2.2 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers. The TAS2781 employs a high-pass filter (HPF) to prevent this from occurring for the PCM playback path. The *HPF_FREQ_PB[2:0]* register bits set the corner frequencies of HPF. The filter can be bypassed by setting the register bits to 3'b000.

8.4.2.3 Amplifier Inversion

The TAS2781 will output a non-inverted signal to the OUT_P and OUT_N pins. The output can be inverted with respect to the digital input value by setting the *AMP_INV* register bit to high.

8.4.2.4 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier output level and the digital volume control (DVC).

Amplifier output level settings are programmed using the *AMP_LVL[4:0]* register bits. The amplifier levels are presented in the register from . The Digital Volume Control (DVC) is set by default to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used only to convey gain.

Equation (1) calculates amplifier output voltage:

$$V_{AMP} = INPUT + A_{DVC} + A_{AMP} \quad (1)$$

where

- V_{AMP} is the amplifier output voltage in dBV
- *INPUT* is the digital input amplitude as a number of dB with respect to 0 dBFS
- A_{DVC} is the digital volume control setting as a number of dB
- A_{AMP} is the amplifier output level setting as a number of dBV

The DVC is configurable from 0 dB to -100 dB in 0.5 dB steps by setting the *DVC_LVL[7:0]* register bits. Settings greater than C8h are interpreted as mute. When a change in digital volume control occurs, the device ramps the volume to the new setting based on the *DVC_SLEW[31:0]* register bits status from . The bits *DVC_RMP_RT[1:0]* of register in enable or disable the volume ramp control

The Class-D amplifier uses a closed-loop architecture. The approximate threshold for output signal clipping is given by equation (2).

$$V_{PK} = V_{SUP} * \frac{R_L}{R_{FET} + R_P + R_L} \quad (2)$$

where:

- V_{PK} is the maximum peak un-clipped output voltage in V
- V_{SUP} is the power supply of Class-D output stage
- R_L is the speaker load in Ω
- R_P is the parasitic resistance on PCB (routing, filters) in Ω
- R_{FET} is the power stage total resistance (HS FET, LS FET, Sense Resistor, bonding, packaging) in Ω

When PVDDL supplies Class-D output stage typical R_{FET} value is 0.5 Ω. For PVDDH supply R_{FET} typical value is 0.25 Ω.

8.4.2.5 PVDDL Supply

The TAS2781 can operate with or without a PVDDL supply. When configured without a PVDDL supply, the PVDDH voltage will be used with an internal LDO to generate this supply voltage. A decoupling capacitor should still be populated as recommended in Table 9-1. In this case, *PVDDL_MODE* bit should be set to high before transitioning from Software Shutdown mode. More details about PVDDL supply modes of operation can be found in Section 11.1.

8.4.2.6 Y - Bridge

The TAS2781 Class-D output uses a Y-Bridge configuration to improve efficiency during playback. The LVS () is internally used to select between the PVDDH and PVDDL supplies. This feature is enabled by setting *CDS_MODE[1:0]* bits to 2'b00 when both PVDDH and PVDDL are supplied to the device. If not configured to

Y-bridge mode the device will use only the selected supply for Class-D output even if clipping would otherwise occur. The device can operate using only PVDDH to supply Class-D output. In this configuration the PVDDL can be provided from external supply (register bit *PVDDL_MODE*=0) or generated by an internal LDO (register bit *PVDDL_MODE[7]*=1). In this case *CDS_MODE[7:6]* bits should be set to 2'b10. The TAS2781 Y-Bridge with low power on PVDDL can be used to switch to the PVDDL rail only at very low power when close to idle. This will reduce the Class-D output swing when near idle and limit the current requirements of the PVDDL supply. Set the *CDS_MODE[7:6]* register to 2'b11 for this mode.

See for details on programming the power mode of operation.

The change to the Class-D supply (PVDDL to PVDDH) determined by the has a delay with respect to input signal crossing threshold and it can be programed using *CDS_DLY[1:0]* bits of register from .

When in Y-Bridge mode, if the PVDDH falls below (PVDDL + 2.5 V) level, the Y-Bridge will stop switching between supplies and will remain on the PVDDH supply.

8.4.2.7 Low Voltage Signaling (LVS)

The TAS2781 is a mechanism used in connection with the Y Bridge confiuration of the output stage of Class-D. It is based on monitoring the absolute value of the audio stream and selecting the proper supply, PVDDH or PVDDL.

When the signal is initially above the programmed LVS threshold the Class-D is supplied by PVDDH rail. If the signal level drops below this threshold for longer than the hysteresis time defined by *LVS_HYS[3:0]* register bits, the Class-D supply will switch to PVDDL. If the signal goes back to the initial level the Class-D supply will switch back to PVDDH.

By default he LVS threshold is configured to be a value relative to the PVDDL voltage (*LVS_DET = 1*). Use the *LVS_RTH[3:0]* register bits for setting the threshold (default = 0.7 V).

Setting bit *LVS_DET* bit to low forces the LVS threshold to a fixed value defined by the *LVS_FTH[4:0]* register bits.

LVS threshold is refered relative to the output signal level and it is measured in dBFS.

In an use case when *CDS_MODE[1:0]=11* (PWR_MODE2 from Section 11.1), the fixed LVS threshold can be set using register bits *LVS_TH_LOW[1:0]*.

8.4.2.8 Noise Gate Mode

The TAS2781 has a noise-gate feature that monitors the input signal and powers down the Class-D when the signal goes below the set threshold set by *NG_TH[1:0]* bits for longer than the time set by *NG_HYST_TIMER[2:0]* bits of register from . When the signal goes above the threshold the Class-D will re-power in seven samples before the samples applied to the audio input interface reach the Class-D output.

The Noise Gate feature is enabled by setting *NG_EN* bit to high. Once enabled it is able to power up and down the channel within the device processing delay requiring no additional external control. Volume ramping can be also used during noise gate operations by setting *NG_DVC_RP* bit to low.

The noise gate can be configured with finer resolution at the expense of additional I^2C writes. Use *NGFR_EN* bit to enable this mode and register bits *NGFR_LVL[23:0]* from to set the fine resolution. The fine resolution hysteresis is set using *NGFR_HYST[18:3]* register bits from and from .

8.4.2.9 Supply Tracking Limiter

The TAS2781 monitors PVDDH supply voltage and the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions. The limiter threshold can be configured to track PVDDH below a programmable inflection point with a programmable slope. A minimum threshold sets the limit of threshold reduction from PVDDH tracking.

The limiter is enabled by setting the *LIM_EN* bit register to high.

Configurable attack rate, hold time and release rate are provided to shape the dynamic response of the limiter (*LIM_ATK[3:0], LIM_HLD[2:0]* and *LIM_RLS[3:0]* bits of registers from and .

A maximum level of attenuation applied by the limiter is configurable via the *LIM_MAX_AT[3:0]* bits of register . If the limiter is attacking and if it reaches the maximum attenuation, gain will not be reduced any further.

The limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track PVDDH below a programmable inflection point with a minimum threshold value. shows the limiter configured to limit to a constant level regardless of PVDDH level. To achieve this behavior, set the limiter maximum threshold to the desired level via the *LIM_MAX_TH[31:0]* register bits. Set the limiter inflection point (register bits *LIM_INF[31:0]*) below the minimum allowable PVDDH setting. The limiter minimum threshold, set by register bits *LIM_MIN_TH[31:0]*, does not impact limiter behavior in this use case.

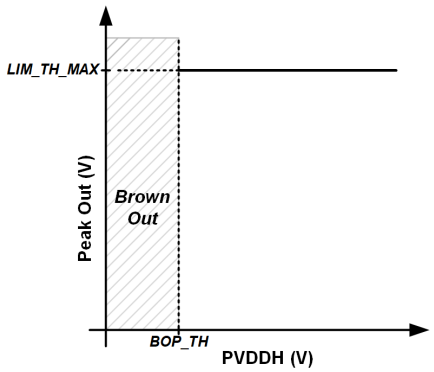


Figure 8-1. Limiter with Fixed Threshold

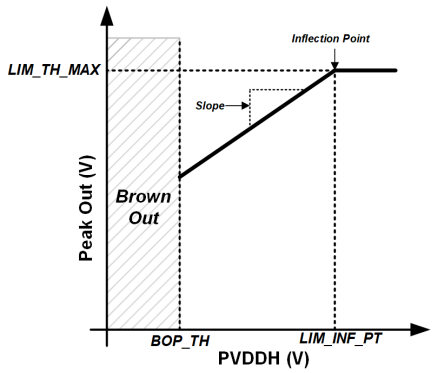


Figure 8-2. Limiter with Inflection Point

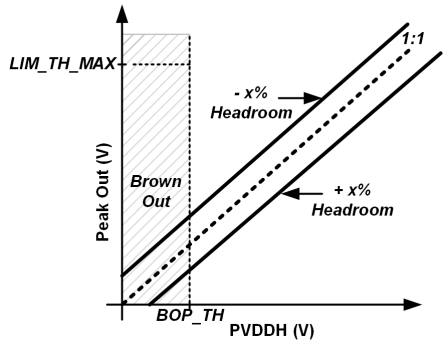


Figure 8-3. Limiter with Dynamic Threshold

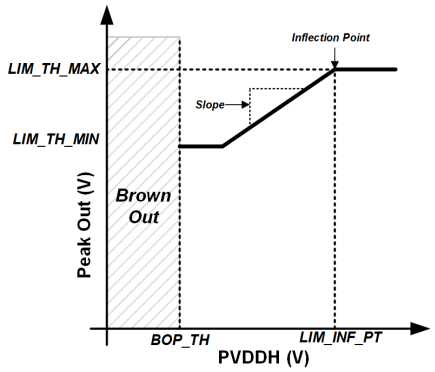


Figure 8-4. Limiter with Inflection Point and Minimum Threshold

shows how to configure the limiter to track PVDDH below a threshold without a minimum threshold. Set the *LIM_MAX_TH[31:0]* register bits to the desired threshold and *LIM_INF[31:0]* register bits to the desired inflection point where the limiter will begin reducing the threshold with PVDDH. The *LIM_SLP[31:0]* register bits can be used to change the slope of the limiter tracking with PVDDH. The default value of 1 V/V will reduce the threshold 1 V for every 1 V of drop in PVDDH supply. More aggressive tracking slopes can be programmed if desired. Program the *LIM_MIN_TH[31:0]* bits below the minimum PVDDH to prevent the limiter from having a minimum threshold reduction when tracking PVDDH.

The limiter with a supply tracking slope can be configured in an alternate way. By setting *LIM_DYHDR* register bit to 1'b1 in register in , a headroom can be specified as a percentage of the supply voltage using a 1V/V slope by setting *LIM_HDR[4:0]* register bits. For example if a headroom of -10% is specified, the peak output voltage will be set to be 10% higher than PVDDH. In this use case presented in the limiting begins for signals above the supply voltage and will result in a fixed clipping. If a positive headroom of +10% is specified the peak output

voltage will be dynamically set 10% below the current PVDDH. In this use case the limiting will begin at signal levels lower than the supply voltage and prevent clipping from occurring.

To achieve a limiter that tracks PVDDH only up to a minimum threshold, configure the limiter *LIM_MAX_TH[31:0]* and *LIM_SLP[31:0]* register bits as in the previous examples. Then additionally set the *LIM_MIN_TH[31:0]* register bits to the desired minimum threshold. Supply voltage below this minimum threshold will not continue to decrease the signal output voltage. This is shown in .

By setting register bit *LIM_DYHDR* to low the limiter mechanism depends on settings for maximum and minimum thresholds, inflection point and slope. By default this bit is high and the limiter dynamic headroom is enabled.

8.4.2.10 Brownout Prevention

Brownout Prevention (BOP) feature provides a priority input to the limiter to generate a fast response to transient dips in supply voltage at end of charge conditions that can cause system level brownout. When supply voltage dips below the BOP threshold, the limiter begins reducing gain at a configurable attack rate. When supply voltage rises above the BOP threshold, the limiter will begin to release after the programmed hold time. The BOP feature can be enabled by setting the *BOP_EN[0]* register bit high. The brownout supply source can be set using *BOP_SRC* register bit to either PVDDH or PVDDL depending on application.

By default BOP supply source is set to PVDDL input and the SAR converter will digitize the PVDDH and PVDDL voltages and temperature. The PVDDH undervoltage detection will be disabled.

When BOP supply source is set to PVDDH input the SAR ADC converter willl digitize the PVDDH and PVDDL voltages and temperature. The PVDDH undervoltage detection will be enabled in this case.To reduce latency in the first attack of the BOP engine, PVDDL conversion can be bypassed by setting the register bit *CNV_PVDDL*to low.

When BOP supply source is set to PVDDL input the SAR converter willl digitize the PVDDH and PVDDL voltages and temperature. The PVDDH undervoltage detection will be disabled.

When the BOP is engaging the Supply Tracking Limiter is paused.

The BOP threshold is set by the *BOP_TH[31:0]* bits from registers in . The setting of *BOP_MUTE* bit determines if once the supply goes below the threshold the device mutes audio and shuts down or just attenuates the audio signal whit no muting.

The TAS2781 can also immediately mute and then shutdown the device when a BOP event occurs by reaching the threshold set by the *BOPSD_TH[31:0]* bits from registers in if the *BOPSD_EN* register bit is set high. This shutdown feature is auto disabled internally when *BOP_MUTE* is set high.

The BOP has programmable attack rate register bits *BOP_ATK[2:0]*, attack step size register bits *BOP_ATK_ST[1:0]* and hold time register bits *BOP_HLD[2:0]*).

When the system comes out of BOP the supply tracking limiter release will be engaged. If the limiter is disabled the gain will be released as per limiter release settings.

The hold time can be set to Infinite by programming the *BOP_INF_HLD* register bit to high. The device will need to transition through a mute or SW/HW shutdown state or the register bit *BOP_HLD_CLR* can be set to high (which will cause the device to exit the hold state and begin releasing).

When *BOP_INF_HLD* bit is set low the device will hold based on programming of *BOP_HLD[2:0]* bits.

8.4.2.11 ICC Pin and Inter-Chip Communication

The TAS2781 supports dual gain balancing in stereo applications. One device can be paired with only one other device in the system.

The ICC pin will be connected to an ICC bus with bus keeper. Pin 17 (NC_V1P8V) supplying ICC buffer needs to be connected to an 1.8 V supply.

The SDOUT pin cannot be used for gain alignment.

The *ICC_CFG[2:0]* bits of register from configure the functionality of the ICC pin.

The bits from register in enable the ICC feature and set the device pairing and gain transmiting slots.

The sampling rates of 16 kHz and 24 kHz (and 44.1 kHz equivalent) are not supported in this mode of operation.

8.4.2.12 Class-D Settings

8.4.2.12.1 Output Slew Rate Control

The output slew rate can be programmed using bits *EDGE_CTRL[1:0]* from register in .

By default, if PVDDH supply is below 20 V the output slew rate will be at a fast rate, dependant on supply and load. If PVDDH goes above 20 V the slew rate will be automatically change to a slower rate.

Optionally, to improve EMI performance, user can set the slew rate to a slower rate for the entire range of PVDDH supply by setting the bits *EDGE_CTRL[1:0]* to 2'b11.

8.4.2.12.2 Synchronization

The TAS2781 Class-D amplifier supports spread spectrum PWM modulation, which can be enabled by setting the *AMP_SS* register bit high. This can help reduce EMI in the system.

By default the Class-D amplifier switching frequency is based on the device trimmed internal oscillator. To synchronize switching to the audio sample rate, set the *CLASSD_SYNC* register bit high. When the Class-D is synchronized to the audio sample rate, the *RAMP_RATE* register bit must be set depending on the audio sample rate of either 44.1 kHz or 48 kHz (default) based frequency.

8.4.3 SAR ADC

A SAR ADC monitors PVDDH voltage, PVDDL voltage and die temperature. The results of these conversions are available via register readback (*PVDDH_CNV[11:0]*, *PVDDL_CNV[11:0]* and *TMP_CNV[7:0]* register bits). PVDDH and PVDDL voltage conversions are also used by the limiter and brown out prevention blocks.

By default, PVDDL conversion is enabled along with PVDDH and temperature in both cases, when BOP source is PVDDL (*BOP_SRC* = 0) or BOP source is PVDDH (*BOP_SRC* = 1).

The ADC runs at a fixed 192 kHz sample rate with a conversion time of 5.2 µs.

Temperature is sampled once every 18th SAR conversions. Sampling rate for temperature is approximative 10K samples/sec.

PVDDH and PVDDL voltages and the die temperature can be estimated by user using equations from registers in , and .

The register bits content should always be read from MSB to LSB.

The voltage and temperature readings of SAR ADC are also available to the host through the SDOUT pin. Use bits of register from to enable this feature and configure the slots.

8.4.4 Current and Voltage (IV) Sense

The TAS2781 provides speaker voltage and current sense measurements for real time monitoring of loudspeaker behavior. The VSNSP and VSNSN pins should be connected after any ferrite bead filter (or directly to the OUTP and OUTN connections if no EMI filter is used). The V-Sense connections eliminate voltage drop error due to packaging, PCB interconnect or ferrite bead filter resistance. It should be noted that any interconnect resistance after the VSNS terminals will not be corrected for, so it is advised to connect the sense connections as close to the load as possible.

The voltage and current sense internal ADCs have a DC blocking filter. This filter cut-off frequency can be adjusted, or the filter can be bypassed using the *HPF_FREQ_REC[2:0]* register bits.

I-Sense and V-Sense blocks can be powered up by setting the *ISNS_PD* and *VSNS_PD* register bits to low.

8.4.5 Post Filter Feed-Back (PFFB)

The device supports post-filter feedback by closing the amplifier feedback loop after the external filter. The feedback is applied using the VSNSN and VSNSP terminals of the device. This feature can be disabled using

the *PFFB_EN* register bit (if an external filter that violates the amplifier loop stability is implemented). When PFFB is disabled, the feedback will be internally routed from the OUTN and OUTP pins of the device.

In the PFFB mode of operation the following conditions have to be met: f_0 > 10 MHz and f_0/Q > 2.5 MHz (f_0 and Q are the cutoff frequency and the quality factor of the external filter).

8.4.6 Thermal Foldback

The TAS2781 monitors the die temperature and can automatically limit the audio signal when the die temperature reaches a set threshold. It is recommended to use the thermal fold-back registers to configure this protection mechanism as the internal DSP will perform the necessary calculation for each register.

Thermal fold-back can be disabled using *TFB_EN* bit . If the die temperature reaches the value set by *TF_TMP_TH[31:0]* bits of register from this feature will begin to attenuate the audio signal to prevent the device from shutting down due to over-temperature. It will attenuate the audio signal by a value set in *TF_SLP[31:0]* register bits over a range of temperature set by *TF_TMP_TH[31:0]* register bits. The thermal fold-back attack is set using the *TF_ATK[31:0]* register bits. A maximum attenuation can be specified using register bits *TF_MAX_ATN[31:0]*. However, if the device continue to heat up, eventually the device over-temperature will be triggered. The attenuation will be held for a number of samples set by register bits *TF_HLD[31:0]*, before the attenuation will begin releasing.

8.4.7 Over Power Protection

The TAS2781 monitors the temperature of the internal power FETs. If the maximum continue power is high and power FETs temperature goes above a threshold, an internal protection circuit will trigger a thermal foldback and, if temperature still incraeses, shutdown the device.

The protection mechanism is based on two thresholds TH1 and TH2. The TH1 threshold is set at a temperature 116 °C higher than the temperature measured by the internal bandgap but not less than 250 °C. The TH1 threshold triggers a thermal foldback.

The TH2 threshold is 40 °C above TH1 and triggers thermal shutdown.

The two detection mechanisms can be disabled by setting to low the bits *TG_TH2* and *TG_TH1*.

8.4.8 Low Battery Protection

For PVDDL supply below 3.4 V the power FETs can go into saturation at higher load currents which could result in device damage due to the FETs connected to PVDDH going into thermal runaway.

To prevent the damage the OCP limit is adjusted based on PVDDL level measured by the internal SAR ADC. The table below presents the PVDDL thresholds where the OCP will be adjusted automatically. Lower PVDDL level will correspond to lower OC limit setting.

Table 8-4. PVDDL Range and Thresholds

PVDDL Range
PVDDL ≥ 3.4 V
3.1 V ≤ PVDDL < 3.4 V
2.9 V ≤ PVDDL < 3.1 V
2.7 V ≤ PVDDL < 2.9 V

The control of OC limit occurs in power modes where PVDDL is supplied externaly and the output is switching on PVDDH (PWR_MODE0, PWR_MODE1).

8.4.9 Battery Power Limiter

The TAS2781 integrates an algorithm that can control the audio power by regulating the current based on the battery voltage readout.

The algorithm provides three levels of current based on two levels of battery voltage.

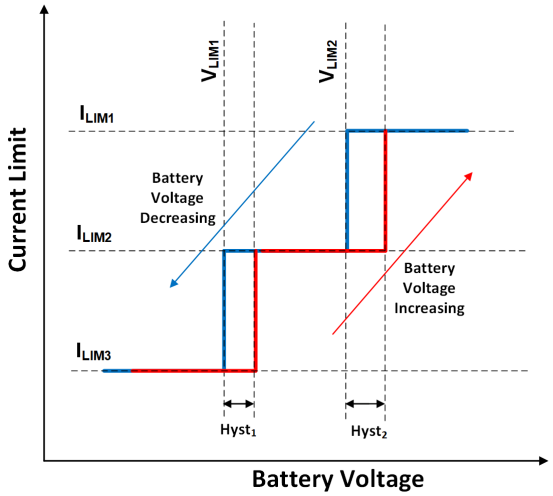


Figure 8-5. Current Limit vs Battery Voltage

The power limiter can be applied to either PVDDL (one cell battery) or PVDDH (multi-cell battery). By default it is set on PVDDL and can be canged to PVDDH by using bit *PWR_LIM_SRC*.

8.4.10 Clocks

The device clocking is derived from the SBCLK input clock. The tables below show the valid SBCLK clock frequencies for each sample rate and SBCLK to FSYNC ratio.

If the sample rate is properly configured via the *SAMP_RATE[2:0]* register bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device will detect improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts. After the clock error is detected, the device will enter a low power halt mode after a time set by *CLK_HALT_TIMER[2:0]* register bits if *DIS_CLK_HALT* bit is low. Additionally, the device can automatically power up and down on valid clock signals if *CLK_PWRUD* register bit is set to high. The device sampling rate should not be changed while this feature is enabled. In this mode the *DIS_CLK_HALT* bit register should be set low in order for this feature to work properly.

Table 8-5. Supported SBCLK Frequencies [MHz] for 48 kHz Based Sample Rates

Sample Rate (kHz)	SBCLK to FSYNC Ratio						
	16	**24**	**32**	**48**	**64**	**96**	**125**
16	NA	NA	0.512	0.768	1.024	1.526	2
24	NA	0.576	0.768	1.152	1.536	2.304	3
32	0.512	0.768	1.024	1.536	2.048	3.072	4
48	0.768	1.152	1.536	2.304	3.072	4.608	6
96	1.536	2.304	3.072	4.608	6.144	9.216	12
192	3.072	4.608	6.144	9.216	12.288	18.432	24
Sample Rate (kHz)	**SBCLK to FSYNC Ratio**						
	128	**192**	**250**	**256**	**384**	**500**	**512**
16	2.048	3.072	4	4.096	6.144	8	8.192
24	3.072	4.608	6	6.144	9.216	12	12.288
32	4.096	6.144	8	8.192	12.288	16	16384
48	6.144	9.216	12	12.288	18.432	24	24.576
96	12.288	18.432	24	24.576	NA	NA	NA
192	24.576	NA	NA	NA	NA	NA	NA

Table 8-6. Supported SBCLK Frequencies [MHz] for 44.1 kHz Based Sample Rates

Sample Rate (kHz)	SBCLK to FSYNC Ratio					
	16	24	32	48	64	96
14.7	NA	NA	NA	0.7056	0.9408	1.4112
22.05	NA	NA	0.7056	1.0584	1.4112	2.1168
29.4	NA	0.7056	0.9408	1.4112	1.8816	2.8224
44.1	0.7056	1.0584	1.4112	2.1168	2.8224	4.2336
88.2	1.4112	2.1168	2.8224	4.2336	5.6448	8.4672
176.4	2.8224	4.2336	5.6448	8.4672	11.2896	16.9344
Sample Rate (kHz)	**SBCLK to FSYNC Ratio**					
	128	**192**	**256**	**384**	**512**	
14.7	1.8816	2.8224	3.7632	5.6448	7.5264	
22.05	2.8224	4.2336	5.6448	8.4672	11.2896	
29.4	3.7632	5.6448	8.4672	8.192	15.0528	
44.1	5.6448	8.4672	11.2896	16.9344	22.5792	
88.2	11.2896	16.9344	22.5792	33.8688	NA	
176.4	211.5792	33.8688	NA	NA	NA	

8.4.11 Ultrasonic

The TAS2781 has a dedicated power mode (PWR_MODE3) to play ultasound in advance ultrasonic applications like presence detection, gesture recognition, etc.

When playing ultrasound it is recommended to set bits *DEM_CTRL[1:0]* to 3h and bit *DIS_DITH* to 1h.

In PWR_MODE3 mode of operation the output stage of Class-D will be supplied by external PVDDL rail.

8.4.12 Echo Reference

The TAS2781 can loop back the DSP output.

This feature allows user to do noise cancellation or echo correction algorithms.

A block diagram is presented in the figure below.

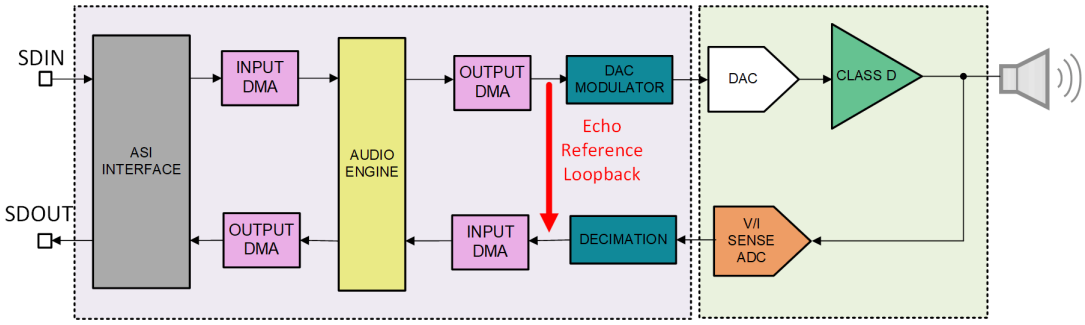


Figure 8-6. Echo Reference Loopback

The echo reference can be enabled by configuring *AUDIO_TX* register bit. The slot length and the time slot can be selected using *AUDIO_SLEN* and *AUDIO_SLOT[5:0]* register bits.

8.4.13 Hybrid-Pro External Boost Controller

The device has implemented an internal Hybrid-Pro algorithm allowing users to optimize the efficiency in the system by controlling the external power supply and maintaining just enough margin to provide high dynamic range without clipping distortions.

Features of Hybrid-Pro control:

- Optional 8 steps 384 kHz PWM format or 16 steps 192 kHz PWM format Hybrid-Pro control waveform for external DC-DC converter.
- Configurable maximum 4 ms look-ahead audio signal delay buffer, which provides capability to fit various applications systems' DC-DC bandwidth and power supply coupling capacitance.
- Maximum 8 ms programmable audio signal peak hold to optimize power supply voltage rail transition from large audio input to small level, useful to avoid clipping distortions.
- Hybrid-Pro automatically adjusts audio signal trigger level and each step level. Fine tune available to achieve the balance between efficiency and envelope tracking speed.

When enabled, the controller generates at PWM_CTRL pin a signal with a duty cycle proportional to the peak voltage on the speaker. Using an external RC filter the signal is converted to an analog voltage and can be used to control boost converters with feedback input.

The figure below shows how the PWM_CTRL pin can be connected to the external boost control RC network.

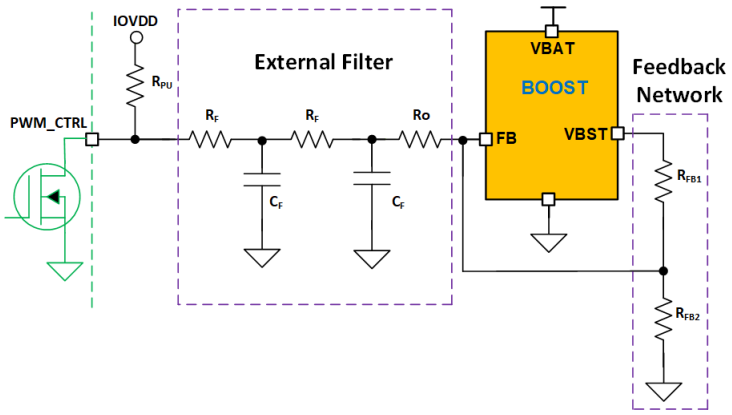


Figure 8-7. PWM_CTRL Pin and External Components

By default, the PWM_CTRL pin has an open drain configuration which allows an easy implementation of a multi-channel control loop using only one RC circuitry as shown in figure below.

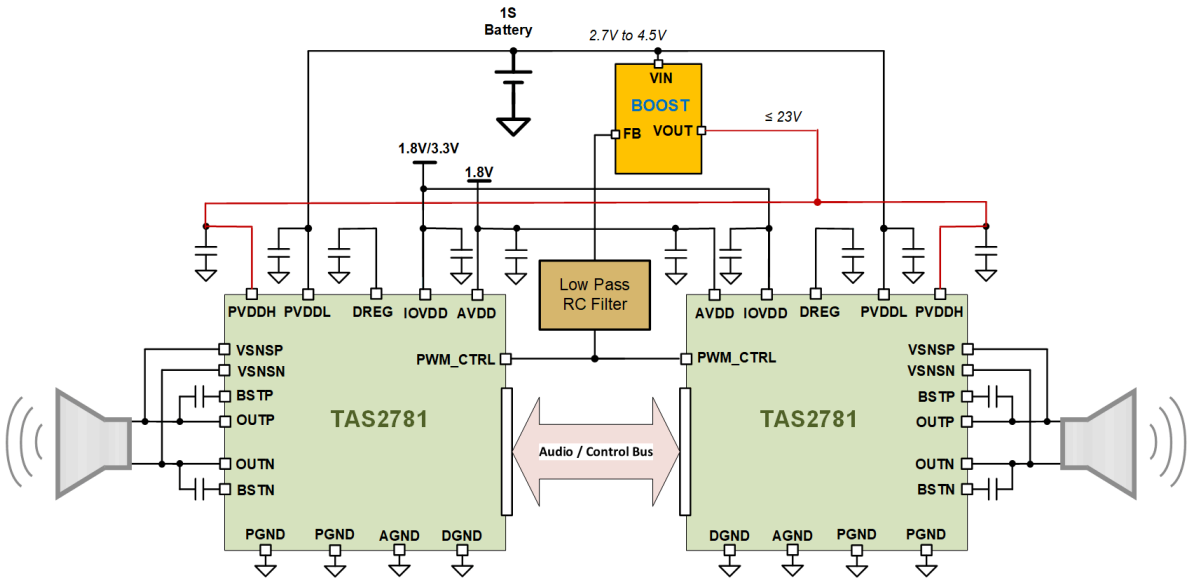


Figure 8-8. Multi - Channel Configuration using PWM_CTRL Pin

When only one device is controlling the boost converter it is recommended to set the *PWM_CTRL[6]* bit to low. The PWM_CTRL pin will change configuration to a push-pull and no pull-up resistor is required.

Note

When using the external boost controller the supply tracking limiter should be either disabled or have the thresholds programmed to a value higher than maximum output voltage of the boost.

To program the internal Class-H controller use registers from pages 0x05 and 0x06.

See TAS2781 User Manual and SLOA326 Application Note for more details on programming the boost controller.

8.5 Operational Modes

8.5.1 Beep Generator

This tone generator produces a simple audio tone (beep) that is transmitted directly to the output (speaker).

The generator relies on a pulsed signal coming into either SDZ or NC_SCLK pin.

The beep generation is executed by pulsating any of these two pins with an input frequency f_{IN} specified in .

The beep output signal will have a frequency given by:

$$f_{BEEP} = f_{IN}/64 \text{ for SDZ pin;} \quad (3)$$

$$f_{BEEP} = f_{IN}/4 \text{ for NC\_SCLK pin.} \quad (4)$$

For example, if an 800 Hz beep is needed, input a 3.2 kHz PWM signal to pin NC_SCLK.

The beep generation can happen when the device is in Software Shutdown mode, by applying pulses on the pin. A deglitch timer will hold-off the shut-down functionality until the tone has finished and the deglitch timer has expired in which case the pin will revert to controlling the hardware shutdown of the device (SDZ) or SPI clock (NC_SCLK).

The output power of the beep signal is controled by the duty cycle of the input signal as discribed in the table below.

Table 8-7. Beep Output Power

Load (Ω)	Duty Cycle (%)	Ouput Power (W)
8	20 - 30	0.125
8	45 - 55	0.25
8	70 - 80	0.5

Note: When NC_SCLK pin is used for beeping, pin 17 should be connected to an 1.8 V supply (AVDD, IOVDD).

8.5.2 Hardware Shutdown

The device enters Hardware Shutdown mode if the SDZ pin is asserted low. In Hardware Shutdown mode, the device consumes the minimum quiescent current from AVDD, IOVDD, PVDDH and PVDDL supplies. All registers lose state in this mode and I^2C or SPI communication is disabled.

By default, when SDZ pin goes low, the device will force a hardware shutdown after a timeout set by the configurable shutdown timer (register bits SDZ_TIMEOUT[1:0]). If SDZ is asserted low while audio is playing, the device will ramp down volume of the audio, stop the Class-D switching, power down analog and digital blocks and finally put the device into Hardware Shutdown mode. The device can also be configured for forced hardware shutdown and in this case it will not attempt to gracefully disable the audio channel. The shutdown mode can be controlled using SDZ_MODE[1:0] register bits.

When SDZ is released, the device will sample the ADDR pin and enter the Software Shutdown mode.

8.5.3 Mode Control and Software Reset

The TAS2781 mode can be configured by writing the *MODE[2:0]* register bits.

A software reset can be accomplished by setting high the *SW_RESET* register bit. This bit is self clearing. Once enabled it will restore all registers to their default values.

8.5.4 Software Shutdown

Software Shutdown mode powers down all analog blocks required to playback audio, but does not cause the device to lose register state.

The registers are available through I^2C or SPI interface.

Software Shutdown is enabled by asserting the *MODE[2:0]* register bits to 3'b010. If audio is playing when Software Shutdown is asserted, the Class-D will volume ramp down before shutting down. When de-asserted, the Class-D will begin switching and volume will ramp back to the programmed digital volume setting.

8.5.5 Mute Mode

The TAS2781 will ramp down volume of the Class-D amplifier to a mute state by setting the *MODE[2:0]* register bits to 3'b001. During mute the Class-D still switches but transmits no audio content. If mute is de-asserted, the device will ramp volume back to the programmed digital setting.

8.5.6 Active Mode

In Active Mode the Class-D switches and plays back audio. Speaker voltage and current sensing are operational if enabled. Set the *MODE[2:0]* register bits to 3'b000 to enter Active Mode.

8.5.7 Noise Gate Mode

In this mode of operation described in section Section 8.4.2.8 the device monitors the signal and powers down the Class-D when signal goes below a threshold.

8.6 Faults and Status in TAS2781

During the power-up sequence, the circuit monitoring the AVDD pin (UVLO) will hold the device in reset (including all configuration registers) until the supply is valid. The device will not exit Hardware Shutdown until AVDD is valid and the SDZ pin is released. Once SDZ is released, the digital core voltage regulator will power up, enabling detection of the operational mode. If AVDD dips below the UVLO threshold, the device will immediately be forced into a reset state.

The device also monitors the PVDDH supply and holds the analog core in power down if the supply is below the UVLO threshold (set by register bits *PVDDH_UV_TH[5:0]*). If the TAS2781 is in active operation and an UVLO fault occurs, the analog blocks will immediately be powered down to protect the device. These faults are latched and require a transition through HW/SW shutdown to clear the fault. The latched registers will report UVLO faults.

When exiting Software Shutdown to Active (for example: MODE[2:0] bits from 010b to 000b), if PVDDH undervoltage is detected, the device will go back into Software Shutdown and an interrupt (IL_PUVLO) will be flagged. To exit this fault user needs to clear the interrupt and program the device in Software Shutdown using MODE[2:0] bits, before making another attempt to go to Active mode.

A similar situation might occur in PWR_MODE2, if internal PVDDL LDO undervoltage is detected and IL_LDO_UV interrupt is flagged.

The device transitions into Software Shutdown mode if it detects any faults with the TDM clocks such as:

- Invalid SBCLK to FSYNC ratio
- Invalid FSYNC frequency
- Halting of SBCLK or FSYNC clocks

Upon detection of a TDM clock error, the device transitions into Software Shutdown mode as quickly as possible to limit the possibility of audio artifacts. Once all TDM clock errors are resolved, the device volume ramps back to its previous playback state. During a TDM clock error, the IRQZ pin will assert low if the clock error interrupt mask register bit *IM_TDMCE* is set low. The clock fault is also available for read-back in the live or latched fault status registers (bits *IL_TDMCE* and *IR_TDMCE*).

Note

It is mandatory to have TDM clocks available before programming I^2C to enter Active mode. Entering Active mode with no clocks present will trigger a clock error, device will go into software shutdown and the interrupts associated with the clock errors will be raised.

The TAS2781 also monitors die temperature and Class-D load current and will enter software shutdown mode if either of these exceed safe values. As with the TDM clock error, the IRQZ pin will assert low for these faults if the appropriate fault interrupt mask register bit is set low for over temperature and for over current. The fault status can also be monitored in the latched fault registers as with the TDM clock error.

Die over temperature and Class-D over current errors can either be latching (i.e. the device will enter Software Shutdown until a HW/SW shutdown sequence is applied) or they can be configured to automatically retry after a prescribed time. This behavior can be configured in the *OTE_RETRY* and *OCE_RETRY* register bits (for over temperature and over current). Even in latched mode, the Class-D will not attempt to retry after an over temperature or over current error until the retry time period (Default = 1.5 s) has elapsed. This prevents applying repeated stress to the device in a rapid fashion that could lead to device damage. If the device has been cycled through SW/HW shutdown, the device will only begin to operate after the retry time period. By default the *RETRY* feature is disabled.

The status registers (and IRQZ pin if enabled, and for un-masked interrupts) also indicate limiter behavior including when the limiter is activated, when PVDDH is below the inflection point, when maximum attenuation has been applied, when the limiter is in infinite hold and when the limiter has muted the audio.

In the situations when the device operates in PWR_MODE2 the PVDDL pin is supplied by an internal LDO. Protection circuits monitor this block and generate faults in case of under voltage, over voltage or if the LDO is over loaded. The device goes into shut down if one of these faults triggers.

The IRQZ pin is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to IOVDD. An internal 20 kΩ pull up resistor is provided. It can be accessed by setting the *IRQZ_PU* register bit of Register 0x04 to high.

The IRQZ interrupt configuration can be set using *IRQZ_CFG[1:0]* register bits in Register 0x5C. The *IRQZ_POL* register bit sets the interrupt polarity and *IRQZ_CLR* register bit allows to clear all the interrupt latch register bits.

Live flag registers are active only when the device is in Active mode of operation. If the device is in Software Shutdown by I^2C command or due to any fault condition described below, the live flags will be reset. Latched flags will not be reset in this condition and available for user to read their status.

Table 8-8. Fault Interrupt Mask

Interrupt	Live Register	Latch Register	Mask Register	Default (1 = Mask)
Temp Over 105 ºC	IL_TO105	IR_TO105	IM_TO105	1
Temp Over 115 ºC	IL_TO115	IR_TO115	IM_TO115	1
Temp Over 125 ºC	IL_TO125	IR_TO125	IM_TO125	1
Temp Over 135 ºC	IL_TO135	IR_TO135	IM_TO135	1
Over Temp Error	Device in shutdown	IR_OT	IM_OT	0
Over Current Error	Device in shutdown	IR_OC	IM_OC	0
TDM Clock Error	Device in shutdown	IR_TDMCE	IM_TDMCE	1
TDM Clock Error: Invalid SBCLK ratio or FS rate	-	IR_TDMCEIR	-	-
TDM Clock Error: FS changed on the fly	-	IR_TDNCEFC	-	-
TDM Clock Error: SBCLK FS ratio changed on the fly	-	IR_TDMCERC	-	-
BOP Active	IL_BOPA	IR_BOPA	IM_BOPA	0
BOP Infinite Hold	IL_BOPIH	IR_BOPIH	IM_BOPIH	0
BOP Mute	IL_BOPM	IR_BOPM	IM_BOPM	-
BOP Detected	IL_BOPD	IR_BOPD	IM_BOPD	0

Table 8-8. Fault Interrupt Mask (continued)

Interrupt	Live Register	Latch Register	Mask Register	Default (1 = Mask)
BOP Power Down	-	IR_BOPPD	IM_BOPPD	1
PVDDH Below Limiter Inflection	IL_PBIP	IR_PBIP	IM_PBIP	1
Limiter Active	IL_LIMA	IR_LIMA	IM_LIMA	1
Limiter Max Atten	IL_LIMMA	IR_LIMMA	IM_LIMMA	1
PVDDH UVLO	Device in shutdown	IR_PUVLO	IM_PUVLO	0
PVDDL UVLO	Device in shutdown	-	-	-
OTP CRC Error	Device in shutdown	IR_OTPCRC	IM_OTPCRC	0
PVDDL Gain Limiter	IL_VBATLIM	IR_VBATLIM	IM_VBATLIM	1
Internal PLL Clock Error	Device in shutdown	IR_PLL_CLK	IM_PLL_CLK	1
Noise Gate Active	IL_NGA	-	-	-
PVDDH - PVDDL Below Threshold	IL_PVBT	IR_PVBT	IM_PVBT	0
Internal PVDDL LDO Under Voltage	Device in shutdown	IR_LDO_UV	IM_LDO_UV	0
Thermal Detector Threshold 2	Device in shutdown	IR_TDTH2	IM_TDTH2	0
Thermal Detector Threshold 1	IL_TDTH1	IR_TDTH1	IM_TDTH1	0

8.7 Power Sequencing Requirements

There are no power sequencing requirements for order of rate of ramping up or down as long as SDZ pin is kept low.

8.8 Digital Input Pull Downs

The I^2S/TDM interface pins and the ICC pin have optional weak pull down resistors to prevent the pins from floating. Register bits *DIN_PD[4:0]* from are used to enable/disable pull downs. The pull downs are not enabled during Hardware Shutdown.

8.9 Register Map

8.9.1 Page = 0x00 Address = 0x00 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	Sets the device page. 00h = Page 0 01h = Page 1 ... FFh = Page 255

8.9.2 Page = 0x00 Address = 0x01 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-1	Reserved	RW	0h	Reserved
0	SW_RESET	RW	0h	Software reset 0b = De-asserted (default) 1b = Asserted

8.9.3 Page = 0x00 Address = 0x02 [Reset = 1Ah]

Bit	Field	Type	Reset	Description
7	BOP_SRC	RW	0h	BOP input source and PVDD UVLO 0b = PVDDL input and PVDDH UVLO disabled (default) 1b = PVDDH input and PVDDH UVLO enabled.
6-5	Reserved	RW	0h	Reserved
4	ISNS_PD	RW	1h	Current Sense 0b = Active 1b = Powered down

Bit	Field	Type	Reset	Description
3	VSNS_PD	RW	1h	Voltage Sense 0b = Active 1b = Powered down
2-0	MODE[2:0]	RW	2h	Device operational mode 000b = Active without Mute 001b = Active with Mute 010b = Software Shutdown (default) 011b -111b = Reserved

8.9.4 Page = 0x00 Address = 0x03 [Reset = 28h]

Bit	Field	Type	Reset	Description
7-6	CDS_MODE[1:0]	RW	0h	Class-D switching mode 00b = Y-Bridge, high power on PVDDL (default) 01b = PVDDL Only Supply of Class D 10b = PVDDH Only Supply of Class D 11b = Y-Bridge, low power on PVDDL
5-1	AMP_LEVEL[4:0]	RW	14h	Setting / @48ksps / @96 ksps 00h / 11 dBV / 9 dBV 01h / 11.5 dBV / 9.5 dBV 02h / 12.0 dBV / 10 dBV 03h / 12.5 dBV / 10.5 dBV ……. / ……. / ……. 13h / 20.5 dBV / 18.5 dBV 14h (default) / 21 dBV / 19 dBV Others : Reserved
0	Reserved	RW	0h	Reserved

8.9.5 Page = 0x00 Address = 0x04 [Reset = 21h]

Bit	Field	Type	Reset	Description
7	PVDDL_MODE	RW	0h	PVDDL supply is: 0h = Supplied externally 1h = Internally generated from PVDDH
6	IRQZ_PU	RW	0h	IRQZ internal pull up 0h = Disabled 1h = Enabled
5	AMP_SS	RW	1h	Spread Spectrum 0h = Disabled 1h = Enabled **When Spread Spectrum and Sync Mode are both enabled, Sync Mode takes priority*
4-3	SAR_FLT[1:0]	RW	0h	SAR filter cut-off frequency 0h = Disabled (default) 1h = 300 kHz 2h = 150 kHz 3h = 50 kHz

Bit	Field	Type	Reset	Description
2-0	HPF_FREQ_PB[2:0]	RW	1h	Forward Path DC blocker cut-off frequency 0h = Disabled (filter bypassed) 1h = 2 Hz 2h = 50 Hz 3h = 100 Hz 4h = 200 Hz 5h = 400 Hz 6h = 800 Hz 7h = Reserved ** For 44.1/88.2 kHz sampling rates divide the values from above by 1.0884*

8.9.6 Page = 0x00 Address = 0x05 [Reset = 41h]

Bit	Field	Type	Reset	Description
7-4	Reserved	RW	4h	Reserved
3	TFB_EN	RW	0h	Thermal Foldback 0h = Disabled 1h = Enabled
2-0	HPF_FREQ_REC[2:0]	RW	1h	Record Path DC blocker 0h = Disabled (filter bypassed) 1h = 2 Hz 2h = 50 Hz 3h = 100 Hz 4h = 200 Hz 5h = 400 Hz 6h = 800 Hz 7h = Reserved ** For 44.1/88.2 kHz sampling rates divide the values from above by 1.0884*

8.9.7 Page = 0x00 Address = 0x06 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	0h	Reserved
5	OCE_RETRY	RW	0h	Retry after over current event. 0h = Disabled 1h = Enabled, retry after timer.
4	OTE_RETRY	RW	0h	Retry after over temperature event. 0h = Disabled 1h = Enabled, retry after timer.
3	PFFB_EN	RW	0h	Post-Filter Feedback is 0h = Disabled (uses OUT_N and OUT_P pins) 1h = Enabled (uses VSNS_N and VSNS_P pins)
2	SAFE_MODE	RW	0h	Safe mode 0h = Disabled 1h = Enabled
1-0	Reserved	RW	0h	Reserved

8.9.8 Page = 0x00 Address = 0x07 [Reset = 20h]

Bit	Field	Type	Reset	Description
7-6	SDZ_MODE[1:0]	RW	0h	Shutdown mode configuration. 0h = Shutdown after timeout (default) 1h = Immediate forced shutdown 2h - 3h = Reserved

Bit	Field	Type	Reset	Description
5-4	SDZ_TMOUT[1:0]	RW	2h	Shutdown timeout 0h = 2 ms 1h = 4 ms 2h = 6 ms (default) 3h = 23.8 ms
3-2	DVC_RMP_RT[1:0]	RW	0h	Digital volume control ramp rate 0h = Volume ramp enabled (default) 1h - 2h = Reserved 3h = Volume ramp disabled
1	I2C_GBL_EN	RW	0h	I^2C global address 0h = Disabled 1h = Enabled
0	I2C_AD_DET	RW	0h	Re-detect I^2C peripheral address (self clearing bit) 0h = Normal detection 1h = Re-detect address after power up

8.9.9 Page = 0x00 Address = 0x08 [Reset = 09h]

Bit	Field	Type	Reset	Description
7	AMP_INV	RW	0h	Invert audio amplifier ouput 0h = Normal 1h = Inverted
6	CLASSD_SYNC	RW	0h	Class-D synchronization mode 0h = Not synchronized to audio clocks 1h = Synchronized to audio clocks **When Spread Spectrum and Sync Mode are both enabled, Sync Mode takes priority*
5	RAMP_RATE	RW	0h	When CLASSD_SYNC = 1 sample rate is based 0h = 48 kHz 1bh = 44.1 kHz
4	AUTO_RATE	RW	0h	Auto-detection of TDM sample rate 0h = Enabled 1h = Disabled
3-1	SAMP_RATE[2:0]	RW	4h	Sample rate of the TDM bus 0h = Reserved 1h = 14.7/16 kHz 2h = 22.05/24 kHz 3h = 29.4/32 kHz 4h = 44.1/48 kHz 5h = 88.2/96 kHz 6h = 176.4/192 kHz 7h = Reserved
0	FRAME_START	RW	1h	TDM frame start polarity 0h = Low to High on FSYNC 1h = High to Low on FSYNC

8.9.10 Page = 0x00 Address = 0x09 [Reset = 02h]

Bit	Field	Type	Reset	Description
7	RMP_FREQ_INCR	RW	0h	When CLASSD_SYNC = 1, ramp rate is 0h = 352 kHz 1h = 376 kHz
6	RX_JSTF	RW	0h	TDM RX sample justification within the time slot 0h = Left 1h = Right
5-1	RX_OFF[4:0]	RW	1h	TDM RX start of frame to time slot 0 offset (number of SBCLK cycles)

Bit	Field	Type	Reset	Description
0	RX_EDGE	RW	0h	TDM RX capture clock polarity 0h = Rising edge of SBCLK 1h = Falling edge of SBCLK

8.9.11 Page = 0x00 Address = 0x0A [Reset = 0Ah]

Bit	Field	Type	Reset	Description
7-6	IVMON_EN[1:0]	RW	0h	Sets the current and voltage data to length of 0h = 16 bits (default) 1h = 12 bits 2h = 8 bits 3h = Reserved
5-4	RX_SCFG[1:0]	RW	0h	TDM RX time slot select configuration 0h = Mono with time slot equal to I^2C address offset (default) 1h = Mono left channel 2h = Mono right channel 3h = Stereo downmix (L+R)/2
3-2	RX_WLEN[1:0]	RW	2h	TDM RX word length 0h = 16 bits 1h = 20 bits 2h = 24 bits (default) 3h = 32 bits
1-0	RX_SLEN[1:0]	RW	2h	TDM RX slot length 0h = 16 bits 1h = 24 bits 2h = 32 bits 3h = Reserved

8.9.12 Page = 0x00 Address = 0x0C [Reset = 10h]

Bit	Field	Type	Reset	Description
7-4	RX_SLOT_R[3:0]	RW	1h	TDM RX Right Channel Time Slot (default = 1h)
3-0	RX_SLOT_L[3:0]	RW	0h	TDM RX Left Channel Time Slot (default = 0h)

8.9.13 Page = 0x00 Address = 0x0D [Reset = 13h]

Bit	Field	Type	Reset	Description
7	TX_KEEPCY	RW	0h	TDM TX SDOUT LSB data will be driven when TX_KEEPEN is enabled 0h = Full cycle 1h = Half cycle
6	TX_KEEPLN	RW	0h	TDM TX SDOUT will hold the bus, when TX_KEEPEN is enabled, for: 0h = 1 LSB cycle 1h = Always
5	TX_KEEPEN	RW	0h	TDM TX SDOUT bus keeper 0h = Disabled 1h = Enabled
4	TX_FILL	RW	1h	TDM TX SDOUT unused bit field fill 0h = Transmit 0 1h = Transmit Hi-Z
3-1	TX_OFFSET[2:0]	RW	1h	TDM TX start of frame to time slot 0 offset (default = 1h)
0	TX_EDGE	RW	1h	TDM TX launch clock polarity 0h = Rising edge of SBCLK 1h = Falling edge of SBCLK

8.9.14 Page = 0x00 Address = 0x0E [Reset = C2h]

Bit	Field	Type	Reset	Description
7	CLASSH_RES	RW	1h	Class-H resolution 0h = 8 bits 1h = 16 bits
6	VSNS_TX	RW	1h	TDM TX voltage sense transmit 0h = Disabled 1h = Enabled
5-0	VSNS_SLOT[5:0]	RW	2h	TDM TX voltage sense time slot (default = 02h)

8.9.15 Page = 0x00 Address = 0x0F [Reset = 40h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	ISNS_TX	RW	1h	TDM TX current sense transmit 0h = Disabled 1h = Enabled
5-0	ISNS_SLOT[5:0]	RW	0h	TDM TX current sense time slot (default = 00h)

8.9.16 Page = 0x00 Address = 0x10 [Reset = 04h]

Bit	Field	Type	Reset	Description
7	SAR_DATA_SL	RW	0h	TDM TX SAR data time slot length 0h = Truncate to 8 bits 1h = Left justify to 16 bits
6	SAR_DATA_TX	RW	0h	TDM TX SAR data transmit enable 0h = Disabled 1h = Enabled
5-0	SR_DATA_SLOT[5:0]	RW	4h	TDM TX SAR time slot (default = 4h)
	1. Sequence for 96 ksps: PVDDL, PVDDH, Temp, Marker. 2. Sequence for 192 ksps: PVDDL, PVDDL, PVDDH, PVDDH, Temp, Temp, Marker, Marker.			

8.9.17 Page = 0x00 Address = 0x13 [Reset = 08h]

Bit	Field	Type	Reset	Description
7	STAT_SLOT_TG	RW	0h	Over Power STATUS bits - TH1 and TH2 0h = Disabled 1h = *Bit [5]* from STATUS = TH2 OR-ed with OTS 1h = *Bit [6]* from STATUS = TH1
6	STATUS_TX	RW	0h	TDM TX status transmit 0h = Disabled 1h = Enabled

Bit	Field	Type	Reset	Description
5-0	STATUS_SLOT[5:0]	RW	8h	TDM TX status time slot (default = 08h) Bit [7] - PVDDH status) 0h = PVDDH UVLO not detected 1h = PVDD UVLO detected *Bit [6]* - Over current status 0h = No over current detected 1h = Over current detected *Bit [5]* - Over temperature status 0h= No over temperature detected 1h = Over temperature detected *Bit [4] - BOP status 0h = BOP not detected 1h = BOP detected *Bit [3] - Signal distorsion limiter status 0h = No distortion limiter 1h = Gain attenuation done due to distortion limiter Bit [2] - Noise Gate status 0h = Device in normal mode 1h = Device in Noise Gate mode Bit [1] - Class-D power stage status 0h = Class D Power switch connected to PVDDL 1h = Class D Power switch connected to PVDDH Bit [0] - Power up state 0h = Device in powered down 1h = Device in active state

8.9.18 Page = 0x00 Address = 0x15 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-5	LS_OC[2:0]	RW	0h	Low side OC threshold 0h = Nominal OC threshold (default) 1h = OC threshold increased by 10% of nominal 2h = OC threshold increased by 20% of nominal 3h = OC threshold increased by 30% of nominal 4h = OC threshold reduced by 40% of nominal 5h = OC threshold reduced by 30% of nominal 6h = OC threshold reduced by 20% of nominal 7h = OC threshold reduced by 10% of nominal
4-2	ICC_CFG[2:0]	RW	0h	ICC pin function 0h = Gain slot transmission (default) 1h = Reserved 2h = ICC pin buffers disabled 3h = ICC pin is a general purpose input 4h = ICC pin is a general purpose output 5h - 7h = Reserved
1-0	Reserved	R	0h	Reserved

8.9.19 Page = 0x00 Address = 0x16 [Reset = 12h]

Bit	Field	Type	Reset	Description
7	AUDIO_SLEN	RW	0h	TDM audio slot length 0h = 16 bits 1h = 24 bits
6	AUDIO_TX	RW	0h	TDM audio output transmit 0h = Disabled 1h = Enabled
5-0	AUDIO_SLOT[5:0]	RW	12h	TDM TX status time slot (default = 12h)

8.9.20 Page = 0x00 Address = 0x17 [Reset = 80h]

Bit	Field	Type	Reset	Description
7-4	LIM_MAX_AT[3:0]	RW	8h	Limiter maximum attenuation (default = 8h) 0h = -1 dB 1h = -2 dB 2h = -3 dB … 0Eh = -15 dB 0Fh = Reserved
3-0	Reserved	R	0h	Reserved

8.9.21 Page = 0x00 Address = 0x1A [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	DVC_LVL[7:0]	RW	00h	Digital volume control 00h = 0 dB 01h = -0.5 dB 02h = -1 dB ... C8h = -100 dB Others : Mute

8.9.22 Page = 0x00 Address = 0x1B [Reset = 62h]

Bit	Field	Type	Reset	Description
	LIMB_SRC	RW	0h	Voltage limiter input source 0h = PVDDL input 1h = PVDDH input
7 - 6	Reserved	R	1h	Reserved
5	LIM_HR_EN	RW	1h	Limiter dynamic headroom 0h = Disabled 1h = Enabled
4-1	LIM_ATK_RT[3:0]	RW	1h	Limiter attack rate 00h = 20 µs/dB 01h = 40 µs/dB 02h = 80 µs/dB 03h = 160 µs/dB 04h = 320 µs/dB 05h = 640 µs/dB 06h = 1280 µs/dB 07h = 2560 µs/dB 08h = 5120 µs/dB 09h = 10240 µs/dB 10h = 20480 µs/dB 11h = 40960 µs/dB 12h = 81920 µs/dB 13h = 163840 µs/dB Others : Reserved
0	LIM_EN	RW	0h	Limiter is 0h = Disabled 1h = Enabled

8.9.23 Page = 0x00 Address = 0x1C [Reset = 36h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved

Bit	Field	Type	Reset	Description
6-3	LIM_RLS_RT[3:0]	RW	6h	Limter release rate 0h = 2 ms/dB 1h = 4 ms/dB 2h = 8 ms/dB 3h = 16 ms/dB 4h = 32 ms/dB 5h = 64 ms/dB 6h = 128 ms/dB 7h = 256 ms/dB 8h = 512 ms/dB 9h = 1024 ms/dB Ah = 2048 ms/dB Bh = 4096 ms/dB Ch = 8192 ms/dB Ch = 16384 ms/dB Eh - Fh = Reserved
2-0	LIM_HLD[2:0]	RW	6h	Limiter hold time 0h = Reserved 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms (default) 7h = 1000 ms

8.9.24 Page = 0x00 Address = 0x1D [Reset = 00h]

Bit	Field	Type	Reset	Description
7	ICC_EN	RW	0h	ICC pin 0h = Disabled 1h = Enabled
6-3	ICC_PAIR_DEV[3:0]	RW	0h	ICC device pair number (default = 0h) 0h = Device paired with Device 0 1h = Device paired with Device 1 …….. 7h = Device paired with Device 7 8h - Fh = Device not paired
2-0	ICC_DEV[2:0]	RW	0h	ICC device number (default = 0h) 0h = Device transmits gain in Slot 0 of ICC bus 1h = Device transmits gain in Slot 1 of ICC bus 2h = Device transmits gain in Slot 2 of ICC bus 3h = Device transmits gain in Slot 3 of ICC bus 4h = Device transmits gain in Slot 4 of ICC bus 5h = Device transmits gain in Slot 5 of ICC bus 6h = Device transmits gain in Slot 6 of ICC bus 7h = Device transmits gain in Slot 7 of ICC bus

8.9.25 Page = 0x00 Address = 0x1F [Reset = 01h]

Bit	Field	Type	Reset	Description
7-5	HS_OC[2:0]	RW	0h	High side OC threshold 0h = Nominal OC threshold (default) 1h = OC threshold increased by 10% of nominal 2h = OC threshold increased by 20% of nominal 3h = OC threshold increased by 30% of nominal 4h = OC threshold reduced by 40% of nominal 5h = OC threshold reduced by 30% of nominal 6h = OC threshold reduced by 20% of nominal 7h = OC threshold reduced by 10% of nominal
4	BOPSD_EN	RW	0h	BOP shutdown 0h = Disabled 1h = Enabled
0	BOP_HLD_CLR	RW	0h	BOP infinite hold clear (self clearing) 0h = Do not clear 1h = Clear
	BOP_INF_HLD	RW	0h	Infinite hold in BOP event 0h = Use BOP_HLD after BOP event 1h = Do not release until BOP_HLD_CLR is asserted high
	BOP_MUTE	RW	0h	Mute in BOP event 0h = Do not mute 1h = Mute followed by device shutdown
	BOP_EN	RW	1h	BOP 0h = Disabled 1h = Enabled

8.9.26 Page = 0x00 Address = 0x20 [Reset = 2Eh]

Bit	Field	Type	Reset	Description
7-5	BOP_ATK_RT[2:0]	RW	1h	Brown out prevention attack rate 0h = 1 step in 1 sample 1h = 1 step in 2 samples (default) 2h = 1 step in 4 samples 3h = 1 step in 8 samples 4h = 1 step in 16 samples 5h = 1 step in 32 samples 6h = 1 step in 64 samples 7h = 1 step in 128 samples
4-3	BOP_ATK_ST[1:0]	RW	1h	Brown out prevention attack step size 0h = 0.5 dB 1h = 1 dB (default) 2h = 1.5 dB 3h = 2 dB

Bit	Field	Type	Reset	Description
2-0	BOP_HLD[2:0]	RW	6h	Brown out prevention hold time 0h = 0 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms (default) 7h = 1000 ms

8.9.27 Page = 0x00 Address = 0x34 [Reset = 06h]

Bit	Field	Type	Reset	Description
7-3	Reserved	R	0h	Reserved
2-1	LVS_FTH_LOW[1:0]	RW	3h	Threshold for LVS when CDS_MODE = 3h 0h = -121.5 dBFS 1h= -101.5 dBFS (default) 2h= -81.5 dBFS 3h = -71.5 dBFS (default)
0	Reserved	R	0h	Reserved

8.9.28 Page = 0x00 Address = 0x35 [Reset = BDh]

Bit	Field	Type	Reset	Description
7-5	NG_HYST_TIMER[2:0]	RW	5h	Noise Gate entry hysteris timer 0h = 400 µs 1h = 600 µs 2h = 800 µs 3h = 2 ms 4h = 10 ms 5h = 50 ms (default) 6h = 100 ms 7h = 1 s
4-3	NG_TH[1:0]	RW	3h	Noise Gate audio threshold level 0h = -90 dBFS 1h = -100 dBFS 2h = -110 dBFS 3h = -120 dBFS (default)
2	NG_EN	RW	1h	Noise Gate 0h = Disabled 1h = Enabled
1-0	Reserved	R	1h	Reserved

8.9.29 Page = 0x00 Address = 0x36 [Reset = ADh]

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	2h	Reserved
5	NG_DVC_RP	RW	1h	Volume ramping on Noise Gate 0h = Enabled 1h = Disabled
4	Reserved	R	0h	Reserved

Bit	Field	Type	Reset	Description
3-0	LVS_HYS[3:0]	RW	Dh	PVDDH to PVDDL hysteresis time 0h - 9h = Reserved Ah = 1 ms Bh = 10 ms Ch = 20 ms Dh = 50 ms (default) Eh = 75 ms Fh = 100 ms **For sampling rates f_s < 48 ksps multiply the values by 48/fs*

8.9.30 Page = 0x00 Address = 0x37 [Reset = A8h]

Bit	Field	Type	Reset	Description
7	LVS_DET	RW	1h	Low Voltage Signaling threshold 0h = Fixed 1h = Relative to PVDDL voltage
6-5	Reserved	R	1h	Reserved
4-0	LVS_FTH[4:0]	RW	08h	Threshold for LVS (CDS_MODE = 0h) 00h = -18.5 dBFS 01h = -18.25 dBFS (default) 02h = -18 dBFS 03h = -17.75 dBFS 04h = -17.5 dBFS .. 08h = -16.5 dBFS (default) .. 1Eh = -11 dBFS 1Fh = -10.75 dBFS

8.9.31 Page = 0x00 Address = 0x38 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	DIN_PD[4]	RW	0h	Weak pull down for ICC 0h = Disabled 1h = Enabled
5	DIN_PD[3]	RW	0h	Weak pull down for SDOUT 0h = Disabled 1h = Enabled
4	DIN_PD[2]	RW	0h	Weak pull down for SDIN 0h = Disabled 1h = Enabled
3	DIN_PD[1]	RW	0h	Weak pull down for FSYNC 0h = Disabled 1h = Enabled
2	DIN_PD[0]	RW	0h	Weak pull down for SBCLK 0h = Disabled 1h = Enabled
1-0	Reserved	R	0h	Reserved

8.9.32 Page = 0x00 Address = 0x3B [Reset = FCh]

Bit	Field	Type	Reset	Description
7	IM_BOPM	RW	1h	BOP mute interrupt 0h = No Mask 1h = Mask
6	IM_BOPIH	RW	1h	Bop infinite hold interrupt. 0h = No Mask 1h = Mask

Bit	Field	Type	Reset	Description
5	IM_LIMMA	RW	1h	Limiter max attenuation interrupt 0h = No Mask 1h = Mask
4	IM_PBIP	RW	1h	PVDDH below limiter inflection point interrupt 0h = No Mask 1h = Mask
3	IM_LIMA	RW	1h	Limiter active interrupt 0h = No Mask 1h = Mask
2	IM_TDMCE	RW	1h	TDM clock error interrupt 0h = No Mask 1h = Mask
1	IM_OC	RW	0h	Over current error interrupt 0h = No Mask 1h = Mask
0	IM_OT	RW	0h	Over temp error interrupt 0h = No Mask 1h = Mask

8.9.33 Page = 0x00 Address = 0x3C [Reset = BBh]

Bit	Field	Type	Reset	Description
7	Reserved	R	1h	Reserved
6	IM_OTPCRC	RW	0h	OTP_CRC error interupt 0h = No Mask 1h = Mask
5-1	Reserved	R	1Dh	Reserved
0	IM_VBATLIM	RW	1h	Gain limiter active interrupt 0h = No Mask 1h = Mask

8.9.34 Page = 0x00 Address = 0x3D [Reset = DDh]

Bit	Field	Type	Reset	Description
7	IM_PLL_CLK	RW	1h	Internal PLL derived clock error inerrupt 0h = No Mask 1h = Mask
6-0	Reserved	R	1h	Reserved

8.9.35 Page = 0x00 Address = 0x40 [Reset = F6h]

Bit	Field	Type	Reset	Description
7	IM_TO105	RW	1h	Temperature over 105 ºC interrupt. 0h = No Mask 1h = Mask
6	IM_TO115	RW	1h	Temperature over 115 ºC interrupt. 0h = No Mask 1h = Mask
5	IM_TO125	RW	1h	Temperature over 125 ºC interrupt. 0h = No Mask 1h = Mask
4	IM_TO135	RW	1h	Temperature over 135 ºC interrupt. 0h = No Mask 1h = Mask
3	IM_LDO_UV	RW	0h	Internal PVDDL LDO under voltage 0h = No Mask 1h = Mask

Bit	Field	Type	Reset	Description
2-1	Reserved	R	3h	Reserved
0	IM_PUVLO	RW	0h	PVDDH under voltage 0h = No Mask 1h = Mask

8.9.36 Page = 0x00 Address = 0x41 [Reset = 14h]

Bit	Field	Type	Reset	Description
7	IM_TDTH2	RW	0h	Thermal Detection Threshold 2 0h = No Mask 1h = Mask
6	IM_TDTH1	RW	0h	Thermal Detection Threshold 1 0h = No Mask 1h = Mask
5	IM_PVBT	RW	0h	PVDDH - PVDDL below threshold 0h = No Mask 1h = Mask
4	IM_BOPA	RW	1h	BOP active interrupt 0h = No mask 1h = Mask
3	IM_BOPD	RW	0h	BOP detected interrupt 0h = No mask 1h = Mask
2	IM_BOPPD	RW	1h	BOP device power down start 0h = No mask 1h = Mask
1-0	Reserved	R	0h	Reserved

8.9.37 Page = 0x00 Address = 0x42 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	IL_BOPM	R	0h	Interrupt due to bop mute 0h = No interrupt 1h = Interrupt
6	IL_BOPIH	R	0h	Interrupt due to bop infinite hold 0h = No interrupt 1h = Interrupt
5	IL_LIMMA	R	0h	Interrupt due to limiter max attenuation 0h = No interrupt 1h = Interrupt
4	IL_PBIP	R	0h	Interrupt due to PVDDH below limiter inflection point 0h = No interrupt 1h = Interrupt
3	IL_LIMA	R	0h	Interrupt due to limiter active 0h = No interrupt 1h = Interrupt
2	IL_TDMCE	R	0h	Interrupt due to TDM clock error 0h = No interrupt 1h = Interrupt - *Device in shutdown*
1	IL_OC	R	0h	Interrupt due to over current error 0h = No interrupt 1h = Interrupt - *Device in shutdown*
0	IL_OT	R	0h	Interrupt due to over temp error 0h = No interrupt 1 = Interrupt - *Device in shutdown*

8.9.38 Page = 0x00 Address = 0x43 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	IL_OTPCRC	R	0h	Interrupt due to OTP CRC Error Flag 0h = No interrupt 1h = Interrupt - *Device in shutdown*
5-3	Reserved	R	0h	Reserved
2	IL_NGA	R	0h	Noise Gate active flag 0h = Noise Gate not detected 1h = Noise Gate detected
1	Reserved	R	0h	Reserved
0	IL_VBATLIM	R	0h	Interrupt due to gain limiter active 0h = No interuupt 1h = Interrupt

8.9.39 Page = 0x00 Address = 0x44 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	IL_PLL_CLK	R	0h	Internal PLL Clock Error 0h = No interrupt 1h = Interrupt - *Device in shutdown*
6	Reserved	R	0h	Reserved
5	IL_PVDDL_UV	R	0h	PVDDL under voltage 0h = No interrupt 1h = Interrupt - *Device in shutdown*
4-0	Reserved	R	0h	Reserved

8.9.40 Page = 0x00 Address = 0x47 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	IL_TO105	R	0h	Temperature over 105 ºC 0b = No Interrupt 1b = Interrupt
6	IL_TO115	R	0h	Temperature over 115 ºC 0b = No Interrupt 1b = Interrupt
5	IL_TO125	R	0h	Temperature over 125 ºC 0b = No Interrupt 1b = Interrupt
4	IL_TO135	R	0h	Temperature over 135 ºC 0b = No Interrupt 1b = Interrupt
3	IL_LDO_UV	R	0h	PVDDL internal LDO under voltage 0b = No Interrupt 1b = Interrupt - *Device in shutdown*
2-1	Reserved	R	0h	Reserved
0	IL_PUVLO	R	0h	PVDDH under voltage 0b = No Interrupt 1b = Interrupt - *Device in shutdown*

8.9.41 Page = 0x00 Address = 0x48 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	IL_TDTH2	R	0h	Thermal detection threshold 2 0h = No interrupt 1h = Interrupt - *Device in shutdown*

Bit	Field	Type	Reset	Description
6	IL_TDTH1	R	0h	Thermal detection threshold 1 0h = No interrupt 1h = Interrupt
5	IL_PVBT	R	0h	(PVDDH - PVDDL) below threshold 0h = No interrupt 1h = Interrupt
4	IL_BOPA	R	0h	BOP active 0h = No interrupt 1h = Interrupt
3	IL_BOPD	R	0h	BOP detected 0h = No interrupt 1h = Interrupt
2-0	Reserved	R	0h	Reserved

8.9.42 Page = 0x00 Address = 0x49 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	IR_BOPM	R	0h	Interrupt due to BOP mute 0h = No interrupt 1h = Interrupt
6	IR_BOPIH	R	0h	Interrupt due to BOP infinite hold 0h = No interrupt 1h = Interrupt
5	IR_LIMMA	R	0h	Interrupt due to limiter max attenuation 0h = No interrupt 1h = Interrupt
4	IR_PBIP	R	0h	Interrupt due to PVDDH below limiter inflection point 0h = No interrupt 1h = Interrupt
3	IR_LIMA	R	0h	Interrupt due to limiter active 0h = No interrupt 1h = Interrupt
2	IR_TDMCE	R	0h	Interrupt due to TDM clock error 0h = No interrupt 1h = Interrupt
1	IR_OC	R	0h	Interrupt due to over current 0h = No interrupt 1h = Interrupt
0	IR_OT	R	0h	Interrupt due to over temperature 0h = No interrupt 1h = Interrupt

8.9.43 Page = 0x00 Address = 0x4A [Reset = 00h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	IR_OTPCRC	R	0h	Interrupt due to OTP CRC error 0h = No interrupt 1h = Interrupt
5-1	Reserved	R	00h	Reserved
0	IR_VBATLIM	R	0h	Interrupt due to gain limiter 0h = No interrupt 1h = Interrupt

8.9.44 Page = 0x00 Address = 0x4B [Reset = 00h]

Bit	Field	Type	Reset	Description
7	IR_PLL_CLK	R	0h	Internal PLL Clock Error 0h = No interrupt 1h = Interrupt
6-0	Reserved	R	00h	Reserved

8.9.45 Page = 0x00 Address = 0x4F [Reset = 00h]

Bit	Field	Type	Reset	Description
7	IR_TO105	R	0h	Temperature over 105 ºC 0h = No Interrupt 1h = Interrupt
6	IR_TO115	R	0h	Temperature over 115 ºC 0h = No Interrupt 1h = Interrupt
5	IR_TO125	R	0h	Temperature over 125 ºC 0h = No Interrupt 1h = Interrupt
4	IR_TO135	R	0h	Temperature over 135 ºC 0h = No Interrupt 1h = Interrupt
3	IR_LDO_UV	R	0h	Internal PVDDL LDO under voltage 0h = No Interrupt 1h = Interrupt
2-1	Reserved	R	0h	Reserved
0	IR_PUVLO	R	0h	PVDDH under voltage 0h = No Interrupt 1h = Interrupt

8.9.46 Page = 0x00 Address = 0x50 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	IR_TDTH2	R	0h	Thermal detection threshold 2 0h = No interrupt 1h = Interrupt
6	IR_TDTH1	R	0h	Thermal detection threshold 1 0h = No interrupt 1h = Interrupt
5	IR_PVBT	R	0h	Interrupt due to (PVDDH - PVDDL) below threshold 0h = No interrupt 1h = Interrupt
4	IR_BOPA	R	0h	BOP active flag 0h = No interrupt 1h = Interrupt
3	IR_BOPD	R	0h	BOP detected 0h = No interrupt 1h = Interrupt
2	IR_BOPPD	R	0h	Interrupt due to BOP triggered shutdown 0h = No interrupt 1h = Interrupt
1-0	Reserved	R	0h	Reserved

8.9.47 Page = 0x00 Address = 0x51 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-3	Reserved	R	00h	Reserved

Bit	Field	Type	Reset	Description
2	IR_TDMCEIR	R	0h	TDM clock error: invalid SBCLK ratio or sampling rate 0h = No Interrupt 1h = Interrupt
1	IR_TDMCEFC	R	0h	TDM clock error: sampling rate changed on the fly 0h = No Interrupt 1h = Interrupt
0	IR_TDMCERC	R	0h	TDM clock error: SBCLK to FSYNC ratio changed on the fly 0h = No Interrupt 1h = Interrupt

8.9.48 Page = 0x00 Address = 0x52 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	PVDDL_CNV[11:4]	R	00h	Returns SAR ADC PVDDL conversion MSB 8*{hex2dec(PVDDL_CNV[11:0])}/4096

8.9.49 Page = 0x00 Address = 0x53 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-4	PVDDL_CNV[11:4]	R	0h	Returns SAR ADC PVDDL conversion LSB 8*{hex2dec(PVDDL_CNV[11:0])}/4096
3-0	Reserved	R	0h	Reserved

8.9.50 Page = 0x00 Address = 0x54 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	PVDDH_CNV[11:4]	R	00h	Returns SAR PVDDH conversion MSB 23*{hex2dec(PVDDH_CNV[11:0])}/4096

8.9.51 Page = 0x00 Address = 0x55 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-4	PVDDH_CNV[3:0]	R	0h	Returns SAR PVDDH conversion LSBs 23*{hex2dec(PVDDH_CNV[11:0])}/4096
3-0	Reserved	R	0h	Reserved

8.9.52 Page = 0x00 Address = 0x56 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	TEMP_CNV[7:0]	R	00h	Returns SAR temperature sensor conversion {hex2dec(TEMP_CNV[7:0])} - 93

8.9.53 Page = 0x00 Address = 0x5C [Reset = 19h]

Bit	Field	Type	Reset	Description
7	CLK_PWRUD	RW	0h	Clock based device power up/power down feature 0h = Disabled 1h = Enabled
6	DIS_CLK_HALT	RW	0h	Clock halt timer 0h = Enable clock halt detection after clock error 1h = Disable clock halt detection after clock error

Bit	Field	Type	Reset	Description
5-3	CLK_HALT_TIMER[2:0]	RW	3h	Clock halt timer values 0h = 820 µs 1h = 3.27 ms 2h = 26.21 ms 3h = 52.42 ms (default) 4h = 104.85 ms 5h = 209.71 ms 6h = 419.43 ms 7h = 838.86 ms
2	IRQZ_CLR	RW	0h	Clear interrupt latch registers 0h = Do not clear 1h = Clear (self clearing bit)
1-0	IRQZ_CFG[1:0]	RW	1h	IRQZ interrupt configuration. IRQZ will assert 0h = On any unmasked live interrupt 1h = On any unmasked latched interrupt (default) 2h = For 2 - 4 ms one time on any unmasked live interrupt event 3h = For 2 - 4 ms every 4 ms on any unmasked latched interrupt

8.9.54 Page = 0x00 Address = 0x5D [Reset = 80h]

Bit	Field	Type	Reset	Description
7	IRQZ_POL	RW	1h	IRQZ pin polarity 0h = Active high 1h = Active low
6-0	Reserved	R	00h	Reserved

8.9.55 Page = 0x00 Address = 0x60 [Reset = 0Dh]

Bit	Field	Type	Reset	Description
7-2	SBLK_FS_RATIO[5:0]	RW	3h	SBCLK to FS ratio when AUTO_RATE=1 (disabled). See Table 8-9.
1-0	Reserved	R	1h	Reserved

Table 8-9. SBCLK to FSYNC Ratio (AUTO_RATE=1)

00h = 16	01h = 24	02h = 32	03h = 48 (defaut)	04h = 64
05h = 96	06h = 128	07h = 192	08h = 256	09h = 384
0Ah = 512	0Bh = 125	0Ch = 250	0Dh = 500	0Eh - 3Fh = Reserved

8.9.56 Page = 0x00 Address = 0x63 [Reset = 48]

Bit	Field	Type	Reset	Description
7	IDLE_IND	RW	0h	Idle channel optimization 0h = Used for inductors ,15 µH and higher 1h = Used for 5 µH inductors
6-0	Reserved	R	48h	Reserved

8.9.57 Page = 0x00 Address = 0x65 [Reset = 08]

Bit	Field	Type	Reset	Description
7	PWR_LIM_SRC	RW	0h	Limiter power source 0h = PVDDL 1h = PVDDH
6-0	Reserved	R	08h	Reserved

8.9.58 Page = 0x00 Address = 0x67 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-2	Reserved	R	00h	Reserved
1-0	IDCH_HYST[1:0]	RW	0h	Idle channel hysterisis timer 0h = 50 ms (default) 1h = 100 ms 2h = 200 ms 3h = 1000 ms *For sampling rates f_s < 48 ksps multiply the values by 48/f_s

8.9.59 Page = 0x00 Address = 0x68 [Reset = 30h]

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved
5-0	FS_RATIO[5:0]	RW	30h	Detected SBCLK to FSYNK ratio. See Table 8-10.

Table 8-10. Detected SBCLK to FSYNC Ratio

00h = 16	01h = 24	02h = 32	03h = 48	04h = 64
05h = 96	06h = 128	07h = 192	08h = 256	09h = 384
0Ah = 512	0Bh = 125	0Ch = 250	0Dh = 500	0Eh - 3Fh = Reserved

8.9.60 Page = 0x00 Address = 0x6A [Reset = 12h]

Bit	Field	Type	Reset	Description
7-6	CDS_DLY[1:0]	RW	0h	Delay (1/f_s) of the Y-bridge switching with respect to the input signal. See Table 8-11.
5-4	LVS_DLY[1:0]	RW	1h	Delay (1/f_s) of the PWM_CTRL pin signaling with respect to the input signal, when Class H is disabled. See Table 8-12.
3-0	LVS_RTH[3:0]	RW	2h	Relative threshold for Low Voltage Signaling (headroom from PVDDL voltage). 0h = 0.5 V 1h = 0.6 V 2h = 0.7 V ... Eh = 1.9 V Fh = 2 V

Table 8-11. CDS Delay (1/f_s)

	48 ksps		96 ksps	
	NG Enabled	NG Disabled	NG Enabled	NG Disabled
0h (default)	8.1	6.1	12.6	9.6
1h	7.1	5.1	10.6	7.6
2h	6.1	4.1	8.5	5.6
3h	5.6	3.6	7.6	4.6

Table 8-12. LVS_Delay (1/f_s)

	48 ksps		96 ksps	
	NG Enabled	NG Disabled	NG Enabled	NG Disabled
0h	7.8	5.8	12.1	9.1
1h (default)	6.8	4.8	10.1	7.1
2h	5.8	3.8	8.1	5.1
3h	5.1	3.1	6.6	3.6

8.9.61 Page = 0x00 Address = 0x6B [Reset = 7Bh]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CNV_PVDDL	RW	1h	Convert the PVDDL when BOP source is PVDDH 0h = No PVDDL conversion 1h = PVDDL conversion
5-3	FS_RATE[2:0]	RW	7h	Detected sample rate of TDM bus 0h - 3h = Reserved 4h = 44.1/48 kHz 5h = 88.2/96 kHz 6h = Reserved 7h = Error condition (default)
2	NGFR_EN	RW	0h	Noise Gate fine resolution register mode 0h = Disabled 1h = Enabled
1-0	Reserved	R	3h	Reserved

8.9.62 Page = 0x00 Address = 0x6C - 0x6E [Reset = 00001Ah]

Bit	Field	Type	Reset	Description
23-0	NGFR_LVL[23:0]	RW	00001Ah	Sets Noise Gate threshold to a level NGLV(dBFS) dec2hex[round(10^(NGLV/20)*2^31)]

8.9.63 Page = 0x00 Address = 0x6F [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	NGFR_HYST[18:11]	RW	0h	Sets Noise Gate hysterisis to a value NGHYS(ms) dec2bin[(NGHYS*f_s), 19] f_s = sampling rate in kHz Recommended to be set above 1ms.

8.9.64 Page = 0x00 Address = 0x70 [Reset = 96h]

Bit	Field	Type	Reset	Description
7-0	NGFR_HYST[10:3]	RW	96h	Sets Noise Gate hysterisis to a value NGHYS(ms) dec2bin[(NGHYS*f_s), 19] f_s = sampling rate in kHz

8.9.65 Page = 0x00 Address = 0x71 [Reset = 02h]

Bit	Field	Type	Reset	Description
7	CLASSH_EN	RW	0h	Class-H controller 0h = Disabled (default) 1h = Enabled
6	PWM_POL	RW	0h	Select PWM polarity 0h = Normal 1h = Inverted
5-0	PVDDH_UV_TH[5:0]	RW	02h	PVDDH under voltage threshold 00h = 1.753 V 01h = 2.09 V 02h = 2.428 V (default) ..... 3Fh = 23 V

8.9.66 Page = 0x00 Address = 0x73 [Reset = 08h]

Bit	Field	Type	Reset	Description
7-6	DEM_CTRL[1:0]	RW	0h	DAC MSB and LSB DEM enable/disable control 0h = MSB Enabled, LSB = Enabled (default) 1h = MSB Enabled, LSB = Disabled 2h = MSB Disabled, LSB = Enabled 3h = MSB Disabled, LSB = Disabled - Recommended setting for ultrasonic use case
5	DIS_DITH	RW	0h	DAC MSB modulator dither control 0b = Enabled 1b = Disabled - Recommended for ultrasonic use case
4-0	LIM_HDR[4:0]	RW	08h	Limiter headroom 00h = -20% 01h = -17.5% 02h = -15% …… 0Fh = 17.5% 10h = 20% 11h - 1F = Reserved

8.9.67 Page = 0x00 Address = 0x77 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	SPC_PD	RW	0h	Weak pul down on SPI clock pin (NC_SCLK) 0h = Disabled 1h = Enabled
6	SPM_PD	RW	0h	Weak pul down on SPI data output pin (NC_SDO) 0h = Disabled 1h = Enabled
5-0	Reserved	R	00h	Reserved

8.9.68 Page = 0x00 Address = 0x7A [Reset = 60h]

Bit	Field	Type	Reset	Description
7	Reserved	RW	0h	Reserved
6	PWM_CTRL	RW	1h	PWM_CTRL pin configuration 0h = Push-pull 1h = Open drain
5-0	Reserved	RW	20h	Reserved

8.9.69 Page = 0x00 Address = 0x7E [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	RW	00h	Returns I^2C checksum. Writing to this register will reset the checksum to the written value. This register is updated on writes to other registers on all books and pages.

8.9.70 Page = 0x00 Address = 0x7F [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	BOOK[7:0]	RW	0h	Sets the device book. 00h = Book 0 01h = Book 1 ... FFh = Book 255

8.9.71 Page = 0x01 Address = 0x17 [Reset = D0h]

Bit	Field	Type	Reset	Description
7-5	Reserved	R	6h	Reserved
4	CMP_HYST_LP	RW	1h	Class D comparator dependancy of low power 0h = Disabled 1h = Enabled
3	SAR_IDLE	RW	0h	Idle channel interraction to SAR 0h = Enabled 1h = Disabled
2-0	Reserved	R	0h	Reserved

8.9.72 Page = 0x01 Address = 0x19 [Reset = 60h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	EN_LLSR	RW	1h	Modulation 0b = LSR 1b = Linear LSR
5-0	Reserved	R	20h	Reserved

8.9.73 Page = 0x01 Address = 0x28 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved
5-4	EDGE_CTRL[1:0]	RW	0h	Output slew rate 0h = Auto adjust slew rate based on PVDD range (default) 1h = Reserved 2h = Reserved 3h = Slow slew rate for full range of PVDDH
3-0	Reserved	R	0h	Reserved

8.9.74 Page = 0x01 Address = 0x35 [Reset = 75h]

Bit	Field	Type	Reset	Description
7-2	Reserved	R	1Dh	Reserved
1-0	BIAS_NOISE[1:0]	RW	1h	Settings for noise improvement

8.9.75 Page = 0x01 Address = 0x36 [Reset = 08h]

Bit	Field	Type	Reset	Description
7-6	INT_LDO[1:0	RW	0h	Internal LDO Setting 0h = User can program device with bit PVDDL_MODE, register 0x04, page 0x00 (default) 1h = Use external PVDDL 2h = Use internal LDO for PVDDL supply 3h = Reserved
5-0	Reserved	R	08h	Reserved

8.9.76 Page = 0x01 Address = 0x3D [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ1[7:0]	RW	00h	Force '0' output control for slots 7 down to 0. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.77 Page = 0x01 Address = 0x3E [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ2[7:0]	RW	00h	Force '0' output control for slots 15 down to 8. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.78 Page = 0x01 Address = 0x3F [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ3[7:0]	RW	00h	Force '0' output control for slots 23 down to 16. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.79 Page = 0x01 Address = 0x40 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ4[7:0]	RW	00h	Force '0' output control for slots 31 down to 24. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.80 Page = 0x01 Address = 0x41 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ5[7:0]	RW	00h	Force '0' output control for slots 39 down to 32. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.81 Page = 0x01 Address = 0x42 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ6[7:0]	RW	00h	Force '0' output control for slots 47 down to 40. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.82 Page = 0x01 Address = 0x43 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ7[7:0]	RW	00h	Force '0' output control for slots 55 down to 48. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.83 Page = 0x01 Address = 0x44 [Reset = 00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ8[7:0]	RW	00h	Force '0' output control for slots 63 down to 56. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.84 Page = 0x01 Address = 0x45 [Reset = 00h]

Bit	Field	Type	Reset	Description
7	SDOUT_FCNT	RW	0h	Control over sending "0" to un-used slots 0h = All un-used slots will have 'Hi-Z' transmitted 1h = Un-used slots transmit '0' as per registers 0x3D - 0x44 settings
6-0	Reserved	R	00h	Reserved

8.9.85 Page = 0x01 Address = 0x47 [Reset = AB]

Bit	Field	Type	Reset	Description
7-2	Reserved	R	2Ah	Reserved
1	TG_TH2	RW	1h	Thermal threshold 2 0h = Disabled 1h = Enabled
0	TG_TH1	RW	1h	Thermal threshold 1 0h = Disabled 1h = Enabled

8.9.86 Page = 0x01 Address = 0x4C [Reset = 00h]

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0h	Reserved
1-0	ADC_FLT[1:0]	RW	0h	PVDDL/PVDDH SAR filter frequency 0h = Disabled (default) 1h = 300 kHz 2h = 150 kHz 3h = 50 kHz

8.9.87 Page = 0x04 Address = 0x08 - 0x0B [Reset = 034A516Ch]

Bit	Field	Type	Reset	Description
31-0	DVC_SLEW[31:0]	RW	034A516Ch	Sets slew rate for volume control to a SR(s) value: dec2hex(round {(1-exp[-1/(0.2*fs*SR)])*2^31}) Default SR = 28 µs.

8.9.88 Page = 0x04 Address = 0x10 - 0x13 [Reset = 34000000h]

Bit	Field	Type	Reset	Description
31-0	LIM_MAX_TH[31:0]	RW	34000000h	Sets limiter maximum threshold to a MAX_TH(V) value: dec2hex[round(MAX_TH*2^26)] Default MAX_TH = 13 V.

8.9.89 Page = 0x04 Address = 0x14 - 0x17 [Reset = 14000000h]

Bit	Field	Type	Reset	Description
31-0	LIM_MIN_TH[31:0]	RW	14000000h	Sets limiter minimum threshold to a MIN_TH(V) value: dec2hex[round(MIN_TH*2^26)] Default MIN_TH = 5 V.

8.9.90 Page = 0x04 Address = 0x18 - 0x1B [Reset = 0D333333h]

Bit	Field	Type	Reset	Description
31-0	LIM_INF[31:0]	RW	0D333333h	Sets limiter inflection point to a INF(V) value: dec2hex[round(INF*2^26)] Default INF = 3.3 V.

8.9.91 Page = 0x04 Address = 0x1C - 0x1F [Reset = 10000000h]

Bit	Field	Type	Reset	Description
31-0	LIM_SLP[31:0]	RW	10000000h	Sets limiter slope to a SLP(V/V) value: dec2hex[round(SLP*2^28)] Default SLP = 1 V/V.

8.9.92 Page = 0x04 Address = 0x20 - 0x23 [Reset = 0B999999h]

Bit	Field	Type	Reset	Description
31-0	BOP_TH[31:0]	RW	0B999999h	Sets BOP threshold to a BOP_TH(V) value: dec2hex[round(BOP_TH*2^26)] Default BOP_TH= 2.9 V.

8.9.93 Page = 0x04 Address = 0x24 - 0x27 [Reset = 0ACCCCCDh]

Bit	Field	Type	Reset	Description
31-0	BOP_TH[31:0]	RW	0ACCCCCDh	Sets BOP shutdown threshold to a BOPSD_TH(V) value: dec2hex[round(BOPSD_TH*2^26)] Default BOPSD_TH = 2.7 V.

8.9.94 Page = 0x04 Address = 0x40 - 0x43 [Reset = 721482C0h]

Bit	Field	Type	Reset	Description
31-0	TF_SLP[31:0]	RW	721482C0h	Sets thermal foldback limiter slope to a TF_SLP(dB/ºC) value: dec2hex[round((10^TF_SLP/20)*2^31)] Default TF_SLP = -1 dB/ºC.

8.9.95 Page = 0x04 Address = 0x44 - 0x47 [Reset = 00000258h]

Bit	Field	Type	Reset	Description
31-0	TF_HLD[31:0]	RW	00000258h	Sets thermal foldback limiter hold count to a TF_HLD(s) value: dec2hex[round(TF_HLD*f_s/8)], $f_s \leq 48$ kHz dec2hex[round(TF_HLD*6000)], $f_s > 48$ kHz

8.9.96 Page = 0x04 Address = 0x48 - 0x4B [Reset = 40BDB7C0h]

Bit	Field	Type	Reset	Description
31-0	TF_RLS[31:0]	RW	40BDB7C0h	Sets thermal foldback limiter release rate to a TF_RLS(dB/sample) value: dec2hex[round(10^(8*TF_RLS/20)*2^30)], $f_s \leq 48$ kHz dec2hex[round(10^(16*TF_RLS/20)*2^30)], $f_s > 48$ kHz

8.9.97 Page = 0x04 Address = 0x4C - 0x4F [Reset = 3982607Fh]

Bit	Field	Type	Reset	Description
31-0	TF_TMP_TH[31:0]	RW	3982607Fh	Sets thermal foldback limiter temperature threshold to a TF_TH(ºC) value: dec2hex[round(TF_TH*2^23)] Default TF_TH = 115 ºC.

8.9.98 Page = 0x04 Address = 0x50 - 0x53 [Reset = 2D6A866Fh]

Bit	Field	Type	Reset	Description
31-0	TF_MAX_ATN[31:0]	RW	2D6A866Fh	Sets thermal foldback limiter maximum gain reduction to a TF_MAXA(dB) value: dec2hex[round(10^(TF_MAXA/20)*2^31)] Default TF_MAXA= - 9 dB.

8.9.99 Page = 0x04 Address = 0x54 - 0x57 [Reset = 7C5E4E02h]

Bit	Field	Type	Reset	Description
31-0	TF_ATK[31:0]	RW	7C5E4E02h	Sets thermal foldback limiter attack rate to a TF_ATK(dB/sample) value: dec2hex[round(10^(8*TF_ATK/20)*2^31)], $f_s \leq 48$ kHz dec2hex[round(10^(16*TF_ATK/20)*2^31)], $f_s > 48$ kHz

8.9.100 Page = 0x05 Address = 0x14 - 0x17 [Reset = 6CCCCCCCh]

Bit	Field	Type	Reset	Description
31-0	CLASSD_EFF[31:0]	RW	6CCCCCCCh	Class-D Efficiencyset to an EFF(%) value: dec2hex[round (EFF*2^31)]

8.9.101 Page = 0x05 Address = 0x1C - 0x1F [Reset = 4CCCCCCh]

Bit	Field	Type	Reset	Description
31-0	INF_FCT[31:0]	RW	4CCCCCCh	Inflation factor for Low Voltage Signaling set to IF: dec2hex[round(IF*2^30)]

8.9.102 Page = 0x05 Address = 0x20 - 0x23 [Reset = 00000180h]

Bit	Field	Type	Reset	Description
31-0	MAX_HLD_CLH[31:0]	RW	00000180h	Sets hold time of Class-H to HT (s): dec2hex[round(HT*f_s)] , $f_s \leq 48$ksps dec2hex[round(HT*48kHz)] , $f_s > 48$ksps

8.9.103 Page = 0x05 Address = 0x24 - 0x27 [Reset = 00000000h]

Bit	Field	Type	Reset	Description
31-0	RLS_WD[31:0]	RW	00000000h	Sets release window time of Class-H to RWT (s), when back door is enabled (Section 8.9.125): dec2hex[round(RWT*f_s)] , $f_s \leq 48$ksps dec2hex[round(RWT*48kHz)] , $f_s > 48$ksps

8.9.104 Page = 0x05 Address = 0x28 - 0x2B [Reset = 79999999h]

Bit	Field	Type	Reset	Description
31-0	PHVD[31:0]	RW	79999999h	Sets Class-H peak hold value decay to PHV (decay rate/sample): dec2hex[round(PHV*2^31)]

8.9.105 Page = 0x05 Address = 0x2C - 0x2F [Reset = 0538EF34h]

Bit	Field	Type	Reset	Description
31-0	AL_SMTH[31:0]	RW	0538EF34h	Class-H configuration time constant AS (s): dec2hex[round([1-exp(-1/AS*f_s)]*2^31)] , $f_s \leq 48$ksps dec2hex[round([1-exp(-1/AS*48 kHz)]*2^31)] , $f_s > 48$ksps

8.9.106 Page = 0x05 Address = 0x30 - 0x33 [Reset = 40000000h]

Bit	Field	Type	Reset	Description
31-0	NF_FCT_H[31:0]	RW	40000000h	Inflation factor Class-H set to IF: dec2hex[round(IF*2^30)]

8.9.107 Page = 0x05 Address = 0x34 - 0x37 [Reset = 65AC8C2Fh]

Bit	Field	Type	Reset	Description
31-0	CLH_ST1[31:0]	RW	65AC8C2Fh	Class-H step level 1 set to ST1: dec2hex[round(ST1*2^31)] ST1 = margin*(Vm + (15/16)*(VM-Vm))/15.8489 where: VM = maximum boost output Vm = minimum boost output margin = Class-D efficiency

8.9.108 Page = 0x05 Address = 0x38 - 0x3B [Reset = 50C335D3h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST2[31:0]	RW	50C335D3h	Class-H step level 2 set to ST2: dec2hex[round(ST2*2^31)] ST2 = margin*(Vm + (14/16)*(VM-Vm))/15.8489

8.9.109 Page = 0x05 Address = 0x3C - 0x3F [Reset = 4026E73Ch]

Bit	Field	Type	Reset	Description
31-0	CLH_ST3[31:0]	RW	4026E73Ch	Class-H step level 3 set to ST3: dec2hex[round(ST3*2^31)] ST3 = margin*(Vm + (13/16)*(VM-Vm))/15.8489

8.9.110 Page = 0x05 Address = 0x40 - 0x43 [Reset = 32F52CFEh]

Bit	Field	Type	Reset	Description
31-0	CLH_ST4[31:0]	RW	32F52CFEh	Class-H step level 4 set to ST4: dec2hex[round(ST4*2^31)] ST4 = margin*(Vm + (12/16)*(VM-Vm))/15.8489

8.9.111 Page = 0x05 Address = 0x44 - 0x47 [Reset = 287A26C4h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST5[31:0]	RW	287A26C4h	Class-H step level 5 set to ST5: dec2hex[round(ST5*2^31)] ST5 = margin*(Vm + (11/16)*(VM-Vm))/15.8489

8.9.112 Page = 0x05 Address = 0x48 - 0x4B [Reset = 2026F30Fh]

Bit	Field	Type	Reset	Description
31-0	CLH_ST6[31:0]	RW	2026F30Fh	Class-H step level 6 set to ST6: dec2hex[round(ST6*2^31)] ST6 = margin*(Vm + (10/16)*(VM-Vm))/15.8489

8.9.113 Page = 0x05 Address = 0x4C - 0x4F [Reset = 198A1357h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST7[31:0]	RW	198A1357h	Class-H step level 7 set to ST7: dec2hex[round(ST7*2^31)] ST7 = margin*(Vm + (9/16)*(VM-Vm))/15.8489

8.9.114 Page = 0x05 Address = 0x50 - 0x53 [Reset = 144960C5h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST8[31:0]	RW	144960C5h	Class-H step level 8 set to ST8: dec2hex[round(ST8*2^31)] ST8 = margin*(Vm + (8/16)*(VM-Vm))/15.8489

8.9.115 Page = 0x05 Address = 0x54 - 0x57 [Reset = 101D3F2Dh]

Bit	Field	Type	Reset	Description
31-0	CLH_ST9[31:0]	RW	101D3F2Dh	Class-H step level 9 set to ST9: dec2hex[round(ST9*2^31)] ST9 = margin*(Vm + (7/16)*(VM-Vm))/15.8489

8.9.116 Page = 0x05 Address = 0x58 - 0x5B [Reset = 0CCCCCCCh]

Bit	Field	Type	Reset	Description
31-0	CLH_ST10[31:0]	RW	0CCCCCCCh	Class-H step level 10 set to ST10: dec2hex[round(ST10*2^31)] ST10 = margin*(Vm + (6/16)*(VM-Vm))/15.8489

8.9.117 Page = 0x05 Address = 0x5C - 0x5F [Reset = 0A2AADD1h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST11[31:0]	RW	0A2AADD1h	Class-H step level 11 set to ST11: dec2hex[round(ST11*2^31)] ST11 = margin*(Vm + (5/16)*(VM-Vm))/15.8489

8.9.118 Page = 0x05 Address = 0x60 - 0x63 [Reset = 08138561h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST12[31:0]	RW	08138561h	Class-H step level 12 set to ST12: dec2hex[round(ST12*2^31)] ST12 = margin*(Vm + (4/16)*(VM-Vm))/15.8489

8.9.119 Page = 0x05 Address = 0x64 - 0x67 [Reset = 081385615h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST13[31:0]	RW	081385615h	Class-H step level 13 set to ST13: dec2hex[round(ST13*2^31)] ST13 = margin*(Vm + (3/16)*(VM-Vm))/15.8489

8.9.120 Page = 0x05 Address = 0x68 - 0x6B [Reset = 08138561h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST14[31:0]	RW	08138561h	Class-H step level 14 set to ST14: dec2hex[round(ST14*2^31)] ST14 = margin*(Vm + (2/16)*(VM-Vm))/15.8489

8.9.121 Page = 0x05 Address = 0x6C - 0x6F [Reset = 08138561h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST15[31:0]	RW	08138561h	Class-H step level 15 set to ST15: dec2hex[round(ST15*2^31)] ST15 = margin*(Vm + (1/16)*(VM-Vm))/15.8489

8.9.122 Page = 0x05 Address = 0x70 - 0x73 [Reset = 08138561h]

Bit	Field	Type	Reset	Description
31-0	CLH_ST16[31:0]	RW	08138561h	Class-H step level 16 set to ST16: dec2hex[round(ST16*2^31)] ST16 = margin*Vm/15.8489

8.9.123 Page = 0x05 Address = 0x74 - 0x77 [Reset = 000000BFh]

Bit	Field	Type	Reset	Description
31-0	CLH_DLY[31:0]	RW	000000BFh	Class-H delay HDLY (s) dec2hex[round(HDLY*fs) - 1] *Should be less than 4 ms

8.9.124 Page = 0x05 Address = 0x78 - 0x7B [Reset = 0000000Eh]

Bit	Field	Type	Reset	Description
31-0	LVSPR_DLY[31:0]	RW	0000000Eh	Sets LVS Delay to LVDL(s) dec2hex[round(LVDL* 96k) -1], range: 0 -15, for f_s = 48 kHz/96 kHz round(LVDL* 2*f_s) -1, range: 0 -15, for f_s < 48k

8.9.125 Page = 0x05 Address = 0x7C - 0x7F [Reset = 66676869h]

Bit	Field	Type	Reset	Description
31-0	BKD_EN[31:0]	RW	66676869h	Back door is enabled for any non-zero value

8.9.126 Page = 0x06 Address = 0x08 - 0x0B [Reset = 00000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_01[31:0]	RW	00000000h	8 step Class-H duty cycle is 0 %

8.9.127 Page = 0x06 Address = 0x0C - 0x0F [Reset = 80800000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_02[31:0]	RW	80800000h	8 step Class-H duty cycle is 12.5 %

8.9.128 Page = 0x06 Address = 0x10 - 0x13 [Reset = C0C00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_03[31:0]	RW	C0C00000h	8 step Class-H duty cycle is 25 %

8.9.129 Page = 0x06 Address = 0x14 - 0x17 [Reset = E0E00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_04[31:0]	RW	E0E00000h	8 step Class-H duty cycle is 37.5 %

8.9.130 Page = 0x06 Address = 0x18 - 0x1B [Reset = F0F00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_05[31:0]	RW	F0F00000h	8 step Class-H duty cycle is 50 %

8.9.131 Page = 0x06 Address = 0x1C - 0x1F [Reset = F8F80000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_06[31:0]	RW	F8F80000h	8 step Class-H duty cycle is 62.5 %

8.9.132 Page = 0x06 Address = 0x20 - 0x23 [Reset = FCFC0000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_07[31:0]	RW	FCFC0000h	8 step Class-H duty cycle is 75 %

8.9.133 Page = 0x06 Address = 0x24 - 0x27 [Reset = FCFC0000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_08[31:0]	RW	FCFC0000h	8 step Class-H duty cycle is 75 % For 87.5 % set registers to FEFE0000h

8.9.134 Page = 0x06 Address = 0x28 - 0x2B [Reset = FCFC0000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_09[31:0]	RW	FCFC0000h	8 step Class-H duty cycle is 75 % For 100 % set registers to FFFF0000h

8.9.135 Page = 0x06 Address = 0x2C - 0x2F [Reset = 00000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_01[31:0]	RW	00000000h	16 step Class-H duty cycle is 0 %

8.9.136 Page = 0x06 Address = 0x30 - 0x33 [Reset = 80000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_02[31:0]	RW	80000000h	16 step Class-H duty cycle is 6.25 %

8.9.137 Page = 0x06 Address = 0x34 - 0x37 [Reset = C0000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_03[31:0]	RW	C0000000h	16 step Class-H duty cycle is 12.5 %

8.9.138 Page = 0x06 Address = 0x38 - 0x3B [Reset = E0000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_08_04[31:0]	RW	E0000000h	16 step Class-H duty cycle is 18.75 %

8.9.139 Page = 0x06 Address = 0x3C - 0x3F [Reset = F0000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_05[31:0]	RW	F0000000h	16 step Class-H duty cycle is 25 %

8.9.140 Page = 0x06 Address = 0x40 - 0x43 [Reset = F8000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_06[31:0]	RW	F8000000h	16 step Class-H duty cycle is 31.25 %

8.9.141 Page = 0x06 Address = 0x44 - 0x47 [Reset = FC000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_07[31:0]	RW	FC000000h	16 step Class-H duty cycle is 37.5 %

8.9.142 Page = 0x06 Address = 0x48 - 0x4B [Reset = FE000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_08[31:0]	RW	FE000000h	16 step Class-H duty cycle is 43.75 %

8.9.143 Page = 0x06 Address = 0x4C - 0x4F [Reset = FF000000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_09[31:0]	RW	FF000000h	16 step Class-H duty cycle is 50 %

8.9.144 Page = 0x06 Address = 0x50 - 0x53 [Reset = FF800000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_10[31:0]	RW	FF800000h	16 step Class-H duty cycle is 56.25 %

8.9.145 Page = 0x06 Address = 0x54 - 0x57 [Reset = FFC00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_11[31:0]	RW	FFC00000h	16 step Class-H duty cycle is 62.5 %

8.9.146 Page = 0x06 Address = 0x58 - 0x5B [Reset = FFE00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_12[31:0]	RW	FFE00000h	16 step Class-H duty cycle is 68.75 %

8.9.147 Page = 0x06 Address = 0x5C - 0x5F [Reset = FFF00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_13[31:0]	RW	FFF00000h	16 step Class-H duty cycle is 75 %

8.9.148 Page = 0x06 Address = 0x60 - 0x63 [Reset = FFF00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_14[31:0]	RW	FFF00000h	16 step Class-H duty cycle is 75 % For 81.25 % set registers to FF800000h

8.9.149 Page = 0x06 Address = 0x64 - 0x67 [Reset = FFF00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_15[31:0]	RW	FFF00000h	16 step Class-H duty cycle is 75 % For 87.5 % set registers to FFFC0000h

8.9.150 Page = 0x06 Address = 0x68 - 0x6B [Reset = FFF00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_16[31:0]	RW	FFF00000h	16 step Class-H duty cycle is 75 % For 93.75 % set registers to FFFE0000h

8.9.151 Page = 0x06 Address = 0x6C - 0x6F [Reset = FFF00000h]

Bit	Field	Type	Reset	Description
31-0	WVSH_16_17[31:0]	RW	FFF00000h	16 step Class-H duty cycle is 75 % For 100 % set registers to FFFF0000h

8.9.152 Page = 0x08 Address = 0x18 - 0x1B [Reset = 9C000000h]

Bit	Field	Type	Reset	Description
31-0	VOL_CVR[31:0]	RW	9C000000h	Unmute audio channel Write 00 00 00 00 to unmute

8.9.153 Page = 0x08 Address = 0x28 - 0x2B [Reset = 00000000h]

Bit	Field	Type	Reset	Description
31-0	UNMUTE_CVR[31:0]	RW	00000000h	Unmute audio channel Write 40 00 00 00 to unmute

8.9.154 Page = 0x0A Address = 0x48 - 0x4B [Reset = 9C000000h]

Bit	Field	Type	Reset	Description
31-0	VOL_NVR[31:0]	RW	9C000000h	Unmute audio channel Write 00 00 00 00 to unmute

8.9.155 Page = 0x0A Address = 0x58 - 0x5B [Reset = 00000000h]

Bit	Field	Type	Reset	Description
31-0	UNMUTE_NVR[31:0]	RW	00000000h	Unmute audio channel Write 40 00 00 00 to unmute

8.9.156 Page = 0xFD Address = 0x3E [Reset = 4Dh]

Bit	Field	Type	Reset	Description
7-4	Reserved	R	4h	Reserved
3-0	OPT_DMIN[3:0]	RW	Dh	DMIN optimization settings

8.10 SDOUT Equations

The following equations will alow to convert data read on SDOUT.

$$PVDDH\ (V) = 23 * [Hex2Dec(SDOUTdata)]/2^{PVDDH\_SlotLength} \quad (5)$$

By default, PVDDH_SlotLength = 8.

$$PVDDL\ (V) = 8 * [Hex2Dec(SDOUTdata)]/2^{PVDDL\_SlotLength} \quad (6)$$

By default,PVDDL_SlotLength = 8.

$$TEMP\ (^{0}C) = 256 * [Hex2Dec(SDOUTdata)]/2^{TEMP\_SlotLength} - 93 \quad (7)$$

TEMP_SlotLength = 8.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TAS2781 is a digital input Class-D audio power amplifier with integrated DSP supporting Texas Instruments Smart Amp algorithm for speaker protection. I^2S audio data is supplied by host processor. I^2C or SPI bus is used for configuration and control. The Hybrid-Pro controller for an external boost converter allows efficiency improvement.

9.2 Typical Application

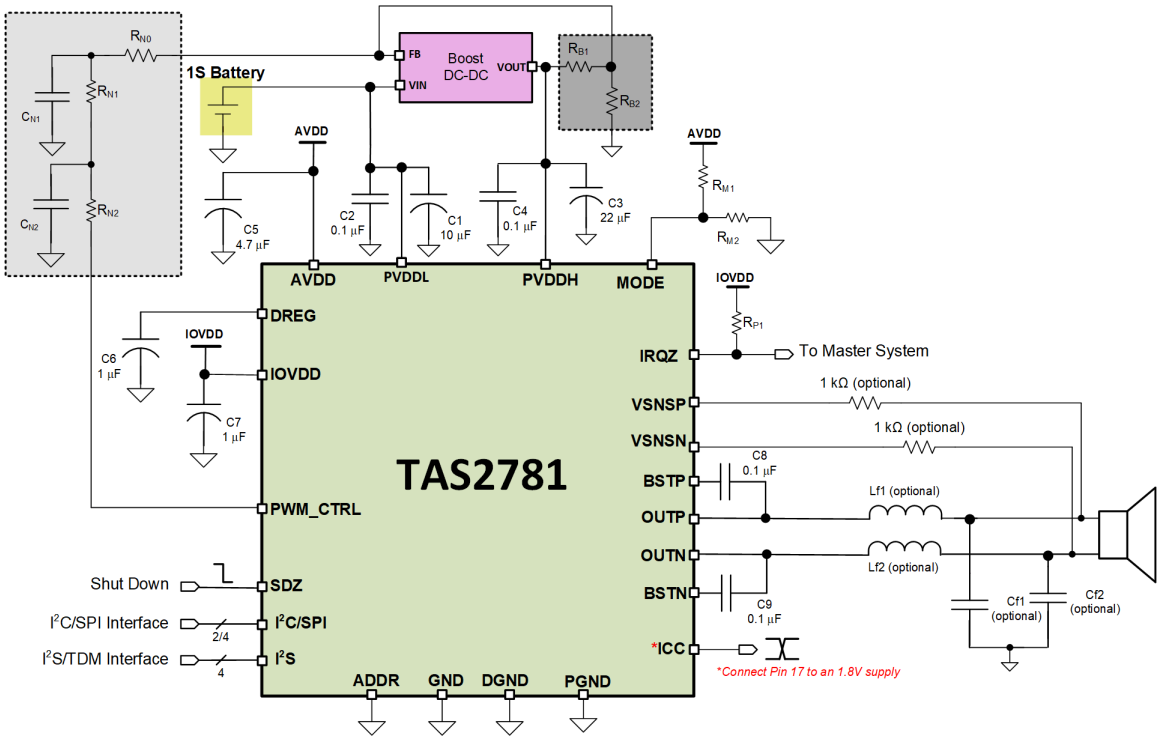


Figure 9-1. Typical Application - 1S Battery Supply and External Boost Control

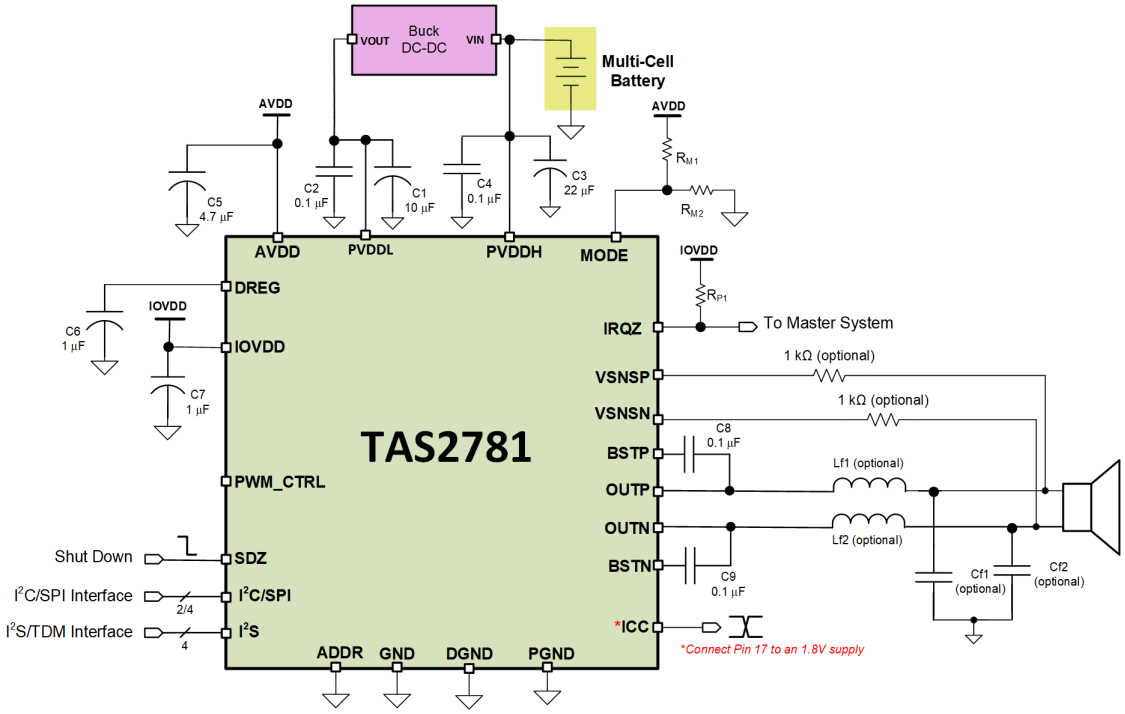


Figure 9-2. Typical Application - Multi-Cell Battery Supply

Table 9-1. Recommended External Components

COMPONENT	DESCRIPTION	SPECIFICATION	MIN	TYP	MAX	UNIT
C1	PVDDL Decoupling Capacitor - PVDDL External Supply (PWR_MODE0/1/3)	Type	X7R			
		Capacitance, 20% Tolerance		10		µF
		Rated Voltage		10		V
	PVDDL Decoupling Capacitor - PVDDL Internally Generated (PWR_MODE2)	Type	X7R			
		Capacitance, 20% Tolerance	0.68	1		µF
		Rated Voltage		10		V
C2	PVDDL Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance		100		nF
		Rated Voltage		10		V
C3	PVDDH Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance	22			µF
		Rated Voltage	30			V
C4	PVDDH Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance		100		nF
		Rated Voltage	30			V
C5	AVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance *AVDD=1.8V, IOVDD=3.3V*	4.7			µF
		Capacitance, 20% Tolerance *AVDD=1.8V and tied to IOVDD*	6.8			
		Rated Voltage	6			V
C6	DREG Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance		1		µF
		Rated Voltage	6			V
C7	IOVDD Decoupling Capacitor *IOVDD=3.3V and not connected to AVDD*	Type	X7R			
		Capacitance, 20% Tolerance		1		µF
		Rated Voltage	6			V

Table 9-1. Recommended External Components (continued)

COMPONENT	DESCRIPTION	SPECIFICATION	MIN	TYP	MAX	UNIT
C8, C9	Bootstrap Capacitors	Type	X7R			
		Capacitance, 20% Tolerance		100		nF
		Rated Voltage	6			V
Lf1, Lf2 (optional)	EMI filter inductors are optional. TAS2781 device support filter less Class-D operation. PFFB feature is recommended if ferrite bead EMI filters are used	Impedance at 100MHz		120		Ω
		DC Resistance			0.095	Ω
		DC Current	7			A
Cf1, Cf2 (optional)	EMI filter capacitors are optional. Design must use Lf2, Lf3 if Cf1, Cf2 are used	Capacitance		1		nF

9.3 Design Requirements

For this design example, use the parameters shown in Section 9.2.

Table 9-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Audio Input	Digital Audio, I^2S
Current and Voltage Data Stream	Digital Audio, I^2S
Mono or Stereo Configuration	Mono
Max Output Power at 1% THD+N, R_L = 4 Ω	25 W

9.4 Detailed Design Procedure

9.4.1 Mono/Stereo Configuration

In applications the device is assumed to be operating in mono mode. See *Section 8.3.2* for information on changing the I^2C address of the TAS2781 to support stereo operation. Mono or stereo configuration does not impact the device performance.

9.4.2 EMI Passive Devices

The TAS2781 supports spread spectrum to minimize EMI. It is allowed to include passive devices on the Class-D outputs. The passive devices (LC filter) have to be properly selected to maintain the stability of the output stage. See Section 8.4.5 for details.

9.5 Application Curves

At T_A = 25 °C, f_{SPK_AMP} = 384 kHz, input signal f_{IN} = 1 kHz - Sine, Load = 4 Ω + 15 µH, unless otherwise noted.

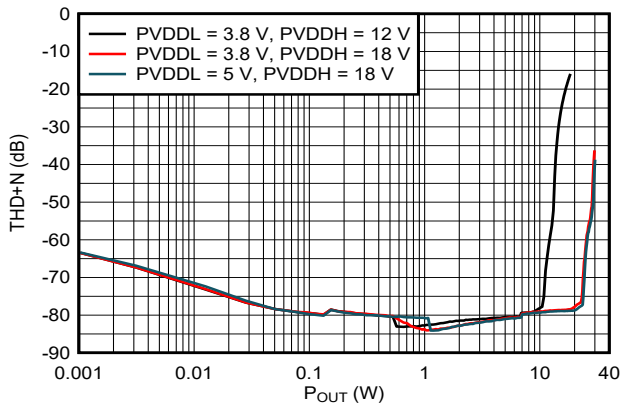


Figure 9-3. THD+N vs Output Power

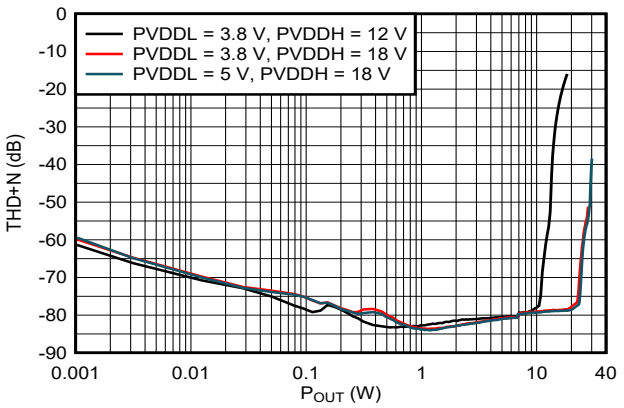


Figure 9-4. THD+N vs Output Power

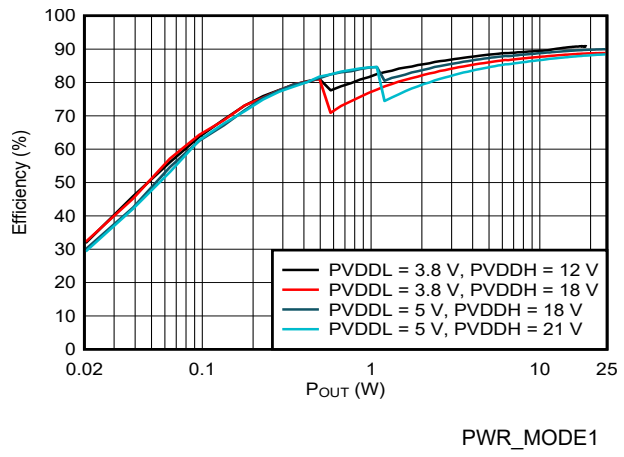


Figure 9-5. Efficiency vs Output Power

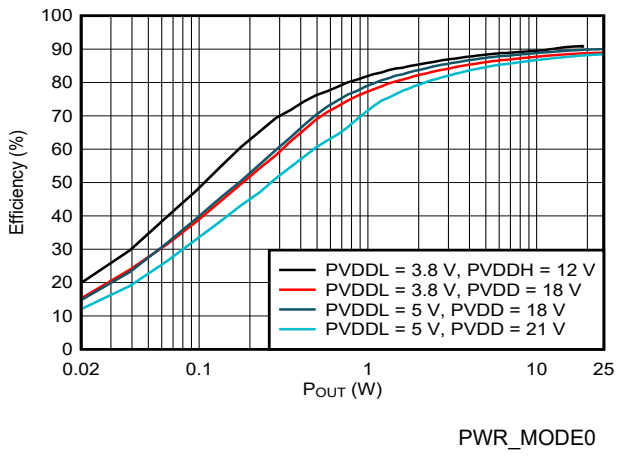


Figure 9-6. Efficiency vs Output Power

10 Initialization Set Up

10.1 Initial Device Configuration - Power Up and Software Reset

The following I²C sequence needs to be used:

- At power up, when SDZ = 1 (out of Hardware Shutdown into Software Shutdown);
- when device is in Software Shutdown or Active mode and user runs a Software Reset command: bit[0] of register 0x01 = 1.

```
###### Pre-Reset Configuration
w 70 00 01 #Page 0x01
w 70 37 3A #Bypass

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access page
w 70 06 C1 #Set Dmin

w 70 00 01 #Page 0x01
w 70 19 E0 #Force modulation
w 70 00 FD #Page 0xFD
w 70 0D 0D #Access page
w 70 06 D5 #Set Dmin

###### Software Reset
w 70 00 00 #Page 0x00
w 70 7F 00 #Book 0x00
w 70 01 01 #Software Reset
d 01 #1 ms Delay

###### Post-Reset Configuration
w 70 00 01 #Page 0x01
w 70 37 3A #Bypass

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access page
w 70 06 C1 #Set Dmin
w 70 06 D5 #Set Dmin
```

10.2 Initial Device Configuration - PWR_MODE0

The following I²C sequence is an example of initializing the device in PWR_MODE0.

```
w 70 00 00 #Page 0x00
w 70 0E C4 #TDM TX vsns transmit enable with slot 4
w 70 0F 40 #TDM TX isns transmit enable with slot 0

w 70 00 01 #Page 0x01
w 70 17 C8 #SARBurstMask=0
w 70 19 20 #LSR Mode
w 70 35 74 #DC noise minimized

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access Page
w 70 3E 4A #Optimal Dmin
w 70 0D 00 #Remove access

w 70 00 04 #Page 0x04
w 70 30 00 00 00 01 #Merge Limiter and Thermal Foldback gains

w 70 00 08 #Page 0x08
w 70 18 00 00 00 00 #0dB volume
w 70 28 40 00 00 00 #Unmute

w 70 00 0A #Page 0x0A
w 70 48 00 00 00 00 #0dB volume
w 70 58 40 00 00 00 #Unmute

w 70 00 00 #Page 0x00
w 70 03 A8 #PWR_MODE0 selected
w 70 71 03 #PVDDH UVLO set to 2.76V
w 70 02 80 #Play audio, power up with playback, IV enabled
```

10.3 Initial Device Configuration - PWR_MODE1

The following I²C sequence is an example of initializing the device in PWR_MODE1.

```
w 70 00 00 #Page 0x00
w 70 0E C4 #TDM TX vsns transmit enable with slot 4
w 70 0F 40 #TDM TX isns transmit enable with slot 0

w 70 00 01 #Page 0x01
w 70 17 C8 #SARBurstMask=0
w 70 35 74 #DC noise minimized
w 70 19 20 #LSR Mode

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access Page 0xFD
w 70 3E 4A #Optimal Dmin
w 70 0D 00 #Remove access Page 0xFD

w 70 00 04 #Page 0x04
w 70 30 00 00 00 01 #Merge Limiter and Thermal Foldback gains

w 70 00 08 #Page 0x08
w 70 18 00 00 00 00 #0dB volume
w 70 28 40 00 00 00 #Unmute

w 70 00 0A #Page 0x0A
w 70 48 00 00 00 00 #0dB volume
w 70 58 40 00 00 00 #Unmute

w 70 00 00 #Page 0x00
w 70 02 00 #Play audio, power up with playback, IV enabled
```

10.4 Initial Device Configuration - PWR_MODE2

The following I²C sequence is an example of initializing the device in PWR_MODE2.

```
w 70 00 00 #Page 0x00
w 70 0E C4 #TDM TX vsns transmit enable with slot 4
w 70 0F 40 #TDM TX isns transmit enable with slot 0

w 70 00 01 #Page 0x01
w 70 17 C0 #SARBurstMask=0
w 70 19 20 #LSR Mode
w 70 35 74 #DC noise minimized

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access Page 0xFD
w 70 3E 4A #Optimal Dmin
w 70 0D 00 #Remove access Page 0xFD

w 70 00 04 #Page 0x04
w 70 30 00 00 00 01 #Merge Limiter and Thermal Foldback gains

w 70 00 08 #Page 0x08
w 70 18 00 00 00 00 #0dB volume
w 70 28 40 00 00 00 #Unmute

w 70 00 0A #Page 0x0A
w 70 48 00 00 00 00 #0dB volume
w 70 58 40 00 00 00 #Unmute

w 70 00 00 #Page 0x00
w 70 03 E8 #PWR_MODE2
w 70 04 A1 #Int LDO mode for internal PVDDL
w 70 71 0E #PVDDH UVLO 6.5V
w 70 02 80 #Power up audio playback with I,V enabled
```

10.5 Initial Device Configuration - PWR_MODE3

The following I²C sequence is an example of initializing the device in PWR_MODE3, for ultrasonic applications.

```
w 70 00 00 #Page 0x00
w 70 0E C4 #TDM TX vsns transmit enable with slot 4
w 70 0F 40 #TDM TX isns transmit enable with slot 0

w 70 00 01 #Page 0x01
w 70 17 C8 #SARBurstMask=0
w 70 19 20 #LSR

w 70 00 04 #Page 0x04
w 70 30 00 00 00 01 #Merge Limiter and Thermal Foldback gains

w 70 00 08 #Page 0x08
w 70 18 00 00 00 00 #0dB volume
w 70 28 40 00 00 00 #Unmute

w 70 00 0A #Page 0x0A
w 70 48 00 00 00 00 #0dB volume
w 70 58 40 00 00 00 #Unmute

w 70 00 00 #Page 0x00
w 70 03 68 #PVDDL only mode
w 70 73 E0 #DEM dither disabled
w 70 02 00 #play audio, power up with playback, IV enabled
```

11 Power Supply Recommendations

The power sequence between the supply rails can be applied in any order as long as SDZ pin is held low. Once all supplies are stable the SDZ pin can be set high to initialize the part. After a hardware or software reset additional commands to the device should be delayed for at least 1 ms to allow the OTP memory to load (see section Section 10).

When PVDDL is internally generated (see Section 11.1) it is recommended that the device enters Software Shutdown mode before entering Hardware Shutdown mode. This ensures that PVDDL pin is discharged using the internal 5 kOhms pull down resistor (not present in Hardware Shutdown mode).

11.1 Power Supply Modes

The TAS2781 can operate with both PVDDL and PVDDH as supplies or with only PVDDH or PVDDL as supply. The table below shows different power supply modes of operation depending on the user need.

Table 11-1. Device Configuration and Power Supply Modes

Supply Power Mode	Output Switching Mode	Supply Condition	PVDDL Mode	Device Configurations	Use Case and Device Functionality
PWR_MODE0	High Power on PVDDH	PVDDH>PVDDL	External	PVDDL_MODE=0 CDS_MODE[1:0]=10	PVDDH is the only supply used to deliver output power.
PWR_MODE1	Y Bridge - High Power on PVDDL	PVDDH	External	PVDDL_MODE=0 CDS_MODE[1:0]=00	PVDDL is used to deliver output power based on level and headroom configured. When audio signal crosses a programmed threshold Class-D output is switched over PVDDH.
PWR_MODE2	Y Bridge - Low Power on PVDDL	PVDDH	Internal	PVDDL_MODE=1 CDS_MODE[1:0]=11	PVDDH is the only supply. PVDDL is delivered by an internal LDO and used to supply at signals close to idle channel levels. When audio signal levels crosses -100dBFS (default), Class-D output switches to PVDDH.
PWR_MODE3	PVDDL	PVDDL	External	PVDDL_MODE=0 CDS_MODE[1:0]=01	The device can be forced to work out of a low power rail mode of operation. For example this can be used for a low power ultrasonic chirp when audio is not played.

When PVDDL is external (PWR_MODE0, PWR_MODE1), if PVDDH falls below (PVDDL + 2.5 V) level, the Y-bridge will stop switching between supplies and will remain on the PVDDH supply.

In PWR_MODE2 user needs to ensure that PVDDH supply level is at least 2.5 V above the PVDDL voltage generated internally in order to take advantage of Y bridge mode of operation. To enable voltage protection the under voltage threshold of PVDDH supply should be set above 7.3 V by using register bits *PVDD_UVLO[5:0]*. This will ensure that, with an internally generated PVDDL of 4.8 V, PVDDH supply is at least 2.5 V higher than PVDDL.

12 Layout

12.1 Layout Guidelines

All supply rails should be bypassed by low-ESR ceramic capacitors as shown and described in Section 9.2.

To create a low impedance connection to PGND, DGND and GND and minimize the ground noise, ground planes with multiple conductive epoxy filled vias should be used in layout.

Specific layout design recommendations should be followed for this device:

- Use wide traces for signals that carry high current: PVDDH, PVDDL, PGND, DGND, GND and the speaker OUTP, OUTN.
- PGND pin should be directly connected and shorted to the ground plane.
- DGND pin should be directly connected to the ground plane.
- Connect VSNSP and VSNSN as close as possible to the speaker.
- VSNSP and VSNSN should be connected between the EMI ferrite filter and the speaker if EMI ferrites are used at the outputs.
- VSNSP and VSNSN routing should be separated and shielded from switching signals (interface signals, speaker outputs, bootstrap pins).
- Place bootstrap capacitors as close as possible to the BST pins.
- Place decoupling capacitors of PVDDH and PVDDL as close as possible to the pins (see Section 12.2).

12.2 Layout Example

Figure 12-1 below describes the placement of critical components as assigned in Figure 9-1.

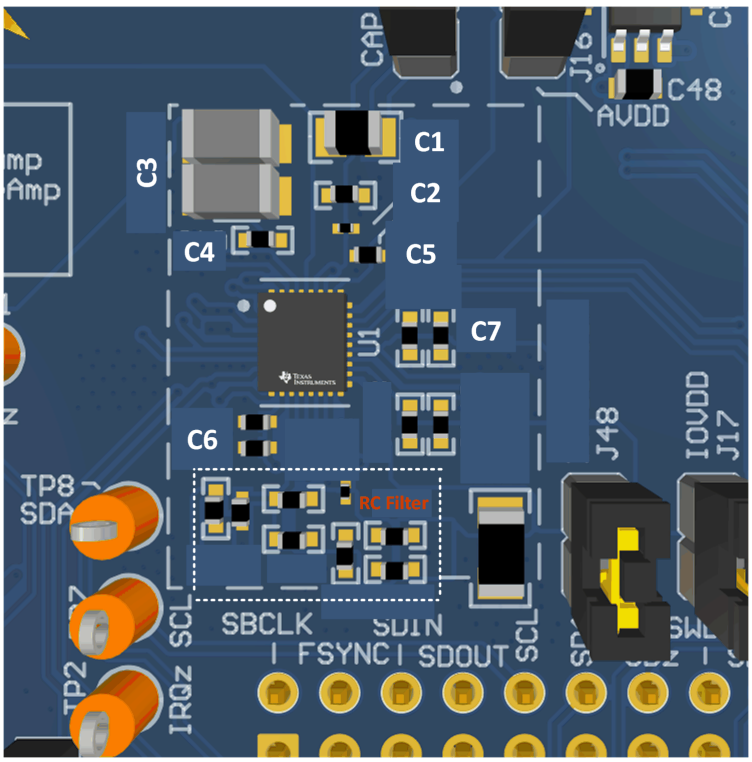


Figure 12-1. Component Placement

An example of layout design is presented in the next two images.

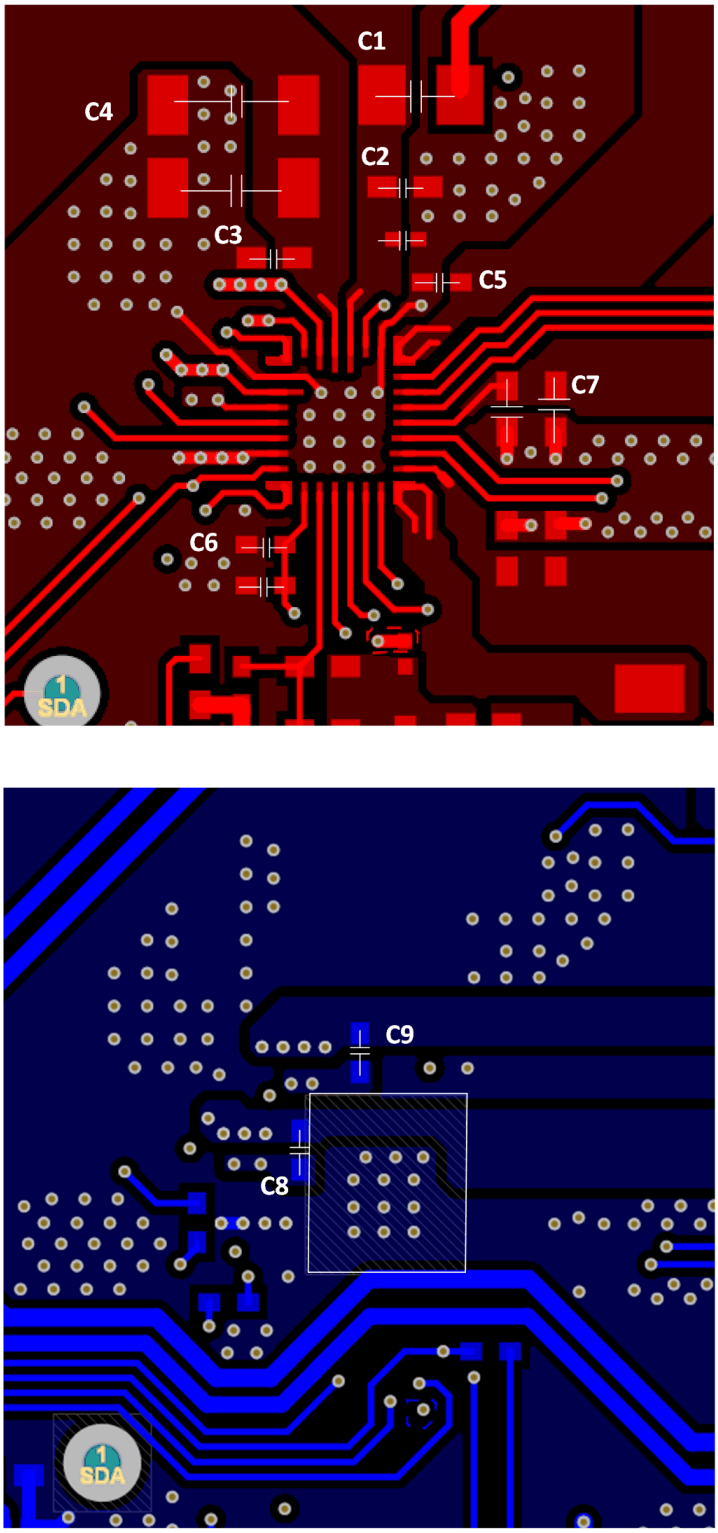


Figure 12-2. Layout Example - Top and Bottom Layers

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

13.3 Trademarks

All trademarks are the property of their respective owners.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

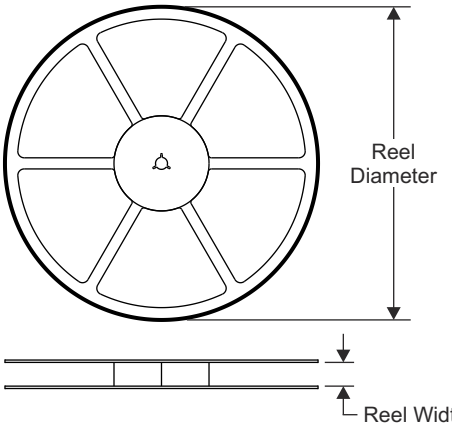
14.1 Package Option Addendum

Packaging Information

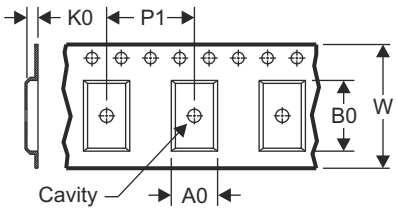
Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4/5)
PTAS2781RYYR	ACTIVE	VQFN-HR	RYY	30	3000	RoHS & Green	NiPdAu	Level-1-260C -UNLIM	-40 to 85	P278-SA
TAS2781RYYR	ACTIVE	VQFN-HR	RYY	30	3000	RoHS & Green	NiPdAu	Level-1-260C -UNLIM	-40 to 85	TAS2781

14.2 Tape and Reel Information

REEL DIMENSIONS

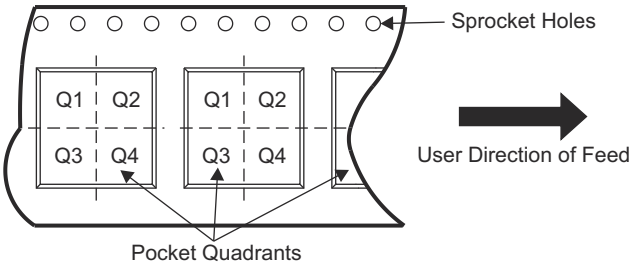


TAPE DIMENSIONS



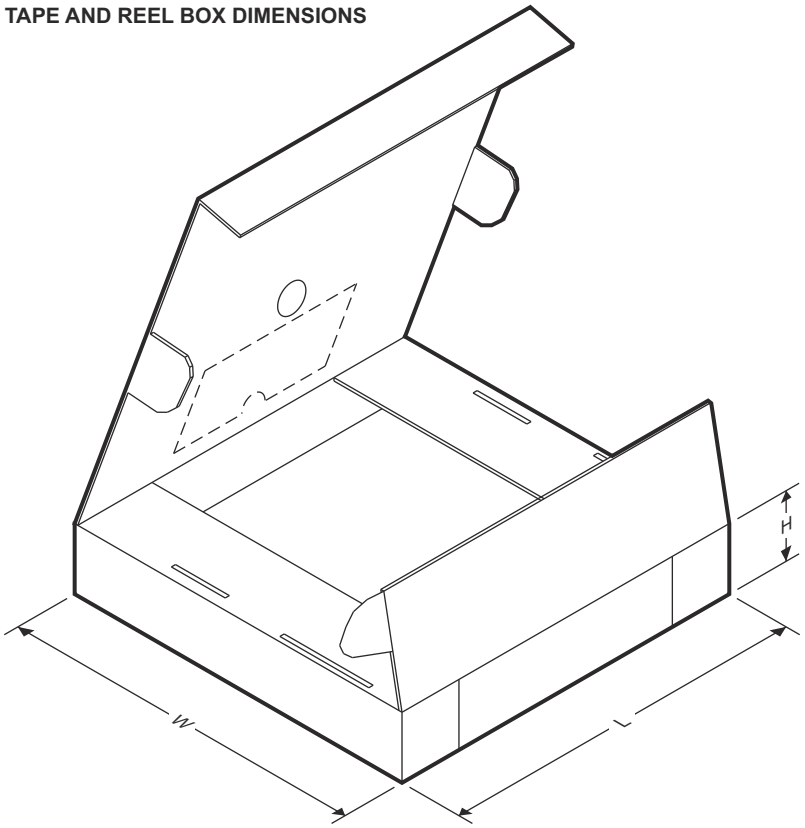
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTAS2781RYYR	VQFN-HR	RYY	30	3000	330	12.4	3.8	4.3	1.5	8	12	Q1
TAS2781RYYR	VQFN-HR	RYY	30	3000	330	12.4	3.8	4.3	1.5	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



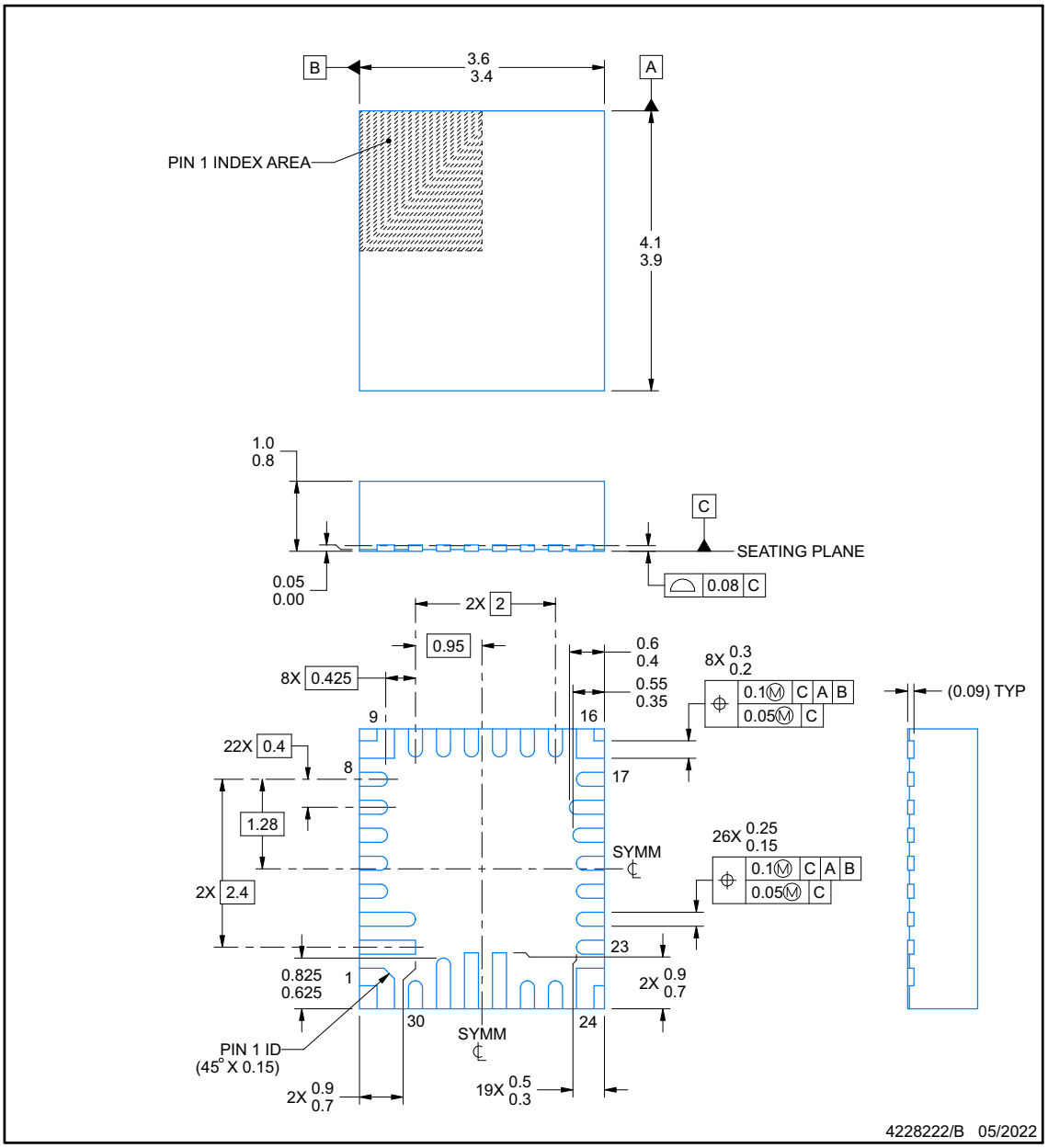
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTAS2781RYYR	VQFN-HR	RYY	30	3000	367	367	35
TAS2781RYYR	VQFN-HR	RYY	30	3000	367	367	35

PACKAGE OUTLINE

RYY0030A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



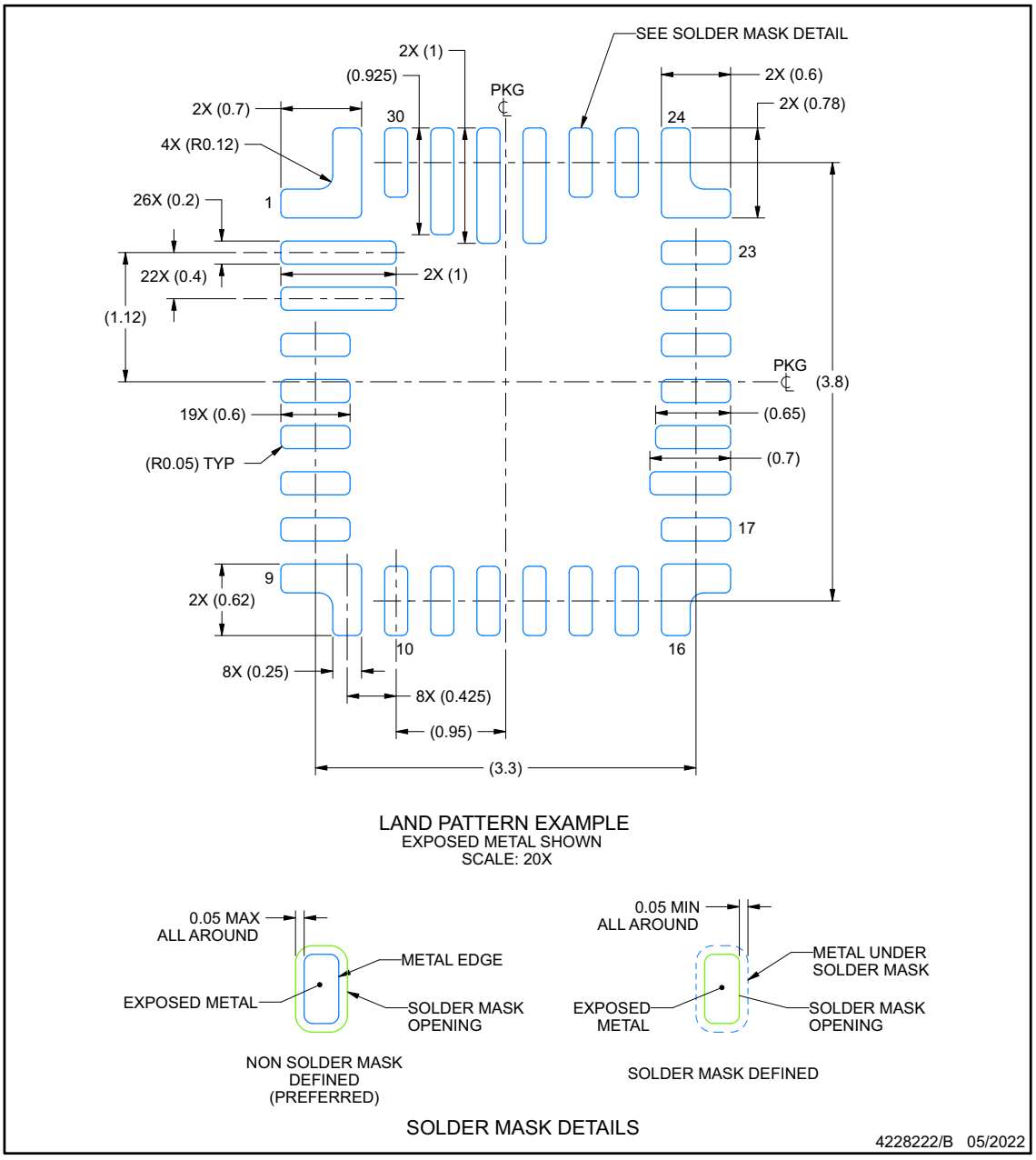
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RYY0030A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

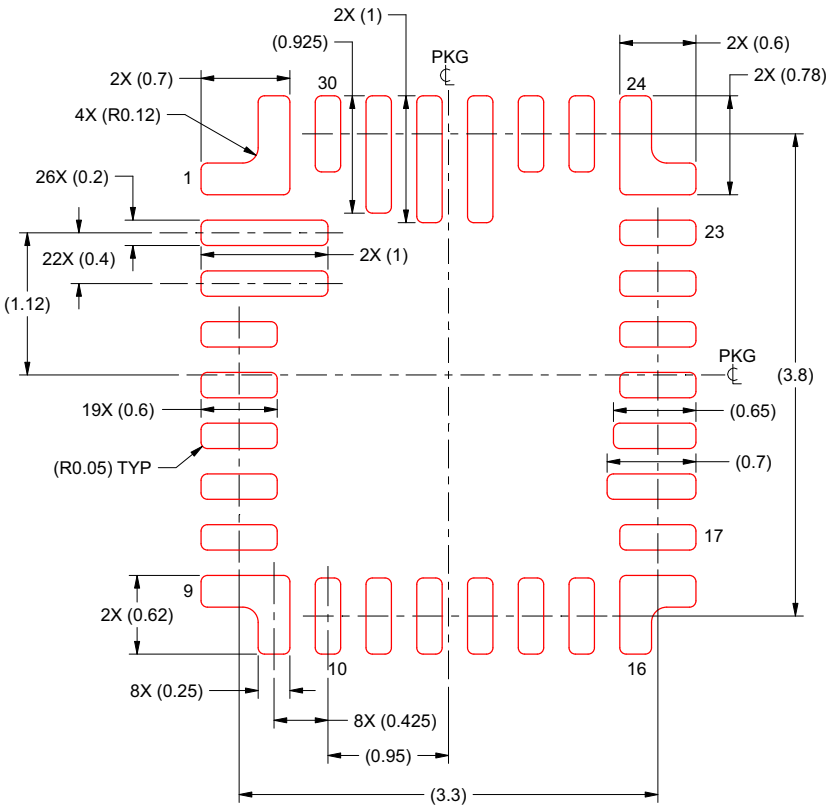
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RYY0030A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS2781RYYR	Active	Production	VQFN-HR (RYY) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TAS2781
TAS2781RYYR.A	Active	Production	VQFN-HR (RYY) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TAS2781

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

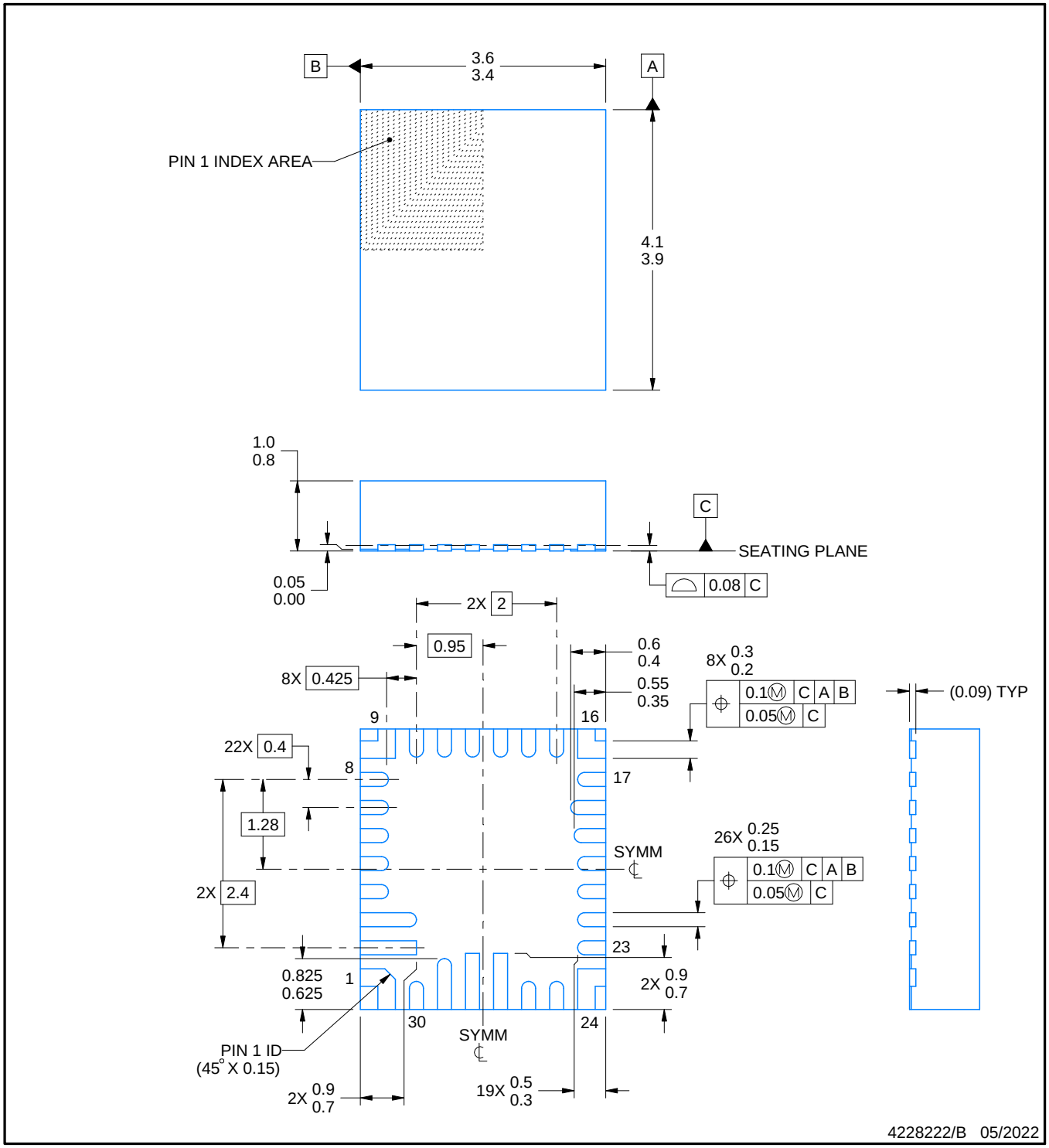
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

RYY0030A

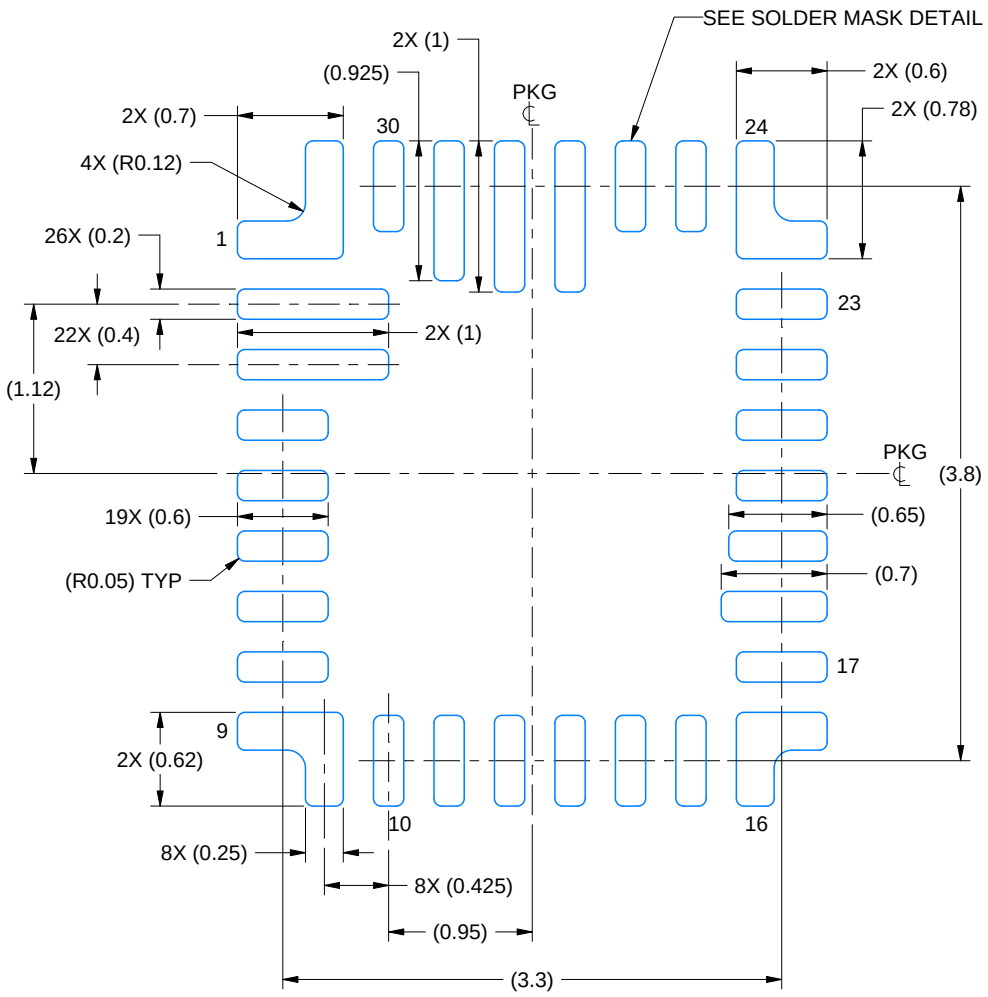
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

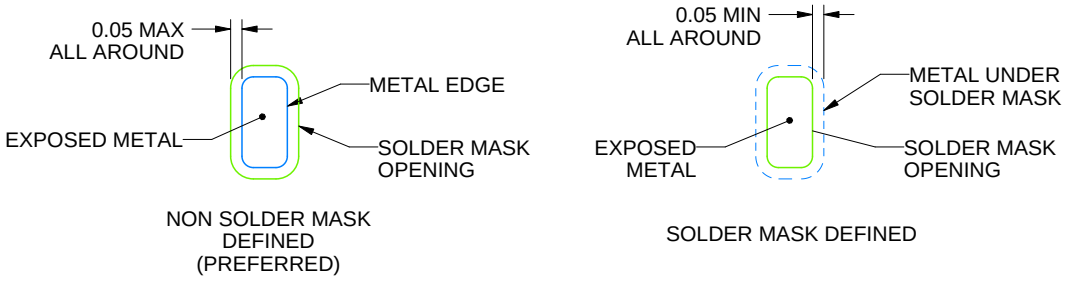


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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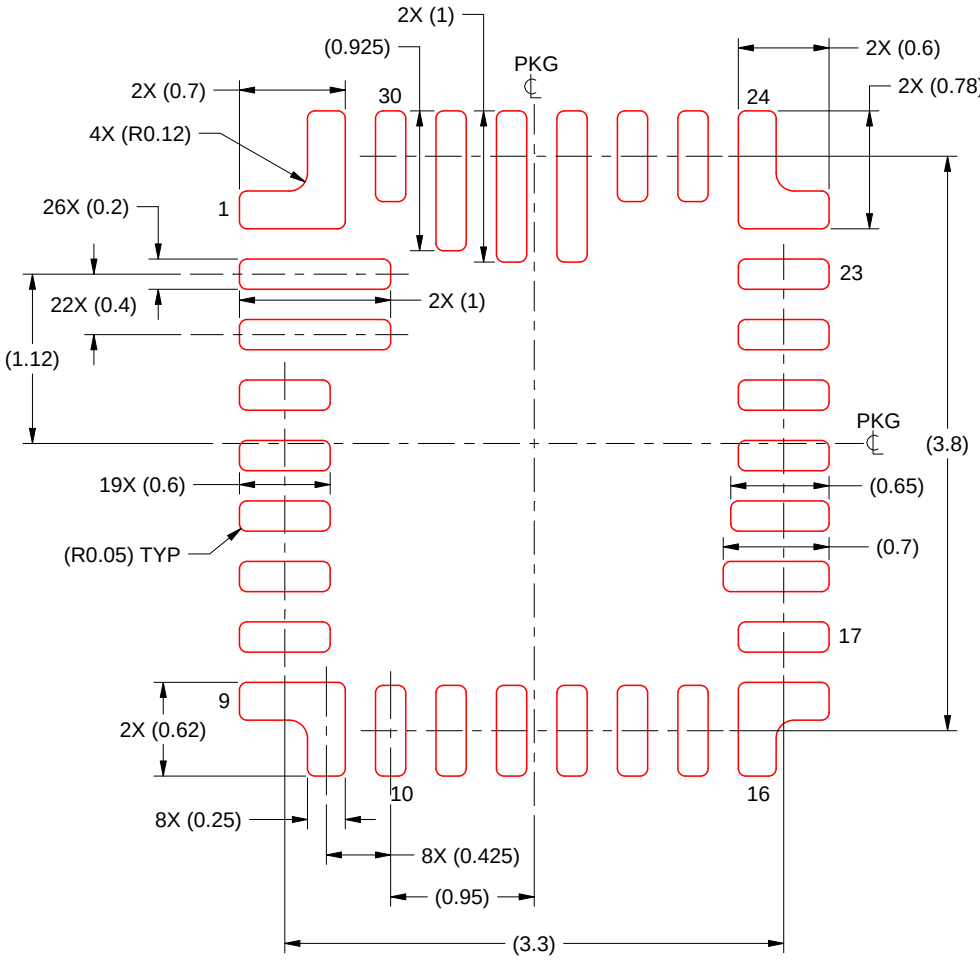
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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