TAS2120 8.2W Mono Digital Input Class-D Speaker Amp with Integrated 14.75V Class-H Boost

1 Features

- Powerful Class-D amplifier
  - 8.2W output power (rms) @1% THD+N
  - 14.75V boost with 5.1A max current limit
- Best-in-class efficiency
  - Up to 91% efficiency @ 1W, 8Ω load
  - 14.7mW idle channel power, noise gate off
  - 5.3mW idle channel power, noise gate on
  - Integrated 1.8V VDD Y-bridge
  - Advanced 33mV step size class-H boost
- High performance audio channel
  - 4.2μV A-wt. idle channel noise
  - 114.4dB Dynamic Range
  - -90dB THD+N
  - Low EMI performance with ERC and SSM
  - < 1μs chip to chip group delay matching
- Advanced integrated features
  - Signal detection high efficiency modes
  - High accuracy supply voltage monitor & temp sensor
  - Programmable battery current limit at 39mA step size
  - Boost sharing between two devices
  - External Class-H Boost control algorithm
- Ease of use features
  - HW pin control or I^2C based control
  - Internal boost or External PVDD supply
  - Clock based power up/down
  - Auto clock rate detection: 16 to 192kHz
  - MCLK free operation
  - Thermal and over current protection
- Power Supplies and user interface
  - VBAT: 2.5V to 5.5V
  - VBAT_SNS: 2.5V to 10.0V
  - VDD: 1.65V to 1.95V
  - IOVDD: 1.8V or 3.3V
  - I^2S/TDM: 8 channels
- 26-Pin, 0.4mm Pitch, QFN package

2 Applications

- Smart Speakers with Voice Assistance
- Bluetooth and Wireless speakers
- Building Automation
- Tablets, Wearables
- Laptop, Desktop Computers

3 Description

The TAS2120 is a mono, digital input Class-D audio amplifier with an integrated Boost for higher power delivery in battery-operated systems.

TAS2120 is optimized to deliver best battery life for real-use cases of music playback and voice calls. Advanced efficiency optimization features like Y-bridge, and other algorithms enable the device to produce best-in-class efficiency across all power regions of operation. The Class-D amplifier is capable of delivering 8.2W output power using integrated Class-H Boost.

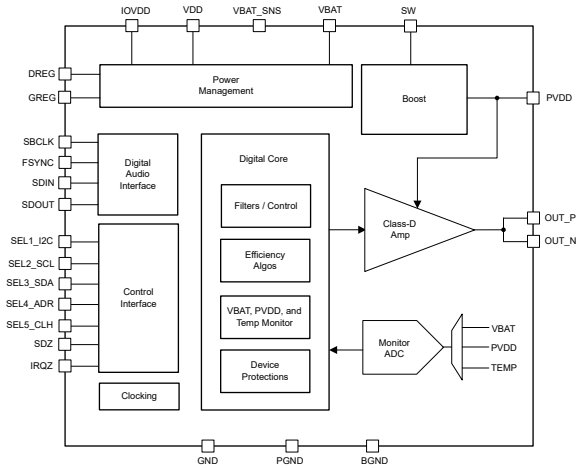
TAS2120 device supports look-ahead algorithm based optimum boost voltage levels to match the output of audio signal. This provides all the power needed for peak output while significantly reducing the average power consumption.

Up to four devices can share a common bus via I^2S/TDM and I^2C interfaces. TAS2120 also supports HW pin based pre-defined controls that can configure the device for desired mode of operation without requiring any I^2C controls.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (2)
TAS2120	QFN	4mm × 3.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional block diagram

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4 Pin Configuration and Functions

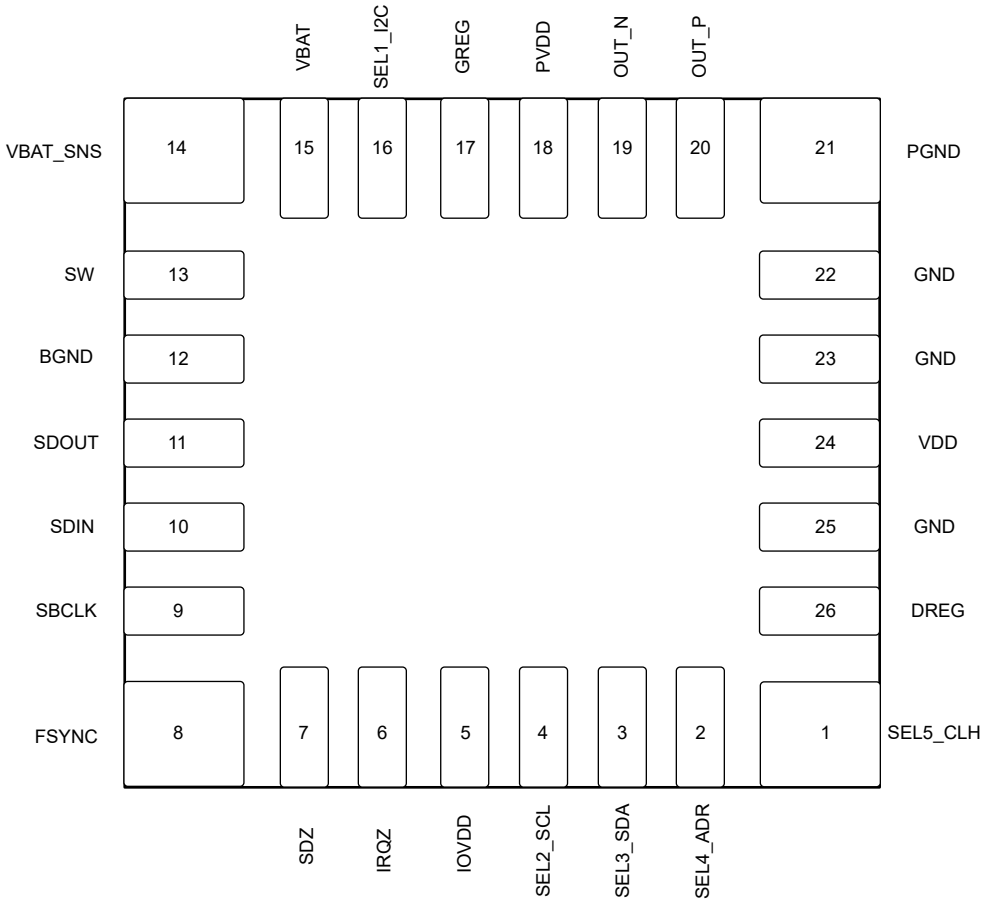


Figure 4-1. QFN Package Bottom View

Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	NO.		
BGND	12	P	Boost ground. Connect to PCB GND plane strongly with multiple vias.
DREG	26	P	Digital core voltage regulator output. Bypass to GND with a capacitor. Do not connect to an external load.
FSYNC	8	I	I^2S word clock or TDM frame sync.
GREG	17	P	High-side gate CP regulator output. Do not connect to an external load.
GND	22, 23, 25	P	Connect to PCB ground plane. Strong connection to ground plane required through multiple vias.
IOVDD	5	P	1.8V or 3.3V Digital IO supply. Decouple to GND with capacitor.
IRQZ	6	O	Open drain, active low interrupt pin. Keep floating or short to GND if not used.
OUT_N	19	O	Class-D negative output.
OUT_P	20	O	Class-D positive output.
PGND	21	P	Class-D Power stage ground. Connect to PCB GND plane strongly through multiple vias.
PVDD	18	P	Integrated boost output and Class-D power stage supply. Decouple to GND with capacitor.
SBCLK	9	I	I^2S or TDM serial bit clock.
SDIN	10	I	I^2S or TDM serial data input.
SDOUT	11	I/O	I^2S or TDM serial data output.
SDZ	7	I	Active low hardware shutdown.
SEL1_I2C	16	I	HW Mode: Select 1 Pin. Amplifier gain level selection with volume ramp enable and disable options. I^2C Mode: Short to GND for I^2C mode selection.
SEL2_SCL	4	I	HW Mode: Select 2 Pin. I^2S, TDM, Left justified selection. I^2C Mode: Clock Pin. Pull up to IOVDD with a resistor.
SEL3_SDA	3	I/O	HW Mode: Select 3 Pin. Data valid rising edge and falling edge selection. I^2C Mode: Data Pin. Pull up to IOVDD with a resistor.
SEL4_ADR	2	I	HW Mode: Select 4 Pin.Y-bridge threshold configuration setting. I^2C Mode: I^2C address pin.
SEL5_CLH	1	I/O	HW Mode: Select5 Pin. Boost 1S, 2S, External PVDD mode selection. I^2C Mode: Class-H boost control. Shared boost input or external boost PWM generation. Short to GND if shared boost or external boost feature is not used.
SW	13	P	Internal boost converter switch input. Keep floating if internal boost is not used.
VBAT	15	P	Battery power supply input. Connect to a 2.5 to 5.5V supply and decouple with a capacitor.
VBAT_SNS	14	I	Battery sense terminal. Connect to battery supply for remote battery sensing. Short to GND if battery sense feature is not used.
VDD	24	P	Connect to 1.8V supply and decouple to GND with capacitor.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage	PVDD	–0.3	19	V
Supply Voltage	VBAT	–0.3	6	V
Supply Voltage Sense	VBAT_SNS	–0.3	12	V
Supply Voltage	VDD	–0.3	2	V
Supply Voltage	IOVDD	–0.3	6	V
Boost Switching Pin	SW	–0.7	19	V
Class-D Output	OUTP, OUTM	–0.7	19	V
High Side Drive Regulator	GREG	–0.3	PVDD + 6	V
Digital Supply Regulator	DREG	–0.3	1.65	V
Digital IO Pins	Digital pins referenced to IOVDD supply	–0.3	6	V
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BAT}	Battery Supply	2.5	3.6	5.5	V
V_{BAT}	Battery Supply (2S Mode of operation)	3	3.6	5.5	V
V_{BAT_SNS}	Battery Sense pin voltage	2.5		10	V
V_{BAT2S}	2S Battery Voltage (connected to SW pin through inductor in 2S Mode of operation)	4.7	7.2	10	V
V_{PVDD}	Amplifier Supply	V_{BAT}	12	15	V
V_{VDD}	Supply Voltage	1.65	1.8	1.95	V
V_{IOVDD}	IO Supply Voltage 1.8V	1.62	1.8	1.98	V
V_{IOVDD}	IO Supply Voltage 3.3V	3.0	3.3	3.6	V
R_{SPK}	Speaker resistance	3.2	8	38.4	Ω
L_{SPK}	Speaker inductance	5	33	100	µH
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		Standard JEDEC[2] HR-QFN 26 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) JEDEC Standard 4 Layer PCB

5.5 Electrical Characteristics

T_A = 25°C, VBAT = 3.6V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12V (External PVDD mode enabled), VDD = 1.8V, IOVDD = 1.8V, RL = 8Ω + 33µH, L_{BOOST}(1S Boost mode) = 1µH, Fin = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost, HW mode) = 4.1A, BST_ILIM (2S Boost, I^2C mode) = 5.1A, SDZ=1, Noise gate disabled, Class-D edge rate set to 2V/ns, I2C mode of operation, Measured filter free with an Audio Precision using 22Hz to 20kHz un-weighted bandwidth (unless otherwise noted).[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AMPLIFIER PERFORMANCE - INTERNAL BOOST 1S Mode						
P_{OUT}	Maximum Output Power - 1% THD+N	R_L = 8 Ω + 33 µH		6.4		W
		R_L = 4 Ω + 33 µH		6.6		W
		R_L = 8 Ω + 33 µH, VBAT = 4.4V		8.0		W
		R_L = 4 Ω + 33 µH, VBAT = 4.4V		8.2		W
P_{OUT}	Maximum Output Power - 10% THD+N	RL = 8 Ω + 33 µH, VBAT = 4.4V		9.5		W
		RL = 4 Ω + 33 µH, VBAT = 4.4V		9.8		W
η_{SYSTEM_1W}	System Efficiency at P_{OUT} = 1.0W	R_L = 8 Ω + 33 µH		86.7		%
		R_L = 4 Ω + 33 µH		85		%
		R_L = 8 Ω + 33 µH, VBAT = 4.4V		87.8		%
		R_L = 4 Ω + 33 µH, VBAT = 4.4V		86.7		%
$\eta_{SYSTEM\_MAX\_POUT}$	System Efficiency at 1% THD+N power Level	R_L = 8 Ω + 33 µH		72.6		%
		R_L = 4 Ω + 33 µH		71.8		%
		R_L = 8 Ω + 33 µH, VBAT = 4.4V		76.6		%
		R_L = 4 Ω + 33 µH, VBAT = 4.4V		76.5		%
V_N	Idle channel Noise	A-Weighted, Gain = 6dBV (Receiver Mode), DAC-Running		4.2		µV
		A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.4		µV
DNR	Dynamic Range	A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 µH, Gain = 6dBV (Receiver Mode)		113.8		dB
		A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 µH, Gain = 21dBV (Speaker Mode)		113.7		dB
THD+N	Total Harmonic distortion + Noise	P_{OUT} = 1 W, R_L = 8 Ω + 33 µH		0.003		%
		P_{OUT} = 1 W, R_L = 4 Ω + 33 µH		0.004		%
K_{CP}	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes in/out of mute, power up and power down, noise gate mode entry and exit. Measured as peak A-weighted voltage. RL = 8 Ω + 33 µH, Input = digital silence		–67		dBV

T_A = 25°C, VBAT = 3.6V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12V (External PVDD mode enabled), VDD = 1.8V, IOVDD = 1.8V, RL = 8Ω + 33µH, L_{BOOST}(1S Boost mode) = 1µH, Fin = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost, HW mode) = 4.1A, BST_ILIM (2S Boost, I²C mode) = 5.1A, SDZ=1, Noise gate disabled, Class-D edge rate set to 2V/ns, I2C mode of operation, Measured filter free with an Audio Precision using 22Hz to 20kHz un-weighted bandwidth (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Amplifier input signal Bandwidth	f_s ≥ 96ksps, Gain error < Pass-Band Ripple		40		kHz
V_{FS}	Full scale equivalent Voltage	Measured at -6dBFS Input, Gain = 6dBV (Receiver Mode)		2.00		V_{RMS}
A_{GAIN}	Audio channel Gain programmability range	Gain programmability in steps of 0.5dB	0		21	dBV
A_{GAIN_ERR}	Amplifier Gain error	POUT = 1W		±0.1		dB
		POUT = 0.25W, Gain = 6dBV (Receiver Mode)		±0.1		dB
V_{OS}	Output Offset Voltage	Idle channel	–1		1	mV
		Idle channel, Gain = 6dBV (Receiver Mode)	–1		1	mV
F_{PWM}	Class-D PWM switching Frequency	Average clock frequency		384		kHz
$PSRR_{VBAT}$	VBAT power-supply rejection ratio	VBAT + 200 mV_{pp}, f_{ripple} = 217 Hz		118		dB
		VBAT + 200 mV_{pp}, f_{ripple} = 1 kHz		115		dB
		VBAT + 200 mV_{pp}, f_{ripple} = 20 kHz		80		dB
$PSRR_{VDD}$	VDD power-supply rejection ratio	VDD + 200 mV_{pp}, f_{ripple} = 217 Hz		113		dB
		VDD + 200 mV_{pp}, f_{ripple} = 1 kHz		113		dB
		VDD + 200 mV_{pp}, f_{ripple} = 20 kHz		91		dB
MUTE_ATTN	Mute Attenuation	Device is MUTE mode. DAC modulator running		113		dB
AMPLIFIER PERFORMANCE - INTERNAL BOOST 2S Mode						
$P_{OUT\_BOOST\_2S}$	Maximum Output Power - 1% THD+N	R_L = 8 Ω + 33 µH		10.0		W
		R_L = 4 Ω + 33 µH		12.8		W
		R_L = 8 Ω + 33 µH, VBAT2S = 8.4V		10.4		W
		R_L = 4 Ω + 33 µH, VBAT2S = 8.4V		14.5		W
$P_{OUT\_BOOST\_2S}$	Maximum Output Power - 10% THD+N	R_L = 8 Ω + 33 µH, VBAT2S = 8.4V		12.6		W
		R_L = 4 Ω + 33 µH, VBAT2S = 8.4V		17.5		W
$\eta_{SYSTEM\_1W\_2S}$	System Efficiency at P_{OUT} = 1.0W	R_L = 8 Ω + 33 µH		89.9		%
		R_L = 8 Ω + 33 µH, VBAT2S = 8.4V		89.5		%
		R_L = 4 Ω + 33 µH		86.2		%
		R_L = 4 Ω + 33 µH, VBAT2S = 8.4V		85.8		%
$\eta_{SYSTEM\_MAX\_POUT\_2S}$	System Efficiency at 1% THD+N power Level	R_L = 8 Ω + 33 µH		85		%
		R_L = 8 Ω + 33 µH, VBAT2S= 8.4V		86.5		%
		R_L = 4 Ω + 33 µH		77.4		%
		R_L = 4 Ω + 33 µH, VBAT2S = 8.4V		78.0		%
V_N_2S	Idle channel Noise	A-Weighted, Gain = 6dBV (Receiver Mode), DAC-Running		7.0		µV
		A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.4		µV
DNR_2S	Dynamic Range	A-Weighted, -60 dBFS Method, Gain = 6dBV (Receiver Mode)		108.9		dB
		A-Weighted, -60 dBFS Method, Gain = 21dBV (Speaker Mode)		114.4		dB

T_A = 25°C, VBAT = 3.6V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12V (External PVDD mode enabled), VDD = 1.8V, IOVDD = 1.8V, RL = 8Ω + 33µH, L_{BOOST}(1S Boost mode) = 1µH, Fin = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost, HW mode) = 4.1A, BST_ILIM (2S Boost, I^2C mode) = 5.1A, SDZ=1, Noise gate disabled, Class-D edge rate set to 2V/ns, I2C mode of operation, Measured filter free with an Audio Precision using 22Hz to 20kHz un-weighted bandwidth (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD+N_2S	Total Harmonic distortion + Noise	P_{OUT} = 1 W, R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		0.003		%
		P_{OUT} = 1 W, R_L = 4 Ω + 33 µH, f_{in} = 1 kHz		0.003		%
		POUT = 0.25 W, RL = 8 Ω + 33 µH, fin = 1 kHz, Gain = 6dBV (Receiver Mode)		0.005		%
K_{CP}_2S	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes In/Out of Mute, Power Up and power Down, Noise Gate mode entry and Exit. Measured at Peak A-weighted Voltage. RL = 8 Ω + 33 µH, Input = Digital silence.		–68		dBV
$PSRR_{VBAT2S}$	VBAT2S power-supply rejection ratio	VBAT2S = 7.2 V + 200 mVpp, fripple = 217 Hz		115		dB
		VBAT2S = 7.2 V + 200 mVpp, fripple = 1 kHz		115		dB
		VBAT2S = 7.2 V + 200 mVpp, fripple = 20 kHz		90		dB
$PSRR_{VBAT}$_2S	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 217 Hz		115		dB
		VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 1 kHz		115		dB
		VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 20 kHz		90		dB
$PSRR_{VDD}$_2S	VDD power-supply rejection ratio	VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		110		dB
		VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 1 kHz		110		dB
		VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		90		dB
AMPLIFIER PERFORMANCE - EXTERNAL PVDD Mode						
$P_{OUT\_EXT\_PVDD}$	Maximum Output Power - 1% THD+N	R_L = 8 Ω + 33 µH		8.2		W
		R_L = 4 Ω + 33 µH		14.6		W
		R_L = 8 Ω + 33 µH, PVDD = 15V		11.2		W
		R_L = 4 Ω + 33 µH, PVDD = 15V		19		W
$P_{OUT\_EXT\_PVDD}$	Maximum Output Power - 10% THD+N	RL = 8 Ω + 33 µH		10.3		W
		RL = 4 Ω + 33 µH		18.0		W
$\eta_{SYSTEM\_EXT\_1W}$	System Efficiency at P_{OUT} = 1.0W	R_L = 8 Ω + 33 µH		88.1		%
		R_L = 4 Ω + 33 µH		84.2		%
$\eta_{SYSTEM\_EXT\_MAX\_POUT}$	System Efficiency at 1% THD+N power Level	R_L = 8 Ω + 33 µH		93.2		%
		R_L = 4 Ω + 33 µH		88.5		%
V_{N_EXT}	Idle channel Noise	A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.2		µV
DNR_EXT	Dynamic Range	A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 µH		114.4		dB
THD+N_EXT	Total Harmonic distortion + Noise	P_{OUT} = 1 W, R_L = 8 Ω + 33 µH		0.003		%
		P_{OUT} = 1 W, R_L = 4 Ω + 33 µH		0.004		%
K_{CP}_EXT	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes In/Out of Mute, Power Up and power Down, Noise Gate mode entry and Exit. Measured at Peak A-weighted Voltage. RL = 8 Ω + 33 µH, Input = Digital Silence		–68		dBV
V_{OS}_EXT	Output Offset Voltage	Idle channel	–1		1	mV

T_A = 25°C, VBAT = 3.6V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12V (External PVDD mode enabled), VDD = 1.8V, IOVDD = 1.8V, RL = 8Ω + 33µH, L_{BOOST}(1S Boost mode) = 1µH, Fin = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost, HW mode) = 4.1A, BST_ILIM (2S Boost, I²C mode) = 5.1A, SDZ=1, Noise gate disabled, Class-D edge rate set to 2V/ns, I2C mode of operation, Measured filter free with an Audio Precision using 22Hz to 20kHz un-weighted bandwidth (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$PSRR_{PVDD\_EXT}$	PVDD power-supply rejection ratio	PVDD + 200 mVpp, fripple = 217 Hz		119		dB
		PVDD + 200 mVpp, fripple = 1 kHz		115		dB
		PVDD + 200 mVpp, fripple = 20 kHz		91		dB
$PSRR_{VBAT\_EXT}$	VBAT power-supply rejection ratio	VBAT + 200 mV_{pp}, f_{ripple} = 217 Hz		118		dB
		VBAT + 200 mV_{pp}, f_{ripple} = 1 kHz		116		dB
		VBAT + 200 mV_{pp}, f_{ripple} = 20 kHz		102		dB
$PSRR_{VDD\_EXT}$	VDD power-supply rejection ratio	VDD + 200 mV_{pp}, f_{ripple} = 217 Hz		113		dB
		VDD + 200 mV_{pp}, f_{ripple} = 1 kHz		113		dB
		VDD + 200 mV_{pp}, f_{ripple} = 20 kHz		91		dB
Boost Converter						
V_{BOOST_RANGE}	Max Output Voltage programmability Range	Programmable in steps of 66mV	5.5		14.75	V
V_{BOOST_STEP}	Class-H Output Voltage Step Size			33		mV
V_{BOOST}	Output Boost Voltage	I_O = 0.1A. Average output value. *VBOOST_MAX_CTRL* = max value		14.9		V
I_{BOOST_CL}	Peak Input Current Limit	*BST_ILIM* = Max Setting		5.1		A
I_{BOOST_CL}	Peak Input Current Limit	*BST_ILIM* = Min Setting		1.5		A
	Peak Input Current Limit Programmable step size			39.1		mA
Boost Converter 2S Mode of operation						
V_{BOOST_RANGE}	Output Voltage Range	Programmable in steps of 66mV	10		14.75	V
V_{BOOST_STEP}	Class-H Output Voltage Step Size			33		mV
I_{BOOST_CL}	Peak Input Current Limit (I²C mode)	Max Setting		5.1		A
I_{BOOST_CL}	Peak Input Current Limit	Min Setting		1.5		A
TDM Serial Port						
	PCM Sample Rates and FSYNC Input Frequency		16		192	kHz
	SBCLK Input Frequency	I²S/TDM Operation	0.512		24.57	MHz
	SBCLK Maximum Input Jitter	RMS Jitter below 40 kHz that can be tolerated without performance degradation			0.5	ns
		RMS Jitter above 40 kHz that can be tolerated without performance degradation			5	ns
	SBCLK Cycles per FSYNC in I²S and TDM Modes	Values: 64, 96, 128, 192, 256, 384 and 512	64		512	Cycles
PCM Playback Characteristics to fs ≤ 48 kHz						
Fs	Sample Rates		16		48	kHz
	Audio Channel Passband LPF Corner	Ripple < pass-band ripple		0.454		fs
	Audio Channel Passband Ripple	20 Hz to LPF cutoff		± 0.1		dB

T_A = 25°C, VBAT = 3.6V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12V (External PVDD mode enabled), VDD = 1.8V, IOVDD = 1.8V, RL = 8Ω + 33µH, L_{BOOST}(1S Boost mode) = 1µH, Fin = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost, HW mode) = 4.1A, BST_ILIM (2S Boost, I^2C mode) = 5.1A, SDZ=1, Noise gate disabled, Class-D edge rate set to 2V/ns, I2C mode of operation, Measured filter free with an Audio Precision using 22Hz to 20kHz un-weighted bandwidth (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Audio Channel Stop Band Attenuation	≥ 0.55 fs		60		dB
		≥ 1 fs		65		dB
	Audio Channel Group Delay	Fin = 1kHz, Lowest latency mode (Y-bridge, Class-H, Noise Gate disabled)		8.5		1/fs
		Fin = 1kHz, Class-H disabled		16.5		1/fs
		Fin = 1kHz, Class-H enabled		31.5		1/fs
		DC to 20kHz, Lowest latency mode (HPF bypassed, Y-bridge, Class-H, Noise Gate disabled)		13		1/fs
		DC to 20kHz, HPF bypassed, Class-H disabled		21		1/fs
		DC to 20kHz, HPF bypassed, Class-H enabled		37		1/fs
PCM Playback Characteristics to fs > 48 kHz						
Fs	Sample Rates		88.2		192	kHz
	Audio Channel Passband LPF Corner	fs = 96 kHz		0.469		fs
		fs = 192 kHz		0.234		fs
	Audio Channel Passband Ripple	20 Hz to LPF cutoff		± 0.2		dB
	Audio Channel Stop Band Attenuation	fs = 96 kHz, fin ≥ 0.55 fs		60		dB
		fs = 96 kHz, fin ≥ 1 fs		65		dB
		fs = 192 kHz, 0.55 fs ≥ fin ≥ 0.275 fs		60		dB
	Audio Channel Group Delay	Fin = 1kHz, Fs = 96kHz, Lowest latency mode (Y-bridge, Class-H, Noise Gate disabled)		11		1/fs
		Fin = 1kHz, Fs = 96kHz, Class-H disabled		6.7		1/fs
		Fin = 1kHz, Fs = 96kHz, Class-H enabled		56.7		1/fs
		DC to 20kHz, Fs = 96kHz, Lowest latency mode (HPF bypassed, Y-bridge, Class-H, Noise Gate disabled)		11.5		1/fs
		DC to 40kHz, Fs=96kHz, HPF bypassed, Class-H disabled		28.6		1/fs
		DC to 40kHz, Fs=192 kHz, HPF bypassed, Class-H enabled		117.8		1/fs
Protection Circuits						
	Thermal shutdown temperature			140		°C
	Thermal shutdown retry time			1.5		s
	VBAT undervoltage lockout threshold (UVLO)	UVLO is asserted	1.9			V
		UVLO is released			2.3	V
	VDD undervoltage lockout threshold (UVLO)	UVLO is asserted	1.4			V
		UVLO is released			1.6	V
	PVDD undervoltage lockout threshold (UVLO)	UVLO is asserted, external PVDD mode only	2.6			V
		UVLO is released, external PVDD mode only			2.8	V
	PVDD overvoltage lockout threshold (OVLO)	OVLO is asserted, OVLO protection enabled.		16		V

T_A = 25°C, VBAT = 3.6V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12V (External PVDD mode enabled), VDD = 1.8V, IOVDD = 1.8V, RL = 8Ω + 33µH, L_{BOOST}(1S Boost mode) = 1µH, Fin = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost, HW mode) = 4.1A, BST_ILIM (2S Boost, I^2C mode) = 5.1A, SDZ=1, Noise gate disabled, Class-D edge rate set to 2V/ns, I2C mode of operation, Measured filter free with an Audio Precision using 22Hz to 20kHz un-weighted bandwidth (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power up/down Time						
T_{STDBY}	Turn ON time from SDZ Asserted to device ready for i2c Command				300	us
T_{ACTIVE}	Turn ON time from release of Software Shutdown to Amplifier output Active	Volume ramping disabled		1.6		ms
		Volume ramping enabled		3.9		ms
$T_{TURNOFF}$	Turn OFF time from assertion of Software Shutdown to Amplifier output Hi-Z	Volume ramping disabled		0.2		ms
		Volume ramping enabled		13.9		ms
Current Consumption - Internal Boost Mode(1)						
$I_{Q\_HW\_SD}$	Current consumption in Hardware Shutdown	VBAT, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA
$I_{Q\_SW\_SD}$	Current consumption in Software Shutdown	VBAT, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA
I_{Q_NG}	Current consumption in Idle channel	VBAT, P_{OUT} = 0, Noise Gate enabled		0.19		mA
		VDD, P_{OUT} = 0, Noise Gate enabled		2.3		mA
		IOVDD, P_{OUT} = 0, Noise Gate enabled		0.1		mA
		Total Power, P_{OUT} = 0, Noise Gate enabled		4.8		mW
I_{Q_IDLE}	Current consumption in Idle channel	VBAT, P_{OUT} = 0, Noise gate disabled		0.62		mA
		VDD, P_{OUT} = 0, Noise gate disabled		6		mA
		IOVDD, P_{OUT} = 0, Noise gate disabled		0.1		mA
		Total Power, P_{OUT} = 0, Noise gate disabled		13.1		mW
Current Consumption - Internal Boost Mode 2S Mode(1)						
$I_{Q\_HW\_SD}$	Current consumption in Hardware Shutdown	VBAT, SDZ=0		0.1		uA
		VBAT2S, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA
$I_{Q\_SW\_SD}$	Current consumption in Software Shutdown	VBAT, All clocks Stopped		0.1		uA
		VBAT2S, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA
I_{Q_NG}	Current consumption in Idle channel	VBAT, P_{OUT} = 0, Noise gate enabled		0.2		mA
		VBAT2S, P_{OUT} = 0, Noise gate enabled		0.1		mA
		VDD, P_{OUT} = 0, Noise gate enabled		2.3		mA
		IOVDD, P_{OUT} = 0, Noise gate enabled		0.1		mA
		Total Power, P_{OUT} = 0, Noise gate enabled		5.1		mW

T_A = 25°C, VBAT = 3.6V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12V (External PVDD mode enabled), VDD = 1.8V, IOVDD = 1.8V, RL = 8Ω + 33µH, L_{BOOST}(1S Boost mode) = 1µH, Fin = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost, HW mode) = 4.1A, BST_ILIM (2S Boost, I^2C mode) = 5.1A, SDZ=1, Noise gate disabled, Class-D edge rate set to 2V/ns, I2C mode of operation, Measured filter free with an Audio Precision using 22Hz to 20kHz un-weighted bandwidth (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q_IDLE}	Current consumption in Idle Channel	VBAT, P_{OUT} = 0, Noise gate disabled		0.5		mA
		VBAT2S, P_{OUT} = 0, Noise gate disabled		0.35		mA
		VDD, P_{OUT} = 0, Noise gate disabled		6		mA
		IOVDD, P_{OUT} = 0, Noise gate disabled		0.1		mA
		Total Power, P_{OUT} = 0, Noise gate disabled		15.1		mW
Current Consumption - External PVDD Mode (1)						
$I_{Q\_HW\_SD}$	Current consumption in Hardware Shutdown	PVDD, SDZ=0		0.1		uA
		VBAT, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA
$I_{Q\_SW\_SD}$	Current consumption in Software Shutdown	PVDD, All clocks Stopped		0.1		uA
		VBAT, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA
I_{Q_NG}	Current consumption in Idle channel	PVDD, P_{OUT} = 0, Noise gate enabled		0.1		mA
		VBAT, P_{OUT} = 0, Noise gate enabled		0.15		mA
		VDD, P_{OUT} = 0, Noise gate enabled		2.2		mA
		IOVDD, P_{OUT} = 0, Noise gate enabled		0.1		mA
		Total Power, P_{OUT} = 0, Noise gate enabled		5.3		mW
I_{Q_IDLE}	Current consumption in Idle channel	PVDD, P_{OUT} = 0, Noise gate disabled		0.2		mA
		VBAT, P_{OUT} = 0, Noise gate disabled		0.5		mA
		VDD, P_{OUT} = 0, Noise gate disabled		6		mA
		IOVDD, P_{OUT} = 0, Noise gate disabled		0.1		mA
		Total Power, P_{OUT} = 0, Noise gate disabled		14.7		mW
DIGITAL IOs						
V_{IH}	High-level digital input logic voltage threshold	All digital pins	0.7 x IOVDD			V
V_{IL}	Low-level digital input logic voltage threshold	All digital pins			0.3 x IOVDD	V
V_{OH}	High-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I_{OH} = 100µA	IOVDD - 0.2 V			V
V_{OL}	Low-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I_{OL} = -100µA			0.2	V
$V_{OL(I2C)}$	Low-level digital output voltage	SDA and SCL; I_{OL} = -1mA			0.2 x IOVDD	V
$V_{OL(IRQZ)}$	Low-level digital output voltage for open drain output	IRQZ pin; I_{OL} = -1mA			0.2	V
I_{IH} (1)	Input logic-high leakage for digital inputs	All digital pins; Input = IOVDD.	-1		1	µA
I_{IL} (1)	Input logic-low leakage for digital inputs	All digital pins; Input = GND	-1		1	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF

T_A = 25°C, VBAT = 3.6V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12V (External PVDD mode enabled), VDD = 1.8V, IOVDD = 1.8V, RL = 8Ω + 33µH, L_{BOOST}(1S Boost mode) = 1µH, Fin = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost, HW mode) = 4.1A, BST_ILIM (2S Boost, I^2C mode) = 5.1A, SDZ=1, Noise gate disabled, Class-D edge rate set to 2V/ns, I2C mode of operation, Measured filter free with an Audio Precision using 22Hz to 20kHz un-weighted bandwidth (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PD}	Pull down resistance for digital input/IO pins when asserted on	All digital pins. Pull down resistance option enabled		18		kΩ

(1) Errata: Additional 2mA to 3mA current consumption expected if IRQZ signal is pulled high. Read more details in section "what to do and what not to do".

5.6 Timing Requirements

T_A = 25 °C, VDD = IOVDD = 1.8 V (unless other wise noted)

		MIN	NOM	MAX	UNIT
I2C - Standard Mode					
f_{SCL}	SCL clock frequency	0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD;DAT}$	Data hold time: For I^2C bus devices	0		3.45	µs
$t_{SU;DAT}$	Data set-up time	250			ns
t_r	SDA and SCL rise time			1000	ns
t_f	SDA and SCL fall time			300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
C_b	Capacitive load for each bus line			400	pF
I2C - Fast Mode					
f_{SCL}	SCL clock frequency	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD;DAT}$	Data hold time: For I^2C bus devices	0		0.9	µs
$t_{SU;DAT}$	Data set-up time	100			ns
t_r	SDA and SCL rise time	20 + 0.1 × Cb		300	ns
t_f	SDA and SCL fall time	20 + 0.1 × Cb		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
C_b	Capacitive load for each bus line			400	pF
TDM Port					
f_{sbclk}	SBCLK Frequency range	0.384		24.576	MHz
$t_{H(SBCLK)}$	SBCLK high period	0.35/f_{sbclk}			ns
$t_{L(SBCLK)}$	SBCLK low period	0.35/f_{sbclk}			ns
$t_{SU(FSYNC)}$	FSYNC setup time	8			ns

T_A = 25 °C, VDD = IOVDD = 1.8 V (unless other wise noted)

		MIN	NOM	MAX	UNIT
$t_{HLD(FSYNC)}$	FSYNC hold time	8			ns
$t_{SU(SDIN)}$	SDIN setup time	8			ns
$t_{HLD(SDIN)}$	SDIN hold time	8			ns
$t_{d(SBCLK-SDOUT)}$	SBCLK to SDOUT delay : 10% of SBCLK falling edge or 90% of SBCLK rising edge to 50% of SDOUT, IOVDD=1.8V			30	ns
$t_{d(SBCLK-SDOUT)}$	SBCLK to SDOUT delay : 10% of SBCLK falling edge or 90% of SBCLK rising edge to 50% of SDOUT, IOVDD=3.3V			18.5	ns
$t_{r(SBCLK)}$	SBCLK rise time : 10 % - 90 % Rise Time			0.15 / f_{sbclk}	ns
$t_{f(SBCLK)}$	SBCLK fall time : 90 % - 10 % Rise Time			0.15 / f_{sbclk}	ns
$t_{f(SBCLK-CLH)}$	SBCLK to CLH delay: Boost share configuration			1 /2* f_{sbclk}	ns

5.7 Timing Diagrams

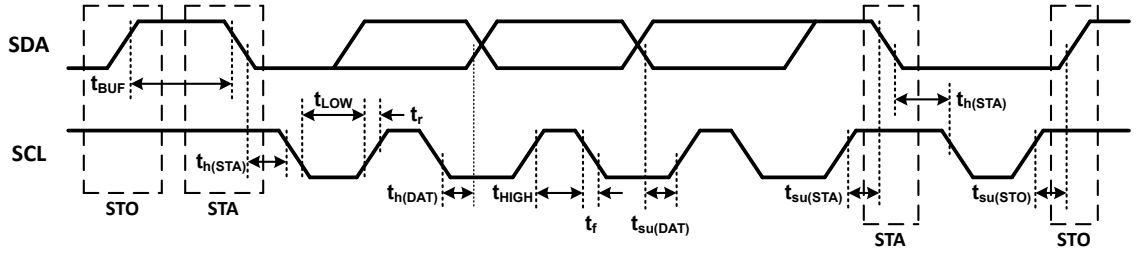


Figure 5-1. I²C timing diagram

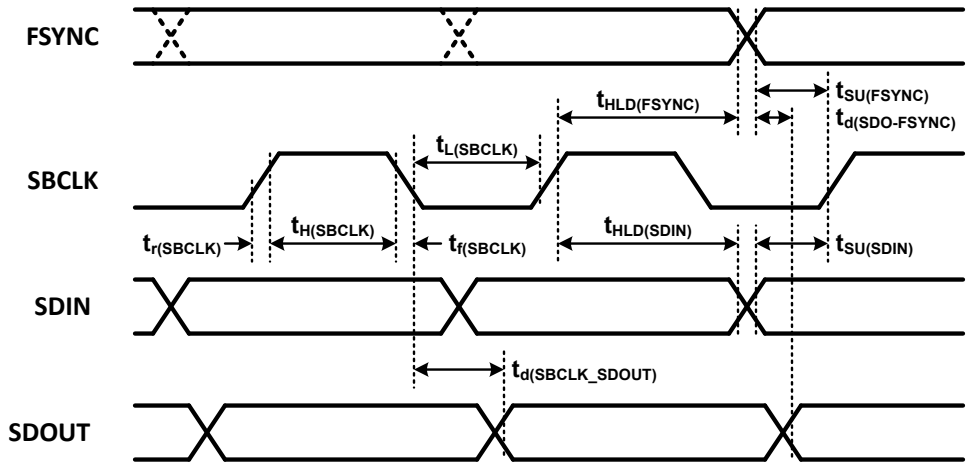
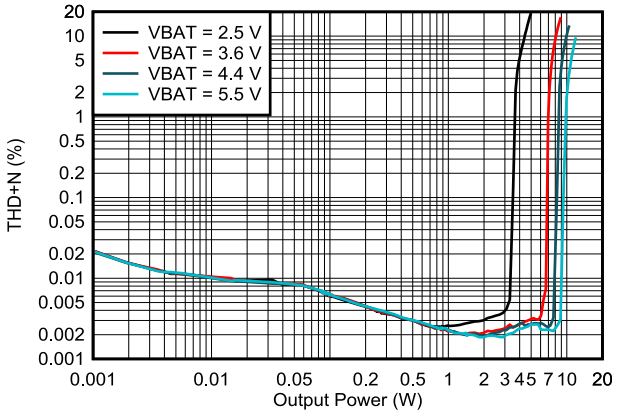


Figure 5-2. I²S/TDM timing diagram

5.8 Typical Characteristics

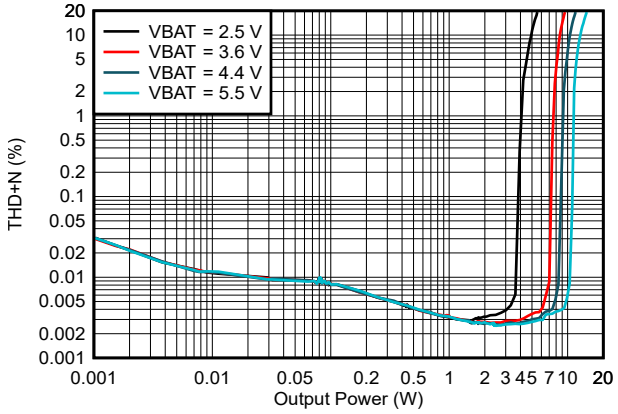
T_A = 25°C, VBAT = 3.6V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12V (External PVDD mode enabled), VDD = 1.8V, IOVDD = 1.8V, L_{BOOST} (1S Boost mode) = 1µH, Fin = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost, HW mode) = 4.1A, BST_ILIM (2S Boost, I_2C mode) = 5.1A,

SDZ=1, Noise gate disabled, Class-D edge rate set to 2V/ns, I^2C mode of operation, Measured filter free with an Audio Precision using 22Hz to 20kHz un-weighted bandwidth (unlessotherwise noted).



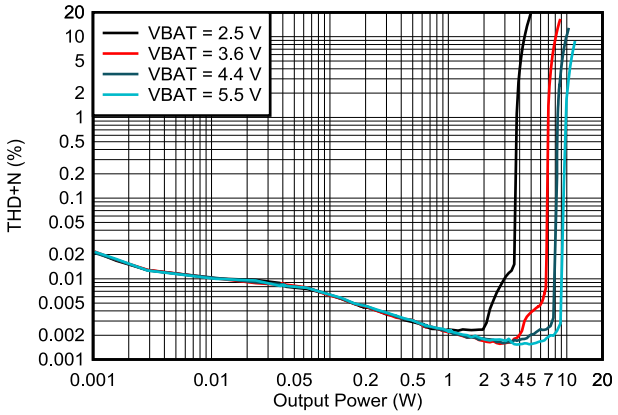
R_L = 8Ω 1S Boost Mode

Figure 5-3. THD+N vs Output Power



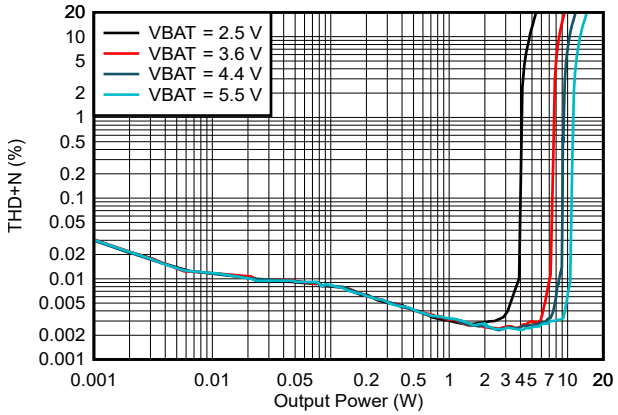
R_L = 4Ω 1S Boost Mode

Figure 5-4. THD+N vs Output Power



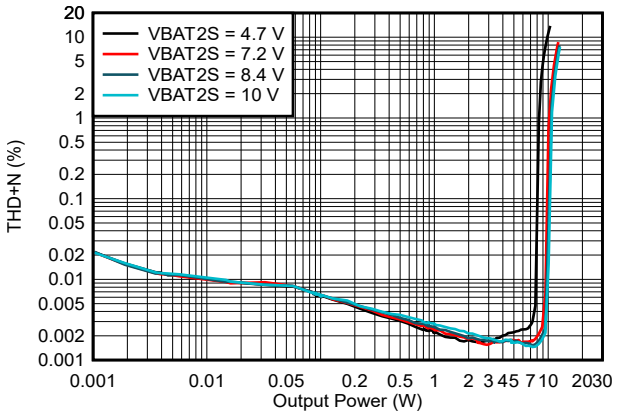
R_L = 8Ω 1S Boost Mode HW Pin Control

Figure 5-5. THD+N vs Output Power



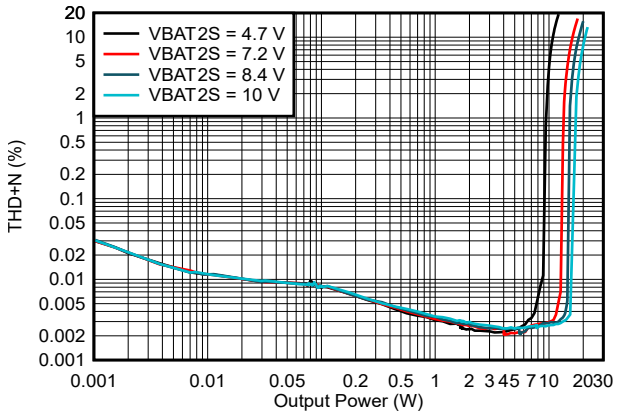
R_L = 4Ω 1S Boost Mode HW Pin Control

Figure 5-6. THD+N vs Output Power



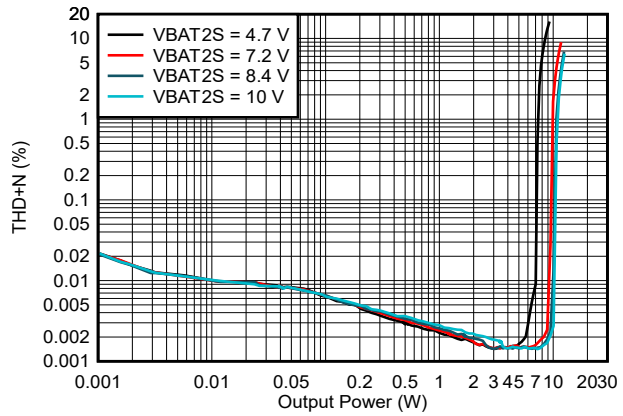
R_L = 8Ω 2S Boost Mode

Figure 5-7. THD+N vs Output Power



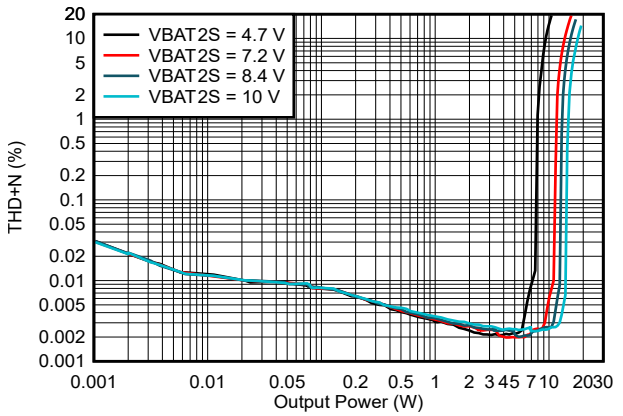
R_L = 4Ω 2S Boost Mode

Figure 5-8. THD+N vs Output Power



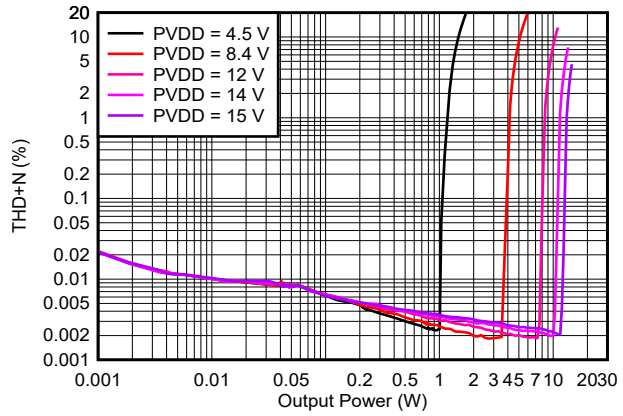
R_L = 8Ω 2S Boost Mode HW Pin Control

Figure 5-9. THD+N vs Output Power



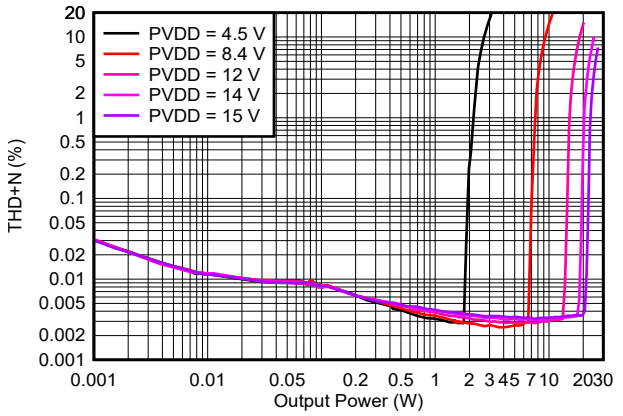
R_L = 4Ω 2S Boost Mode HW Pin Control

Figure 5-10. THD+N vs Output Power



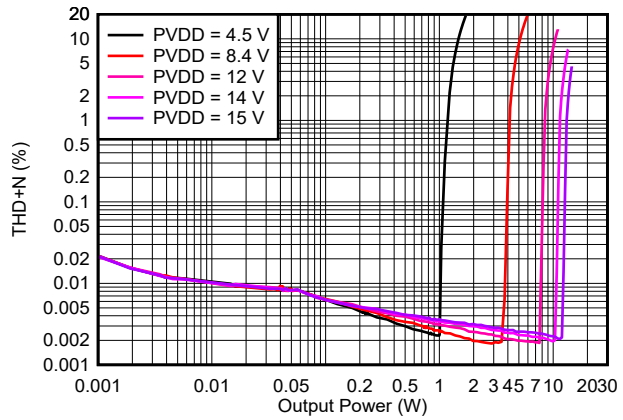
R_L = 8Ω External PVDD Mode

Figure 5-11. THD+N vs Output Power



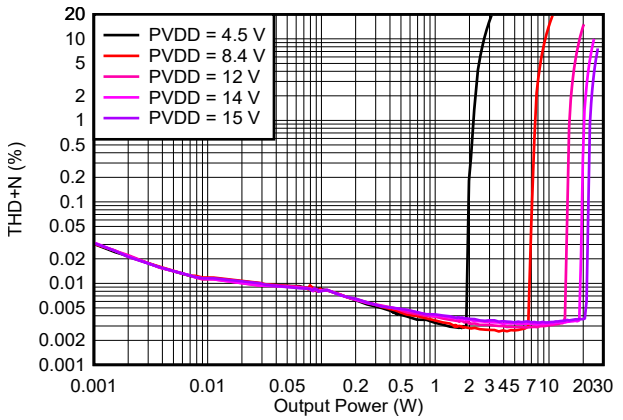
R_L = 4Ω External PVDD Mode

Figure 5-12. THD+N vs Output Power



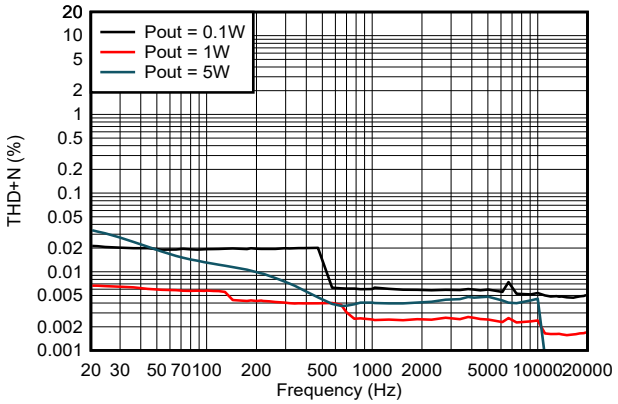
R_L = 8Ω External PVDD Mode HW Pin Control

Figure 5-13. THD+N vs Output Power



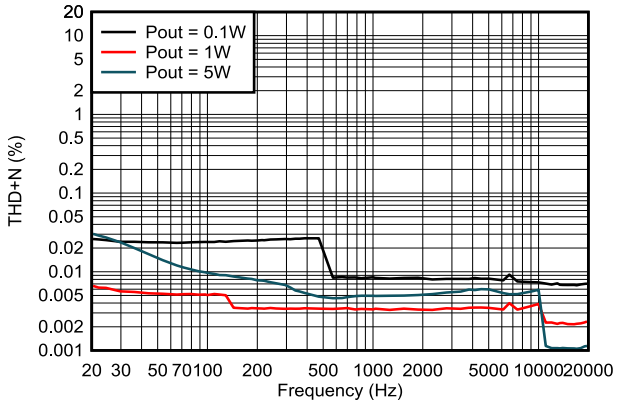
R_L = 4Ω External PVDD Mode HW Pin Control

Figure 5-14. THD+N vs Output Power



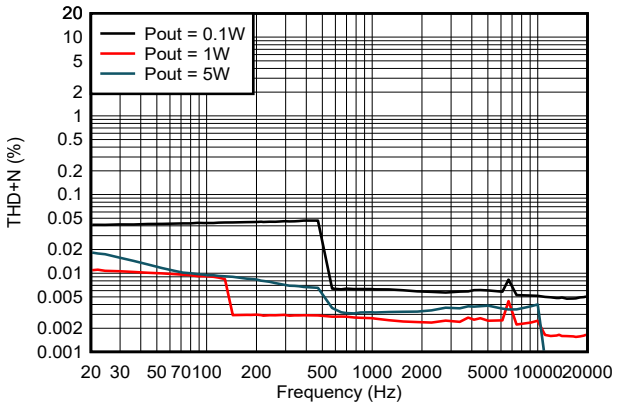
R_L = 8Ω 1S Boost Mode

Figure 5-15. THD+N vs Frequency



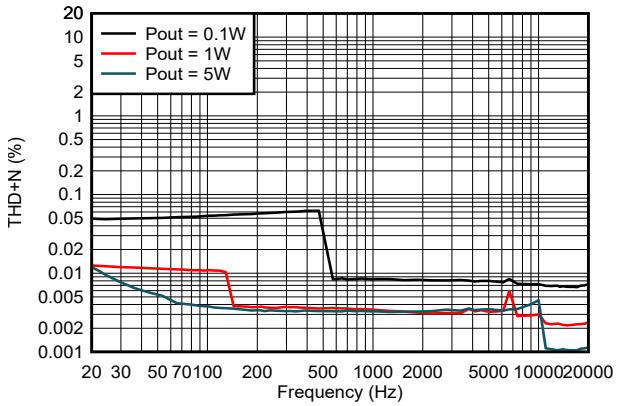
R_L = 4Ω 1S Boost Mode

Figure 5-16. THD+N vs Frequency



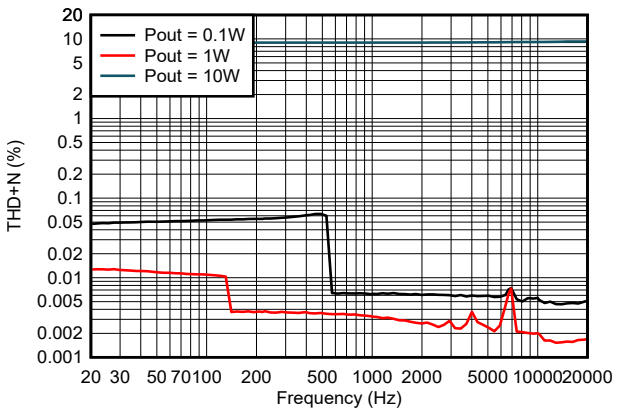
R_L = 8Ω 2S Boost Mode

Figure 5-17. THD+N vs Frequency



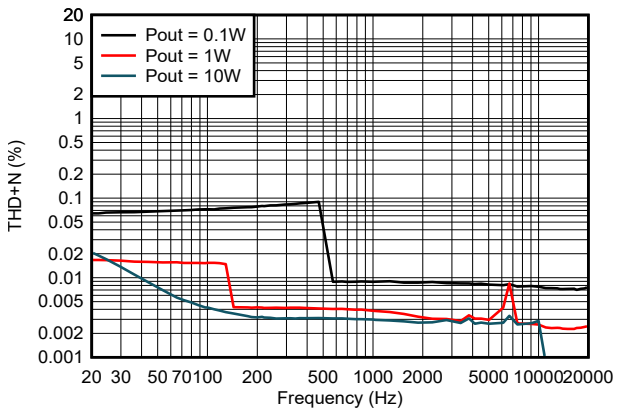
R_L = 4Ω 2S Boost Mode

Figure 5-18. THD+N vs Frequency



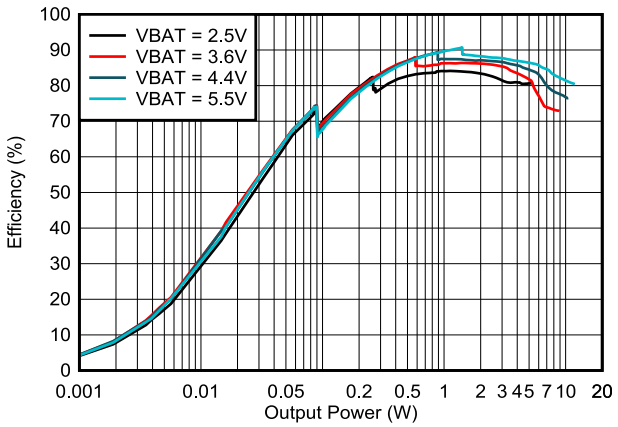
R_L = 8Ω External PVDD Mode

Figure 5-19. THD+N vs Frequency



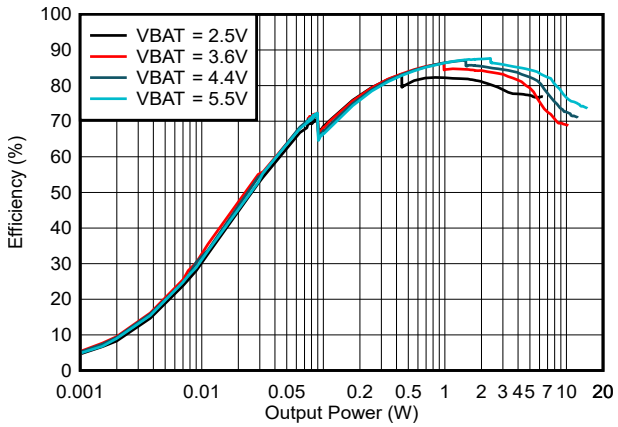
R_L = 4Ω External PVDD Mode

Figure 5-20. THD+N vs Frequency



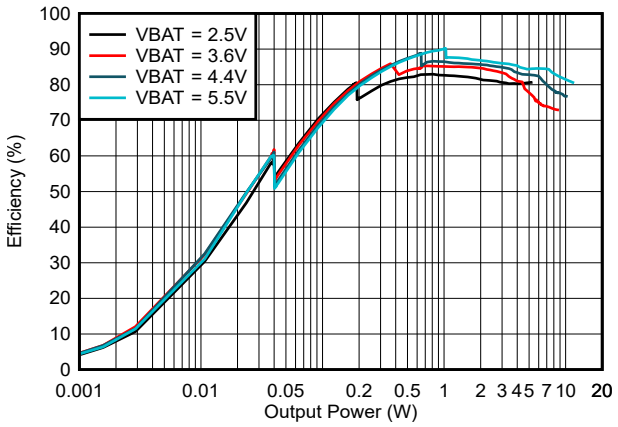
R_L = 8Ω 1S Boost Mode

Figure 5-21. Efficiency vs Output Power



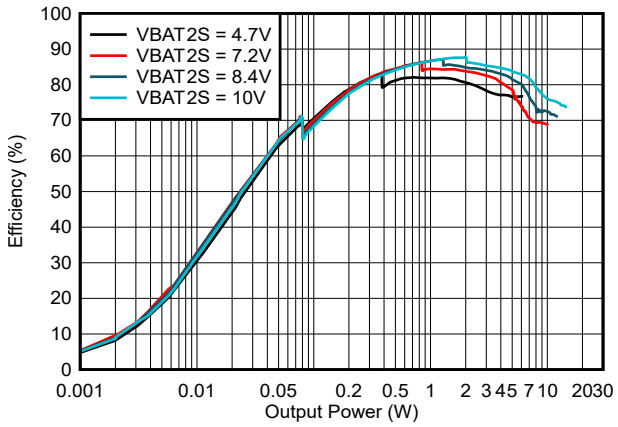
R_L = 4Ω 1S Boost Mode

Figure 5-22. Efficiency vs Output Power



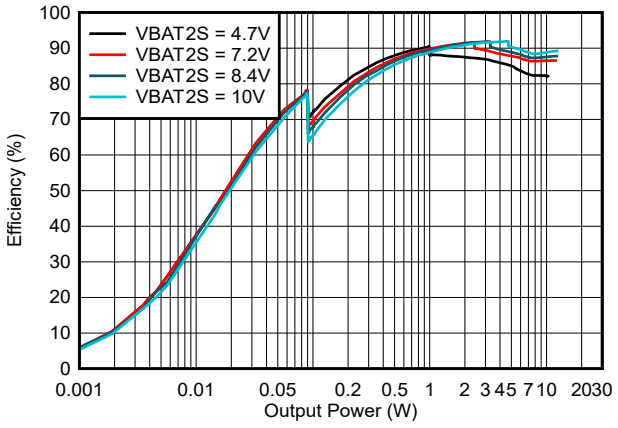
R_L = 8Ω 1S Boost Mode HW Pin Control

Figure 5-23. Efficiency vs Output Power



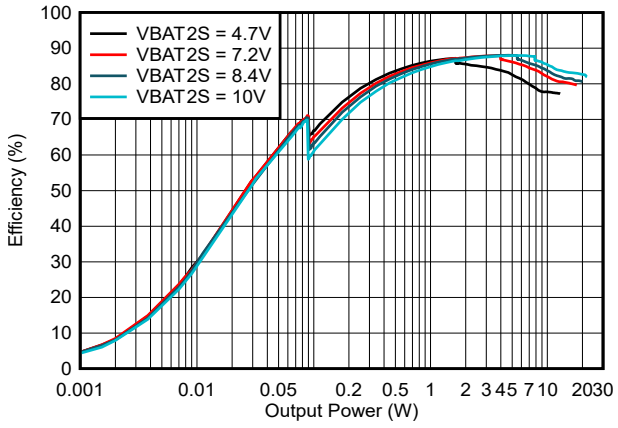
R_L = 4Ω 1S Boost Mode HW Pin Control

Figure 5-24. Efficiency vs Output Power



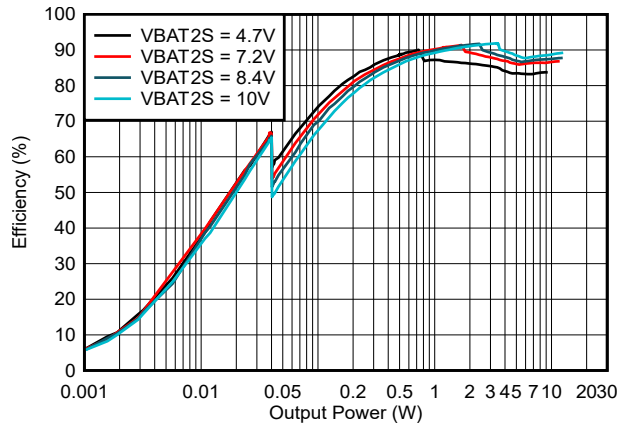
R_L = 8Ω 2S Boost Mode

Figure 5-25. Efficiency vs Output Power



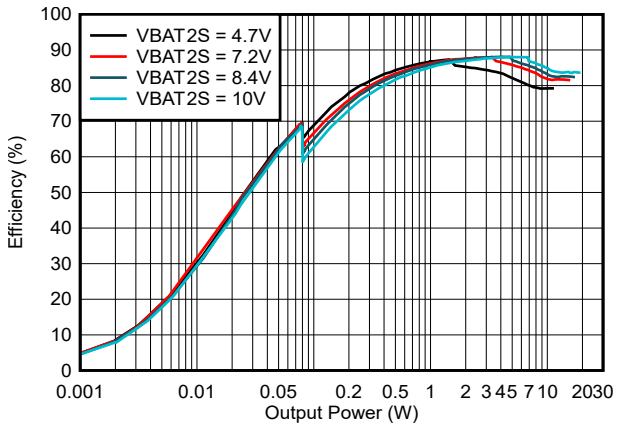
R_L = 4Ω 2S Boost Mode

Figure 5-26. Efficiency vs Output Power



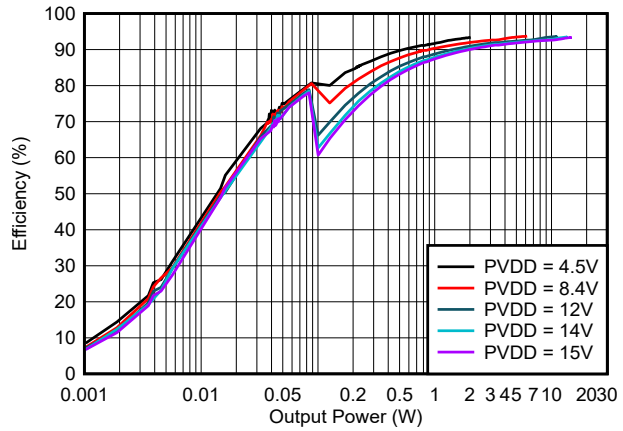
R_L = 8Ω 2S Boost Mode HW Pin Control

Figure 5-27. Efficiency vs Output Power



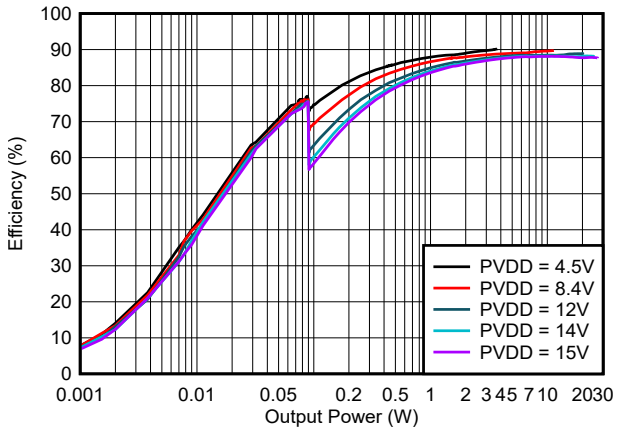
R_L = 4Ω 2S Boost Mode HW Pin Control

Figure 5-28. Efficiency vs Output Power



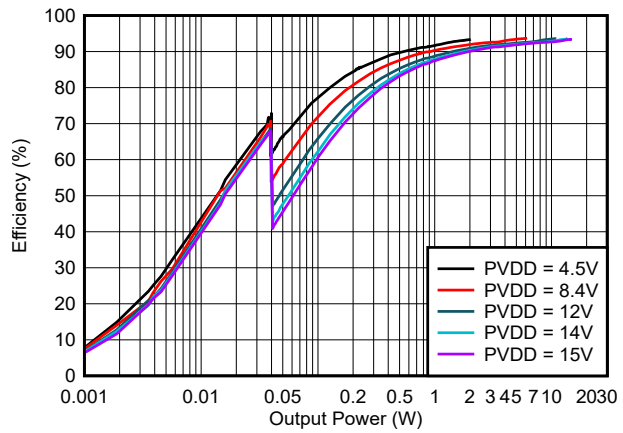
R_L = 8Ω External PVDD Mode

Figure 5-29. Efficiency vs Output Power



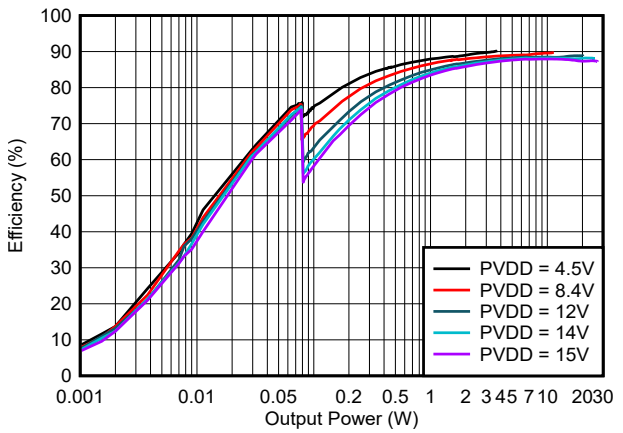
R_L = 4Ω External PVDD Mode

Figure 5-30. Efficiency vs Output Power



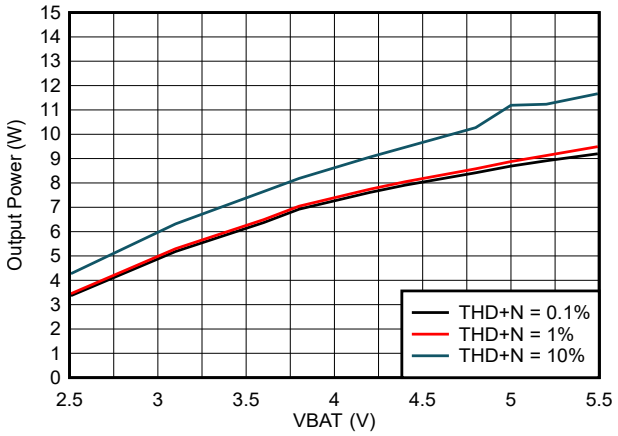
R_L = 8Ω External PVDD Mode HW Pin Control

Figure 5-31. Efficiency vs Output Power



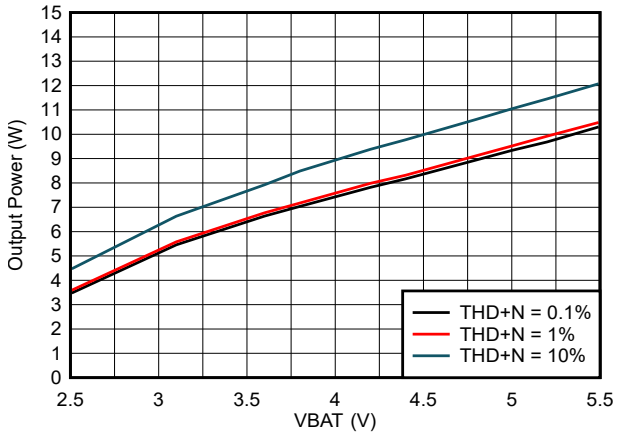
R_L = 4Ω External PVDD Mode HW Pin Control

Figure 5-32. Efficiency vs Output Power



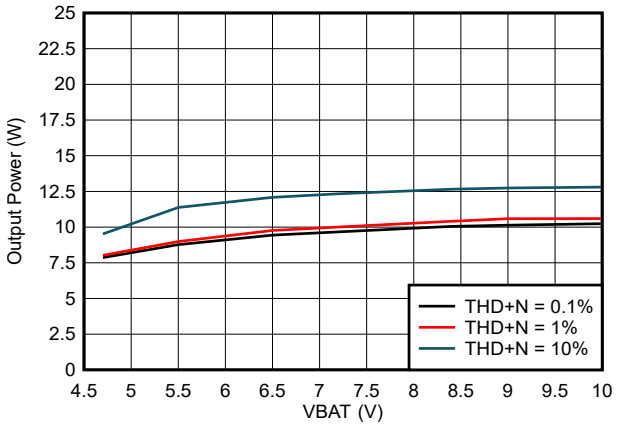
R_L = 8 Ω 1S Boost Mode

Figure 5-33. Output Power vs 1S Battery voltage



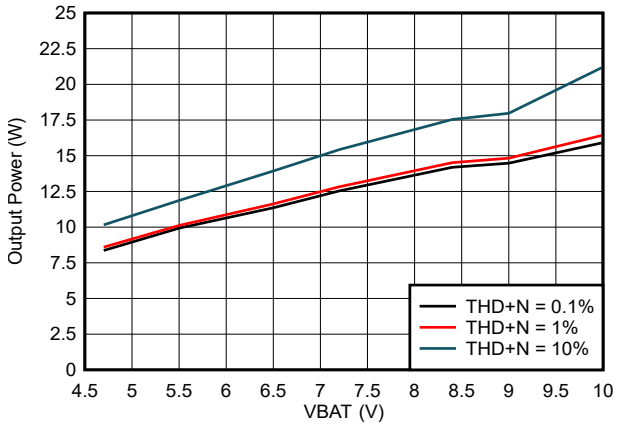
R_L = 4 Ω 1S Boost Mode

Figure 5-34. Output Power vs 1S Battery voltage



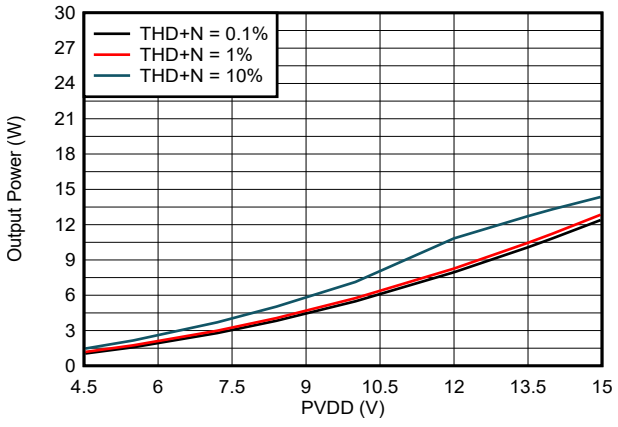
R_L = 8 Ω 2S Boost Mode

Figure 5-35. Output Power vs 2S Battery voltage



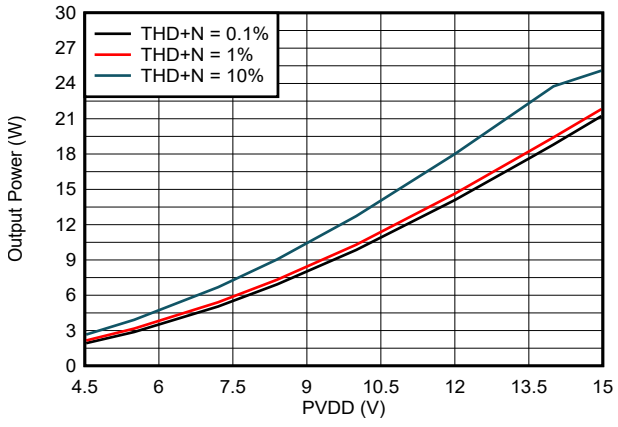
R_L = 4 Ω 2S Boost Mode

Figure 5-36. Output Power vs 2S Battery voltage



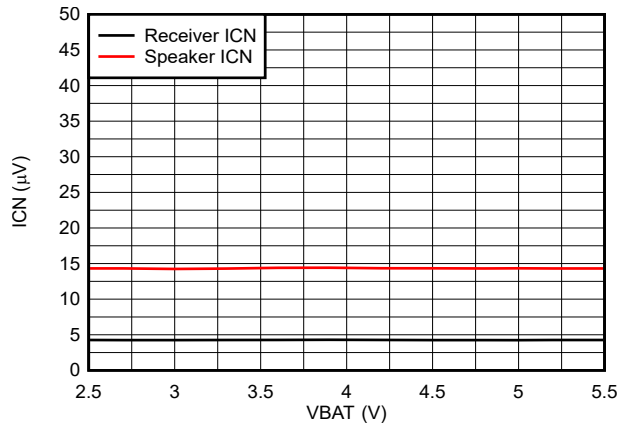
R_L = 8 Ω External PVDD Mode

Figure 5-37. Output Power vs PVDD Voltage



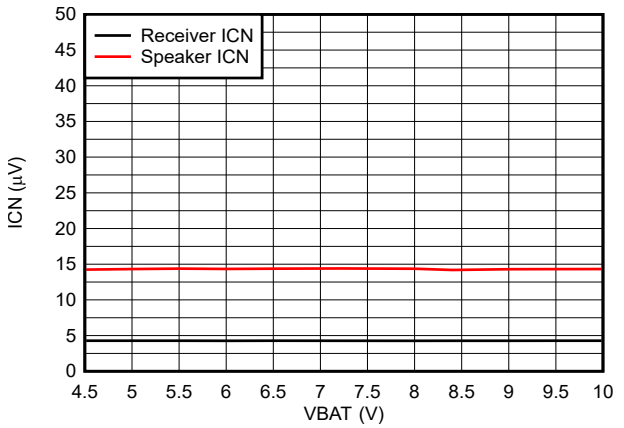
R_L = 4 Ω External PVDD Mode

Figure 5-38. Output Power vs PVDD Voltage



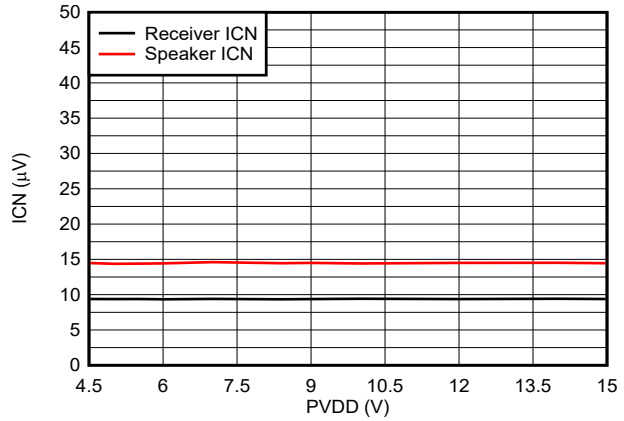
R_L = 8 Ω 1S Boost Mode

Figure 5-39. Idle channel noise vs 1S Battery voltage



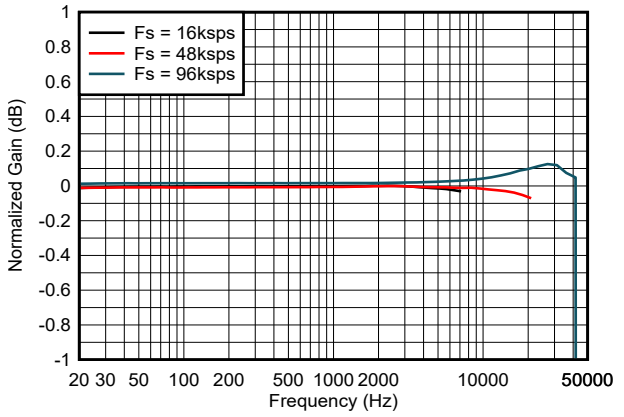
R_L = 8 Ω 1S Boost Mode

Figure 5-40. Idle channel noise vs 2S Battery voltage



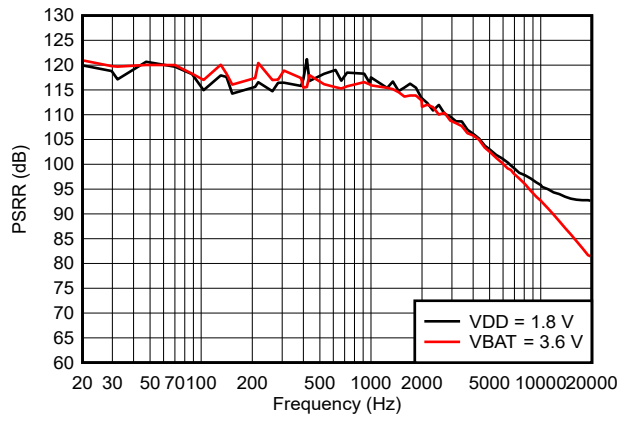
R_L = 8 Ω External PVDD Mode

Figure 5-41. Idle channel noise vs PVDD voltage



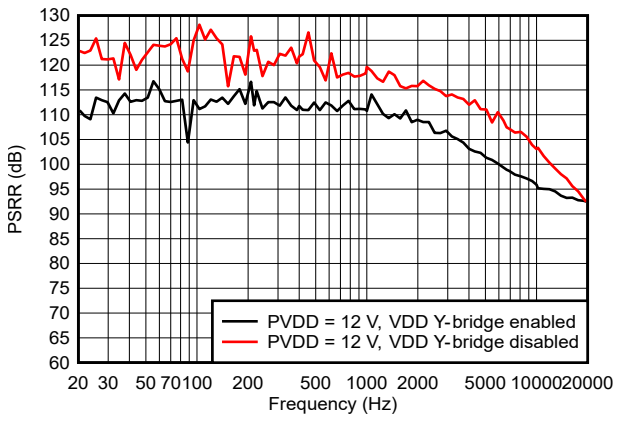
R_L = 8 Ω

Figure 5-42. Audio channel frequency response



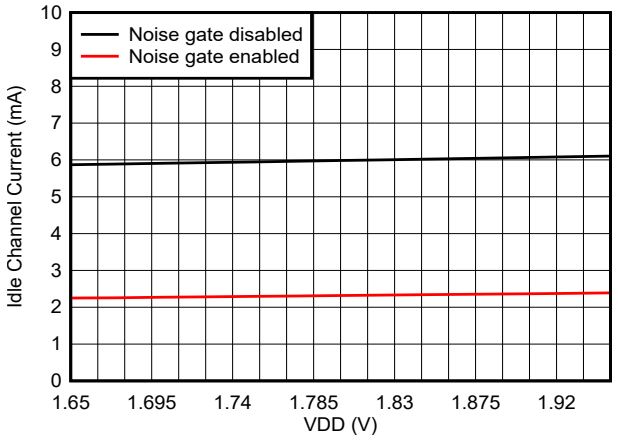
R_L = 8 Ω 1S Boost Mode

Figure 5-43. PSRR vs Frequency



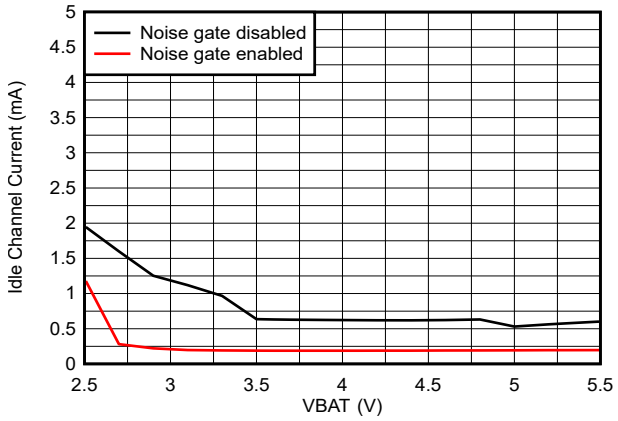
R_L = 8 Ω External PVDD Mode

Figure 5-44. PSRR vs Frequency



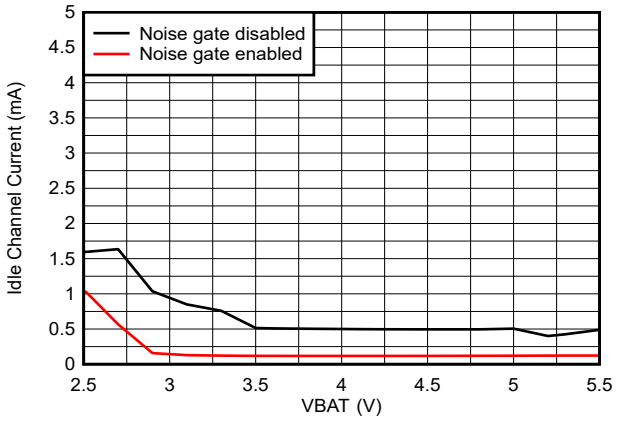
R_L = 8 Ω

Figure 5-45. Idle channel current vs VDD voltage



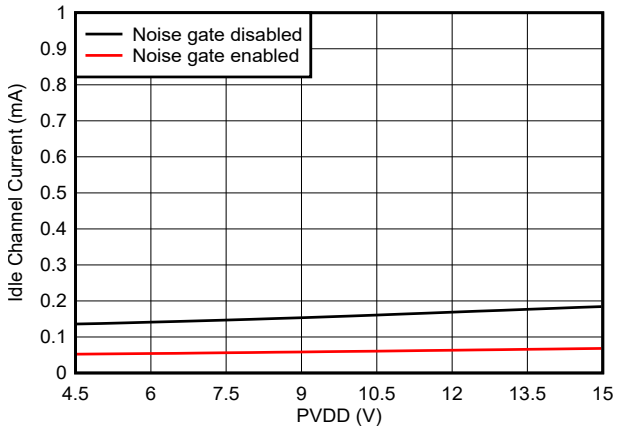
R_L = 8 Ω 1S Boost Mode

Figure 5-46. Idle channel current vs VBAT voltage



R_L = 8 Ω External PVDD Mode

Figure 5-47. Idle channel current vs VBAT voltage



R_L = 8 Ω External PVDD Mode

Figure 5-48. Idle channel current vs PVDD voltage

6 Detailed Description

6.1 Overview

The TAS2120 is a mono digital input Class-D amplifier optimized for delivering the highest efficiency across all powers for longer battery life operation. It comes with a small solution size for board space-constrained applications. It integrates Class-H Boost with 33mV step size resolution for class-H control, battery/temperature sensors for system-level protection features.

6.2 Functional Block Diagram

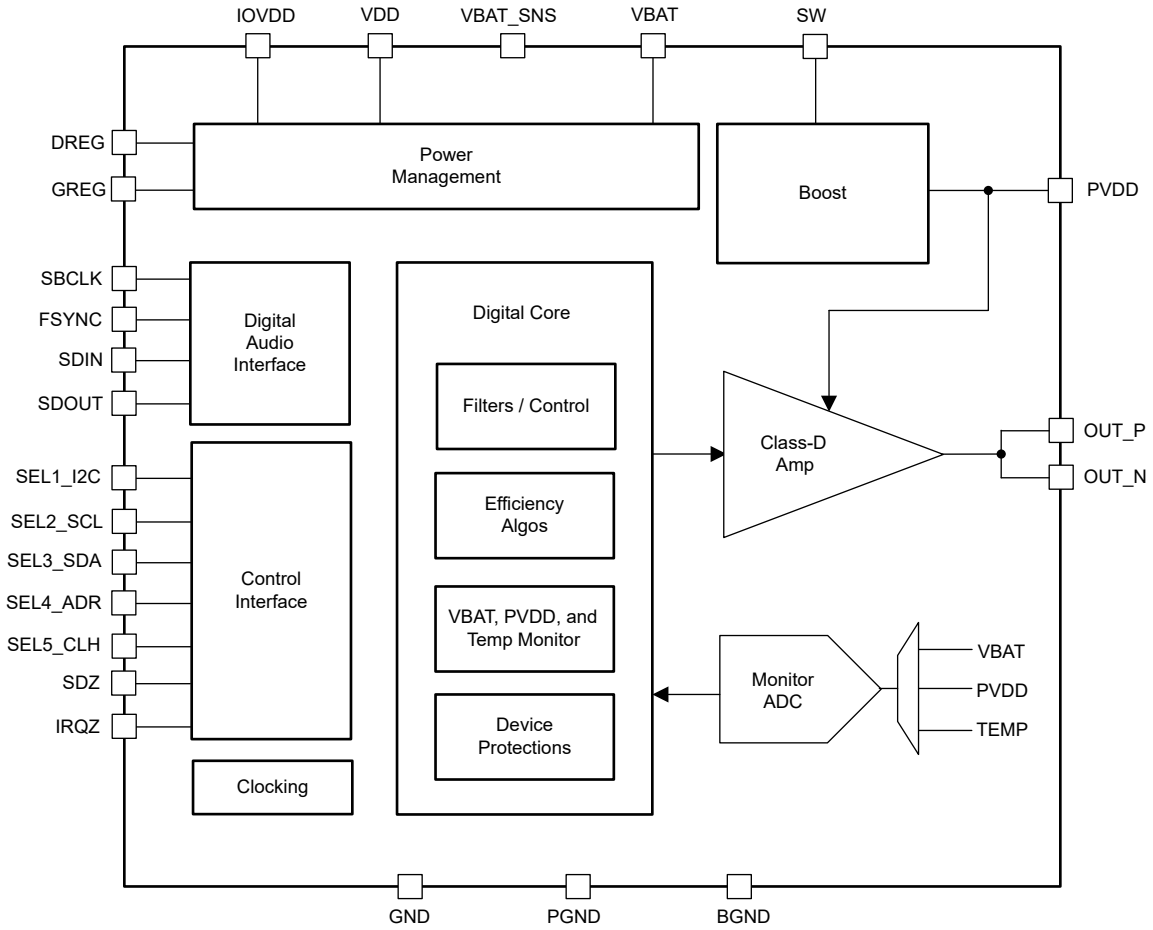


Figure 6-1. Top Level Functional block diagram

6.3 Device Functional Modes

6.3.1 Operational Modes

6.3.1.1 Hardware Shutdown

The device can be powered down by asserting SDZ pin low. The shutdown behavior of the device when SDZ pin is pulled low is controlled by SDZ_MODE register settings.

In Hardware Shutdown mode (SDZ_MODE[1:0] = 00 or 01) if the SDZ pin is asserted low, the device consumes the minimum quiescent current from supplies. All registers lose state in this mode and go back to default settings, and I^2C communication is disabled.

If configured in SDZ_MODE[1:0] = 00, when the SDZ pin is asserted low while audio is playing, the device will follow the normal power down sequencing like volume ramp down on the audio (if enabled), stop the Class-D

switching, power down analog and digital blocks to ensure no power down pop and finally put the device into Hardware Shutdown mode. I²C communication is disabled while the SDZ pin is asserted low in this mode.

If configured in SDZ_MODE[1:0] = 01, when the SDZ pin is asserted low the device will immediately enter the hardware shutdown and will not go through any power-down sequencing routine. It is recommended to ensure that the audio input signal is ramped down to the idle channel before asserting the SDZ pin low in this mode, device software mute mode can be used to realize this. I²C communication is disabled while the SDZ pin is asserted low in this mode.

Finally, the device can be configured to Software shutdown mode by setting SDZ_MODE[1:0] = 10. In this mode, when the SDZ pin is pulled low, the device will follow normal power-down sequencing and enter software shutdown mode. All the device register configuration programmed is retained as is from the state the device was in before the SDZ pin was pulled low. I²C communication is still available while the SDZ pin is asserted low in this mode.

Table 6-1. Shutdown Control

SDZ_MODE[1:0]	Configuration
00 (default)	Hardware shutdown mode with power-down sequencing
01	Hardware shutdown mode - immediate
10	Software shutdown mode (All register values retained)
11	Reserved

When SDZ_MODE[1:0] is 00 or 10, the device goes through shutdown sequencing and the SDZ pin must be held low for the entire duration of the shutdown time. The shutdown time is specified in the Power up/down Time section of the Electrical Characteristics section. When SDZ is released, the device will sample relevant configuration and address pins then enter software shutdown mode.

6.3.1.2 Hardware Config Modes

The TAS2120 device can operate in a Pin control based HW Mode depending on the resistor terminations used for Select Pin1 to Select Pin5. Pin control based HW Mode behavior of the device is designed to simplify device configuration without using any software based configurations through I²C communication.

Table 6-2. Select Pin Functionalities

Select Pin Name	Functionality
SEL1	Amplifier gain setting with volume ramp enable/disable option
SEL2	I2S, TDM, Left justified selection
SEL3	Data valid rising/falling edge selection
SEL4	Y-bridge threshold configuration
SEL5	Supply voltage mode selection

Table 6-3. SEL1 HW Mode configuration

SEL1 Connection	Amplifier Gain	Volume Ramp
Direct Short to GND	Configured through I²C	Configured through I²C
1.2kΩ to GND	6 dBV	Disabled
1.2kΩ to VBAT	12 dBV	Disabled
5kΩ to GND	18 dBV	Disabled
330Ω to VBAT	21 dBV	Disabled
5kΩ to VBAT	6 dBV	Enabled

Table 6-3. SEL1 HW Mode configuration (continued)

SEL1 Connection	Amplifier Gain	Volume Ramp
24kΩ to GND	12 dBV	Enabled
24kΩ to VBAT	18 dBV	Enabled
Direct Short to VBAT	21 dBV	Enabled

Table 6-4. SEL2 HW Mode configuration

SEL2 Connection	Configuration
Direct Short to GND	I^2S L or TDM0
330Ω to IOVDD	I^2S R or TDM1
Direct Short to IOVDD	I^2S (L+R)/2 or TDM2
1.2kΩ to GND	Left-Justified L or TDM3
1.2kΩ to IOVDD	Left-Justified R or TDM4
5kΩ to GND	Left-Justified (L+R)/2 or TDM5
5kΩ to IOVDD	I^2S L or TDM6
24kΩ to GND	I^2S R or TDM7
24kΩ to IOVDD	Reserved

Table 6-5. SEL3 HW Mode configuration

SEL3 Connection	Configuration
Direct Short to GND	Data valid on rising edge
Direct Short to IOVDD	Data valid on falling edge

Table 6-6. SEL4 HW Mode configuration

SEL4 Connection	Configuration
Direct Short to GND	Y-bridge threshold of 80mW
Direct Short to IOVDD	Y-bridge threshold of 40mW
24kΩ to IOVDD	Y-bridge threshold of 1mW

Table 6-7. SEL5 HW Mode configuration

SEL5 Connection	Configuration
Direct Short to GND	1S Boost Mode
Direct Short to IOVDD	External PVDD Mode
24kΩ to IOVDD	2S Boost Mode

6.3.1.3 Software Power Modes Control and Software Reset

When SEL1 pin is shorted to GND, TAS2120 is configured in I^2C Mode and can be configured by modifying configuration registers over I^2C interface.

TAS2120 power state can be controlled using the register MODE[1:0]. Change in any of the MODE settings will not cause the device to lose any of the existing device configuration register settings.

Table 6-8. Software Mode Control

MODE[1:0]	Configuration
00	Device in active mode of operation
01	Reserved
10 (default)	Device in software shutdown mode
11	Device in Clock based Active and shutdown mode

Active state: When MODE[1:0] is configured as '00', the device enters an active mode of operation with proper power-up sequencing to minimize the click and pop.

Software shutdown state: When MODE[1:0] is configured as '10', the device enters software shutdown mode. This mode powers down all analog blocks required to playback audio but does not cause the device to lose register state. If audio is playing when Software Shutdown is asserted, the Class-D will volume ramp down before shutting down. When de-asserted, the Class-D will begin switching and volume ramp back to the programmed digital volume setting.

Clock based Active and shutdown state: When MODE[1:0] is configured as '11' the device toggles between Active and Shutdown state based on valid ASI clock signals applied on the ASI input pins, BCLK and FSYNC. When clocks are applied, the device will automatically detect the clock signals and follow proper power-up sequencing to avoid any power-up click and pop. When the audio channels are powered up and the ASI clock is removed, the device will automatically start power-down sequencing and avoid any click and pop. It is recommended to do a volume ramp-down in the input data stream before stopping the clocks for the best pop & click experience (device software mute mode can be used to realize this).

TAS2120 can be reset to its default configuration by setting the SW_RESET register to '1'. If the device is powered up, when the SW_RESET bit is set high, all the channels are powered down immediately. All the registers are restored to the default state when SW_RESET is set high. This bit is self-clearing and goes back to '0' once the reset is complete.

The device can also signal to the host once the status of the device reaches Active mode of operation using the *INT_LTCH0[1]* bit (Section 6.3.2). This bit is a live device status bit and reflects the device status in real-time. This bit is set high when the device is in Active mode and set low when the device is in shutdown mode.

6.3.1.4 Efficiency and power saving modes

TAS2120 has multiple power-saving modes of operation designed to achieve the highest system level efficiency under all operating conditions. The device transitions from one mode to the next based on the configured mode and the signal condition. The transitions from one mode to another are automatic and designed to ensure high-performance audio levels during the transition of the modes.

EFFICIENCY_MODE[1:0] register allows for configuration of the Music efficiency and Noise gate modes of operation

6.3.1.4.1 Noise Gate

When the Noise gate feature is enabled, the device automatically detects periods of silence during active playback mode and reduces the idle channel power consumption significantly to extend the battery life. This feature is useful for signals playback having long periods of silence, eg voice calls, movie tracks, etc.

The device monitors the input audio signal level against the programmed Noise gate threshold configured by the *NG_TH_LVL[2:0]* register. When the audio signal falls below the threshold, an internal Hysteresis timer is enabled. If the signal level remains below the configured *NG_TH_LVL[2:0]* for the entire duration of the *NG_HYST_TIMER[1:0]*, the device enters into the Noise gate mode and reduces the idle channel power consumption. In the Noise gate mode of operation, the high switching blocks like class-D PWM output are turned OFF and outputs are pulled low. The output impedance of class-D can be controlled when the Noise gate mode is active using the *CLASSD_HIZ_MODE* register. While the Noise gate mode is active, class-D outputs are not switching and the device does not produce any audio output signal. When the device is in Noise gate mode, the *NG_STATUS* bit is set as high and when the device comes out of noise gate mode, the status bit is set to low.

When the signal level increases above the NG_TH_LVL[1:0], the device automatically wakes up the blocks in low IQ mode and starts playing out the audio input signals. The wake up from Noise gate maintains the signal fidelity by buffering the input signal data during the transition time from noise gate mode to active playback mode. The device does not lose any audio input samples while transitioning from noise gate to active playback.

The transition into noise gate mode and recovery out of noise gate mode is designed to be click and pop-free by following the proper shutdown and power up sequencing.

Table 6-9. Noise gate threshold

NG_TH_LVL[2:0]	Configuration
000	-85 dBFs
001	-90 dBFs
010	-95 dBFs
011	-100 dBFs
100 (default)	-105 dBFs
101	-110 dBFs
110	-115 dBFs
111	-120 dBFs

Table 6-10. Noise gate hysteresis timer

NG_HYST_TIMER[1:0]	Configuration
00	10 ms
01 (default)	50 ms
10	100 ms
11	1000 ms

6.3.1.4.2 Music Efficiency Mode

When the Music efficiency mode feature is enabled, the device automatically detects low-power signal states during active playback mode and reduces the overall I_Q power consumption to extend the battery life. This feature is useful for dynamic audio signals with varying signal levels for example music tracks, voice calls movie tracks, and so forth.

The device monitors the input audio signal level against the programmed Music efficiency threshold configured by the *MUSIC_EFF_MODE_THR[23:0]* register. When the audio signal falls below the threshold, an internal hysteresis timer is enabled. If the signal level remains below the configured *MUSIC_EFF_MODE_THR[23:0]* for the entire duration of the *MUSIC_EFF_MODE_TIMER[23:0]*, the device enters into the Music efficiency mode. When the device is in Music efficiency mode, the *MUSIC_EFF_STATUS* bit is set as high and when the device comes out of music efficiency mode, the status bit is set low.

When the signal level increases above the *MUSIC_EFF_MODE_THR[23:0]*, the device automatically wakes up the blocks in low I_Q mode and continues playing out the audio input signals. The transition from Music efficiency mode to normal operation occurs with minimal click and pop. While the device is in Music efficiency mode, the audio channel performance is maintained and doesn't impact the output signal level or noise.

The *MUSIC_EFF_MODE_THR[23:0]* and *MUSIC_EFF_MODE_TIMER[23:0]* registers can be configured using the PPC3 Software Section 6.4.1.

6.3.1.4.3 VDD Y-bridge

TAS2120 uses a Y-bridge output stage for switching the class-D output PWM voltage between the VDD and PVDD supply. When the feature is enabled using *EN_Y_BRIDGE_MODE* set to high, the device will automatically select the output voltage to switch the output PWM at. When the signal level is low, the output will switch at VDD to enable higher system-level efficiency by reducing the class-D output switching voltage. When the signal level is high, the output switches on the PVDD voltage rail set by the integrated Boost, or external PVDD in the external PVDD mode of operation.

The device monitors the input audio signal level against the programmed Y-bridge mode threshold configured by *VDD_MODE_THR_LVL[23:0]* register. When the audio signal falls below the threshold, an internal hysteresis

timer is enabled. If the signal level remains below the configured *YBRIDGE_HYST_TIMER[1:0]* for the entire duration of the selected time, the device enters into the lower voltage VDD supply-based PWM switching mode.

When the signal level increases above the *VDD_MODE_THR_LVL[23:0]* plus *VDD_MODE_HYST[23:0]*, the device starts switching the output PWM signal on PVDD supply without introducing any signal clipping.

The *VDD_MODE_THR_LVL[23:0]* and *VDD_MODE_HYST[23:0]* registers can be configured using the PPC3 Software Section 6.4.1.

Table 6-11. VDD Y-bridge hysteresis timer

YBRIDGE_HYST_TIMER[1:0]	Configuration
00	100us
01 (default)	500us
10	5ms
11	50ms

Table 6-12. VDD Y-bridge enable

EN_Y_BRIDGE_MODE	Configuration
0	Y-bridge mode is disabled
1 (default)	Y-bridge mode is enabled

6.3.1.4.4 Class-H Boost

TAS2120 has an advanced class-H algorithm to control the integrated Boost. The class-H algorithm enables Boost supply to closely track audio signal levels and achieve high system level efficiency for extending battery life. Class-H mode is enabled using the *BST_MODE[1:0]* register.

The class-H algorithm buffers the input signal to enable sufficient look-ahead time required to charge the Boost output capacitor and avoid any signal clipping. The algorithm monitors the input signal level and uses system-level parameters configured in PPC3 software like Boost output voltage, Boost output capacitor, channel gain, and so forth. and computes the most optimum class-H tuning parameters. These tuning parameter registers are then calculated in the PPC3 software and configured in the corresponding *CLASSH_TUNING_x[23:0]* registers.

When the BST_MODE[1:0] is configured to use the device in Class-G mode or Boost always-ON mode, the max inrush current from the battery can be controlled by setting the Inrush current parameter in PPC3 software. The software generates the required coefficients in the CLASSH_TUNING_x[23:0] register based on the system level parameters configured like Boost output capacitor, Inrush current required, and so forth.

6.3.1.5 2S Battery Mode

TAS2120 can be configured to function for different battery systems like single series cell (1S) Li-ion battery (2.5V to 5.5V) or 2-series cell (2S) series cell battery (4.7V to 10V). When the 2S battery is selected for the device, the diagram below shows the conceptual connections in the system to connect the 2S battery. When selected for 2S battery operation, the VBAT pin of the device is used for biasing internal blocks and needs to be supplied from external power source between 3.0V to 5.5V.

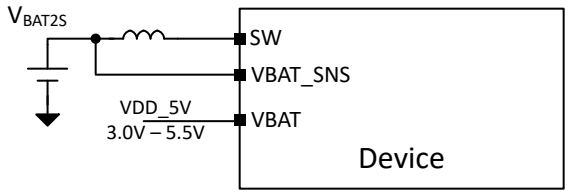


Figure 6-2. 2S Battery Mode System Configuration

The internal battery voltage monitor needs to be switched to sense the voltage on the VBAT_SNS pin instead of the default sensing done on the VBAT pin. *SEL_VBAT_MODE[1:0]* configures the internal voltage monitor and the device configuration between 1S or 2S battery systems.

When SEL_VBAT_MODE[1:0] is set as '10', in example 2S mode of operation, the device internal bias voltage needs to be configured based on *VBAT_BIAS_SELx* registers. If the VBAT pin voltage is available from the center tap or half of the 2S battery voltage, the *VBAT_BIAS_SEL1* needs to be set high. For other VBAT voltage configurations the *VBAT_BIAS_SEL1* should be set low and appropriate *VBAT_BIAS_SEL2* configuration should be selected.

Table 6-13. Battery mode selection

SEL_VBAT_MODE[1:0]	Configuration
00 (default)	Voltage monitor on VBAT pin. 1S mode of operation
01	Voltage monitor on VBAT_SNS pin. 1S mode of operation
10	Voltage monitor on VBAT_SNS pin. 2S mode of operation
11	Reserved

Table 6-14. VBAT pin bias voltage selector

VBAT_BIAS_SEL1	Configuration
0 (default)	VBAT pin biasing based on *VBAT_BIAS_SEL2* register
1	VBAT pin voltage is half of 2S battery voltage

Table 6-15. VBAT pin bias voltage selector

VBAT_BIAS_SEL2[1:0]	Configuration
00	Reserved
01(default)	Minimum VBAT pin voltage > 2.9V
10	Minimum VBAT pin voltage > 3.3V
11	Minimum VBAT pin voltage > 3.7V

6.3.1.6 External PVDD Mode

The internal Boost of TAS2120 can be disabled by setting *BST_EN* register low. When the external PVDD mode is used, the class-D amplifier is directly powered from the voltage source on PVDD pin. The device configurations needs to be updated using PPC3 software to configure the device in required performance configurations for external PVDD mode of operation.

6.3.2 Faults and Status

During power-up sequencing, the power-on-reset circuit (POR) monitors the VDD and IOVDD pins and holds device in reset (including all the configuration registers) until the supplies are valid. Any supply voltage dip on VDD or IOVDD below the UVLO voltage thresholds resets the device immediately along with all the register configurations.

During operation modes, the device monitors internal device status and fault conditions and can notify the host of error and status conditions using the IRQZ interrupt pin and internal I^2C based interrupt registers. The interrupt generation in IRQZ pin can be masked by configuring the corresponding Interrupt mask register bit.

Table 6-16 lists the different faults and interrupts that the device monitors and the corresponding configuration bits to enable/disable the interrupt generation and reading the I2C interrupt status

Table 6-16. Faults and Interrupts

Category	Interrupt	Interrupt Mask register bit	Default Mask status	Interrupt Latched status bit
Limiter & Brown out protection Section 6.4.2.4	Brownout detected	*INT_MASK0[3]*	Not Masked	*INT_LTCH0[3]*
	BOP Active	*INT_MASK0[2]*	Not Masked	*INT_LTCH0[2]*
	BOP infinite hold	*INT_MASK0[7]*	Not Masked	*INT_LTCH0[7]*
	Limiter Active	*INT_MASK0[4]*	Not Masked	*INT_LTCH0[4]*
	Limiter attenuation	*INT_MASK0[6]*	Not Masked	*INT_LTCH0[6]*
	Supply below inflection point	*INT_MASK0[5]*	Not Masked	*INT_LTCH0[5]*
Supply Voltage Monitors Section 6.4.7	PVDD Over voltage	*INT_MASK3[2]*	Not Masked	*INT_LTCH3[2]*
	PVDD Under voltage	*INT_MASK1[7]*	Not Masked	*INT_LTCH1[7]*
	VBAT2S supply under voltage	*INT_MASK1[6]*	Not Masked	*INT_LTCH1[6]*
	VBAT supply under voltage	*INT_MASK4[7]*	Not Masked	*INT_LTCH4[7]*
Thermal protection Section 6.4.8	Thermal warning at 135C	*INT_MASK1[4]*	Masked	*INT_LTCH1[4]*
	Thermal warning at 125C	*INT_MASK1[3]*	Masked	*INT_LTCH1[3]*
	Thermal warning at 115C	*INT_MASK1[2]*	Masked	*INT_LTCH1[2]*
	Thermal warning at 105C	*INT_MASK1[1]*	Masked	*INT_LTCH1[1]*
	Over temperature error	*INT_MASK3[7]*	Not Masked	*INT_LTCH3[7]*
Clock protection Section 6.4.9.1	Watchdog expiry	*INT_MASK2[7]*	Not Masked	*INT_LTCH2[7]*
	Frame out of sync	*INT_MASK2[5]*	Masked	*INT_LTCH2[5]*
	PLL clock error	*INT_MASK2[4]*	Not Masked	*INT_LTCH2[4]*
	TDM clock error	*INT_MASK2[3]*	Masked	*INT_LTCH2[3]*
	Pre-Power-up Clock error	*INT_MASK4[2]*	Not Masked	*INT_LTCH4[2]*
	Clock ratio change error	*INT_MASK2[2]*	Masked	*INT_LTCH2[2]*
	Fs change error	*INT_MASK2[1]*	Masked	*INT_LTCH2[1]*
	Fs invalid error	*INT_MASK2[0]*	Masked	*INT_LTCH2[0]*
	Frame out of sync	*INT_MASK2[5]*	Masked	*INT_LTCH2[5]*
	Internal PLL Clock error	*INT_MASK2[4]*	Not Masked	*INT_LTCH2[4]*
	Digital watchdog	*INT_MASK2[7]*	Not Masked	*INT_LTCH2[7]*
Other Protections & Status	Class-D Over current error	*INT_MASK3[3]*	Not Masked	*INT_LTCH3[3]*
	Device Active	*INT_MASK0[1]*	Masked	*INT_LTCH0[1]*

6.3.2.1 Interrupt generation and clearing

The IRQZ is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to IOVDD. An internal pull up resistor (18kΩ) is provided in the device and can be assessed by setting the *IRQZ_PU* register bit.

The interrupt generation on IRQZ pin can be configured using *IRQZ_PIN_CFG[1:0]* register. For the interrupts that have auto retry feature, the retry timer can be configured using *RETRY_WAIT_TIME* register. The interrupt pin polarity can be changed from the default case of Active Low to Active high by setting the *IRQZ_POL* register bit high.

Any latched interrupt can be cleared by setting INT_CLR_LTCH bit high. This is self clearing bit and automatically gets updated to low once the interrupt is cleared. Interrupts can also be cleared by hardware shutdown by pulling the SDZ pin low, or by software reset using SW_RESET bit.

Table 6-17. IRQZ pin configuration

IRQZ_PIN_CFG[1:0]	Configuration
00	Reserved
01(default)	Interrupt generated on any unmasked latched interrupt
10	Reserved
11	Interrupt generated for 2 to 4 ms every 4 ms on any unmasked latched interrupt

Table 6-18. Retry wait timer

RETRY_WAIT_TIME	Configuration
0 (default)	Retry every 1.5sec
1	Retry every 100ms

6.4 Feature Description

6.4.1 PurePath™ Console 3 Software

The TAS2120's advanced features and device configuration can be performed using PurePath Console 3 (PPC3) software. The base PPC3 software can be downloaded and installed from TI website. Once installed the TAS2120 application can be downloaded with-in base PPC3 software. The TAS2120 PPC3 application calculates necessary register coefficients that are described in the following sections so it is highly recommended to use PPC3 in I^2C Mode. The device configurations are optimized using register updates based on the options selected in PPC3. This is the recommended method to configure the device for best performance. Once TAS2120 PPC3 application calculates and updates the device, End System Integration tab in PPC3 can be used to generate files for final system integration.

6.4.2 Playback Signal Path

6.4.2.1 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier's analog gain level (A_{AMP}) and digital volume control (A_{DVC}). Equation 1 calculates the amplifiers output voltage. Amplifier analog gain setting should be set before powering up the playback channel and shouldn't be changed while the channel is active. The digital volume control can be modified while the channel is active and also allows for soft volume ramp up/down feature to allow for smooth transition of output voltage from one level to another.

$$V_{AMP} = \text{Input} + A_{dvc} + A_{AMP} \ \text{dBV} \quad (1)$$

where

- V_{AMP} is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0 dBFS
- A_{DVC} is the digital volume control setting, 6 dB to -110 dB in 0.5 dB steps
- A_{AMP} is the amplifier output level setting, -0.071dBV to 21.0dBV in 0.5017dBV steps.

Amplifier output level settings are presented in dBV (dB relative to 1 V_{rms}) with a full scale digital audio input (0 dBFS) and the digital volume control set to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used to convey gain only.

Table below shows gain settings that can be programmed via the *AMP_LVL* register. When AMP_LVL is set to less than 9dBV settings, the playback channel is automatically configured to low noise mode or receiver mode of operation.

Table 6-19. Amplifier Output Level Settings

AMP_LVL[5:0]	FULL SCALE OUTPUT	
	dBV	V_{PEAK} (V)
0x00	21.000	15.9
0x01	20.498	15.0
0x02	19.997	14.1
0x03	19.495	13.3
0x04	18.993	12.6
...	...	...
0x27	1.434	1.7
0x28	0.932	1.6
0x29	0.430	1.5
0x2A	-0.071	1.4
0x2B-0x3F	Reserved	Reserved

When a change in digital volume control occurs, the device ramps the volume to the new setting based on the *DVC_SLEW_RATE* register bits. If *DVC_SLEW_RATE* is set to 0x7FFFFF, volume ramp is disabled. This can be used to speed up start up, shutdown and digital volume changes when volume ramp is handled by the system host. When volume ramp is disabled, the input audio data stream should be held at digital silence during shutdown and power up of the device to avoid any clicks and pops.

The device can be put in software based mute by setting DVC_LEVEL to 0x000000 setting.

The digital voltage control registers *DVC_LEVEL* and DVC_SLEW_RATE registers can be configured using the PPC3 Software Section 6.4.1.

Table 6-20. Digital Volume Control

DVC_LEVEL[23:0]	VOLUME (dB)
0x000000	Software MUTE
0x00000D (MIN)	-110
...	...
0x400000	0 (default)
...	...
0x7FB261 (MAX)	6

Table 6-21. Digital Volume Ramp Rate

DVC_SLEW_RATE[23:0]	RAMP RATE @ 48kHz (s)
0x00036A	1000ms
...	
0x034A51	4ms (default)
...	
0x7FFFFF	0 - Ramp disabled

6.4.2.2 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers. The playback path employs a high-pass filter (HPF) to prevent this from occurring. The HPF is a 1st order filter and can be changed from the default 2 Hz for 48ksps fs using the *AUDIO_HPF_N0*, *AUDIO_HPF_N1*, *AUDIO_HPF_D1* registers. The HPF filter frequency scales with change in the FSYNC clock and can be re-configured to achieve the required cutoff frequency for different FSYNC clock frequencies. The coefficients can also be changed to disable the HPF coefficients appropriately. These coefficients should be calculated and set using PPC3 Software Section 6.4.1.

6.4.2.3 Class-D Amplifier

TAS2120 has integrated high performance class-D amplifier with low idle channel noise, low distortion and high PSRR. The Class-D amplifier switches on a clock frequency derived from the SBCLK frequency and is always synchronized to the input clock source. The *SAMP_RATE_CFG* register enables selection between input clock source based out of multiple of 44.1kHz vs 48kHz multiples.

Table 6-22. Sample rate configuration

SAMP_RATE_CFG	Configuration
0 (default)	Audio data rate is multiple/sub-multiple of 48ksps
1	Audio data rate is multiple/sub-multiple of 44.1ksps

For improvements in EMI performance the class-D amplifier supports programmable Edge rate control (ERC) and class-D clock spread spectrum modulation (SSM).

The edge rate of class-D can be controlled using *CLASSD_OUTPUT_EDGERATE_CTRL[1:0]* register. By default the class-D output edge rate is configured to fastest setting to enable high efficiency in the system. The class-D output edge rate can be slowed down using other configuration settings to reduce the EMI energy at high frequency with reduction in efficiency. The exact rate of change of output edge rate varies based on output load conditions, and the values mentioned in the tables below are approximate edge rate levels for default loading conditions.

Table 6-23. Class-D output edge rate control

CLASSD_OUTPUT_EDGERATE_CTRL[1:0]	Configuration
00	Class-D output edge rate of 0.5 V/ns
01	Class-D output edge rate of 1.0 V/ns
10	Reserved
11(default)	Class-D output edge rate of 2 V/ns

The class-D amplifier has over current protection on each of the output power FETs, including the PVDD High side, VDD high side and the ground power FETs.

The class-D amplifier output impedance can be controlled when the outputs stop switching during Noise gate mode using *CLASSD_HIZ_MODE* control register.

Table 6-24. Class-D high-Z mode control

CLASSD_HIZ_MODE	Configuration
0 (default)	Output pulled down with 2.5kΩ
1	Output pulled down with >13kΩ

6.4.2.4 Supply Tracking Limiters with Brown Out Prevention

TAS2120 monitors class-D supply voltage along with the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions. The limiter and brown out module calculates the signal attenuation required based on the condition of the signal level, channel gain and the selected supply voltage.

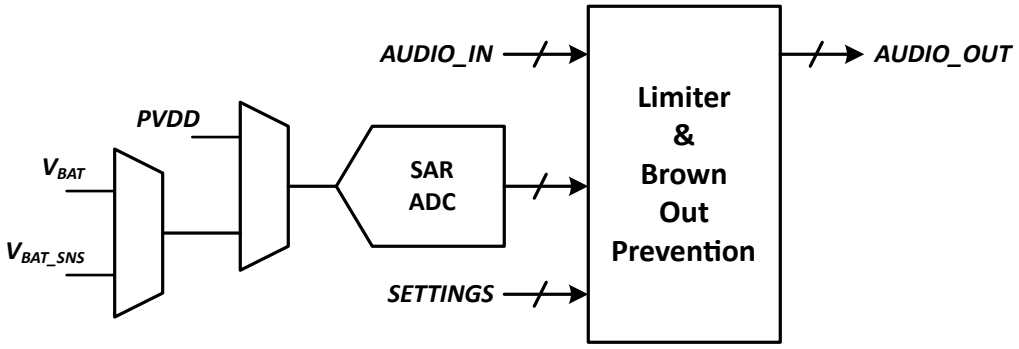


Figure 6-3. Limiter and Brown out protection module

The Brown Out Prevention (BOP) module provides a priority input to provide a fast response to transient dips in the battery supply. The BOP feature can be enabled by configuring the register bit *BOP_EN* high. The supply voltage that is tracked to determine Brown out conditions can be configured as V_{BAT}/V_{BAT_SNS} or PVDD based on system configuration needs by using *BOP_SRC* register bit. When the selected supply dips below the brown-out threshold configured by setting register *BOP_THR_LVL[23:0]*, the BOP will begin reducing gain. The rate of gain reduction (db/sample) can be configured by setting the *BOP_ATK_RATE[23:0]* registers . When the supply voltage rises above the brownout threshold, the BOP will begin to release the gain after the programmed hold timer, *BOP_HLD_COUNT[23:0]*. The BOP feature uses the *LIM_RLS_RATE[23:0]* register setting to release after a brown out event. The release rate is rate of gain increase in db/sample ratio. During a BOP event the limiter updates will be paused. This is to prevent a limiter from releasing during a BOP event.

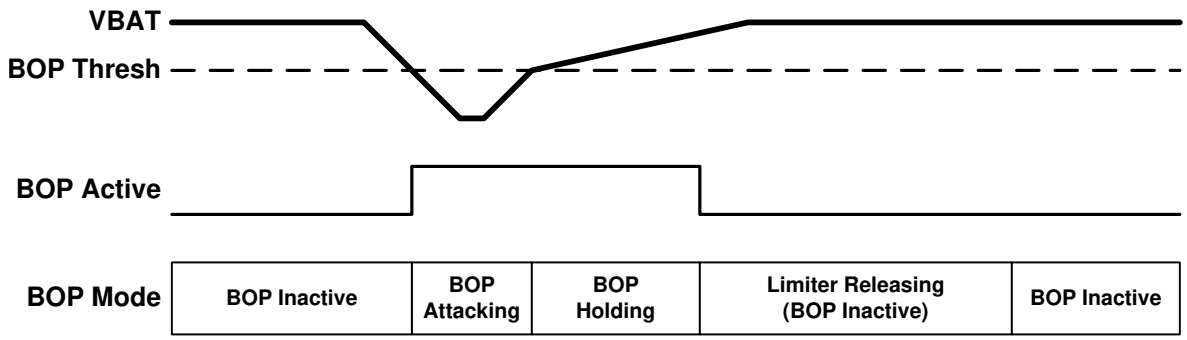


Figure 6-4. Brown Out Prevention Event

The device can be configured to hold the gain attenuation once a BOP event is detected by setting the register bit *BOP_INF_HLD* high. When the bit is programmed high, the Limiter and BOP module does not release the gain attenuation and holds the device in the programmed min gain attenuation level until the infinite hold is cleared by setting the register bit *BOP_HLD_CLR* high. The hold clearing bit is self clearing and will automatically reset to low state once the hold is cleared.

A hard brownout level can be set to shutdown the device if the BOP gain attenuation cannot mitigate the drop in battery voltage. The brown out based shutdown of the device is enabled when *BOPSD_EN* bit is set high and shuts down when the battery voltage falls below the voltage threshold set by *BOSD_THR_LVL[23:0]* register bits.

A maximum level of attenuation applied by the limiters and brown out prevention feature is configurable via the *LIM_MAX_ATN* register. This attenuation limit is shared between the features. For instance, if the maximum attenuation is set to 6 dB and the limiters have reduced gain by 4 dB, the brown out prevention feature will only be able to reduce the gain further by another 2 dB. If the limiter or brown out prevention feature is attacking and it reaches the maximum attenuation, gain will not be reduced any further.

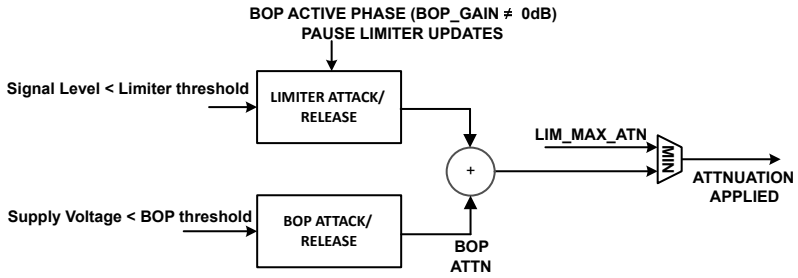


Figure 6-5. Limiter and Brown out gain attenuation

6.4.2.4.1 Voltage Limiter and Clipping protection

The supply tracking limiter can be configured using *LIM_MODE[1:0]* register. In the VBAT voltage mode, the limiter tracks the VBAT supply voltage for voltage limiter and in PVDD voltage mode, the limiter tracks the PVDD voltage for external PVDD mode of use case.

Table 6-25. Limiter mode selection

LIM_MODE[1:0]	Configuration
00 (default)	Disabled
01	VBAT voltage based limiter
10	PVDD voltage based limiter
11	Reserved

The limiter can be configured to reduce the output signal based on fixed signal threshold level, or it can attenuate signal based on a dynamic threshold which tracks the selected supply voltage. The register bit *SUPPLY_HEADROOM_LIM_MODE* enables the dynamic supply tracking and can be used to limit the clipping distortion when the supply voltage is varying in the system.

Table 6-26. Limiter dynamic supply headroom tracking mode

SUPPLY_HEADROOM_LIM_MODE	Configuration
0(default)	Disabled
1	Enabled. Limiter threshold is dynamically changed based as a fixed percentage of monitored supply voltage.

When *SUPPLY_HEADROOM_LIM_MODE* is set high, the limiter sets the threshold as a fixed percentage of the monitored supply voltage. The limiter begins reducing gain when the output signal level is greater than the threshold configured. For eg, if voltage limiting is desired to be 10% below the supply voltage, then *LIM_SLOPE[23:0]* is configured as 0.9 and the threshold is calculated as monitored supply voltage multiplied by 1.1. Similarly if the *LIM_SLOPE[23:0]* is configured at > 1.0, the limiter threshold is set at higher than the supply voltage, and a small amount of controlled clipping occurs.

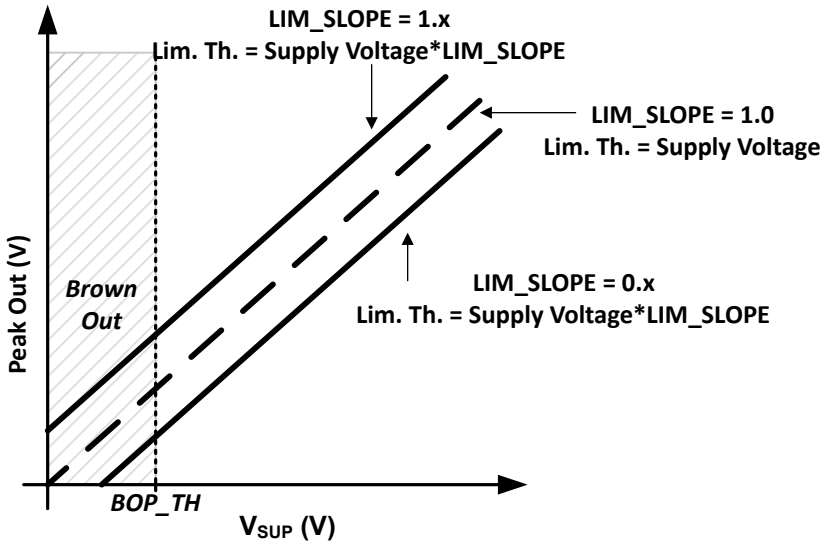


Figure 6-6. Limiter with dynamic supply headroom

When *SUPPLY_HEADROOM_LIM_MODE* is set low, the limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track selected supply below a programmable inflection point with a minimum threshold value. Figure 6-7below shows the limiter configured to limit to a constant level regardless of the selected supply level. To achieve this behavior, set the limiter maximum threshold to the desired level using *LIM_TH_MAX[23:0]*. Set the limiter inflection point using *LIM_INF_PT[23:0]* below the minimum allowable supply setting. The limiter minimum threshold register *LIM_TH_MIN[23:0]* does not impact limiter behavior in this use case.

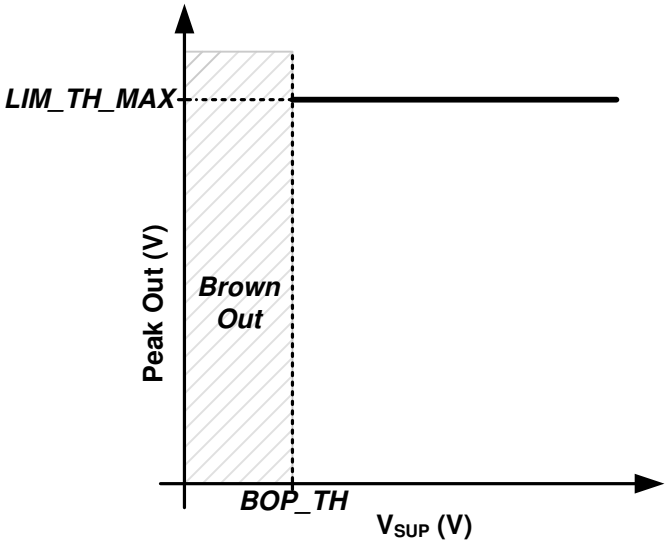


Figure 6-7. Limiter with Fixed Threshold

Figure 6-8 shows how to configure the limiter to track selected supply below a threshold without a minimum threshold. Set the *LIM_TH_MAX[23:0]* register to the desired threshold and *LIM_INF_PT[23:0]* register to the desired inflection point where the limiter begins to reduce the threshold with the selected supply. The *LIM_SLOPE[23:0]* register bits can be used to change the slope of the limiter tracking the supply voltage in V/V. For example, a slope value of 1 V/V reduces the limiter threshold 1 V for every 1 V of drop in the supply voltage. Program the *LIM_TH_MIN[23:0]* below the minimum of the selected supply to prevent the limiter from having a minimum threshold reduction when tracking the selected supply.

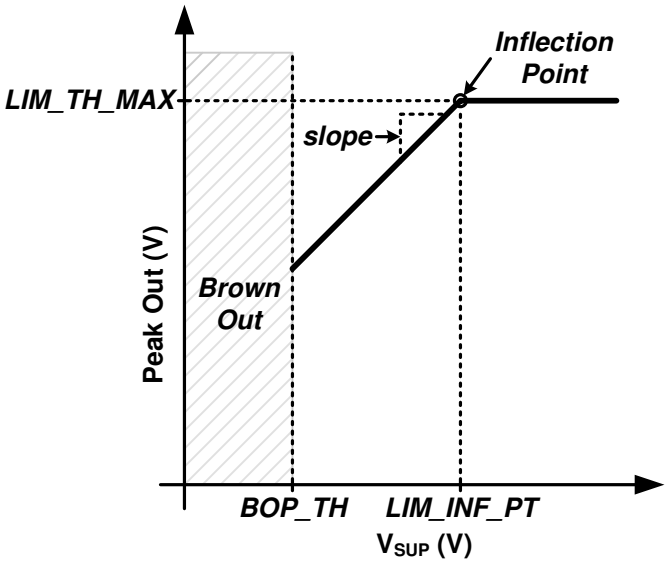


Figure 6-8. Limiter with Inflection Point

To achieve a limiter that tracks the selected supply below a threshold, configure the limiter as explained in the previous example, except program the *LIM_TH_MIN[23:0]* register to the desired minimum threshold. This is shown in Figure 6-9 below.

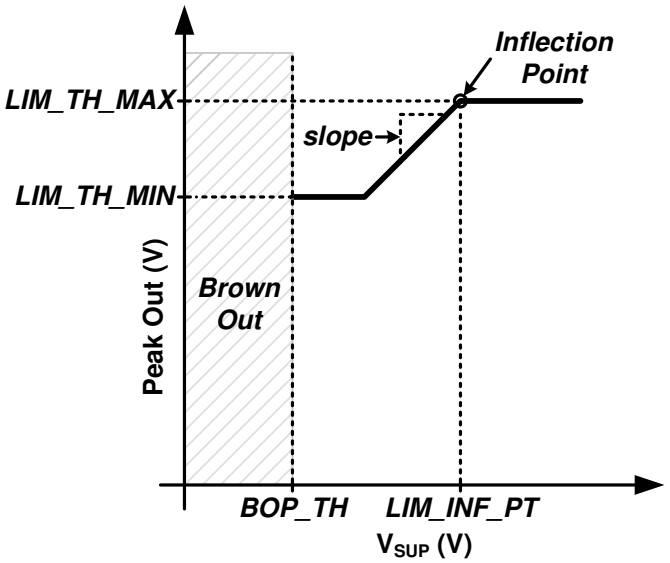


Figure 6-9. Limiter with Inflection Point and Minimum Threshold

The limiter has a configurable attack rate (dB/Sample), hold time (no of samples) and release rate (db/Sample), which are available via the *LIM_ATK_RATE[23:0]*, *LIM_HLD_COUNT[23:0]*, *LIM_RLS_RATE[23:0]* register bits.

6.4.2.5 Tone Generator

TAS2120 can generate internally a sine tone using an integrated tone generator. This feature can be enabled by configuring the register bit *INTERNAL_TONE_GEN_ENZ* to low. The tone signal will start playing back on the output by configuring the *INTERNAL_TONE_PLAYBACK_EN* bit high. When set high, the device will start generating a sine tone based on the programmed *TONE_GEN_CNTRL_xx* registers. The tone generator can generate any frequency from 16Hz to a maximum frequency of 0.45*Fs, where Fs is the sampling rate of the input digital clocks. The amplitude of the tone signal can also be controlled using the *TONE_GEN_CNTRL_xx* registers. It is recommended to program the tone frequency and amplitude using the PPC3 Software.

The internally generated tone can be mixed with incoming audio stream, or can replace the input audio stream and only tone signal is generated using *INTERNAL_TONE_MIXING_EN* register.

Table 6-27. Internal tone generator mixing options

INTERNAL_TONE_MIXING_EN	Configuration
0	Only internal tone is generated.
1(default)	Internally generated tone is mixed with input audio data and played together.

The tone generator can use external clock source like BCLK, or it can be generated using internal oscillator to generate tone signals even with no external clock sources using *INTERNAL_TONE_CLK_SEL* register.

Table 6-28. Internal tone clock source selection

INTERNAL_TONE_CLK_SEL	Configuration
0 (default)	Tone generator uses external clocks
1	Tone generator uses internal oscillator

6.4.3 Digital Audio Serial Interface

The device provides a flexible Audio Serial Interface (ASI) port. The port can be configured to support a variety of formats including stereo I^2S, Left Justified, and TDM. Mono audio playback is available via the SDIN pin. The SDOUT pin is used to transmit sample streams including PVDD voltage, VBAT voltage, die temperature, status and audio for echo reference.

The TDM serial audio port supports up to 16 32-bit time slots at 44.1/48 kHz, 8 32-bit time slots at a 88.2/96 kHz sample rate and 4 32-bit time slots at a 176.4/192 kHz sample rate. The device supports 2 time slots at 32 bits in width and 4 or 8 time slots at 16, 24 or 32 bits in width. The device automatically detects the number of time slots and this does not need to be programmed. PCM data sampling rate and SBCLK to FSYNC ratio detected on the TDM bus is reported back on the read-only register bits *FS_RATE_DETECTED[2:0]* and *FS_RATIO_DETECTED[3:0]* respectively.

Table 6-29. PCM Data Sample Rate Detected

FS_RATE_DETECTED[2:0] (Read Only)	Setting
000	Reserved
001	14.7kHz / 16kHz
010	22.05kHz / 24kHz
011	29.4kHz / 32kHz
100 (default)	44.1kHz / 48kHz
101	88.2 kHz / 96 kHz
110	176.4 kHz / 192 kHz
111	Error condition

A frame begins with the transition of FSYNC from either high to low or low to high (set by the *FRAME_START* register bit). FSYNC and SDIN are sampled by SBCLK using either the rising or falling edge set by the *RX_EDGE* register bit. The *RX_OFFSET[4:0]* register bits define the number of SBCLK cycles from the transition of FSYNC until the beginning of time slot 0. This is typically set to a value of 0 for Left Justified format and 1 for an I^2S format.

The *RX_SLEN[1:0]* register bits set the length of the RX time slot to 16, 24 or 32 (default) bits. The length of the audio sample word within the time slot is configured by the *RX_WLEN[1:0]* register bits. The RX port will

left justify the audio sample within the time slot by default, but this can be changed to right justification via the *RX_JUSTIFY* register bit. The device supports mono and stereo down mix playback ([L+R]/2). By default the device will playback mono from the time slot equal to the I^2C base address offset (set by the AD1 and AD2 pins) for playback. The *RX_SCFG[1:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX_SLOT_R[3:0]* and *RX_SLOT_L[3:0]* register bits.

If time slot selection places reception either partially or fully beyond the frame boundary, the receiver returns a null sample equivalent to a digitally muted sample.

The TDM port can transmit a number of sample streams on the SDOUT pin including interrupts and status, PVDD voltage, VBAT voltage and die temperature.

Either the rising or falling edge of SBCLK can be used to transmit data on the SDOUT pin. This can be configured by setting the *TX_EDGE* register bit. The *TX_OFFSET[2:0]* register bits define the number SBCLK cycles between the start of a frame and the beginning of time slot 0. This is programmed to 0 for Left Justified format and 1 for I^2S format. The TDM TX can either transmit logic 0 or Hi-Z depending on the setting of the *TX_FILL* register bit. An optional bus keeper can weakly hold the state of SDOUT pin when all devices are driving Hi-Z. Since only one bus keeper is required on SDOUT, this feature can be disabled via the *TX_KEEPEN* register bit. The bus keeper can be configured to hold the bus for only 1 LSB or Always (permanent) using *TX_KEEPLN* register bit. Additionally, the keeper LSB can be driven for a full cycle or half of cycle using *TX_KEEPCY* register bit.

The device also support monitoring and TDM transmit of input supply voltages. For PVDD slot, enable and length settings *PVDD_SLOT[5:0]*, *PVDD_TX* and *PVDD_SLEN* register bits can be use. Similarly for VBAT slot, enable and length settings *VBAT_SLOT[5:0]*, *VBAT_TX* and *VBAT_SLEN* register bits can be used. Die temperature can also be transmitted from the device in same manner. Enable and slot settings for Die temperature are done using *TEMP_TX* and *TEMP_SLOT [5:0]* register bits.

Information about status of slots can be found in *STATUS_SLOT[5:0]* register bits. *STATUS_TX* register bit set high enables the status transmit. If time slot selections place transmission beyond the frame boundary, the transmitter will truncate transmission at the frame boundary.

Table 6-30. Status Bits transmitted

Status Slot bit location	Status signal
Bit 0	PVDD UVLO status bit
Bit 1	Over current protection status bit
Bit 2	Over temperature protection status bit
Bit 3	Brown out protection active status bit
Bit 4	Limiter active status bit
Bit 5	Noise gate mode status bit
Bit 6	Y-bridge status bit. 1 = PVDD switching, 0 = VDD switching
Bit 7	Device Active status bit

6.4.3.1 Digital Loopback

The device supports loop back feature to loop SDIN data to SDOUT at two levels. When this feature is enabled through *TDM_LOOPBACK* register bit, loop back is done at the IO Pin level without any ASI data decoding within the device. Other option is to enable the loop back feature through *TDM_DESER_LOOPBACK* register bit in which case SDIN data first goes through ASI protocol decoding within the device and then sent back via SDOUT. These SDIN to SDOUT loop back options can be useful for board level debug of an audio system.

Device can also loop back echo reference digital audio data at the end of the internal signal processing blocks like Limiter, BOP etc. through SDOUT signal. This allows audio system to perform noise and echo cancellation algorithms in a host processor that is connected to the device. The echo reference can be enabled by configuring AUDIO_TX register bit. The slot length and the time slot can be selected using AUDIO_SLEN and AUDIO_SLOT[5:0] register bits.

6.4.4 Internal Boost

The TAS2120 internal processing algorithm automatically enables the boost when needed. A look-ahead algorithm monitors the battery voltage and the digital audio stream. When the speaker output approaches the battery voltage the boost is enabled in-time to supply the required speaker output voltage. When the boost is no longer required it is disabled and bypassed to maximize efficiency. The boost can be configured in one of two modes. The first is low in-rush (Class-G) supporting only boost on-off and has the lowest in-rush current. The second is high-efficiency (Class-H) where the boost voltage level is adjusted to a value just above what is needed. This mode is more efficient but has a higher in-rush current to quickly transition the levels. This can be configured using *BST_MODE[1:0]* register bits.

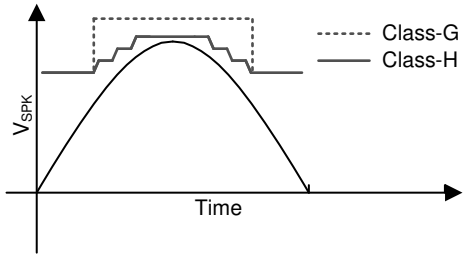


Figure 6-10. Boost Mode Signal Tracking Example

Table 6-31. Boost Mode

BST_MODE[1:0]	BOOST MODE
00	Class-H - High efficiency (default)
01	Class-G - Low in-rush
10	Always On
11	Always Off - Pass-through

The boost can be enabled and disabled using *BST_EN* register. When driving the Class-D amplifier using an external supply through the PVDD pin, the boost should be disabled and the SW pin should be left floating.

Table 6-32. Boost Enable

BST_EN	BOOST IS
0	Disabled (External PVDD mode)
1	Enabled (default)

The maximum boost voltage is set by *VBOOST_MAX_CTRL[7:0]*. When operating in class-G mode, the boost when needed will be at this voltage. In class-H mode of operation the boost voltage is automatically selected based on the audio signal but will not exceed this set value. In class-H mode, the class-H controller controls the Boost with a minimum step size of 33mV to generate the required PVDD voltage. The max boost voltage that the device generates is controlled by *VBOOST_MAX_CTRL[7:0]* and it can be configured with a step size of 66mV.

Table 6-33. Boost Max Regulation Voltage

VBOOST_MAX_CTRL[7:0]	BOOST VOLTAGE (V)
0x00 - 0x53	Reserved
0x54	5.54 V
0x55	5.61 V

Table 6-33. Boost Max Regulation Voltage (continued)

VBOOST_MAX_CTRL[7:0]	BOOST VOLTAGE (V)
...	…..steps of 66mV per LSB step …...
0xA7	11.02 V
...	…..steps of 66mV per LSB step …...
0xE3	14.98 V (default)
0xE4	15.05 V
0xE5	15.11V
0xE6 - 0xFF	Reserved

At light loads (eg. near zero cross of sine waves), the boost automatically enters PFM mode to improve the system efficiency. When the Boost is running in PFM mode, the minimum pulse frequency can be adjusted using *BST_MIN_FREQ_SEL*. Setting a higher PFM frequency will ensure the Boost frequency is always above the set threshold at the cost of increasing the system power consumption.

Table 6-34. Active Mode PFM Lower Frequency Limit

BST_MIN_FREQ_SEL[1:0]	LOWER LIMIT
00	No lower limit (default)
01	25 kHz
10	50 kHz
11	RESERVED

The peak current drawn by the boost is controlled using *BST_ILIM[23:0]* register and it limits the current drawn from the VBAT supply. This setting allows flexibility in the inductor selection for various saturation currents. The system should always use inductors which have minimum saturation current (I_{SAT}) atleast 5% higher than programmed BST_ILIM setting. The Boost circuit can go unstable if the inductor's I_{SAT} is lower than the BST_ILIM setting. The current limit can be adjusted in 39.1 mA steps with a range from 1.5A to 5.1A using PPC3 Software.

The change in boost configurations like *BST_ILIM*, *VBOOST_MAX_CTRL* etc requires re-tuning of device parameters such as *CLASSH_TUNING_xx[23:0]* registers to achieve best performance while ensuring no functionality failures. This configuration should be changed using PPC3 tool to enable automatic reconfiguration of all the associated device parameters.

For multiple channel systems, the boost phase can be shifted to ensure each device will draw peak current from the battery at different instance of times and enable lower instantaneous peak current from the battery. The boost syncing among multiple devices is enabled using *BOOST_PHASE_SYNC_EN*. The individual device boost phase can be automatically configured to different values using the I^2C target address device detected by using *BOOST_PHASE_FROM_ADDRESS_PIN* register, or it can be manually configured using BOOST_PHASE register. The Boost phase shift is done by each device using the FSYNC pulse to synchronize each device and all the devices which require the Boost phase synchronization should be connected to same FSYNC from the host in the system.

Table 6-35. Boost Sync

BOOST_PHASE_SYNC_EN	Status
0	Disabled
1	Enabled(default)

Table 6-36. Boost Phase selection from I²C target address

BOOST_PHASE_FROM_ADDRESS_PIN	Status
0	Disabled(default)
1	Enabled

Table 6-37. Boost Phase manual selection (when *BOOST_PHASE_FROM_ADDRESS_PIN = 0*)

BOOST_PHASE[1:0]	Phase Delay
00	Phase shift is 0ns (default)
01	Phase shift is 65ns (~90° for max clock)
10	Phase shift is 130ns (~180° for max clock)
11	Phase shift is 195ns (~270° for max clock)

6.4.5 Boost Share

The TAS2120 support boost sharing feature with non-boosted device like TAS2320. This feature can be used to reduce board solution size and optimize BOM cost for stereo use cases. In this scenario primary device (TAS2120) with integrated boost can pair with secondary non-boosted device and create stereo solution. Reduced BOM cost can be achieved as only one inductor needed for boost share topology. When share boost configuration is used, total power is split between two devices and max simultaneous power for channels will be half of what primay device integrated boost would deliver. In such solution Class-H information from secondary device is shared with TAS2120 by connecting CLH pins of both devices together. When powering up shared boost solution, secondary device must be powered up first followed by primary device.

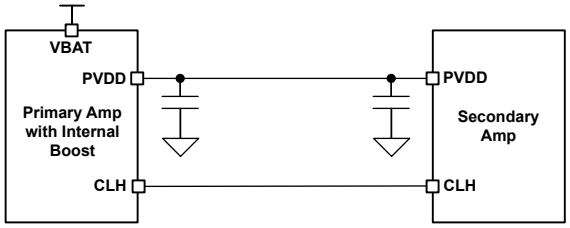


Figure 6-11. Boost Share System Configuration

6.4.6 External Class-H Boost Controller

The TAS2120device has implemented Class-H algorithm allowing users to optimize the efficiency in the system by controlling external power supply and maintaining just enough margin to provide high dynamic range without clipping distortions.

When enabled, the controller generates PWM signal at device CLH pin with duty cycle proportional to peak voltage on the speaker. Using an external RC filter signal is converted to an analog voltage and can be used to control boost converters with feedback input.

The figure below shows how CLH pin can be connected to the external boost control RC network.

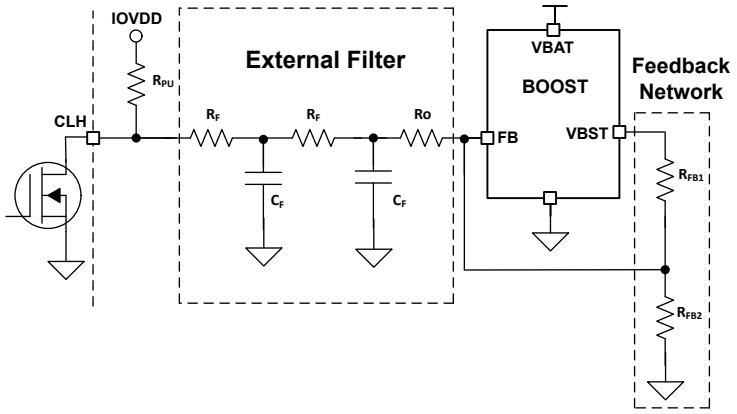


Figure 6-12. CLH Pin and External Components

By default, the CLH pin has an open drain configuration which allows an easy implementation of a multi-channel control loop using only one RC circuitry in wired-or configuration.

6.4.7 Supply Voltage Monitors

TAS2120 has integrated SAR ADC to monitor the supply voltage pins. The sensed voltages are used for internal device features, protections and can also be streamed out over digital data bus or read through I2C registers.

The battery voltage can be sensed through either VBAT or VBAT_SNS pins based on the register *SEL_VBAT_MODE[1:0]*

Table 6-38. Battery mode selection

SEL_VBAT_MODE[1:0]	Configuration
00 (default)	Voltage monitor on VBAT pin. 1S mode of operation
01	Voltage monitor on VBAT_SNS pin. 1S mode of operation
10	Voltage monitor on VBAT_SNS pin. 2S mode of operation
11	Reserved

The monitor ADC samples the VBAT pin at higher rate compared to PVDD pin voltage. This sampling speed can be swapped to prioritize PVDD pin sampling rate over VBAT, for example in case of external PVDD mode of operation.

Table 6-39. Supply monitor sampling rate

SUPPLY_SAMPLING_RATE	Configuration
0(default)	VBAT Sampling rate is higher than PVDD
1	PVDD Sampling rate is higher than VBAT

The VBAT and PVDD monitored voltages are stored in the register *VBAT_CNV* and *PVDD_CNV* and can be read using I2C commands.

The supply monitors are also used for voltage protection like VBAT under voltage, PVDD over voltage and under voltage and VBAT2S under voltage. The voltage protection features monitors the supply voltages, and shuts down the device when the voltage crosses the protection threshold levels. The device also sets the corresponding fault register and can generate an interrupt on IRQZ pin based on configured interrupt Mask register as described in Section 6.3.2. Once the device is shutdown due to fault condition, the device can be re-powered up using the *MODE[1:0]* register bits.

PVDD over voltage protection is based on the monitored PVDD voltage compared against a programmable threshold which can be controlled using *PVDD_OVLO_TH_SEL* in the internal boost mode, and *PVDD_OVLO_TH_SEL_EXT* in the external PVDD mode of operation. The PVDD Over voltage protection is enabled by default and can be disabled by setting *PVDD_OV_DET_DIS* bit high.

Table 6-40. PVDD Over voltage protection threshold, internal Boost mode

PVDD_OVLO_TH_SEL[1:0]	Configuration
00	Over voltage threshold is 13.5V
01	Over voltage threshold is 14V
10	Over voltage threshold is 15V
11 (default)	Over voltage threshold is 16V

6.4.8 Thermal Protection

TAS2120 has internal device junction temperature monitor which protects the device against over temperature. When the internal temperature rises above the Over temperature threshold, the device automatically shuts down and sets the Over temperature flag in the corresponding Interrupt registers. The device can automatically retry to power up if *OTE_RETRY* bit is set high. When set high, the device attempts to re-power up after every *RETRY_WAIT_TIME* setting (default 1.5 seconds of retry)

Along with over temperature protection, the device has thermal warning thresholds to allow for system to raise interrupts or flags as the junction temperature is approaching the shutdown. There are four thermal warning flags available at the internal temperature of 105C, 115C, 125C and 135C. Each thermal warning flag can be independently set to control the Interrupt generation on the IRQZ pad. The minimum temperature and the step size of the temperature warning flag can be programmed using the registers *THERMAL_WARN_MIN_TEMP[23:0]* and *THERMAL_WARN_TEMP_STEP[23:0]*

The real time internal junction temperature is monitored are stored in the register *TMP_CNV* and can be read using i2c commands.

6.4.9 Clocks and PLL

In TDM/I^{2}S Mode, the device operates from SBCLK. Table 6-41 below shows the valid SBCLK frequencies for each sample rate and SBCLK to FSYNC ratio. For 44.1kHz based clocking, the same table is applicable with the associated ratio change between 48ksps to 44.1ksps.

While the sampling rate of 192kHz is supported, data is internally down-sampled to 96kHz. Therefore audio content greater than 40kHz should not be applied to prevent aliasing. This additionally affects all processing blocks like BOP and limiter which should use 96 kHz fs when accepting 192 kHz audio.

If the sample rate is properly configured via the *SAMPLE_RATE_CFG* bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device automatically detects the input PCM FSYNC and BCLK frequency and auto configures itself to playback audio signal. The detected clock rates can be read using the read only registers *FS_RATIO_DETECTED* and *FS_RATE_DETECTED*. The device will detect improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts.

Table 6-41. Supported SBCLK Frequencies (MHz) (48 kHz based sample rates)

Sample Rate (kHz)	SBCLK to FSYNC Ratio													
	16	24	32	48	64	96	128	192	256	384	512	125	250	500
16 kHz	NA	0.384	0.512	0.768	1.024	1.536	2.048	3.072	4.096	6.144	8.192	2	4	8
24 kHz	0.384	0.576	0.768	1.152	1.536	2.304	3.072	4.608	6.144	9.216	12.288	3	6	12
32 kHz	0.512	0.768	1.024	1.536	2.048	3.072	4.096	6.144	8.192	12.288	16.384	4	8	16
48 kHz	0.768	1.152	1.536	2.304	3.072	4.608	6.144	9.216	12.288	18.432	24.576	6	12	24
96 kHz	1.536	2.304	3.072	4.608	6.144	9.216	12.288	18.432	24.576	NA	NA	12	24	NA

Table 6-41. Supported SBCLK Frequencies (MHz) (48 kHz based sample rates) (continued)

Sample Rate (kHz)	SBCLK to FSYNC Ratio													
	16	24	32	48	64	96	128	192	256	384	512	125	250	500
192 kHz	3.027	4.608	6.144	9.216	12.288	18.432	24.576	NA	NA	NA	NA	24	NA	NA

6.4.9.1 Auto clock based wakeup and clock errors

TAS2120 supports flexible operating mode transition from active to shutdown and vice-verse using ASI clock auto detection feature. When MODE[1:0] is configured as '11' the device toggles between Active and Software shutdown state based on valid ASI clock signals applied on the ASI input pins, ie BCLK and FSYNC. If no ASI clocks are detected in this mode, the device remains in software shutdown, with software shutdown mode I_Q on VDD pin, until a valid BCLK and FSYNC clock is detected. Once a valid clock is detected, the device is powered up in active state until the clocks are valid or device is shutdown using software or hardware shutdown commands.

The device can detect and raise interrupt flags on detection of incorrect clock configurations based on status of *CLK_ERR_PWR_EN*. When this bit is set high, the device monitors for activity on the clock pins and flags any error using the latched interrupts status register. The device can also raise interrupts using IRQZ pin based on status of the corresponding interrupt MASK registers. When the error protection bit is enabled, if a clock error is detected, the device will automatically shutdown with proper shutdown sequencing and minimize any clicks and pops due to invalid clocks.

When the device is in shutdown state, the clock error detection can be delayed to provide system with time required to settle the input clocks. This power up delay in clock error detection is controlled using an internal pre-power up clock error detection timer configured by *CLK_HALT_TIMER*. If device doesn't detect a valid clock at the end of the *CLK_HALT_TIMER* expiry, the Pre-Power-up Clock error is flagged on *INT_LTCH4[2]* bit, and corresponding interrupt can be generated on IRQZ pin based on status of *INT_MASK4[2]* bit. When MODE[1:0] is configured as '11' (Wake-up on ASI mode), CLK_HALT_TIMER of '000' is not recommended and it stops the device from entering the software shutdown and increases the VDD I_Q while the device is shutdown.

Once the device is powered up, the external and internally generated clocks are constantly monitored based on status of *CLK_ERR_PWR_EN* bit. If enabled, any error in external or internal clock is flagged using the clock error status register *INT_LTCH2[3]* bit, and corresponding interrupt can be generated on IRQZ pin based on status of *INT_MASK2[3].*

For system flexibility, the device will also set the error status for the type of detected clock error. The device can also be configured to raise an interrupt on IRQZ pin for any specific type of clock error, instead of using the generic clock error interrupt generation. Table 6-44 below explains the different type of clock errors and corresponding status bits and interrupt MASK register bits. One or more register bits in the table below can be set based on the type of clock error detected.

If the device shuts down due to any type of clock error, it can attempt to re-power itself automatically when *MODE[1:0]* is set to '11'.

Table 6-42. Clock Error detection control

CLK_ERR_PWR_EN	Setting
0	Disabled
1	Enabled (default)

Table 6-43. Clock Halt Timer

CLK_HALT_TIMER[2:0]	Setting
000	Disabled (infinite time).
001	0.8 ms (default)
010	3.2 ms
011	34.1 ms
100	68.3 ms

Table 6-43. Clock Halt Timer (continued)

CLK_HALT_TIMER[2:0]	Setting
101	256 ms
110	768 ms
111	1.3 s

Table 6-44. Clock error type description

Clock error type	Description	Status flag register bit	IRQZ generation Mask bit
Clock error	Clock error for any internal or external clocking configuration errors. This bit will be set along with specific clock errors detected in the rest of the table below except for Pre-Power-up Clock errors.	*INT_LTCH2[3]*	*INT_MASK2[3]*
Pre-Power-up Clock error	Clock error detected during shutdown mode after clock error is detected at end of CLK_HALT_TIMER.	*INT_LTCH4[2]*	*INT_MASK4[2]*
Clock ratio change error	Clock error detected due to on the fly change in FSYNC to SBCLK ratio.	*INT_LTCH2[2]*	*INT_MASK2[2]*
Fs change error	Clock error detected due to on the fly change in FSYNC clock frequency	*INT_LTCH2[1]*	*INT_MASK2[1]*
Fs invalid error	Clock error detected due to incorrect FSYNC clock frequency	*INT_LTCH2[0]*	*INT_MASK2[0]*
Frame out of sync	Clock error detected due to Frame out of sync	*INT_LTCH2[5]*	*INT_MASK2[5]*
Internal PLL Clock error	Clock error detected due to internally generated clock frequency error.	*INT_LTCH2[4]*	*INT_MASK2[4]*

The device also has a digital watchdog timer which monitors for errors in the internal digital state machine and shuts down the device on detection of such errors. This error can also raise an interrupt on IRQZ pin and flag to the host device of the error state.

6.4.10 Digital IO pins

TAS2120 supports 1.8V and 3.3V IO voltage supply based on the voltage applied on the IOVDD pin.

I2S digital input pin has an optional weak pull down to prevent the pin from floating. Pull downs are not enabled during HW shutdown. The pull downs are disabled by default and can be enabled by setting the corresponding Pull down enable bit high.

Table 6-45. Digital pin weak pull down

Pin Name	Pull down control register name
SDOUT	*SDOUT_PD_EN*
SDIN	*SDIN_PD_EN*
FSYNC	*FSYNC_PD_EN*
SBCLK	*SBCLK_PD_EN*

6.5 Programming

The device contains configuration registers and programming coefficients that can be set to the desired values for a specific system and application use. These registers are called device control registers and are each eight bits in width, mapped using a page scheme.

Each page contains 128 configuration registers. All key device configuration registers are stored in page 0, which is the default page setting at power up and after a software reset. All programmable coefficient registers are located in page 2, page 3 and later pages. The current page of the device can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

6.5.1 I²C Control Interface

The device supports the I²C control protocol as a target device, and is capable of operating in standard mode, fast mode, and fast mode plus. Device configuration and status are provided via the SDA and SCL pins using the I²C protocol.

6.5.2 I²C Address Selection

The TAS2120 can operate using one of four selectable device addresses. I²C target addresses is defined as the 7 MSBs followed by read/write bit. Table 6-46 below illustrates how to select the device I²C address and the address corresponds to R/W bit set to 0 (ie ADDR[6:0],1b'0). The I²C address is detected by sampling the address pins when SDZ pin is released or when device is reset using software reset bit.

Table 6-46. I²C Mode Address Selection

I²C TARGET ADDRESS	ADDR PIN
0x80 (global address)	NA
0x90	Short to GND
0x92	24k to GND
0x94	24k to IOVDD
0x96	Connect to IOVDD

The TAS2120 has a global 7-bit I²C address 0x40 (0x80 in 8-bit format with R/W bit set to 0). When enabled the device will additionally respond to I²C commands at this address regardless of the address pins selected . This is used to speed up device configuration when using multiple TAS2120 devices and programming similar settings across all devices. The I²C ACK / NACK cannot be used during the multi-device writes since multiple devices are responding to the I²C command. The I²C CRC function should be used to ensure each device properly received the I²C commands. At the completion of writing multiple devices using the global address, the CRC at *I2C_CKSUM* register should be checked on each device using the local address for a proper value. The global I²C address can be disabled using *I2C_GBL_EN* register.

Table 6-47. I²C Global Address Enable

I2C_GBL_EN	SETTING
0	Disabled
1	Enabled (default)

6.5.3 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred MSB first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the controller device driving a start condition on the bus and ends with the controller device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The controller device drives a start condition followed by the 7-bit target address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledgment condition. The target device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the controller device transmits the next byte of the sequence. Each target device is addressed by a unique 7-bit target address plus the R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the controller device generates a stop condition to release the bus. Figure 6-13 shows a generic data transfer sequence.

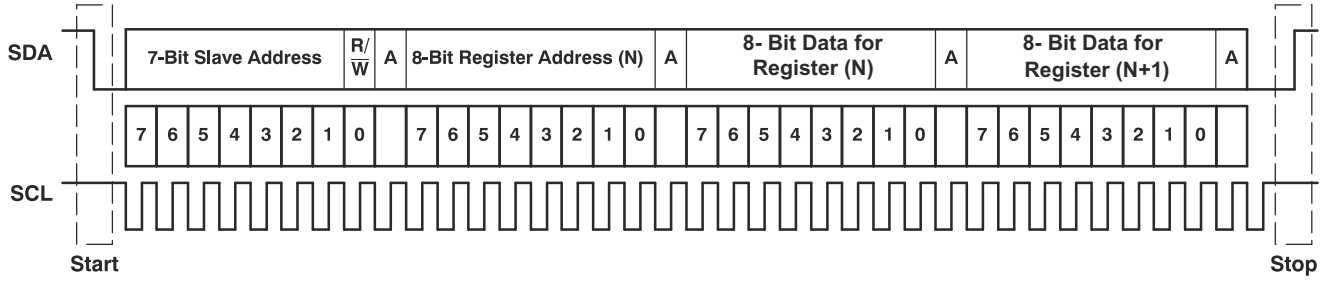


Figure 6-13. Typical I²C Sequence

In the system, use external pullup resistors for the SDA and SCL signals to set the logic high level for the bus. The SDA and SCL voltages must not exceed the device supply voltage, IOVDD.

6.5.4 I²C Single-Byte and Multiple-Byte Transfers

The device I²C interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the device responds with data, a byte at a time, starting at the register assigned, as long as the controller device continues to respond with acknowledges.

The device supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction takes place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many registers are written.

6.5.5 I²C Single-Byte Write

As shown in Figure 6-14, a single-byte data write transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C target address and the read/write bit, the device responds with an acknowledge bit (ACK). Next, the controller device transmits the register byte corresponding to the device internal register address being accessed. After receiving the register byte, the device again responds with an acknowledge bit (ACK). Then, the controller transmits the byte of data to be written to the specified register. When finished, the target device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition to complete the single-byte data write transfer.

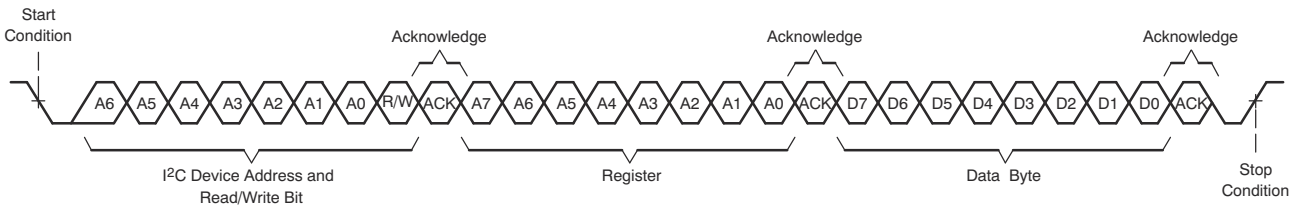


Figure 6-14. I²C Single-Byte Write Transfer

6.5.6 I²C Multiple-Byte Write

As shown in Figure 6-15, a multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the controller device to the target device. After receiving each data byte, the device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition after the last data-byte write transfer.

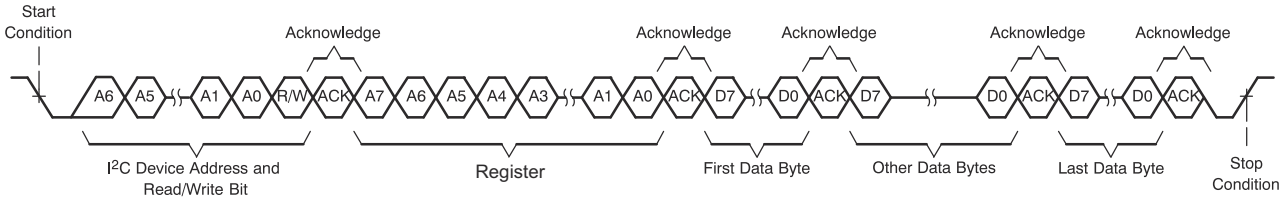


Figure 6-15. I²C Multiple-Byte Write Transfer

6.5.7 I²C Single-Byte Read

As shown in Figure 6-16, a single-byte data read transfer begins with the controller device transmitting a start condition followed by the I²C target address and the read/write bit. For the data read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte of the internal register address to be read. As a result, the read/write bit is set to 0.

After receiving the target address and the read/write bit, the device responds with an acknowledge bit (ACK). The controller device then sends the internal register address byte, after which the device issues an acknowledge bit (ACK). The controller device transmits another start condition followed by the target address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the device transmits the data byte from the register address being read. After receiving the data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the single-byte data read transfer.

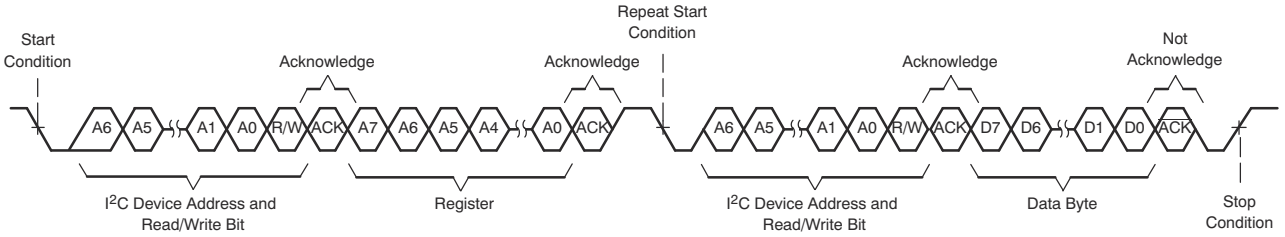


Figure 6-16. I²C Single-Byte Read Transfer

6.5.8 I²C Multiple-Byte Read

As shown in Figure 6-17, a multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the device to the controller device. With the exception of the last data byte, the controller device responds with an acknowledge bit after receiving each data byte. After receiving the last data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the data read transfer.

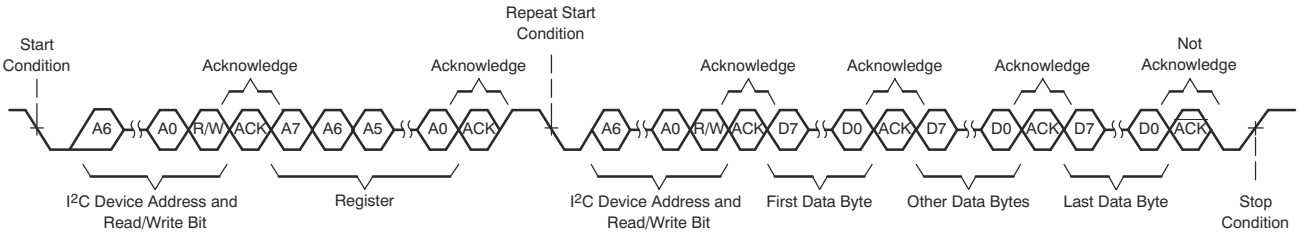


Figure 6-17. I²C Multiple-Byte Read Transfer

7 Register Maps

The TAS2120device registers are organized into pages and books. The registers from Page 0 to Page 8 are all in Book 0, while the registers in Page 9 are in Book 100. The register map book number can be changed by programming the *BOOK[7:0]* register bit, and page number can be changed by programing *PAGE[7:0]* register bits.

7.1 PAGE 0 Registers

Table 7-1 lists the memory-mapped registers for the PAGE 0 registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. PAGE 0 Registers

Address	Acronym	Description	Section
0h	Page	Device Page	Section 7.1.1
1h	SW_RESET	Software Reset	Section 7.1.2
2h	PWR_CTL	Power Control	Section 7.1.3
3h	DEVICE_CFG_01	Device configuration registers	Section 7.1.4
4h	DEVICE_CFG_02	Device configuration registers	Section 7.1.5
5h	DEVICE_CFG_03	Device configuration registers	Section 7.1.6
6h	DEVICE_CFG_04	Device configuration registers	Section 7.1.7
7h	DEVICE_CFG_05	Device configuration registers	Section 7.1.8
8h	TDM_CFG1	TDM Configuration registers	Section 7.1.9
9h	TDM_CFG2	TDM Configuration registers	Section 7.1.10
Ah	TDM_CFG3	TDM Configuration registers	Section 7.1.11
Ch	TDM_CFG5	TDM Configuration registers	Section 7.1.12
Fh	TDM_CFG8	TDM Configuration registers	Section 7.1.13
10h	TDM_CFG9	TDM Configuration registers	Section 7.1.14
11h	TDM_CFG10	TDM Configuration registers	Section 7.1.15
12h	TDM_CFG11	TDM Configuration registers	Section 7.1.16
13h	TDM_CFG12	TDM Configuration registers	Section 7.1.17
14h	TDM_DET	TDM Clock detection monitor	Section 7.1.18
15h	MONITOR_CFG_01	Monitoring Configuration	Section 7.1.19
17h	LIM_CFG_0	Limiter configuration	Section 7.1.20
18h	BOP_CFG_0	Brown out protection configuration	Section 7.1.21
1Ch	IO_CFG_02	IO Configuration	Section 7.1.22
1Dh	IO_CFG_03	IO Configuration	Section 7.1.23
1Eh	NG_CFG0	Noise Gate Controls	Section 7.1.24
21h	BST_CFG_01	Boost Configuration	Section 7.1.25
22h	BST_CFG_02	Boost Configuration	Section 7.1.26
24h	BST_CFG_03	Boost Configuration	Section 7.1.27
25h	INTERRUPT_CFG1	IRQZ clear	Section 7.1.28
26h	SAR_MONITOR_01	VBAT Monitor MSB	Section 7.1.29
27h	SAR_MONITOR_02	VBAT Monitor MSB	Section 7.1.30
28h	SAR_MONITOR_03	PVDD Monitor MSB	Section 7.1.31
29h	SAR_MONITOR_04	PVDD Monitor MSB	Section 7.1.32
2Ah	SAR_MONITOR_06	Temperature monitor	Section 7.1.33
31h	CLASSD_CFG_01	ClassD amp configurations	Section 7.1.34
32h	CLASSD_CFG_02	ClassD amp configurations	Section 7.1.35
3Bh	BST_CFG_05	Boost Configuration	Section 7.1.36
3Ch	THERM_CFG	Thermal warning configuration	Section 7.1.37
5Bh	INT_MASK_0	Interrupt Masks	Section 7.1.38
5Ch	INT_MASK_1	Interrupt Masks	Section 7.1.39
5Dh	INT_MASK_2	Interrupt Masks	Section 7.1.40
5Eh	INT_MASK_3	Interrupt Masks	Section 7.1.41

Table 7-1. PAGE 0 Registers (continued)

Address	Acronym	Description	Section
5Fh	INT_MASK_4	Interrupt Masks	Section 7.1.42
60h	INT_LATCH_0	Latched interrupt readback	Section 7.1.43
61h	INT_LATCH_1	Latched interrupt readback	Section 7.1.44
62h	INT_LATCH_2	Latched interrupt readback	Section 7.1.45
63h	INT_LATCH_3	Latched interrupt readback	Section 7.1.46
64h	INT_LATCH_4	Latched interrupt readback	Section 7.1.47
65h	NG_IDLE_STATUS	Latched interrupt readback	Section 7.1.48
78h	REV_ID	Revision ID	Section 7.1.49
7Fh	BOOK	Device Book	Section 7.1.50

7.1.1 Page Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The device's memory map is divided into pages and books. This register sets the page.

Table 7-2. Page Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.1.2 SW_RESET Register (Address = 1h) [Reset = 00h]

Return to the Summary Table.

Asserting Software Reset will place all register values in their default POR (Power on Reset) state.

Table 7-3. SW_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	SW_RESET	R/W	0h	Software reset. Bit is self clearing. 0h = Don't reset 1h = Reset

7.1.3 PWR_CTL Register (Address = 2h) [Reset = 03h]

Return to the Summary Table.

Sets device's mode of operation and Power Configuration.

Table 7-4. PWR_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	MODE[1:0]	R/W	3h	Device operational mode. 0h = Active 1h = Reserved 2h = Software Shutdown 3h = Wake-up and Shutdown on ASI Clock

7.1.4 DEVICE_CFG_01 Register (Address = 3h) [Reset = 81h]

Return to the Summary Table.

This register configures various device modes.

Table 7-5. DEVICE_CFG_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EFFICIENCY_MODE[1:0]	R/W	2h	Device operational mode. 0h = Music Efficiency and Noise Gate mode disabled 1h = Noise Gate Mode Only 2h = Music Efficiency Only 3h = Music Efficiency and Noise Gate mode
5-2	RESERVED	R	0h	Reserved
1-0	SDZ_MODE[1:0]	R/W	1h	SDZ Mode configuration. 0h = Soft shutdown and device reset 1h = Immediate shutdown and device reset 2h = Soft shutdown only 3h = Reserved

7.1.5 DEVICE_CFG_02 Register (Address = 4h) [Reset = 8Ch]

Return to the Summary Table.

This register configures various device modes.

Table 7-6. DEVICE_CFG_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C_GBL_EN	R/W	1h	I2C global address. 0h = Disabled 1h = Enabled
6	RESERVED	R/W	0h	Reserved
5-3	CLK_HALT_TIME[2:0]	R/W	1h	Pre-power-up valid clock checking time duration. 0h = Disabled (infinite time) 1h = 800 us 2h = 3.2 ms 3h = 34.1 ms 4h = 68.3 ms 5h = 256 ms 6h = 768 ms 7h = 1.3 s
2	CLK_BASED_PWR_UP	R/W	1h	Clock error detection enable/disable. 0h = Disable 1h = Enabled
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

7.1.6 DEVICE_CFG_03 Register (Address = 5h) [Reset = 00h]

Return to the Summary Table.

This register configures various device modes.

Table 7-7. DEVICE_CFG_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved

Table 7-7. DEVICE_CFG_03 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	OTE_RETRY	R/W	0h	Retry after over temperature event. 0h = Do not retry 1h = Retry after "RETRY_WAIT_TIME"
3	RESERVED	R/W	0h	Reserved
2	CLKE_RETRY	R/W	0h	Retry after Internal Clock Error event. 0h = Do not retry 1h = Retry after "RETRY_WAIT_TIME"
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

7.1.7 DEVICE_CFG_04 Register (Address = 6h) [Reset = 04h]

Return to the Summary Table.

This register configures various device modes.

Table 7-8. DEVICE_CFG_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	SEL_VBAT_MODE[1:0]	R/W	0h	Selects VBAT mode of operation. 0h = VBAT 1S mode, supply sense on VBAT 1h = VBAT 1S mode, supply sense on VBAT_SNS 2h = VBAT 2S mode, supply sense on VBAT_SNS 3h = RESERVED
3-2	IRQZ_PIN_CFG[1:0]	R/W	1h	IRQZ interrupt configuration. IRQZ will assert. 0h = Reserved 1h = on any unmasked latched interrupts 2h = Reserved 3h = for 2-4ms every 4ms on any unmasked latched interrupts
1	RESERVED	R	0h	Reserved
0	RETRY_WAIT_TIME	R/W	0h	Retry wait time after device detects error (Valid only for errors with retry options available). 0h = 1.5 sec 1h = 100ms

7.1.8 DEVICE_CFG_05 Register (Address = 7h) [Reset = 00h]

Return to the Summary Table.

This register configures various device modes.

Table 7-9. DEVICE_CFG_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	SAMPLE_RATE_CFG	R/W	0h	Sampling Rate selection. 0h = Audio data rate is multiple/sub-multiple of 48 Ksps 1h = Audio data rate is multiple/sub-multiple of 44.1 Ksps

Table 7-9. DEVICE_CFG_05 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	AMP_LVL[5:0]	R/W	0h	Device Channel Gain setting 0h = 21.000dB 1h = 20.498dB 2h = 19.997dB 3h = 19.495dB 4h = 18.993dB 26h = 1.935dB 27h = 1.434dB 28h = 0.932dB 29h = 0.430dB 2Ah = -0.071dB

7.1.9 TDM_CFG1 Register (Address = 8h) [Reset = 82h]

Return to the Summary Table.

This register configures device TDM modes.

Table 7-10. TDM_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FRAME_START	R/W	1h	TDM frame start polarity. 0h = Low to High on FSYNC 1h = High to Low on FSYNC
6	RX_JUSTIFY	R/W	0h	TDM RX sample justification within the time slot. 0h = Left 1h = Right
5-1	RX_OFFSET[4:0]	R/W	1h	TDM RX start of frame to time slot 0 offset (SBCLK cycles).
0	RX_EDGE	R/W	0h	TDM RX capture clock polarity. 0h = Rising edge of SBCLK 1h = Falling edge of SBCLK

7.1.10 TDM_CFG2 Register (Address = 9h) [Reset = 0Ah]

Return to the Summary Table.

This register configures device TDM modes.

Table 7-11. TDM_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5-4	RX_SCFG[1:0]	R/W	0h	TDM RX time slot select config. 0h = Mono with time slot equal to I2C address offset 1h = Mono left channel 2h = Mono right channel 3h = Stereo downmix (L+R)/2
3-2	RX_WLEN[1:0]	R/W	2h	TDM RX word length. 0h = 16 bits 1h = 20 bits 2h = 24 bits 3h = 32 bits
1-0	RX_SLEN[1:0]	R/W	2h	TDM RX time slot length. 0h = 16 bits 1h = 24 bits 2h = 32 bits 3h = Reserved

7.1.11 TDM_CFG3 Register (Address = Ah) [Reset = 10h]

Return to the Summary Table.

This register configures device TDM modes.

Table 7-12. TDM_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RX_SLOT_R[3:0]	R/W	1h	TDM RX Right Audio Channel Time Slot.
3-0	RX_SLOT_L[3:0]	R/W	0h	TDM RX Left Audio Channel Time Slot.

7.1.12 TDM_CFG5 Register (Address = Ch) [Reset = 13h]

Return to the Summary Table.

This register configures device TDM modes.

Table 7-13. TDM_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_KEEPCY	R/W	0h	TDM TX SDOUT LSB data will be driven for 0h = full-cycle 1h = half-cycle
6	TX_KEEPLN	R/W	0h	TDM TX SDOUT will hold the bus for the following when TX_KEEPEN is enabled 0h = 1 LSB cycle 1h = always
5	TX_KEEPEN	R/W	0h	TDM TX SDOUT bus keeper enable. 0h = Disable bus keeper 1h = Enable bus keeper
4	TX_FILL	R/W	1h	TDM TX SDOUT unused bitfield fill. 0h = Transmit 0 1h = Transmit Hi-Z
3-1	TX_OFFSET[2:0]	R/W	1h	TDM TX start of frame to time slot 0 offset.
0	TX_EDGE	R/W	1h	TDM TX launch clock polarity. 0h = Rising edge of SBCLK 1h = Falling edge of SBCLK

7.1.13 TDM_CFG8 Register (Address = Fh) [Reset = 04h]

Return to the Summary Table.

This register configures device TDM modes.

Table 7-14. TDM_CFG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBAT_SLEN	R/W	0h	TDM TX VBAT time slot length. 0h = Truncate to 8-bits 1h = Left justify to 16-bits
6	VBAT_TX	R/W	0h	TDM TX VBAT transmit enable. 0h = Disabled 1h = Enabled
5-0	VBAT_SLOT[5:0]	R/W	4h	TDM TX VBAT time slot.

7.1.14 TDM_CFG9 Register (Address = 10h) [Reset = 05h]

Return to the Summary Table.

This register configures device TDM modes.

Table 7-15. TDM_CFG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	TEMP_TX	R/W	0h	TDM TX temp sensor transmit enable. 0h = Disabled 1h = Enabled
5-0	TEMP_SLOT[5:0]	R/W	5h	TDM TX temp sensor time slot.

7.1.15 TDM_CFG10 Register (Address = 11h) [Reset = 07h]

Return to the Summary Table.

This register configures device TDM modes

Table 7-16. TDM_CFG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	STATUS_TX	R/W	0h	TDM TX status bits transmit enable. 0h = Disabled 1h = Enabled
5-0	STATUS_SLOT[5:0]	R/W	7h	TDM TX status bits time slot.

7.1.16 TDM_CFG11 Register (Address = 12h) [Reset = 06h]

Return to the Summary Table.

This register configures device TDM modes.

Table 7-17. TDM_CFG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PVDD_SLEN	R/W	0h	TDM TX PVDD time slot length. 0h = Truncate to 8-bits 1h = Left justify to 16-bits
6	PVDD_TX	R/W	0h	TDM TX PVDD transmit enable. 0h = Disabled 1h = Enabled
5-0	PVDD_SLOT[5:0]	R/W	6h	TDM TX PVDD time slot.

7.1.17 TDM_CFG12 Register (Address = 13h) [Reset = 12h]

Return to the Summary Table.

This register configures device TDM modes.

Table 7-18. TDM_CFG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AUDIO_SLEN	R/W	0h	TDM audio slot length 0h = 16-bits 1h = 24-bits
6	AUDIO_TX	R/W	0h	TDM audio output transmit is 0h = Disabled 1h = Enabled
5-0	AUDIO_SLOT[5:0]	R/W	12h	TDM TX status time slot.

7.1.18 TDM_DET Register (Address = 14h) [Reset = 7Fh]

Return to the Summary Table.

Readback of internal auto clock detection.

Table 7-19. TDM_DET Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-3	FS_RATIO_DETECTED[3:0]	R	Fh	Detected SBCLK to FSYNC ratio. 0h = 16 1h = 24 2h = 32 3h = 48 4h = 64 5h = 96 6h = 128 7h = 192 8h = 256 9h = 384 Ah = 512 Bh = 250 Dh = 500 Eh = Reserved Fh = Invalid ratio
2-0	FS_RATE_DETECTED[2:0]	R	7h	Detected sample rate of TDM bus. 0h = Reserved 1h = 14.7/16 KHz 2h = 22.05/24 KHz 3h = 29.4/32 KHz 4h = 44.1/48 KHz 5h = 88.2/96 kHz 6h = 176.4/192 kHz 7h = Error condition

7.1.19 MONITOR_CFG_01 Register (Address = 15h) [Reset = 00h]

Return to the Summary Table.

This register configures the Monitor channels of the device.

Table 7-20. MONITOR_CFG_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SUPPLY_SAMPLING_RATE	R/W	0h	Configure VBAT and PVDD sampling rates 0h = VBAT Sampling rate is higher than PVDD 1h = PVDD Sampling rate is higher than VBAT
6-0	RESERVED	R	0h	Reserved

7.1.20 LIM_CFG_0 Register (Address = 17h) [Reset = 00h]

Return to the Summary Table.

This register configures the voltage limiter module.

Table 7-21. LIM_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LIM_MODE[1:0]	R/W	0h	Limiter enable. 0h = Disabled 1h = VBAT voltage based limiter mode 2h = PVDD voltage based limiter mode 3h = RESERVED

Table 7-21. LIM_CFG_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SUPPLY_HEADROOM_LIM_MODE	R/W	0h	Select limiter threshold based on supply headroom. 0h = Disabled 1h = Enabled
4-0	RESERVED	R	0h	Reserved

7.1.21 BOP_CFG_0 Register (Address = 18h) [Reset = 00h]

Return to the Summary Table.

This register configures brown out protection module.

Table 7-22. BOP_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	BOP_SRC	R/W	0h	Brown out prevention Source control 0h = VBAT 1h = PVDD
3	BOPSD_EN	R/W	0h	Brown out prevention shutdown enable. 0h = Disabled 1h = Enabled
2	BOP_HLD_CLR	R/W	0h	BOP infinite hold clear (self clearing). Available when BOP_INF_HLD = 1 0h = Don't clear 1h = Clear
1	BOP_INF_HLD	R/W	0h	Infinite hold on brown out event. 0h = Use BOP_HLD_TM after brown out event 1h = Don't release until BOP_HLD_CLR is asserted high
0	BOP_EN	R/W	0h	Brown out prevention (BOP) enable. 0h = Disabled 1h = Enabled

7.1.22 IO_CFG_02 Register (Address = 1Ch) [Reset = 3Fh]

Return to the Summary Table.

This register configures the IO buffers.

Table 7-23. IO_CFG_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IRQZ_POL	R/W	0h	IRQZ pin polarity for interrupt. 0h = Active Low 1h = Active High
6	RESERVED	R	0h	Reserved
5	RESERVED	R/W	1h	Reserved
4	IRQZ_PD	R/W	1h	Weak pull down for IRQZ. 0h = Disabled 1h = Enabled
3	RESERVED	R/W	1h	Reserved
2	RESERVED	R/W	1h	Reserved
1	SDZ_PD	R/W	1h	Weak pull down for SDZ. 0h = Disabled 1h = Enabled

Table 7-23. IO_CFG_02 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SDA_PD	R/W	1h	Weak pull down for SDA. 0h = Disabled 1h = Enabled

7.1.23 IO_CFG_03 Register (Address = 1Dh) [Reset = F0h]

Return to the Summary Table.

This register configures the IO buffers.

Table 7-24. IO_CFG_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADR_PD	R/W	1h	Weak pull down for ADR. 0h = Disabled 1h = Enabled
6	SDZ_PD	R/W	1h	Weak pull down for SDZ. 0h = Disabled 1h = Enabled
5	RESERVED	R/W	1h	Reserved
4	CLH_PD	R/W	1h	Weak pull down for CLH. 0h = Disabled 1h = Enabled
3	SDOUT_PD	R/W	0h	Weak pull down for SDOUT. 0h = Disabled 1h = Enabled
2	SDIN_PD	R/W	0h	Weak pull down for SDIN. 0h = Disabled 1h = Enabled
1	FSYNC_PD	R/W	0h	Weak pull down for FSYNC. 0h = Disabled 1h = Enabled
0	SBCLK_PD	R/W	0h	Weak pull down for SBCLK. 0h = Disabled 1h = Enabled

7.1.24 NG_CFG0 Register (Address = 1Eh) [Reset = 60h]

Return to the Summary Table.

Noise gate hysteresis, threshold level, and enable.

Table 7-25. NG_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NG_HYST_TIMER[1:0]	R/W	1h	Noise Gate Entry hysteris timer. 0h = 10ms 1h = 50ms 2h = 100ms 3h = 1000ms
5-3	NG_TH_LVL[2:0]	R/W	4h	Noise-gate audio threshold level. 0h = -85 dBFS 1h = -90 dBFS 2h = -95 dBFS 3h = -100 dBFS 4h = -105 dBFS 5h = -110 dBFS 6h = -115 dBFS 7h = -120 dBFS

Table 7-25. NG_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	RESERVED	R	0h	Reserved

7.1.25 BST_CFG_01 Register (Address = 21h) [Reset = 10h]

Return to the Summary Table.

This register configures internal Boost controller.

Table 7-26. BST_CFG_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	BOOST_PHASE_SYNC_EN	R/W	1h	Boost Phase sync enable. 0h = Disabled 1h = Enabled
3-2	BOOST_PHASE[1:0]	R/W	0h	Boost Phase sync delay control, applicable only when boost_phase_sync_en = 1 0h = Phase shift is 0ns 1h = Phase shift is 65ns 2h = Phase shift is 130ns 3h = Phase shift is 195ns
1	BOOST_PHASE_FROM_ADDRESS_PIN	R/W	0h	Boost Phase shift sync control selected automatically based on i2c target address detected from Address pin. Applicable only when boost_phase_sync_en = 1 0h = Disabled 1h = Enabled
0	RESERVED	R/W	0h	Reserved

7.1.26 BST_CFG_02 Register (Address = 22h) [Reset = 23h]

Return to the Summary Table.

This register configures internal Boost controller.

Table 7-27. BST_CFG_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BST_MODE[1:0]	R/W	0h	Boost Mode. 0h = Class-H 1h = Class-G 2h = Always ON 3h = Always OFF (Passthrough)
5	BST_EN	R/W	1h	Boost enable. 0h = Disabled (External PVDD mode) 1h = Enabled
4-3	BST_MIN_FREQ_SEL[1:0]	R/W	0h	Boost active mode PFM lower limit. 0h = No Limit 1h = 25 kHz 2h = 50 kHz 3h = RESERVED
2-1	RESERVED	R/W	1h	Reserved
0	RESERVED	R/W	1h	Reserved

7.1.27 BST_CFG_03 Register (Address = 24h) [Reset = 48h]

Return to the Summary Table.

This register configures Boost controller.

Table 7-28. BST_CFG_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	2h	Reserved
4-3	RESERVED	R/W	1h	Reserved
2	RESERVED	R/W	0h	Reserved
1	External_boost_classh_en	R/W	0h	Support for external_boost PWM control 0h = Disabled 1h = Enabled
0	Sel_pwm_out_polarity	R/W	0h	External_boost PWM control polarity 0h = Default 1h = Inverted

7.1.28 INTERRUPT_CFG1 Register (Address = 25h) [Reset = 00h]

Return to the Summary Table.

This register clears all the latched interrupt registers.

Table 7-29. INTERRUPT_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Shared_boost_primary_en	R/W	0h	Primary device control in shared boost mode 0h = Disabled 1h = Enabled
6	Shared_boost_secondary_en	R/W	0h	Secondary device control in shared boost mode 0h = Disabled 1h = Enabled
5-2	RESERVED	R	0h	Reserved
1	INT_CLR_LTCH	R/W	0h	Clear INT_LTCH registers. 0h = Don't clear 1h = Clear
0	RESERVED	R	0h	Reserved

7.1.29 SAR_MONITOR_01 Register (Address = 26h) [Reset = 00h]

Return to the Summary Table.

This register provides sensed VBAT Voltage.

Table 7-30. SAR_MONITOR_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VBAT_CNV_MSB[7:0]	R	0h	Returns the SAR ADC VBAT monitored voltage MSBs. VBAT value converted is based on selection of SEL_VBAT_MODE

7.1.30 SAR_MONITOR_02 Register (Address = 27h) [Reset = 00h]

Return to the Summary Table.

This register provides sensed VBAT Voltage.

Table 7-31. SAR_MONITOR_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	VBAT_CNV_LSB[3:0]	R	0h	Returns the SAR ADC VBAT monitored voltage LSBs. VBAT value converted is based on selection of SEL_VBAT_MODE

Table 7-31. SAR_MONITOR_02 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	RESERVED	R	0h	Reserved

7.1.31 SAR_MONITOR_03 Register (Address = 28h) [Reset = 00h]

Return to the Summary Table.

This register provides sensed VBAT Voltage.

Table 7-32. SAR_MONITOR_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PVDD_CNV_MSB[7:0]	R	0h	Returns the SAR ADC PVDD monitored voltage MSBs.

7.1.32 SAR_MONITOR_04 Register (Address = 29h) [Reset = 00h]

Return to the Summary Table.

This register provides sensed VBAT Voltage.

Table 7-33. SAR_MONITOR_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PVDD_CNV_LSB[3:0]	R	0h	Returns the SAR ADC PVDD monitored voltage LSBs.
3-0	RESERVED	R	0h	Reserved

7.1.33 SAR_MONITOR_06 Register (Address = 2Ah) [Reset = 00h]

Return to the Summary Table.

This register provides sensed temperature.

Table 7-34. SAR_MONITOR_06 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TMP_CNV[7:0]	R	0h	Returns the SAR ADC Temperature monitored data.

7.1.34 CLASSD_CFG_01 Register (Address = 31h) [Reset = 04h]

Return to the Summary Table.

This register configures the class-D amplifier.

Table 7-35. CLASSD_CFG_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5-4	CLASSD_OUTPUT_EDGERATE_CTRL[1:0]	R/W	0h	Edgerate programmability control. 0h = Class-D output edge rate of approximately 0.5 V/ns 1h = Class-D output edge rate of approximately 1 V/ns 2h = Reserved 3h = Class-D output edge rate of approximately 2 V/ns
3	CLASSD_HIZ_MODE	R/W	0h	Amp output state in Noise gate mode (0 = Not Hi-Z, 1 = Hi-Z) 0h = Disabled 1h = Enabled
2	RESERVED	R/W	1h	Reserved
1-0	RESERVED	R	0h	Reserved

7.1.35 CLASSD_CFG_02 Register (Address = 32h) [Reset = 9Ch]

Return to the Summary Table.

This register configures the class-D amplifier.

Table 7-36. CLASSD_CFG_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_Y_BRIDGE_MODE	R/W	1h	Enable/Disable VDD Bridge mode during device operation 0h = VDD Bridge mode disabled 1h = VDD Bridge mode enabled
6	RESERVED	R/W	0h	Reserved
5-4	RESERVED	R/W	1h	Reserved
3-2	Ybridge_hyst_timer[1:0]	R/W	3h	Time hysteresis programability 0h = 100 us 1h = 500 us 2h = 5 ms 3h = 50 ms
1-0	RESERVED	R	0h	Reserved

7.1.36 BST_CFG_05 Register (Address = 3Bh) [Reset = E3h]

Return to the Summary Table.

This register configures internal Boost controller.

Table 7-37. BST_CFG_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VBOOST_MAX_CTRL[7:0]	R/W	E3h	Boost VMAX setting in class-H mode. 54h = 5.54V (Min setting) E5h = 15.11V (Max setting)

7.1.37 THERM_CFG Register (Address = 3Ch) [Reset = 00h]

Return to the Summary Table.

This register configures thermal warning detection.

Table 7-38. THERM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	EN_THERM_WARN_DET	R/W	0h	Enable control for thermal warning detection feature. 0h = Disabled 1h = Enabled

7.1.38 INT_MASK_0 Register (Address = 5Bh) [Reset = 03h]

Return to the Summary Table.

This register configures Masks for Interrupt flags.

Table 7-39. INT_MASK_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK0[7]	R/W	0h	Mask for Interrupt due to BOP Inf Hold flag. 0h = Don't Mask 1h = Mask

Table 7-39. INT_MASK_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INT_MASK0[6]	R/W	0h	Mask for Interrupt due to limiter attentuation flag. 0h = Don't Mask 1h = Mask
5	INT_MASK0[5]	R/W	0h	Mask for Interrupt due to supply less than inf pt flag. 0h = Don't Mask 1h = Mask
4	INT_MASK0[4]	R/W	0h	Mask for Interrupt due to limiter active flag. 0h = Don't Mask 1h = Mask
3	INT_MASK0[3]	R/W	0h	Mask for Interrupt due to brownout detected flag. 0h = Don't Mask 1h = Mask
2	INT_MASK0[2]	R/W	0h	Mask for Interrupt due to bop active flag. 0h = Don't Mask 1h = Mask
1	INT_MASK0[1]	R/W	1h	Mask for Interrupt due to device active flag. 0h = Don't Mask 1h = Mask
0	RESERVED	R/W	1h	Reserved

7.1.39 INT_MASK_1 Register (Address = 5Ch) [Reset = 1Fh]

Return to the Summary Table.

This register configures Masks for Interrupt flags.

Table 7-40. INT_MASK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK1[7]	R/W	0h	Mask for Interrupt due to PVDD Under voltage. 0h = Don't Mask 1h = Mask
6	INT_MASK1[6]	R/W	0h	Mask for Interrupt due to VBAT 2S supply under voltage. 0h = Don't Mask 1h = Mask
5	RESERVED	R/W	0h	Reserved
4	INT_MASK1[4]	R/W	1h	Mask for Interrupt due to Thermal Warning 135C 0h = Don't Mask 1h = Mask
3	INT_MASK1[3]	R/W	1h	Mask for Interrupt due to Thermal Warning 125C 0h = Don't Mask 1h = Mask
2	INT_MASK1[2]	R/W	1h	Mask for Interrupt due to Thermal Warning 115C 0h = Don't Mask 1h = Mask
1	INT_MASK1[1]	R/W	1h	Mask for Interrupt due to Thermal Warning 105C 0h = Don't Mask 1h = Mask
0	RESERVED	R/W	1h	Reserved

7.1.40 INT_MASK_2 Register (Address = 5Dh) [Reset = 2Fh]

Return to the Summary Table.

This register configures Masks for Interrupt flags.

Table 7-41. INT_MASK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK2[7]	R/W	0h	Mask for Interrupt due to watchdog expiry 0h = Don't Mask 1h = Mask
6	RESERVED	R/W	0h	Reserved
5	INT_MASK2[5]	R/W	1h	Mask for Interrupt due to frame out of sync 0h = Don't Mask 1h = Mask
4	INT_MASK2[4]	R/W	0h	Mask for Interrupt due to PLL clock error 0h = Don't Mask 1h = Mask
3	INT_MASK2[3]	R/W	1h	Mask for Interrupt due to tdm error 0h = Don't Mask 1h = Mask
2	INT_MASK2[2]	R/W	1h	Mask for Interrupt due to ratio change error flag 0h = Don't Mask 1h = Mask
1	INT_MASK2[1]	R/W	1h	Mask for Interrupt due to fs change error flag 0h = Don't Mask 1h = Mask
0	INT_MASK2[0]	R/W	1h	Mask for Interrupt due to invalid ratio fs flag 0h = Don't Mask 1h = Mask

7.1.41 INT_MASK_3 Register (Address = 5Eh) [Reset = 10h]

Return to the Summary Table.

This register configures Masks for Interrupt flags.

Table 7-42. INT_MASK_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK3[7]	R/W	0h	Mask for Interrupt due to over temperature detected 0h = Don't Mask 1h = Mask
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	1h	Reserved
3	INT_MASK3[3]	R/W	0h	Mask for Interrupt due to Class-D Over current protection 0h = Don't Mask 1h = Mask
2	INT_MASK3[2]	R/W	0h	Mask for Interrupt due to pvdd_ov_flag 0h = Don't Mask 1h = Mask
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

7.1.42 INT_MASK_4 Register (Address = 5Fh) [Reset = 0Ah]

Return to the Summary Table.

This register configures Masks for Interrupt flags.

Table 7-43. INT_MASK_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK4[7]	R/W	0h	Mask for Interrupt due to vbat_por 0h = Don't Mask 1h = Mask
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	1h	Reserved
2	INT_MASK4[2]	R/W	0h	Mask for Interrupt due to clock halt flag. This interrupt also flags errors due to Pre-power-up clock error while using Wake-up-on-ASI feature 0h = Don't Mask 1h = Mask
1	RESERVED	R/W	1h	Reserved
0	RESERVED	R/W	0h	Reserved

7.1.43 INT_LATCH_0 Register (Address = 60h) [Reset = 00h]

Return to the Summary Table.

This register provides the status of latched interrupts.

Table 7-44. INT_LATCH_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH0[7]	R	0h	Interrupt due to BOP Inf Hold flag 0h = No interrupt 1h = Interrupt
6	INT_LTCH0[6]	R	0h	Interrupt due to limiter attentuation flag 0h = No interrupt 1h = Interrupt
5	INT_LTCH0[5]	R	0h	Interrupt due to supply less than inf pt flag 0h = No interrupt 1h = Interrupt
4	INT_LTCH0[4]	R	0h	Interrupt due to limiter active flag 0h = No interrupt 1h = Interrupt
3	INT_LTCH0[3]	R	0h	Interrupt due to brownout detected flag 0h = No interrupt 1h = Interrupt
2	INT_LTCH0[2]	R	0h	Interrupt due to bop active flag 0h = No interrupt 1h = Interrupt
1	INT_LTCH0[1]	R	0h	Live Interrupt due to device active flag 0h = No interrupt 1h = Interrupt
0	RESERVED	R	0h	Reserved

7.1.44 INT_LATCH_1 Register (Address = 61h) [Reset = 00h]

Return to the Summary Table.

This register provides the status of latched interrupts.

Table 7-45. INT_LATCH_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH1[7]	R	0h	Interrupt due to PVDD under voltage detection 0h = No interrupt 1h = Interrupt
6	INT_LTCH1[6]	R	0h	Interrupt due to VBAT2S under voltage detection 0h = No interrupt 1h = Interrupt
5	RESERVED	R	0h	Reserved
4	INT_LTCH1[4]	R	0h	Interrupt due to Thermal Warning 135C 0h = No interrupt 1h = Interrupt
3	INT_LTCH1[3]	R	0h	Interrupt due to Thermal Warning 125C 0h = No interrupt 1h = Interrupt
2	INT_LTCH1[2]	R	0h	Interrupt due to Thermal Warning 115C 0h = No interrupt 1h = Interrupt
1	INT_LTCH1[1]	R	0h	Interrupt due to Thermal Warning 105C 0h = No interrupt 1h = Interrupt
0	RESERVED	R	0h	Reserved

7.1.45 INT_LATCH_2 Register (Address = 62h) [Reset = 00h]

Return to the Summary Table.

This register provides the status of latched interrupts.

Table 7-46. INT_LATCH_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH2[7]	R	0h	Interrupt due to watchdog expiry 0h = No interrupt 1h = Interrupt
6	RESERVED	R	0h	Reserved
5	INT_LTCH2[5]	R	0h	Interrupt due to frame out of sync 0h = No interrupt 1h = Interrupt
4	INT_LTCH2[4]	R	0h	Interrupt due to PLL clock error 0h = No interrupt 1h = Interrupt
3	INT_LTCH2[3]	R	0h	Interrupt due to tdm error 0h = No interrupt 1h = Interrupt
2	INT_LTCH2[2]	R	0h	Interrupt due to ratio change error flag 0h = No interrupt 1h = Interrupt
1	INT_LTCH2[1]	R	0h	Interrupt due to fs change error flag 0h = No interrupt 1h = Interrupt
0	INT_LTCH2[0]	R	0h	Interrupt due to invalid ratio fs flag 0h = No interrupt 1h = Interrupt

7.1.46 INT_LATCH_3 Register (Address = 63h) [Reset = 00h]

Return to the Summary Table.

This register provides the status of latched interrupts.

Table 7-47. INT_LATCH_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH3[7]	R	0h	Interrupt due to over temperature detected 0h = No interrupt 1h = Interrupt
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	INT_LTCH3[3]	R	0h	Interrupt due to Class-D Over current protection 0h = No interrupt 1h = Interrupt
2	INT_LTCH3[2]	R	0h	Interrupt due to Over voltage on PVDD supply. 0h = No interrupt 1h = Interrupt
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.1.47 INT_LATCH_4 Register (Address = 64h) [Reset = 00h]

Return to the Summary Table.

This register provides the status of latched interrupts.

Table 7-48. INT_LATCH_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH4[7]	R	0h	Interrupt due to VBAT under voltage detection 0h = No interrupt 1h = Interrupt
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	INT_LTCH4[2]	R	0h	Interrupt due to clock halt flag 0h = No interrupt 1h = Interrupt
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.1.48 NG_IDLE_STATUS Register (Address = 65h) [Reset = 00h]

Return to the Summary Table.

This register provides the status of noise gate.

Table 7-49. NG_IDLE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NG_STATUS	R	0h	Noise mode status bit 0h = Device not in Noise gate mode 1h = Device in Noise gate mode
6	MUSIC_EFF_STATUS	R	0h	Music efficiency mode status bit 0h = Device not in music efficiency mode 1h = Device in music efficiency mode

Table 7-49. NG_IDLE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	RESERVED	R	0h	Reserved

7.1.49 REV_ID Register (Address = 78h) [Reset = 00h]

Return to the Summary Table.

Returns Revision ID (REV_ID).

Table 7-50. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	REV_ID[3:0]	R	0h	Returns the revision ID.
3-0	RESERVED	R	0h	Reserved

7.1.50 BOOK Register (Address = 7Fh) [Reset = 00h]

Return to the Summary Table.

Device's memory map is divided into pages and books. This register sets the book.

Table 7-51. BOOK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOOK[7:0]	R/W	0h	Sets the device book. 0h = Book 0 1h = Book 1 FFh = Book 255

7.2 PAGE 1 Registers

Table 7-52 lists the memory-mapped registers for the PAGE 1 registers. All register offset addresses not listed in Table 7-52 should be considered as reserved locations and the register contents should not be modified.

Table 7-52. PAGE 1 Registers

Address	Acronym	Description	Section
0h	PAGE	Device Page	Section 7.2.1
Ah	BOOST_TUNING_12	Boost configuration	Section 7.2.2
Eh	DEV_PERF_TUNING_07	Device performance tuning register	Section 7.2.3
18h	PVDD_OVLO1	PVDD Over voltage	Section 7.2.4
19h	DEVICE_CFG0	Device configuration	Section 7.2.5
1Ah	PVDD_OVLO2	PVDD Over voltage	Section 7.2.6
29h	DEVICE_CFG2	Device configuration	Section 7.2.7
2Bh	DEV_PERF_TUNING_04	Device performance Tuning register	Section 7.2.8
64h	I2C_CKSUM	I2C Checksum	Section 7.2.9

7.2.1 PAGE Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The device's memory map is divided into pages and books. This register sets the page.

Table 7-53. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.2.2 BOOST_TUNING_12 Register (Address = Ah) [Reset = 98h]

Return to the Summary Table.

Boost configuration

Table 7-54. BOOST_TUNING_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	2h	Reserved
5-2	BOOST_TUNING_12[3:0]	R/W	6h	Boost tuning register. Can be configured using the PPC3 software
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.2.3 DEV_PERF_TUNING_07 Register (Address = Eh) [Reset = 0Bh]

Return to the Summary Table.

Device performance tuning register

Table 7-55. DEV_PERF_TUNING_07 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5-4	RESERVED	R/W	0h	Reserved

Table 7-55. DEV_PERF_TUNING_07 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DEV_PERF_TUNING_07[3:0]	R/W	Bh	Device performance tuning register 0h = External PVDD mode tuning Bh = 1S mode tuning

7.2.4 PVDD_OVLO1 Register (Address = 18h) [Reset = EBh]

Return to the Summary Table.

Configures PVDD OVLO voltage in external PVDD mode

Table 7-56. PVDD_OVLO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	pvdd_ovlo_th_sel_ext_boost[1:0]	R/W	3h	Pvdd ovlo threshold selection during external PVDD mode 0h = 13.5V 1h = 14V 2h = 15V 3h = 16V
5-4	RESERVED	R/W	2h	Reserved
3-2	BOOST_TUNING_13[1:0]	R/W	2h	Boost tuning register 0h = Reserved 1h = 2S mode of operation 2h = 1S mode of operation 3h = Reserved
1-0	RESERVED	R/W	3h	Reserved

7.2.5 DEVICE_CFG0 Register (Address = 19h) [Reset = 23h]

Return to the Summary Table.

This register is to get boost performance to meet the device specification

Table 7-57. DEVICE_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	DEV_PERF_TUNING_03	R/W	1h	Device performance tuning register 0h = Device performance configuration 1h = Reserved
4	RESERVED	R/W	0h	Reserved
3-0	RESERVED	R/W	3h	Reserved

7.2.6 PVDD_OVLO2 Register (Address = 1Ah) [Reset = C4h]

Return to the Summary Table.

Configures PVDD OVLO voltage in Internal boost mode

Table 7-58. PVDD_OVLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	pvdd_ovlo_th_sel[1:0]	R/W	3h	Pvdd ovlo threshold selection - Internal boost mode 0h = 13.5V 1h = 14V 2h = 15V 3h = 16V
5-3	RESERVED	R	0h	Reserved

Table 7-58. PVDD_OVLO2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R/W	1h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.2.7 DEVICE_CFG2 Register (Address = 29h) [Reset = 04h]

Return to the Summary Table.

This register is to select device internal bias votlage requirements

Table 7-59. DEVICE_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	DEVICE_CFG_1[2:0]	R/W	0h	Configures internal Bias voltage 0h = Device performance configuration 1h = Reserved 2h = Reserved 3h = Reserved 4h = Reserved 5h = Reserved 6h = Reserved 7h = Reserved
4	VBAT_BIAS_SEL1	R/W	0h	Configures internal Bias voltages based on VBAT pin voltage 0h = based on VBAT_BIAS_SEL2 register 1h = interpolated as VBAT_2S/2
3-2	VBAT_BIAS_SEL2[1:0]	R/W	1h	Configures internal Bias voltages when VBAT_BIAS_SEL1=0 0h = Reserved 1h = Minimum VBAT pin voltage > 2.9V 2h = Minimum VBAT pin voltage >3.3V 3h = Minimum VBAT pin voltage >3.7V
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.2.8 DEV_PERF_TUNING_04 Register (Address = 2Bh) [Reset = 80h]

Return to the Summary Table.

Device performance Tuning register

Table 7-60. DEV_PERF_TUNING_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEV_PERF_TUNING_04[7:0]	R/W	80h	Device performance tuning. PPC3 software generates the correct configuration required

7.2.9 I2C_CKSUM Register (Address = 64h) [Reset = 00h]

Return to the Summary Table.

Returns I2C checksum.

Table 7-61. I2C_CKSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	R/W	0h	Returns I2C checksum. Writing to this register will reset the checksum to the written value. This register is updated on writes to other registers on all books and pages.

7.3 PAGE 2 Registers

Table 7-62 lists the memory-mapped registers for the PAGE 2 registers. All register offset addresses not listed in Table 7-62 should be considered as reserved locations and the register contents should not be modified.

Table 7-62. PAGE 2 Registers

Address	Acronym	Description	Section
0h	PAGE	Device Page	Section 7.3.1
Ch	DVC_LEVEL	Digital Volume Control Level	Section 7.3.2
10h	DVC_SLEW_RATE	Digital Volume Control Slew Rate	Section 7.3.3
18h	AUDIO_HPF_N0	Set Audio DC Blocker filter coefficients	Section 7.3.4
1Ch	AUDIO_HPF_N1	Set Audio DC Blocker filter coefficients	Section 7.3.5
20h	AUDIO_HPF_D1	Set Audio DC Blocker filter coefficients	Section 7.3.6
54h	TONE_GEN_CNTRL_01	Tone generator Frequency Control register	Section 7.3.7
58h	TONE_GEN_CNTRL_02	Tone generator Frequency Control register	Section 7.3.8
5Ch	TONE_GEN_CNTRL_03	Tone generator Frequency Control register	Section 7.3.9
60h	TONE_GEN_CNTRL_04	Tone generator Frequency Control register	Section 7.3.10
64h	TONE_GEN_CNTRL_05	Tone generator Frequency Control register	Section 7.3.11
68h	TONE_GEN_CNTRL_06	Tone generator amplitude control register	Section 7.3.12
6Ch	CLASSH_TUNING_01	ClassH Tuning Coefficient	Section 7.3.13
70h	CLASSH_TUNING_02	ClassH Tuning Coefficient	Section 7.3.14
74h	CLASSH_TUNING_03	ClassH Tuning Coefficient	Section 7.3.15
78h	CLASSH_TUNING_04	ClassH Tuning Coefficient	Section 7.3.16
7Ch	CLASSH_TUNING_05	ClassH Tuning Coefficient	Section 7.3.17

7.3.1 PAGE Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The devices memory map is divided into pages and books. This register sets the page.

Table 7-63. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.3.2 DVC_LEVEL Register (Address = Ch) [Reset = 400000h]

Return to the Summary Table.

Digital Volume Control Level

Table 7-64. DVC_LEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DVC_LEVEL[23:0]	R/W	400000h	Addresses 0xC to 0xE are combined. Can be configured using the PPC3 Software.

7.3.3 DVC_SLEW_RATE Register (Address = 10h) [Reset = 034A51h]

Return to the Summary Table.

Digital Volume Control Slew Rate

Table 7-65. DVC_SLEW_RATE Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DVC_SLEW_RATE[23:0]	R/W	34A51h	Addresses 0x10 to 0x12 are combined. Can be configured using the PPC3 Software.

7.3.4 AUDIO_HPF_N0 Register (Address = 18h) [Reset = 7FFBB6h]

Return to the Summary Table.

Set Audio DC Blocker filter coefficients

Table 7-66. AUDIO_HPF_N0 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	AUDIO_HPF_N0[23:0]	R/W	7FFBB6h	Addresses 0x18 to 0x1A are combined. Can be configured using the PPC3 Software.

7.3.5 AUDIO_HPF_N1 Register (Address = 1Ch) [Reset = 80044Ah]

Return to the Summary Table.

Set Audio DC Blocker filter coefficients

Table 7-67. AUDIO_HPF_N1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	AUDIO_HPF_N1[23:0]	R/W	80044Ah	Addresses 0x1C to 0x1E are combined. Can be configured using the PPC3 Software.

7.3.6 AUDIO_HPF_D1 Register (Address = 20h) [Reset = 7FF76Ch]

Return to the Summary Table.

Set Audio DC Blocker filter coefficients

Table 7-68. AUDIO_HPF_D1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	AUDIO_HPF_D1[23:0]	R/W	7FF76Ch	Addresses 0x20 to 0x22 are combined. Can be configured using the PPC3 Software.

7.3.7 TONE_GEN_CNTRL_01 Register (Address = 54h) [Reset = 7FFFEDh]

Return to the Summary Table.

Tone generator Frequency Control register

Table 7-69. TONE_GEN_CNTRL_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	TONE_GEN_CNTRL_01[23:0]	R/W	7FFFEDh	Addresses 0x54 to 0x56 are combined. Can be configured using the PPC3 Software.

7.3.8 TONE_GEN_CNTRL_02 Register (Address = 58h) [Reset = 4D0582h]

Return to the Summary Table.

Tone generator Frequency Control register

Table 7-70. TONE_GEN_CNTRL_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	TONE_GEN_CNTRL_02[23:0]	R/W	4D0582h	Addresses 0x58 to 0x5A are combined. Can be configured using the PPC3 Software.

7.3.9 TONE_GEN_CNTRL_03 Register (Address = 5Ch) [Reset = 002250h]

Return to the Summary Table.

Tone generator Frequency Control register

Table 7-71. TONE_GEN_CNTRL_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	TONE_GEN_CNTRL_03[23:0]	R/W	2250h	Addresses 0x5C to 0x5E are combined. Can be configured using the PPC3 Software.

7.3.10 TONE_GEN_CNTRL_04 Register (Address = 60h) [Reset = 42FC96h]

Return to the Summary Table.

Tone generator Frequency Control register

Table 7-72. TONE_GEN_CNTRL_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	TONE_GEN_CNTRL_04[23:0]	R/W	42FC96h	Addresses 0x60 to 0x62 are combined. Can be configured using the PPC3 Software.

7.3.11 TONE_GEN_CNTRL_05 Register (Address = 64h) [Reset = 000BB8h]

Return to the Summary Table.

Tone generator Frequency Control register

Table 7-73. TONE_GEN_CNTRL_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	TONE_GEN_CNTRL_05[23:0]	R/W	BB8h	Addresses 0x64 to 0x66 are combined. Can be configured using the PPC3 Software.

7.3.12 TONE_GEN_CNTRL_06 Register (Address = 68h) [Reset = 01235Ah]

Return to the Summary Table.

Tone generator amplitude control register

Table 7-74. TONE_GEN_CNTRL_06 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	TONE_GEN_CNTRL_06[23:0]	R/W	1235Ah	Addresses 0x68 to 0x6A are combined. Can be configured using the PPC3 Software.

7.3.13 CLASSH_TUNING_01 Register (Address = 6Ch) [Reset = 000280h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-75. CLASSH_TUNING_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_01[23:0]	R/W	280h	Addresses 0x6C to 0x6E are combined. Can be configured using the PPC3 Software.

7.3.14 CLASSH_TUNING_02 Register (Address = 70h) [Reset = 800000h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-76. CLASSH_TUNING_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_02[23:0]	R/W	800000h	Addresses 0x70 to 0x72 are combined. Can be configured using the PPC3 Software.

7.3.15 CLASSH_TUNING_03 Register (Address = 74h) [Reset = 507480h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-77. CLASSH_TUNING_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_03[23:0]	R/W	507480h	Addresses 0x74 to 0x76 are combined. Can be configured using the PPC3 Software.

7.3.16 CLASSH_TUNING_04 Register (Address = 78h) [Reset = 400000h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-78. CLASSH_TUNING_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_04[23:0]	R/W	400000h	Addresses 0x78 to 0x7A are combined. Can be configured using the PPC3 Software.

7.3.17 CLASSH_TUNING_05 Register (Address = 7Ch) [Reset = 006666h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-79. CLASSH_TUNING_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_05[23:0]	R/W	6666h	Addresses 0x7C to 0x7E are combined. Can be configured using the PPC3 Software.

7.4 PAGE 3 Registers

Table 7-80 lists the memory-mapped registers for the PAGE 3 registers. All register offset addresses not listed in Table 7-80 should be considered as reserved locations and the register contents should not be modified.

Table 7-80. PAGE 3 Registers

Address	Acronym	Description	Section
0h	PAGE	Device Page	Section 7.4.1
8h	BST_ILIM	Set Boost Current Limit	Section 7.4.2
Ch	BOOST_TUNING_15	Boost Performance tuning register	Section 7.4.3
10h	BOOST_TUNING_01	Boost Performance tuning register	Section 7.4.4
14h	BOOST_TUNING_02	Boost Performance tuning register	Section 7.4.5
18h	BOOST_TUNING_03	Boost Performance tuning register	Section 7.4.6
1Ch	BOOST_TUNING_04	Boost Performance tuning register	Section 7.4.7
20h	BOOST_TUNING_05	Boost Performance tuning register	Section 7.4.8
24h	BOOST_TUNING_06	Boost Performance tuning register	Section 7.4.9
28h	BOOST_TUNING_07	Boost Performance tuning register	Section 7.4.10
2Ch	BOOST_TUNING_08	Boost Performance tuning register	Section 7.4.11
30h	BOOST_TUNING_09	Boost Performance tuning register	Section 7.4.12
34h	BOOST_TUNING_10	Boost Performance tuning register	Section 7.4.13
38h	BOOST_TUNING_11	Boost Performance tuning register	Section 7.4.14

7.4.1 PAGE Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The devices memory map is divided into pages and books.This register sets the page.

Table 7-81. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.4.2 BST_ILIM Register (Address = 8h) [Reset = 2B8000h]

Return to the Summary Table.

Set Boost Current Limit

Table 7-82. BST_ILIM Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BST_ILIM[23:0]	R/W	2B8000h	Addresses 0x8 to 0xA are combined. Can be configured using the PPC3 Software.

7.4.3 BOOST_TUNING_15 Register (Address = Ch) [Reset = 400000h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-83. BOOST_TUNING_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_15[23:0]	R/W	400000h	Addresses 0xC to 0xE are combined. Can be configured using the PPC3 Software.

7.4.4 BOOST_TUNING_01 Register (Address = 10h) [Reset = FEA000h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-84. BOOST_TUNING_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_01[23:0]	R/W	FEA000h	Addresses 0x10 to 0x12 are combined. Can be configured using the PPC3 Software.

7.4.5 BOOST_TUNING_02 Register (Address = 14h) [Reset = 180000h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-85. BOOST_TUNING_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_02[23:0]	R/W	180000h	Addresses 0x14 to 0x16 are combined. Can be configured using the PPC3 Software.

7.4.6 BOOST_TUNING_03 Register (Address = 18h) [Reset = 000000h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-86. BOOST_TUNING_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_03[23:0]	R/W	0h	Addresses 0x18 to 0x1A are combined. Can be configured using the PPC3 Software.

7.4.7 BOOST_TUNING_04 Register (Address = 1Ch) [Reset = FF9555h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-87. BOOST_TUNING_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_04[23:0]	R/W	FF9555h	Addresses 0x1C to 0x1E are combined. Can be configured using the PPC3 Software.

7.4.8 BOOST_TUNING_05 Register (Address = 20h) [Reset = FFF8B2h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-88. BOOST_TUNING_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_05[23:0]	R/W	FFF8B2h	Addresses 0x20 to 0x22 are combined. Can be configured using the PPC3 Software.

7.4.9 BOOST_TUNING_06 Register (Address = 24h) [Reset = 000466h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-89. BOOST_TUNING_06 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_06[23:0]	R/W	466h	Addresses 0x24 to 0x26 are combined. Can be configured using the PPC3 Software.

7.4.10 BOOST_TUNING_07 Register (Address = 28h) [Reset = 080000h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-90. BOOST_TUNING_07 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_07[23:0]	R/W	80000h	Addresses 0x28 to 0x2A are combined. Can be configured using the PPC3 Software.

7.4.11 BOOST_TUNING_08 Register (Address = 2Ch) [Reset = 001400h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-91. BOOST_TUNING_08 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_08[23:0]	R/W	1400h	Addresses 0x2C to 0x2E are combined. Can be configured using the PPC3 Software.

7.4.12 BOOST_TUNING_09 Register (Address = 30h) [Reset = 000000h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-92. BOOST_TUNING_09 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_09[23:0]	R/W	0h	Addresses 0x30 to 0x32 are combined. Can be configured using the PPC3 Software.

7.4.13 BOOST_TUNING_10 Register (Address = 34h) [Reset = 000000h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-93. BOOST_TUNING_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_10[23:0]	R/W	0h	Addresses 0x34 to 0x36 are combined. Can be configured using the PPC3 Software.

7.4.14 BOOST_TUNING_11 Register (Address = 38h) [Reset = 000000h]

Return to the Summary Table.

Boost Performance tuning register

Table 7-94. BOOST_TUNING_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOOST_TUNING_11[23:0]	R/W	0h	Addresses 0x38 to 0x3A are combined. Can be configured using the PPC3 Software.

7.5 PAGE 4 Registers

Table 7-95 lists the memory-mapped registers for the PAGE 4 registers. All register offset addresses not listed in Table 7-95 should be considered as reserved locations and the register contents should not be modified.

Table 7-95. PAGE 4 Registers

Address	Acronym	Description	Section
0h	PAGE	Device Page	Section 7.5.1
8h	VDD_MODE_THR_LVL	VDD Y Bridge Set Threshold	Section 7.5.2
Ch	VDD_MODE_HYST	VDD Y Bridge Set Threshold hysterisis	Section 7.5.3
18h	MUSIC_EFF_MODE_THR	Set Music Efficiency Mode Threshold	Section 7.5.4
1Ch	MUSIC_EFF_MODE_TIMER	Set Music Efficiency Mode Hysteresis	Section 7.5.5
38h	LIM_MAX_ATT	Limiter Set Maximum Attenuation	Section 7.5.6
3Ch	LIM_TH_MAX	Limiter Set maximum audio limiting threshold	Section 7.5.7
40h	LIM_TH_MIN	Limiter Set minimum audio limiting threshold	Section 7.5.8
44h	LIM_INF_PT	Limiter Set Inflection Point	Section 7.5.9
48h	LIM_SLOPE	Limiter Set Slope	Section 7.5.10
4Ch	LIM_ATK_RATE	Limiter Set Attack Rate	Section 7.5.11
50h	LIM_RLS_RATE	Limiter Set Release Rate	Section 7.5.12
54h	LIM_HLD_COUNT	Limiter Set Hold Count	Section 7.5.13
58h	BOP_ATK_RATE	Brown Out Protection Set Attack Rate	Section 7.5.14
5Ch	BOP_HLD_COUNT	Brown Out Protection Set Hold Count	Section 7.5.15
60h	BOP_THR_LVL	Brown Out Protection Set Threshold Level	Section 7.5.16
64h	BOSD_THR_LVL	Brown Out Protection ShutDown Set Threshold Level	Section 7.5.17
74h	DEV_PERF_TUNING_01	Device performance tuning register	Section 7.5.18
78h	DEV_PERF_TUNING_02	Device performance tuning register	Section 7.5.19

7.5.1 PAGE Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The devices memory map is divided into pages and books. This register sets the page.

Table 7-96. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.5.2 VDD_MODE_THR_LVL Register (Address = 8h) [Reset = 50A3D7h]

Return to the Summary Table.

VDD Y Bridge Set Threshold

Table 7-97. VDD_MODE_THR_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	VDD_MODE_THR_LVL[23:0]	R/W	50A3D7h	Addresses 0x8 to 0xA are combined. Can be configured using the PPC3 Software.

7.5.3 VDD_MODE_HYST Register (Address = Ch) [Reset = 00DA74h]

Return to the Summary Table.

VDD Y Bridge Set Threshold hysterisis

Table 7-98. VDD_MODE_HYST Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	VDD_MODE_HYST[23:0]	R/W	DA74h	Addresses 0xC to 0xE are combined. Can be configured using the PPC3 Software.

7.5.4 MUSIC_EFF_MODE_THR Register (Address = 18h) [Reset = 0443F5h]

Return to the Summary Table.

Set Music Efficiency Mode Threshold

Table 7-99. MUSIC_EFF_MODE_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	MUSIC_EFF_MODE_THR[23:0]	R/W	443F5h	Addresses 0x18 to 0x1A are combined. Can be configured using the PPC3 Software.

7.5.5 MUSIC_EFF_MODE_TIMER Register (Address = 1Ch) [Reset = 000034h]

Return to the Summary Table.

Set Music Efficiency Mode Hysteresis

Table 7-100. MUSIC_EFF_MODE_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	MUSIC_EFF_MODE_TIMER[23:0]	R/W	34h	Addresses 0x1C to 0x1E are combined. Can be configured using the PPC3 Software.

7.5.6 LIM_MAX_ATT Register (Address = 38h) [Reset = 2D6A86h]

Return to the Summary Table.

Limiter Set Maximum Attenuation

Table 7-101. LIM_MAX_ATT Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LIM_MAX_ATT[23:0]	R/W	2D6A86h	Addresses 0x38 to 0x3A are combined. Can be configured using the PPC3 Software.

7.5.7 LIM_TH_MAX Register (Address = 3Ch) [Reset = 400000h]

Return to the Summary Table.

Limiter Set maximum audio limiting threshold

Table 7-102. LIM_TH_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LIM_TH_MAX[23:0]	R/W	400000h	Addresses 0x3C to 0x3E are combined. Can be configured using the PPC3 Software.

7.5.8 LIM_TH_MIN Register (Address = 40h) [Reset = 0A0000h]

Return to the Summary Table.

Limiter Set minimum audio limiting threshold

Table 7-103. LIM_TH_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LIM_TH_MIN[23:0]	R/W	A0000h	Addresses 0x40 to 0x42 are combined. Can be configured using the PPC3 Software.

7.5.9 LIM_INF_PT Register (Address = 44h) [Reset = 0D3333h]

Return to the Summary Table.

Limiter Set Inflection Point

Table 7-104. LIM_INF_PT Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LIM_INF_PT[23:0]	R/W	D3333h	Addresses 0x44 to 0x46 are combined. Can be configured using the PPC3 Software.

7.5.10 LIM_SLOPE Register (Address = 48h) [Reset = 100000h]

Return to the Summary Table.

Limiter Set Slope

Table 7-105. LIM_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LIM_SLOPE[23:0]	R/W	100000h	Addresses 0x48 to 0x4A are combined. Can be configured using the PPC3 Software.

7.5.11 LIM_ATK_RATE Register (Address = 4Ch) [Reset = 7C5E4Eh]

Return to the Summary Table.

Limiter Set Attack Rate

Table 7-106. LIM_ATK_RATE Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LIM_ATK_RATE[23:0]	R/W	7C5E4Eh	Addresses 0x4C to 0x4E are combined. Can be configured using the PPC3 Software.

7.5.12 LIM_RLS_RATE Register (Address = 50h) [Reset = 400179h]

Return to the Summary Table.

Limiter Set Release Rate

Table 7-107. LIM_RLS_RATE Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LIM_RLS_RATE[23:0]	R/W	400179h	Addresses 0x50 to 0x52 are combined. Can be configured using the PPC3 Software.

7.5.13 LIM_HLD_COUNT Register (Address = 54h) [Reset = 005DC0h]

Return to the Summary Table.

Limiter Set Hold Count

Table 7-108. LIM_HLD_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LIM_HLD_COUNT[23:0]	R/W	5DC0h	Addresses 0x5C to 0x5E are combined. Can be configured using the PPC3 Software.

7.5.14 BOP_ATK_RATE Register (Address = 58h) [Reset = 78D67Ch]

Return to the Summary Table.

Brown Out Protection Set Attack Rate

Table 7-109. BOP_ATK_RATE Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOP_ATK_RATE[23:0]	R/W	78D67Ch	Addresses 0x58 to 0x5A are combined. Can be configured using the PPC3 Software.

7.5.15 BOP_HLD_COUNT Register (Address = 5Ch) [Reset = 005DC0h]

Return to the Summary Table.

Brown Out Protection Set Hold Count

Table 7-110. BOP_HLD_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOP_HLD_COUNT[23:0]	R/W	5DC0h	Addresses 0x5C to 0x5E are combined. Can be configured using the PPC3 Software.

7.5.16 BOP_THR_LVL Register (Address = 60h) [Reset = 0B9999h]

Return to the Summary Table.

Brown Out Protection Set Threshold Level

Table 7-111. BOP_THR_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOP_THR_LVL[23:0]	R/W	B9999h	Addresses 0x60 to 0x62 are combined. Can be configured using the PPC3 Software.

7.5.17 BOSD_THR_LVL Register (Address = 64h) [Reset = 0ACCCCh]

Return to the Summary Table.

Brown Out Protection ShutDown Set Threshold Level

Table 7-112. BOSD_THR_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	BOSD_THR_LVL[23:0]	R/W	ACCCCh	Addresses 0x64 to 0x66 are combined. Can be configured using the PPC3 Software.

7.5.18 DEV_PERF_TUNING_01 Register (Address = 74h) [Reset = 079BCCh]

Return to the Summary Table.

Device performance tuning register

Table 7-113. DEV_PERF_TUNING_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_01[23:0]	R/W	79BCCh	Addresses 0x74 to 0x76 are combined. Can be configured using the PPC3 Software.

7.5.19 DEV_PERF_TUNING_02 Register (Address = 78h) [Reset = 000034h]

Return to the Summary Table.

Device performance tuning register

Table 7-114. DEV_PERF_TUNING_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_02[23:0]	R/W	34h	Addresses 0x78 to 0x7A are combined. Can be configured using the PPC3 Software.

7.6 PAGE 5 Registers

Table 7-115 lists the memory-mapped registers for the PAGE 5 registers. All register offset addresses not listed in Table 7-115 should be considered as reserved locations and the register contents should not be modified.

Table 7-115. PAGE 5 Registers

Address	Acronym	Description	Section
0h	PAGE	Device Page	Section 7.6.1
64h	THERMAL_WARN_MIN_TEMP	Thermal Flag	Section 7.6.2
68h	THERMAL_WARN_TEMP_STEP	Thermal Flag	Section 7.6.3

7.6.1 PAGE Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The devices memory map is divided into pages and books. This register sets the page.

Table 7-116. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.6.2 THERMAL_WARN_MIN_TEMP Register (Address = 64h) [Reset = 348000h]

Return to the Summary Table.

Set the minimum threshold for Thermal Flag

Table 7-117. THERMAL_WARN_MIN_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	THERMAL_WARN_MIN_TEMP[23:0]	R/W	348000h	Addresses 0x64 to 0x66 are combined. Can be configured using the PPC3 Software.

7.6.3 THERMAL_WARN_TEMP_STEP Register (Address = 68h) [Reset = 050000h]

Return to the Summary Table.

Set the delta threshold for Thermal Flag

Table 7-118. THERMAL_WARN_TEMP_STEP Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	THERMAL_WARN_TEMP_STEP[23:0]	R/W	50000h	Addresses 0x68 to 0x6A are combined. Can be configured using the PPC3 Software.

7.7 PAGE 6 Registers

Table 7-119 lists the memory-mapped registers for the PAGE 6 registers. All register offset addresses not listed in Table 7-119 should be considered as reserved locations and the register contents should not be modified.

Table 7-119. PAGE 6 Registers

Address	Acronym	Description	Section
0h	PAGE	Device Page	Section 7.7.1
1Ch	CLASSH_TUNING_07	ClassH Tuning Coefficient	Section 7.7.2
20h	CLASSH_TUNING_08	ClassH Tuning Coefficient	Section 7.7.3
24h	CLASSH_TUNING_09	ClassH Tuning Coefficient	Section 7.7.4
30h	DEV_PERF_TUNING_14	Device performance tuning	Section 7.7.5
34h	DEV_PERF_TUNING_24	Device performance tuning	Section 7.7.6
38h	DEV_PERF_TUNING_18	Device performance tuning	Section 7.7.7
48h	DEV_PERF_TUNING_25	Device performance tuning	Section 7.7.8
60h	CLASSH_TUNING_10	ClassH Tuning Coefficient	Section 7.7.9
70h	CLASSH_TUNING_11	ClassH Tuning Coefficient	Section 7.7.10
74h	CLASSH_TUNING_12	ClassH Tuning Coefficient	Section 7.7.11
78h	CLASSH_TUNING_13	ClassH Tuning Coefficient	Section 7.7.12
7Ch	CLASSH_TUNING_14	ClassH Tuning Coefficient	Section 7.7.13

7.7.1 PAGE Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The devices memory map is divided into pages and books. This register sets the page.

Table 7-120. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.7.2 CLASSH_TUNING_07 Register (Address = 1Ch) [Reset = 0A72ABh]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-121. CLASSH_TUNING_07 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_07[23:0]	R/W	A72ABh	Addresses 0x1C to 0x1E are combined. Can be configured using the PPC3 Software.

7.7.3 CLASSH_TUNING_08 Register (Address = 20h) [Reset = 103F46h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-122. CLASSH_TUNING_08 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_08[23:0]	R/W	103F46h	Addresses 0x20 to 0x22 are combined. Can be configured using the PPC3 Software.

7.7.4 CLASSH_TUNING_09 Register (Address = 24h) [Reset = 0A45F1h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-123. CLASSH_TUNING_09 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_09[23:0]	R/W	A45F1h	Addresses 0x24 to 0x26 are combined. Can be configured using the PPC3 Software.

7.7.5 DEV_PERF_TUNING_14 Register (Address = 30h) [Reset = 400000h]

Return to the Summary Table.

Device performance tuning

Table 7-124. DEV_PERF_TUNING_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_14[23:0]	R/W	400000h	Addresses 0x30 to 0x32 are combined. Can be configured using the PPC3 Software.

7.7.6 DEV_PERF_TUNING_24 Register (Address = 34h) [Reset = 400000h]

Return to the Summary Table.

Device performance tuning

Table 7-125. DEV_PERF_TUNING_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_24[23:0]	R/W	400000h	Addresses 0x34 to 0x36 are combined. Can be configured using the PPC3 Software.

7.7.7 DEV_PERF_TUNING_18 Register (Address = 38h) [Reset = 400000h]

Return to the Summary Table.

Device performance tuning

Table 7-126. DEV_PERF_TUNING_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_18[23:0]	R/W	400000h	Addresses 0x38 to 0x3A are combined. Can be configured using the PPC3 Software.

7.7.8 DEV_PERF_TUNING_25 Register (Address = 48h) [Reset = 166666h]

Return to the Summary Table.

Device performance tuning

Table 7-127. DEV_PERF_TUNING_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_25[23:0]	R/W	166666h	Addresses 0x48 to 0x4A are combined. Can be configured using the PPC3 Software.

7.7.9 CLASSH_TUNING_10 Register (Address = 60h) [Reset = 074969h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-128. CLASSH_TUNING_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_10[23:0]	R/W	74969h	Addresses 0x60 to 0x62 are combined. Can be configured using the PPC3 Software.

7.7.10 CLASSH_TUNING_11 Register (Address = 70h) [Reset = 133333h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-129. CLASSH_TUNING_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_11[23:0]	R/W	133333h	Addresses 0x70 to 0x72 are combined. Can be configured using the PPC3 Software.

7.7.11 CLASSH_TUNING_12 Register (Address = 74h) [Reset = 04999Ah]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-130. CLASSH_TUNING_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_12[23:0]	R/W	4999Ah	Addresses 0x74 to 0x76 are combined. Can be configured using the PPC3 Software.

7.7.12 CLASSH_TUNING_13 Register (Address = 78h) [Reset = 046666h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-131. CLASSH_TUNING_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_13[23:0]	R/W	46666h	Addresses 0x78 to 0x7A are combined. Can be configured using the PPC3 Software.

7.7.13 CLASSH_TUNING_14 Register (Address = 7Ch) [Reset = 280000h]

Return to the Summary Table.

ClassH Tuning Coefficient

Table 7-132. CLASSH_TUNING_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_14[23:0]	R/W	280000h	Addresses 0x7C to 0x7E are combined. Can be configured using the PPC3 Software.

7.8 PAGE 7 Registers

Table 7-133 lists the memory-mapped registers for the PAGE 7 registers. All register offset addresses not listed in Table 7-133 should be considered as reserved locations and the register contents should not be modified.

Table 7-133. PAGE 7 Registers

Address	Acronym	Description	Section
0h	PAGE	Device Page	Section 7.8.1
30h	DEV_PERF_TUNING_17	Device performance Tuning	Section 7.8.2
44h	CLASSH_TUNING_15	ClassH Tuning register	Section 7.8.3
78h	DEV_PERF_TUNING_21	Device performance Tuning	Section 7.8.4
7Ch	DEV_PERF_TUNING_05	Device performance Tuning	Section 7.8.5

7.8.1 PAGE Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The devices memory map is divided into pages and books. This register sets the page.

Table 7-134. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.8.2 DEV_PERF_TUNING_17 Register (Address = 30h) [Reset = 0E9DDFh]

Return to the Summary Table.

Device performance Tuning

Table 7-135. DEV_PERF_TUNING_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_17[23:0]	R/W	E9DDFh	Addresses 0x30 to 0x32 are combined. Can be configured using the PPC3 Software.

7.8.3 CLASSH_TUNING_15 Register (Address = 44h) [Reset = 580000h]

Return to the Summary Table.

ClassH Tuning register

Table 7-136. CLASSH_TUNING_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CLASSH_TUNING_15[23:0]	R/W	580000h	Addresses 0x44 to 0x46 are combined. Can be configured using the PPC3 Software.

7.8.4 DEV_PERF_TUNING_21 Register (Address = 78h) [Reset = 000070h]

Return to the Summary Table.

Device performance Tuning

Table 7-137. DEV_PERF_TUNING_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_21[23:0]	R/W	70h	Addresses 0x78 to 0x7A are combined. Can be configured using the PPC3 Software.

7.8.5 DEV_PERF_TUNING_05 Register (Address = 7Ch) [Reset = 000000h]

Return to the Summary Table.

Device performance Tuning

Table 7-138. DEV_PERF_TUNING_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_05[23:0]	R/W	0h	Addresses 0x7C to 0x7E are combined. Can be configured using the PPC3 Software.

7.9 PAGE 8 Registers

Table 7-139 lists the memory-mapped registers for the PAGE 8 registers. All register offset addresses not listed in Table 7-139 should be considered as reserved locations and the register contents should not be modified.

Table 7-139. PAGE 8 Registers

Address	Acronym	Description	Section
0h	PAGE	Device Page	Section 7.9.1
8h	DEV_PERF_TUNING_08	Device performance tuning	Section 7.9.2
Ch	DEV_PERF_TUNING_09	Device performance tuning	Section 7.9.3
10h	DEV_PERF_TUNING_10	Device performance tuning	Section 7.9.4
14h	DEV_PERF_TUNING_06	Device performance tuning	Section 7.9.5

7.9.1 PAGE Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The devices memory map is divided into pages and books. This register sets the page.

Table 7-140. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.9.2 DEV_PERF_TUNING_08 Register (Address = 8h) [Reset = 002D0Eh]

Return to the Summary Table.

Device performance tuning

Table 7-141. DEV_PERF_TUNING_08 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_08[23:0]	R/W	2D0Eh	Addresses 0x8 to 0xA are combined. Can be configured using the PPC3 Software.

7.9.3 DEV_PERF_TUNING_09 Register (Address = Ch) [Reset = F8CCCDh]

Return to the Summary Table.

Device performance tuning

Table 7-142. DEV_PERF_TUNING_09 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_09[23:0]	R/W	F8CCCDh	Addresses 0xC to 0xE are combined. Can be configured using the PPC3 Software.

7.9.4 DEV_PERF_TUNING_10 Register (Address = 10h) [Reset = 009AC0h]

Return to the Summary Table.

Device performance tuning

Table 7-143. DEV_PERF_TUNING_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_10[23:0]	R/W	9AC0h	Addresses 0x10 to 0x12 are combined. Can be configured using the PPC3 Software.

7.9.5 DEV_PERF_TUNING_06 Register (Address = 14h) [Reset = 000007h]

Return to the Summary Table.

Device performance tuning

Table 7-144. DEV_PERF_TUNING_06 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_06[23:0]	R/W	7h	Addresses 0x14 to 0x16 are combined. Can be configured using the PPC3 Software.

7.10 BOOK100 PAGE9 Registers

Table 7-145 lists the memory-mapped registers for the BOOK100 PAGE9 registers. All register offset addresses not listed in Table 7-145 should be considered as reserved locations and the register contents should not be modified.

Table 7-145. BOOK100 PAGE9 Registers

Address	Acronym	Description	Section
0h	PAGE	Device Page	Section 7.10.1
58h	DEV_PERF_TUNING_19	Device performance tuning	Section 7.10.2

7.10.1 PAGE Register (Address = 0h) [Reset = 00h]

Return to the Summary Table.

The devices memory map is divided into pages and books. This register sets the page.

Table 7-146. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0h	Sets the device page. 0h = Page 0 1h = Page 1 FFh = Page 255

7.10.2 DEV_PERF_TUNING_19 Register (Address = 58h) [Reset = 000000h]

Return to the Summary Table.

Device performance tuning

Table 7-147. DEV_PERF_TUNING_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	DEV_PERF_TUNING_19[23:0]	R/W	0h	Addresses 0x58 to 0x5A are combined. Can be configured using the PPC3 Software.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TAS2120 is a mono channel digital-in Class-D amplifier with integrated Boost, battery voltage and temperature monitoring capabilities. I^2S audio data is supplied by host processor via SDIN data port along with the bit clock and frame sync signals. I^2C bus is used for configuration and control.

The device needs external power supply voltage rails of VBAT: 2.5V to 5.5V, VDD : 1.65V to 1.95V and IOVDD: 1.8V or 3.3V for operation.

PurePath™ Console 3 (PPC3) software is the recommended tool to configure the device, and it enables optimization of device performance parameters depending on different application scenarios.

8.2 Typical Application

Diagrams below show typical application connections for Internal Boost and for External PVDD mode. SEL1_I2C pin is used for HW Mode selection or I^2C Mode selection of the Device.

System can use same 1.8V supply source to power the IOVDD and VDD if required. The decoupling caps C2 and C3 should be placed close to the device pins.

VBAT, VDD, PVDD power rails are critical for device performance and wide trace should be used from the source PMIC to these pins to minimize parasitic inductance. Supply ripple should be kept at minimum for these rails and should be connected to common supply planes.

Errata: Additional 2mA to 3mA current consumption expected if IRQZ singal is pulled high. Read more details in What to Do and What Not to Do section.

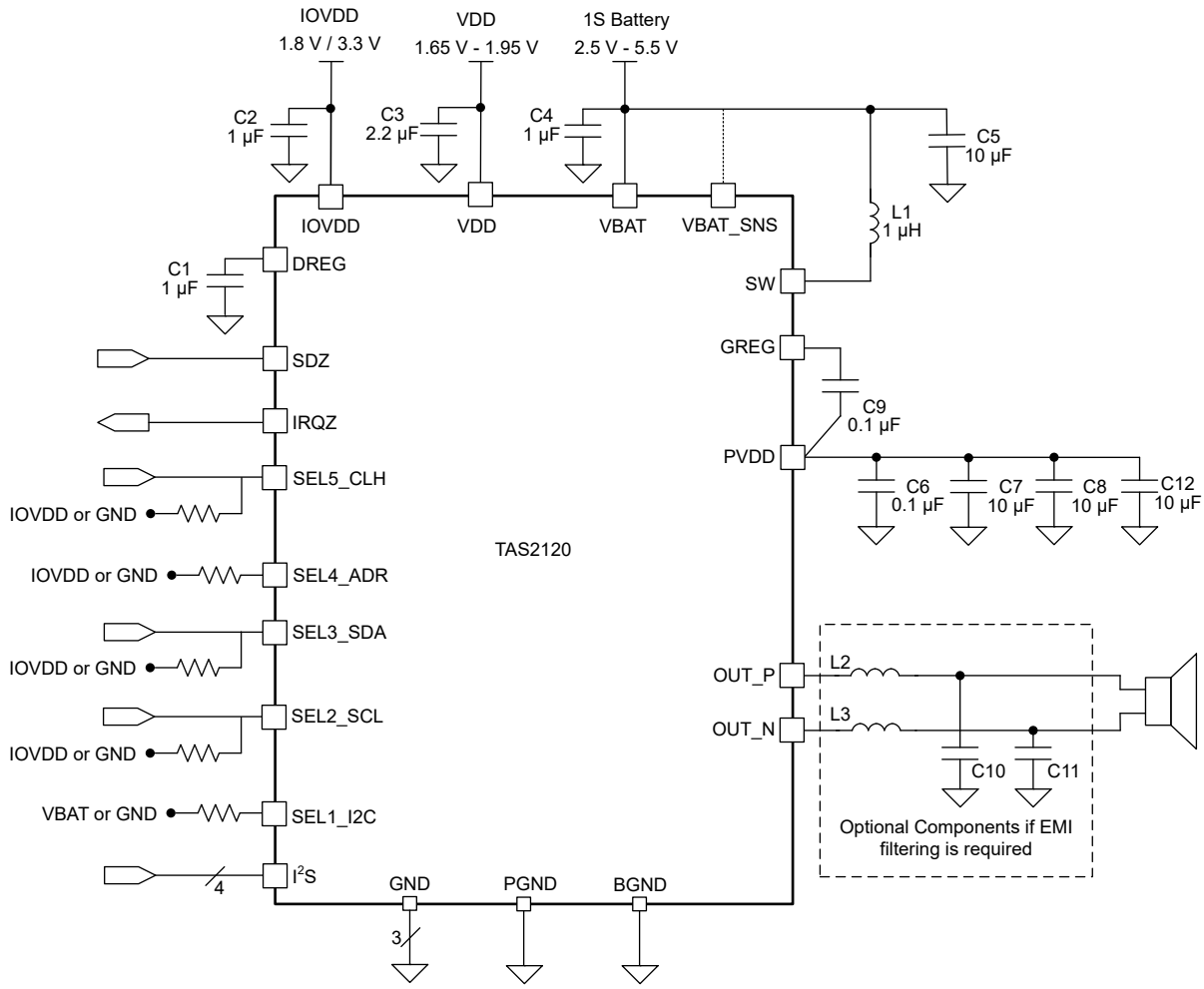


Figure 8-1. Application Diagram for 1S Battery system

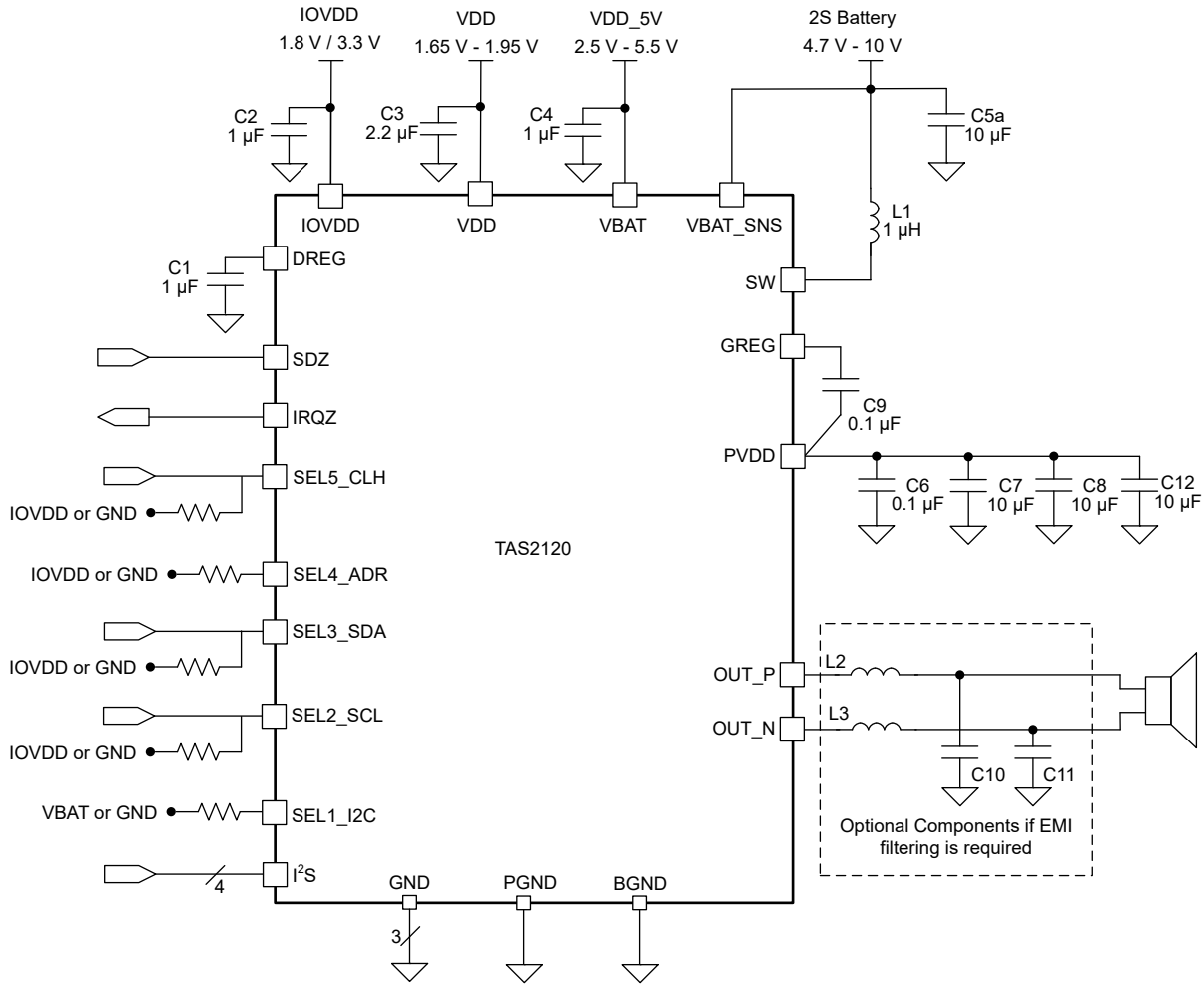


Figure 8-2. Application Diagram for 2S Battery system

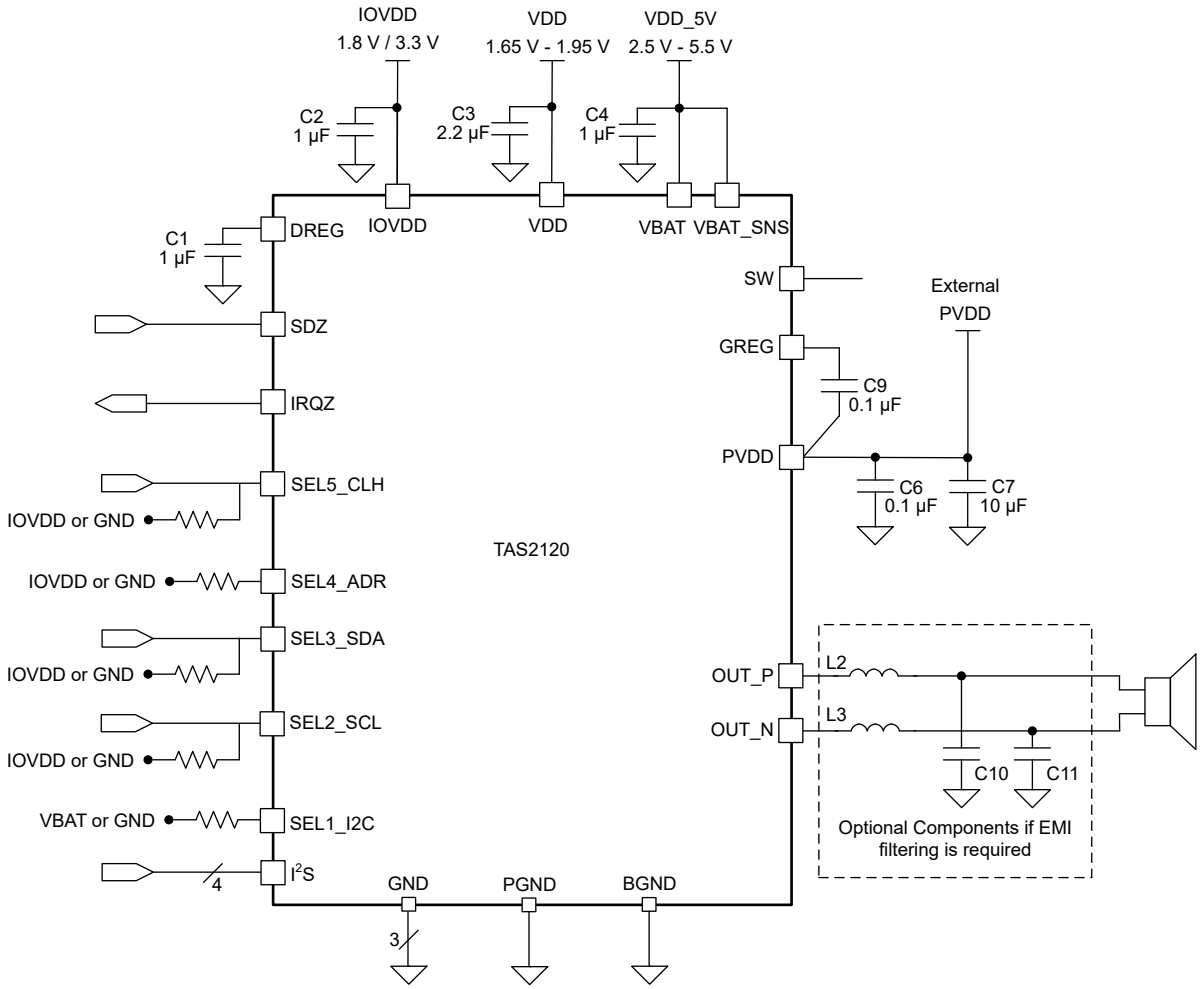


Figure 8-3. Application Diagram for External PVDD system

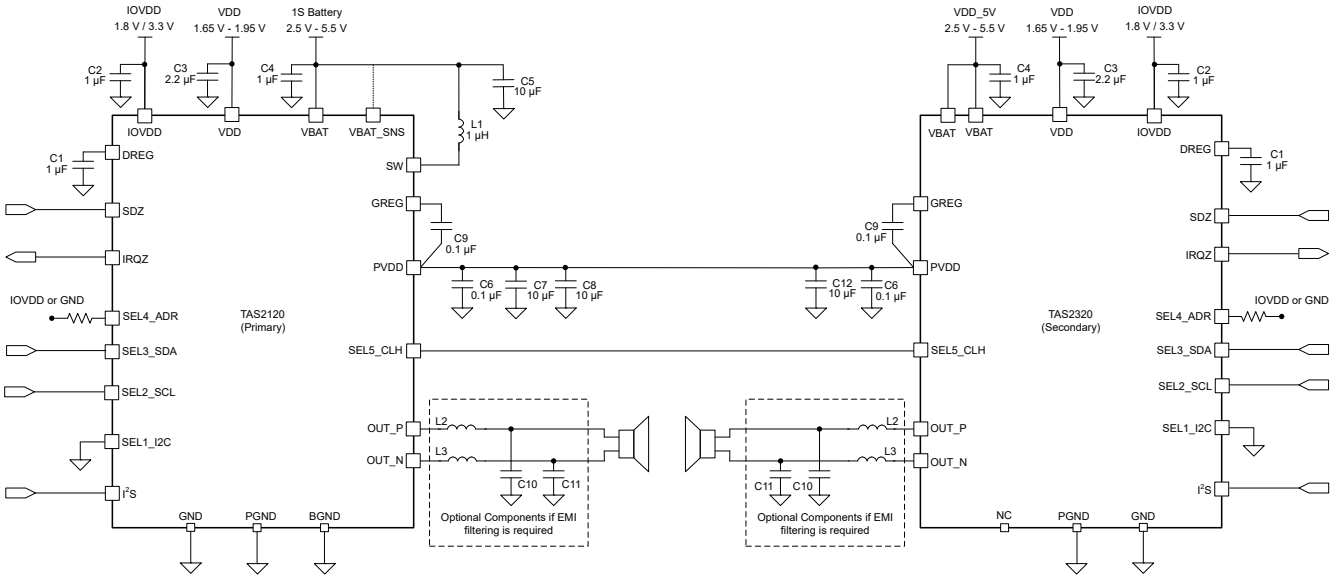


Figure 8-4. Application Diagram for Boost Share Topology

Table 8-1. Recommended External Components

Component	Description	Specification	Min	Typ	Max	Unit
L1	Boost Convertor Inductor	Inductance, 20% Tolerance	0.47	1		µH
		Saturation current		5.3		A
L2, L3	Optional EMI Filter Inductors (must use C10, C11 if L2, L3 are used)	DC Current	2			A
C1, C2	DREG, IOVDD decap	Capacitance, 20% tolerance		1		µF
		Voltage rating	2	6.3		V
C3	VDD decap	Capacitance, 20% tolerance		2.2		µF
		Voltage rating	2	6.3		V
C4	VBAT decap	Capacitance, 20% tolerance		1		µF
		Voltage rating	6.3	10		V
C5	1S Battery Power decap	Capacitance, 20% tolerance		10		µF
		Voltage rating	6.3	10		V
C6	PVDD Low ESL decap	Capacitance, 20% tolerance		0.1		µF
		Voltage rating	16	25		V
C7, C8, C12	PVDD Power decap	Capacitance, 20% tolerance		10		µF
		Voltage rating	16	25		V
		Effective total PVDD Capacitance after deratings for 1S battery systems	3			µF
C9	GREG decap	Capacitance, 20% tolerance		0.1		µF
		Voltage rating	6.3	10		V
C10, C11	Optional EMI Filter capacitors (must use L2, L3 if C10, C11 are used)	Voltage rating	2xPVDD			V

8.2.1 Design Requirements

Table 8-1 lists the BOM components required for the application. Table 8-2 lists other requirements for the application.

Table 8-2. Design Parameters

PARAMETER	CONDITION	SPECIFICATION
VDD supply current(1)	VDD Y-bridge disabled, 48ksps mode, all blocks enabled	< 15mA
	VDD Y-bridge disabled, 96ksps mode, all blocks enabled	< 20mA
IOVDD supply current	1.8V mode	< 1mA
	3.3V mode	< 1mA
VBAT supply current	1S or 2S mode of operation. *Note: Current only through device VBAT pin, and not battery current taken through Boost inductor/SW pin.*	< 10mA
LC filter cut-off frequency(2)	Optional EMI filter	Fc > 2.4 MHz
LC filter inductor	Optional EMI filter	L_IND > 4*VBST/(pi*Fc)

(1) When VDD Y-bridge is enabled, additional power taken from VDD supply based on the selected switchover threshold voltage and the output load impedance.
(2) In I^2C mode, VDD Y-bridge feature can be disabled to use lower LC filter cut-off frequency.

8.2.2 Detailed Design Procedure

8.2.2.1 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See Section 6.5.2 for information on changing the I^2C address of the TAS2120 to support stereo or multi-channel operation. Mono or stereo configuration does not impact the device performance.

8.2.2.2 Boost Converter Passive Devices

The boost converter requires multiple passive devices that are labeled L1, C7, C8, C12 in Section 8.2 and whose specifications are provided in Table 8-1. These specifications are based on the design of the TAS2120 and are necessary to meet the performance targets of the device. In particular, L1 should not be allowed to enter in the current saturation region. The saturation current (I_{SAT}) for L1 should be > (ILIM + 5%) to deliver Class-D peak power. I_{SAT} and ILIM values should be selected based on peak output power required in the application.

Additionally, the ratio of L1/C (the derated value of C7,C8,C12) has to be less than 1/3 for boost stability. This ratio is relaxed to 1/2 in 2S battery mode of operation. This ratio should be maintained including the worst case variation of boost inductor and output capacitors.

To satisfy sufficient energy transfer, L1 needs to be ≥ 0.47µH at the boost switching frequency (100kHz to 4MHz). Using a 0.47µH will help in reducing the capacitor requirements and save board space, but comes at the cost of increased voltage ripple on VBAT and reduces average input current and hence max P_{OUT} of the device. High PSRR of TAS2120 should minimize the effect from the additional ripple on VBAT supply.

The L1 inductor series resistance (ESR) is another critical parameter to be selected in the application. Lower ESR reduces power loss and helps in improving overall system efficiency. Based on available board space, smallest ESR inductors which meet the application needs will give better efficiency performance.

8.2.2.3 EMI Passive Devices

The TAS2120 supports edge-rate control to minimize EMI, but the system designer may want to include passive devices on the Class-D output for further reduction in EMI . These passive devices that are labeled L2, L3, C10 and C11 in Section 8.2. If C10 and C11 are used, L2 and L3 must also be installed, and C10 and C11 must be placed after L2 and L3 respectively to maintain the stability of the output stage.

The component value selection for the EMI filters depends on the application need on the frequency band that needs to be suppressed using these filters. Higher cutoff frequency helps in reducing the BOM size and reduces the switching power loss associated with the filters. Application should select the highest cutoff frequency filter which will meet the system's frequency suppression target to get better efficiency performance.

The DC resistance of the inductors or ferrite beads used in the EMI filters also plays a critical role in system efficiency. Lower resistance reduces power loss and helps in improving overall system efficiency. Based on available board space, smallest DC resistance components which meet the application needs will give better efficiency performance.

8.2.2.4 Miscellaneous Passive Devices

The GREG Capacitor requires 100 nF to meet Class-D power delivery and efficiency specs. For device functionality, the GREG capacitor should be kelvin/star connected to PVDD pin of the device.

In order to maintain the device performance and keep the supply ripple within the device specification, minimizing the parasitic inductance on supply/ground paths for decoupling capacitors is required. All supply decapacitors should be selected as smallest package footprint to minimize the ESL of the capacitors. The layout placement and routing of the capacitors is critical for minimizing the trace parasitic inductance. Refer to Layout section (Section 8.5.1) to get detailed recommendations.

8.2.3 Application Performance Plots

T_A = 25°C, VBAT = 3.6V, PVDD = 12V, VDD = 1.8V, IOVDD = 1.8V, R_L = 8Ω + 33µH, LBOOST = 1µH, F_{in} = 1kHz, Fs = 48kHz, Gain = 21dBV, BST_ILIM = 5.1A, SDZ=1, Noise gate mode disabled, Measured on EVM with

typical application use case (Section 8.2). Measured filter free with an Audio Precision with a 22Hz to 20kHz un-weighted bandwidth, unless otherwise noted.

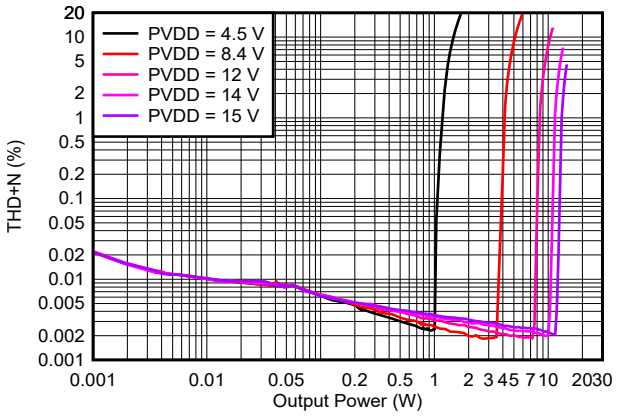


Figure 8-5. THDN vs Output Power

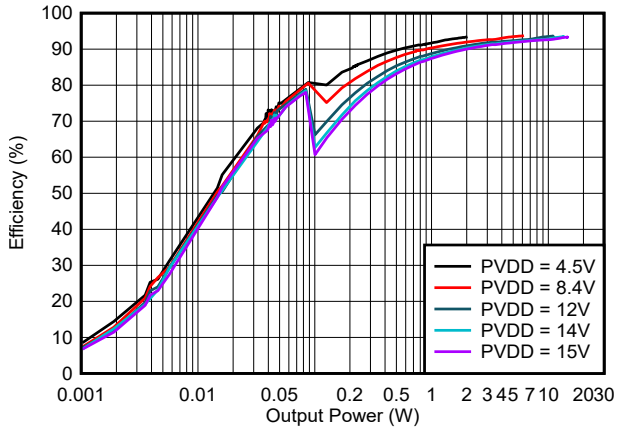


Figure 8-6. Efficiency vs Output Power

8.3 What to Do and What Not to Do

- Additional 2mA to 3mA leakage current from VDD supply is expected when IRQZ pin is pulled high.
- IRQZ pin should be left floating or grounded on the board instead of connecting pull-up resistor to avoid leakage current issue.
- I^2C polling based interrupt mechanism can be implemented in host instead of HW pin based interrupt from device.
- For HW pin based interrupt, recommend to change IRQZ polarity to active high instead of the default active low state. This can be done by writing '1' to IRQZ_POL register in IO_CFG_02 register in Page0 (Section 7.1).

8.4 Power Supply Recommendations

TAS2120 power up sequence of supply rails and ASI clocks can be applied in any order as long as SDZ pin is held low. Once all supplies and ASI clocks are stable the SDZ pin can be pulled high to initialize the device.

For power down sequence recommedation is to mute the device first. Following that SDZ pin must be pulled low before supply rails are ramped down in any order.

If using the device in external PVDD mode, the SW pad must be kept floating.

Once all the supplies are valid and SDZ pin is released to high, the digital core voltage regulator powers up, and starts the internal initialization sequence. After a hardware or software reset, additional I^2C commands to the device should be delayed by at-least 300us to allow the device internal blocks to be initialized.

VBAT supply voltage needs to be 2.2V or higher at all times including ripple conditions to avoid device VBAT UVLO.

8.5 Layout

8.5.1 Layout Guidelines

- Use wide traces for signals that carry high current and avoid VIAs wherever possible. If VIAs can't be avoided, multiple VIAs should be added to enable low parasitic inductance and high current capability. These include traces for PVDD, VBAT, VDD, PGND, BGND, GND, OUT_P and OUT_N.
- PGND and BGND signal should be directly connected and shorted to the ground plane of board to minimize parasitic inductance. Common inductance between ground pins (eg GND and PGND or GND and BGND common routing) before connecting to ground plane should be avoided.

- The coupling between high switching signal traces like OUT_P, OUT_N, SW, should be avoided from sensitive low voltage signals.
- Minimize capacitance between high switching lines like OUT_P, OUT_N, SW, to ground/static nodes. Larger capacitance will result in efficiency drop. Coupling between OUT_P and OUT_N will also cause degraded efficiency.
- VBAT routing to the boost inductor and the device VBAT pin should be star connected to the common VBAT supply plane. Ensure the decoupling capacitor C4 is placed close to the device and decoupling capacitor C5 is placed close to the inductor.
- Place the boost inductor between VBAT and SW close to the device terminal with no VIAs between device terminal and the inductor. VBAT routing to the boost inductor should be routed with minimal routing resistance to achieve best performance from device.
- Decoupling capacitors should be placed close to the device. Smallest possible package size is recommended for the decaps to achieve best performance from device. DREG, VDD, IOVDD, VBAT (C4 cap), PVDD low ESL (C6 cap) are recommended to be 0201 case size or lower. VIAs between decapacitors and device pins should be avoided, or multiple VIAs added to minimize parasitic inductances.
- All decoupling capacitor's ground terminal should be strongly connected to the ground plane with multiple ground VIAs. The ground routing loop between the cap ground and the device ground pins should be minimized.
- For VDD Y-bridge functionality, the routing from the host PMIC to the device VDD should be wide supply plane trace with minimal routing parasitic inductance.
- For the capacitor between GREG-PVDD (C9 cap), PVDD side of capacitor should not be connected directly to the PVDD decoupling capacitors (C6, C7 and C8), and should be connected as close as possible to the device PVDD pin.
- In external PVDD mode of operation, SW pin should be left floating and not connected to any supply or ground signals.

8.5.2 Layout Example

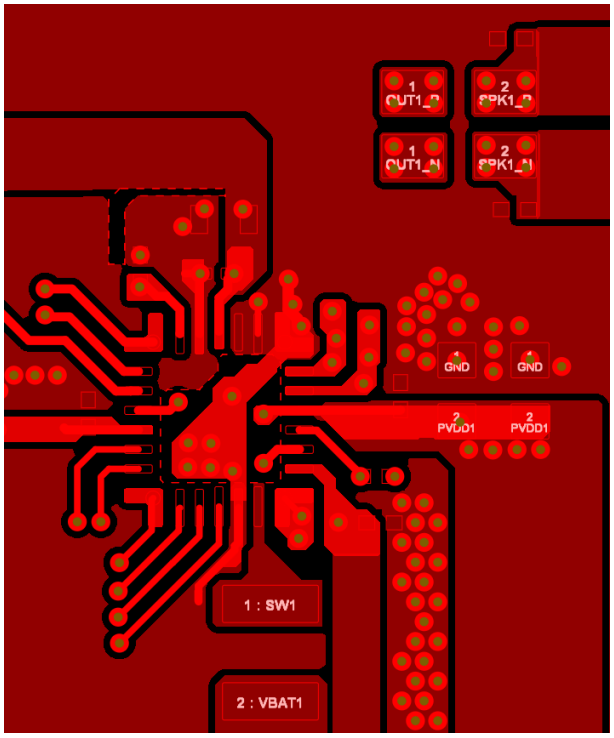


Figure 8-7. Example Layout Top

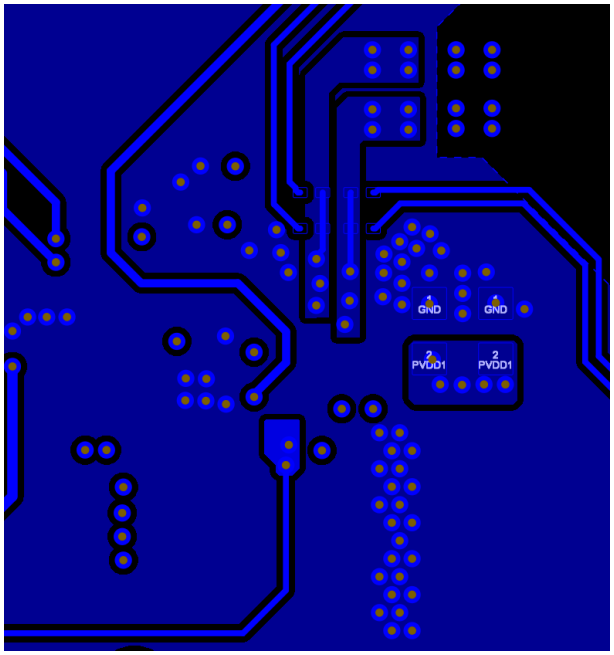


Figure 8-8. Example Layout Bottom

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documents see the following

- Texas Instruments, Purepath Console 3 (PPC3) Software

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2024) to Revision A (August 2025)	Page
• Updated device status to production data.	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTAS2120RBGR.A	Active	Preproduction	VQFN-HR (RBG) | 26	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TAS2120RBGR	Active	Production	VQFN-HR (RBG) | 26	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TAS2X20

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

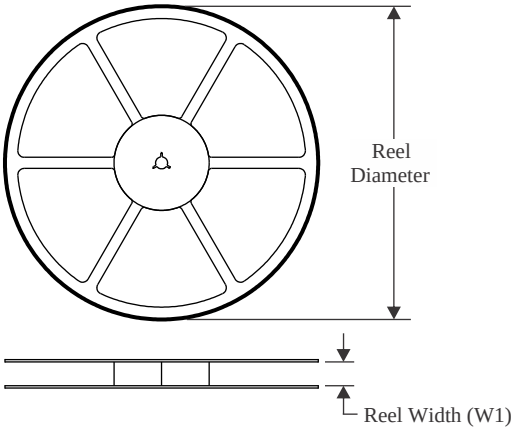
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

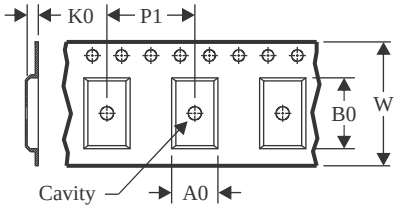
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

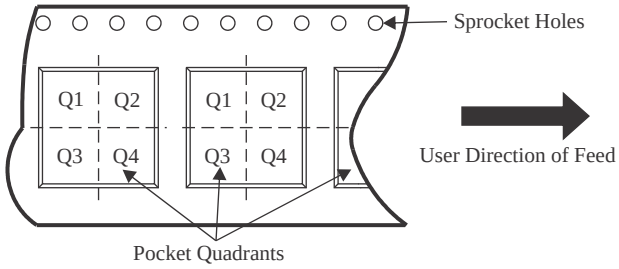


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

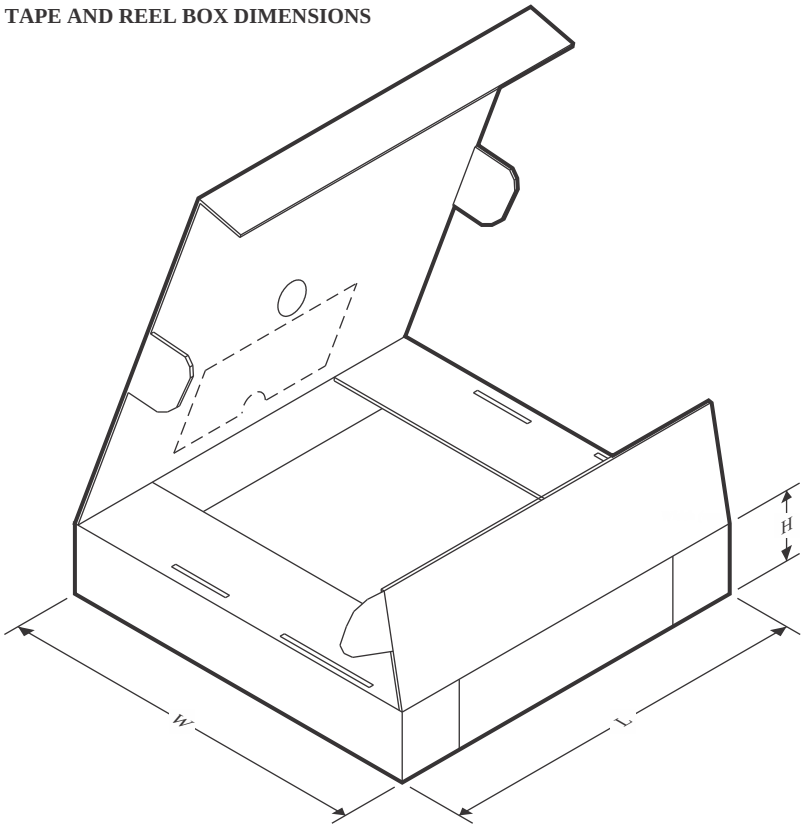
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS2120RBGR	VQFN-HR	RBG	26	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

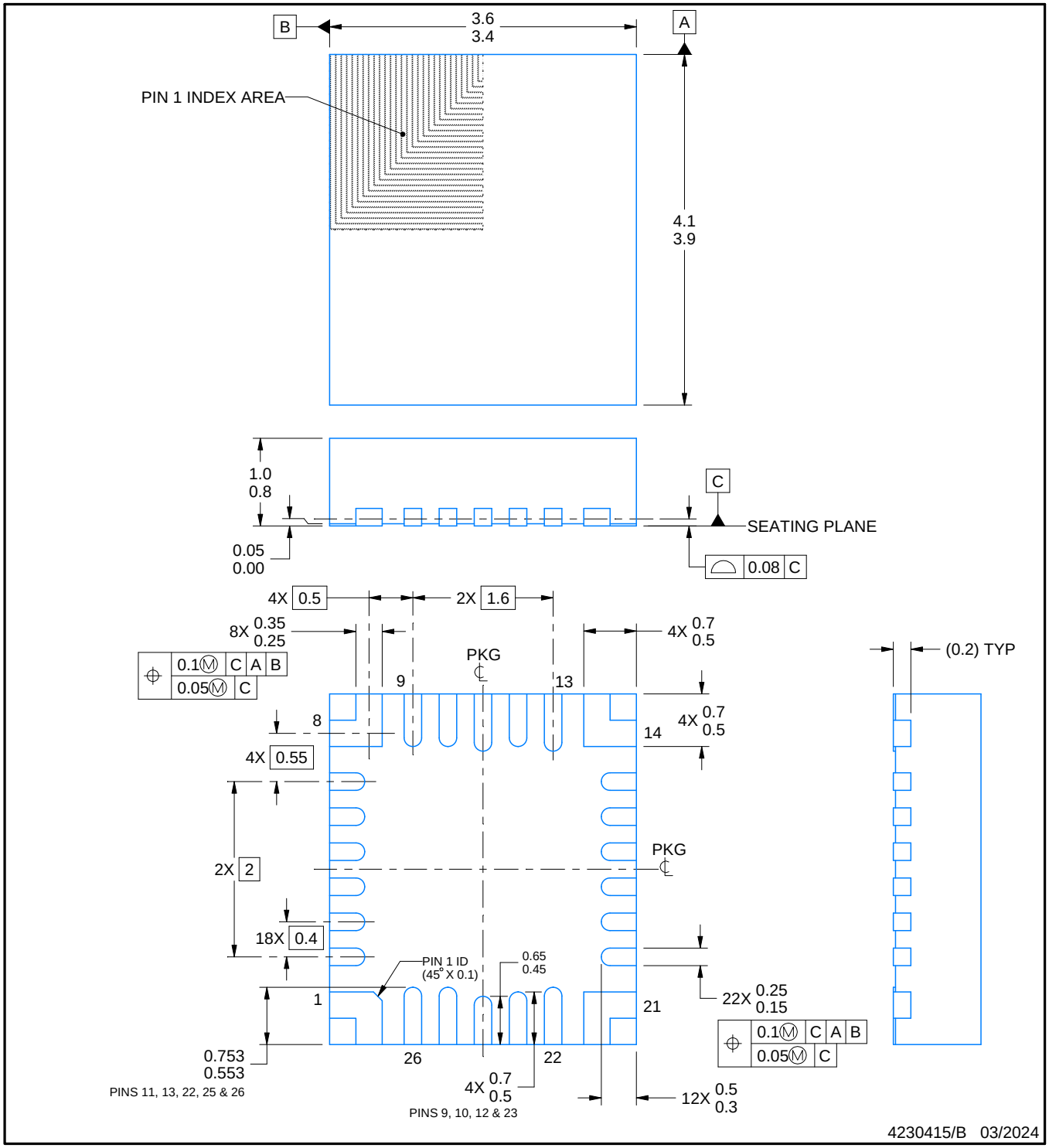
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS2120RBGR	VQFN-HR	RBG	26	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RBG0026A

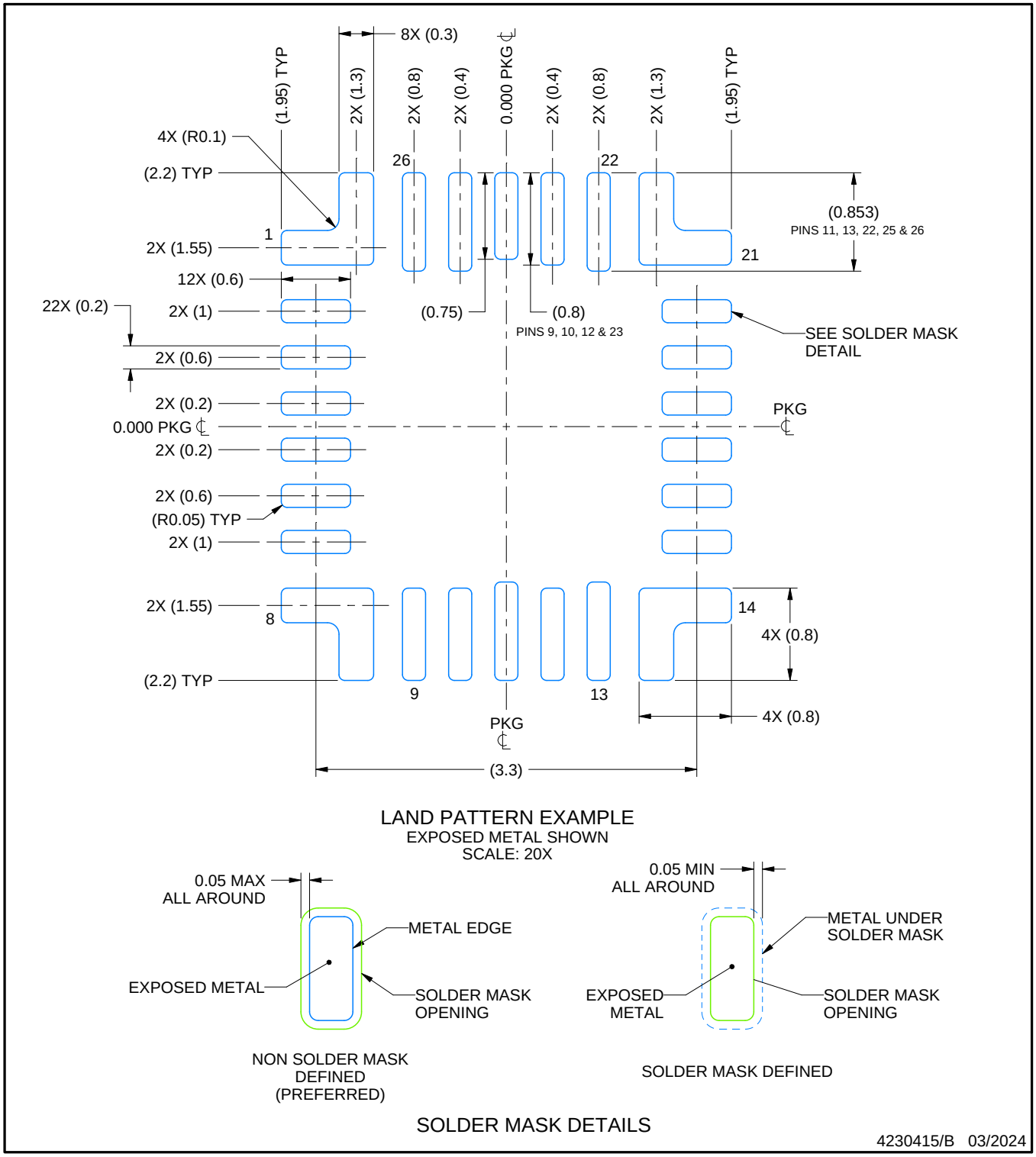
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



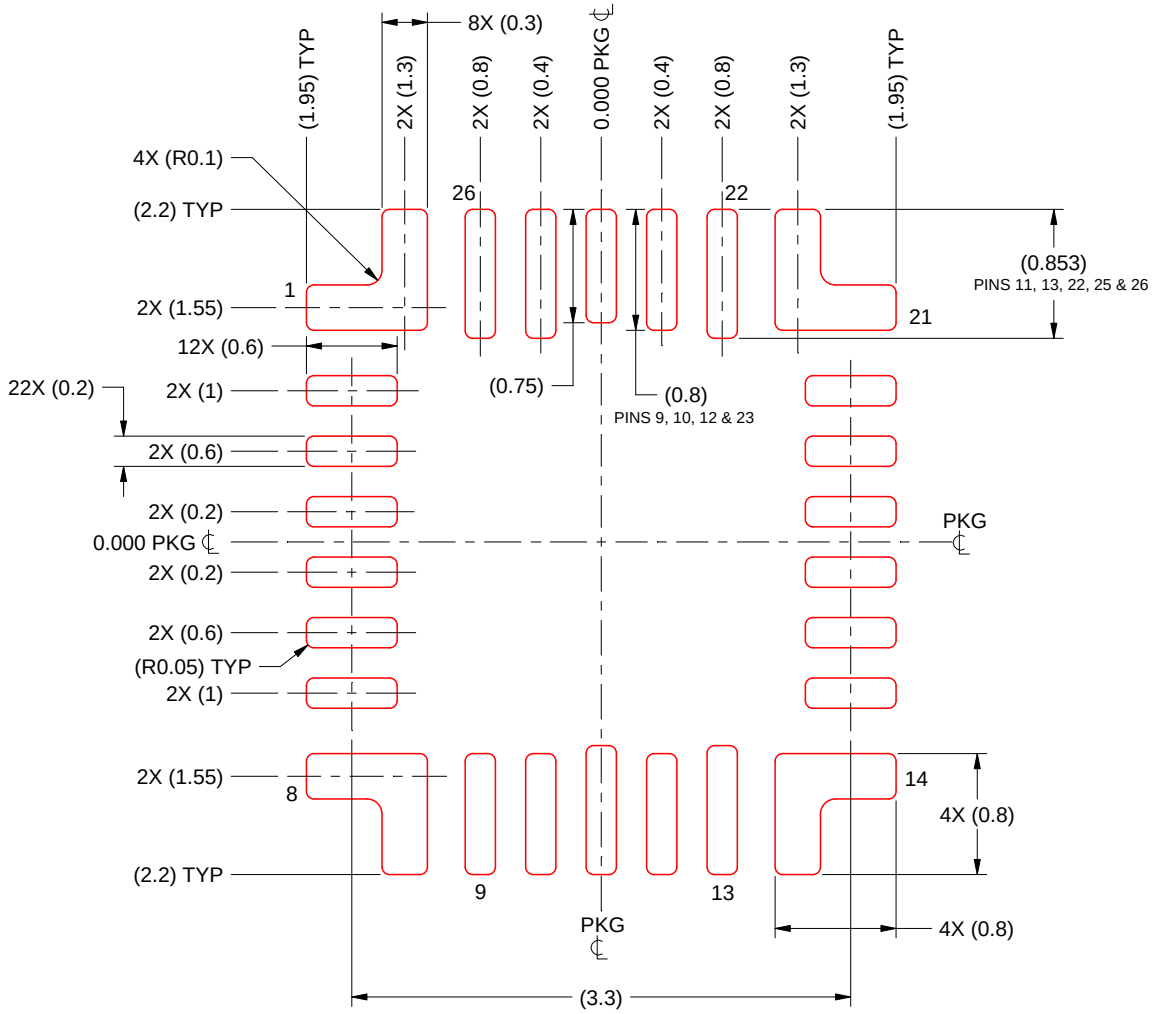
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 20X

4230415/B 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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