TAC5242 Hardware-control stereo audio codec with 119dB dynamic range ADC and 120dB dynamic range DAC

1 Features

- Stereo audio ADC Channels
  - Performance:
    - Line/Microphone differential input dynamic range: 119dB
    - Differential input THD+N: –98dB
  - Input voltage:
    - Differential, $2V_{RMS}$ full-scale inputs
    - Single-ended, $1V_{RMS}$ full-scale inputs
  - ADC sample rates (f_S) = 8kHz to 192kHz
  - Digital HPF with configurable cut-off frequency:
    - 1Hz or 12Hz, at 48kHz sampling rate
  - Low noise microphone bias
- Stereo audio DAC Channels
  - Performance:
    - DAC to differential line-out dynamic range: 120 dB
    - DAC to pseudo-differential headphone-out dynamic range: 110 dB
    - THD+N: –100 dB
  - Output voltage:
    - Differential line-out/receiver, $2V_{RMS}$ full-scale
    - Pseudo-differential headphone, $1V_{RMS}$ full-scale
    - Single-ended line-out, $1V_{RMS}$ full-scale
  - DAC sample rates (f_s) = 8kHz to 192kHz
- Common Features
  - Pin or Hardware Control
  - Audio Serial Interface
    - Format: TDM, I^2S, or Left-justified (LJ)
    - Bus Controller and Target Modes
    - Configurable TDM Slots
    - Word Length: Selectable 24 or 32 Bits
  - Pin-selectable digital decimation/interpolation filter options:
    - Linear-phase or Low-latency
  - Integrated PLL
  - Auto clock & sample rate detection
  - Interrupt output on clock error
  - Single Supply Operation AVDD: 1.8V or 3.3V
  - I/O Supply Operation: 1.8V or 3.3V
  - Temperature grade 1: –40°C ≤ T_A ≤ +125°C

2 Applications

- Video Conference System
- IP Network Camera
- IP Telephone
- Smart Speakers
- Professional audio mixer/control surface

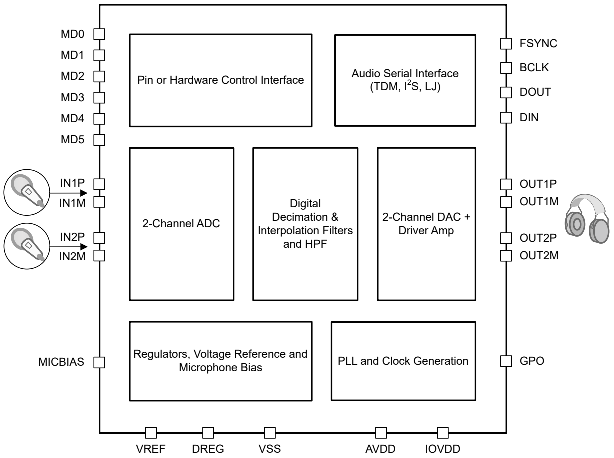
3 Description

The TAC5242 is a high-performance low-power stereo audio codec with $2V_{RMS}$ differential input, 119dB dynamic range ADC and $2V_{RMS}$ differential output, 120dB dynamic range DAC. The TAC5242 supports both differential and single-ended inputs and outputs. The ADC supports both line/microphone input signals with options for AC or DC coupling configurations and the DAC output can be configured for either line-output or headphone loads. The DAC can drive upto 62.5mW into a 16Ω headphone load. The device integrates a phase-locked loop (PLL) and supports sample rates up to 192kHz for both the ADC and DAC signal chains. The device also integrates a DC-removal digital high-pass filter (HPF) with configurable cut-off for the ADC signal chain. The TAC5242 supports time-division multiplexing (TDM), left-justified (LJ), or I^2S audio formats in controller and target modes, and is pin or hardware controlled. These integrated high-performance features, pin control along with a single supply operation, make TAC5242 an excellent choice for space-constrained audio applications.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)(2)
TAC5242	VQFN (24)	4mm x 4mm with 0.5mm pitch

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable



Simplified Block Diagram

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4 Device Comparison Table

FEATURE	TAC5242	TAC5142	TAC5212	TAC5112	TAC5211	TAC5111
Control interface	Pin or Hardware control		I^2C or SPI			
Digital audio serial interface	TDM or I^2S or left-justified (LJ)					
Audio ADC channel	2		2		1	
Digital microphone channel	Not available (N/A)		4		2	
Microphone bias	Yes (Fixed Voltage)		Yes (Programmable Voltage)			
ADC dynamic range	119dB	103dB	119dB	105dB	119dB	105dB
Audio DAC channel	2		2		1	
DAC dynamic range	120dB	110dB	120dB	114dB	120dB	114dB
Compatibility	Pin-to-pin, package, and control configuration compatible; drop-in replacements of each other		Pin-to-pin, package, and control registers compatible; drop-in replacements of each other		Pin-to-pin, package, and control registers compatible; drop-in replacements of each other	
Package	VQFN, 24-pins, 4.00mm × 4.00mm with 0.5mm pitch					

5 Pin Configuration and Functions

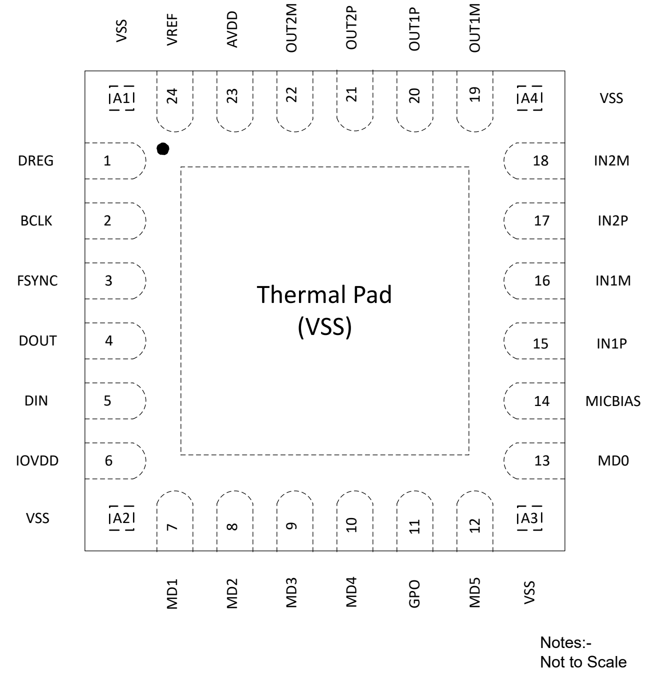


Figure 5-1. 24-Pin QFN Package with Exposed Thermal Pad and Corner Pins, Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VSS	A1	Ground	Ground pin. Short directly to board ground plane.
DREG	1	Digital Supply	Digital on-chip regulator output voltage for digital supply (1.55V, nominal)
BCLK	2	Digital I/O	Audio serial data interface bus bit clock
FSYNC	3	Digital I/O	Audio serial data interface bus frame synchronization signal
DOUT	4	Digital Output	Audio serial data interface bus output
DIN	5	Digital Input	Audio serial data interface bus input
IOVDD	6	Digital Supply	Digital I/O power supply (1.8V or 3.3V, nominal)
VSS	A2	Ground	Ground pin. Short directly to board ground plane.
MD1	7	Digital Input	Controller Mode: Frame rate and BCLK frequency selection
			Target Mode: AVDD supply, word length, and decimation/interpolation filter type selection
MD2	8	Digital Input	Controller Mode: Frame rate and BCLK frequency selection
			Target Mode: AVDD supply, word length, and decimation/interpolation filter type selection
MD3	9	Digital Input	Controller Mode: Controller clock input
			TDM Target Mode: Data slot selection
			I^2S/LJ Target Mode: Digital HPF cut-off frequency and input cap quick charge setting for the ADC
MD4	10	Digital Input	ADC/DAC input/output configuration selection

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
GPO	11	Digital Output	Interrupt output (latched)
MD5	12	Digital Input	ADC/DAC input/output configuration selection
VSS	A3	Ground	Ground pin. Short directly to board ground plane.
MD0	13	Analog Input	Multi-level analog input for Controller/Target and I^{2}S/TDM/LJ mode selection
MICBIAS	14	Analog	Microphone bias output
IN1P	15	Analog Input	Analog input 1P pin
IN1M	16	Analog Input	Analog input 1M pin
IN2P	17	Analog Input	Analog input 2P pin
IN2M	18	Analog Input	Analo input 2M pin
VSS	A4	Ground	Ground pin. Short directly to board ground plane.
OUT1M	19	Analog Output	Analog output 1M pin
OUT1P	20	Analog Output	Analog output 1P pin
OUT2P	21	Analog Output	Analog output 2P pin
OUT2M	22	Analog Output	Analog output 2M pin
AVDD	23	Analog Supply	Analog power supply (1.8V or 3.3V, nominal)
VREF	24	Analog	Analog reference voltage filter output
VSS	Thermal pad	Ground	Thermal pad shorted to internal device ground. Short directly to board ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	AVDD to VSS (thermal pad)	–0.3	3.9	V
Supply voltage	IOVDD to VSS (thermal pad)	–0.3	3.9	V
Ground voltage differences	VSS to VSS (thermal pad)	–0.3	0.3	V
Analog input voltage	Analog input pins voltage to VSS (thermal pad)	–0.3	AVDD + 0.3	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Functional ambient, T_A	–55	125	°C
	Operating ambient, T_A	–40	125	
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD[1]	Analog supply voltage to VSS (thermal pad) - AVDD 3.3V operation	3.0	3.3	3.6	V
	Analog supply voltage to VSS (thermal pad) - AVDD 1.8V operation	1.65	1.8	1.95	
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8V operation	1.65	1.8	1.95	
INPUTS					
INxx	Analog input pins voltage to VSS (thermal pad)	0		AVDD	V
IO	Digital input pins (MD1 to MD5) voltage to VSS (thermal pad)	0		IOVDD	V
MD0	MD0 pin w.r.t VSS (thermal pad)	0		AVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C

		MIN	NOM	MAX	UNIT
OTHERS					
CCLK	MD3 controller mode clock frequency (CCLK) - IOVDD 3.3V operation			36.864(2)	MHz
	MD3 controller mode clock frequency (CCLK) - IOVDD 1.8V operation			24.576(2)	
C_L	Digital output load capacitance		20	50	pF

(1) VSS and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2V.
(2) CCLK input rise time (V_{IL} to V_{IH}) and fall time (V_{IH} to V_{IL}) must be less than 5ns. For better audio noise performance, CCLK input must be used with low jitter.

6.4 Thermal Information

THERMAL METRIC(1)		TAC5242	UNIT
		RGE (VQFN)	
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear-phase decimation/interpolation filters, with 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC PERFORMANCE FOR INPUT RECORDING						
	Differential input full-scale AC signal voltage	AC-coupled input		2		V_{RMS}
	Single-ended input full-scale AC signal voltage	AC-coupled input		1		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	INxx differential AC-coupled input and AC signal shorted to ground		119		dB
		INxx differential DC-coupled input and AC signal shorted to ground, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01)		112		
SNR	Signal-to-noise ratio, A-weighted(1) (2)	INxx differential AC-coupled input and AC signal shorted to ground, AVDD = 1.8V		113		dB
		INxx differential DC-coupled input and AC signal shorted to ground, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01), AVDD = 1.8V		105		
SNR	Signal-to-noise ratio, A-weighted(1) (2)	INxx single-ended AC-coupled input and AC signal shorted to ground		110		dB
		INxx single-ended AC-coupled input and AC signal shorted to ground, AVDD = 1.8V		104		
DR	Dynamic range, A-weighted(2)	INxx differential AC-coupled input and –60dBFS AC signal input		119		dB
		INxx differential DC-coupled input and –60dBFS dB AC signal input, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01)		112		

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear-phase decimation/interpolation filters, with 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DR	Dynamic range, A-weighted(2)	INxx differential AC-coupled input and –60dBFS AC signal input, AVDD = 1.8V		113		dB
		INxx differential DC-coupled input and –60dBFS dB AC signal input, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01), AVDD = 1.8V		105		
DR	Dynamic range, A-weighted(2)	INxx single-ended AC-coupled input and –60dBFS AC signal input		110		dB
		INxx single-ended AC-coupled input and –60dBFS AC signal input, AVDD = 1.8V		105		
THD+N	Total harmonic distortion(2)	INxx differential AC-coupled input and –1dBFS AC signal input		–98		dB
		INxx differential DC-coupled input and –1dBFS AC signal input, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01)		–98		
ADC OTHER PARAMETERS						
	AC Input impedance	Input pins INxP or INxM		5		kΩ
	Output data word length	Pin Selectable, based on MD1/MD2 Configuration	24		32	Bits
	Digital high-pass filter cutoff frequency	First-order IIR filter, –3dB point (Pin Selectable)	1		12	Hz
	Interchannel isolation	–1dBFS AC signal line-in differential input to non-measurement channel		–134		dB
	Interchannel gain mismatch	–6dBFS AC signal line-in differential input, 1kHz sinusoidal signal		±0.1		dB
	Interchannel phase mismatch	–6dBFS AC signal line-in differential input, 1kHz sinusoidal signal		±0.01		Degrees
PSRR	Power-supply rejection ratio	100mV_{PP}, 1kHz sinusoidal signal on AVDD, differential input		120		dB
MICROPHONE BIAS						
	MICBIAS noise	Bandwidth = 20Hz to 20kHz, A-weighted, 1µF capacitor between MICBIAS and VSS (thermal pad)		2		µV_{RMS}
	MICBIAS voltage	AVDD = 1.8V		1.375		V
		AVDD = 3.3V		2.75		

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear-phase decimation/interpolation filters, with 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DAC Performance for Line Output/Head Phone Playback						
	Full Scale Output Voltage	Differential output between OUTxP and OUTxM, AVDD = 3.3V		2		V_{RMS}
		Differential output between OUTxP and OUTxM, AVDD = 1.8V		1		
		Single-ended output, AVDD = 3.3V		1		
		Single-ended output, AVDD = 1.8V		0.5		
		Pseudo-differential output between OUTxP and OUT1M with external common-mode sense, AVDD = 3.3V		1		
		Pseudo-differential output between OUTxP and OUT1M with external common-mode sense, AVDD = 1.8V		0.5		
SNR	Signal-to-noise ratio, A-weighted(1) (2)	Differential output, 0dBFS signal, AVDD = 3.3V		120		dB
		Single-ended output, 0dBFS signal, AVDD = 3.3V		111		
		Pseudo-differential output, 0dBFS signal, AVDD = 3.3V		110		
		Differential output, 0dBFS signal, AVDD = 1.8V		115		
		Single-ended output, 0dBFS signal, AVDD = 1.8V		105		
		Pseudo-differential output, 0dBFS signal, AVDD = 1.8V		104		
DR	Dynamic range, A-weighted(2)	Differential output, –60dBFS signal, AVDD = 3.3V		120		dB
		Single-ended output, –60dBFS signal, AVDD = 3.3V		111		
		Pseudo-differential output, –60dBFS signal, AVDD = 3.3V		110		
		Differential output, –60dBFS signal, AVDD = 1.8V		115		
		Single-ended output, –60dBFS signal, AVDD = 1.8V		105		
		Pseudo-differential output, –60dBFS signal, AVDD = 1.8V		104		
THD+N	Total harmonic distortion(2)	Differential output, –1dBFS Signal, AVDD = 3.3V		–100		dB
		Single-ended output, –1dBFS Signal, AVDD = 3.3V		–96		
	Headphone Load Range		8	16	300	Ω
	Headphone/Line-out Cap Load		0	100	550	pF
	Line-out Load Range		600			Ω
DAC Channel OTHER PARAMETERS						
	Output Offset	0 Input, Differential Line-output		±0.5		mV
	Output Common Mode	Common Mode Level for OUTxP and OUTxM, AVDD = 1.8V		0.9		V
		Common Mode Level for OUTxP and OUTxM, AVDD = 3.3V		1.65		
	Common Mode Error	DC Error in Common Mode Voltage		±10		mV
	Output Signal Bandwidth			20		kHz
	Input data word length	Pin Selectable, based on MD1/MD2 Configuration	24		32	Bits

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear-phase decimation/interpolation filters, with 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Interchannel isolation	Differential output, –1dBFS input signal on non-measurement channel		–120		dB
	Gain Error	Differential output, –6dBFS Input signal		±0.1		
	Interchannel gain mismatch	Differential output, –6dBFS Input signal		±0.1		dB
	Interchannel phase mismatch	Differential output, –6dBFS Input signal		±0.01		Degrees
PSRR	Power-supply rejection ratio	100mV$_{PP}$, 1kHz sinusoidal signal on AVDD, differential input, 0dB channel gain		120		dB
P_{out}	Output Power Delivery	Receiver/Headphone R_L=16Ω, THD+N<1% in Differential or Pseudo-differential mode		62.5		mW
DIGITAL I/O						
V_{IL}	Low-level digital input logic voltage threshold	All digital pins, IOVDD 1.8V operation	–0.3		0.35 x IOVDD	V
		All digital pins, IOVDD 3.3V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins, IOVDD 1.8V operation	0.65 x IOVDD		IOVDD + 0.3	V
		All digital pins, IOVDD 3.3V operation	2		IOVDD + 0.3	
V_{OL}	Low-level digital output voltage	All digital pins, I_{OL} = –2 mA, IOVDD 1.8V operation			0.45	V
		All digital pins, I_{OL} = –2 mA, IOVDD 3.3V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins, I_{OH} = 2 mA, IOVDD 1.8V operation	IOVDD – 0.45			V
		All digital pins, I_{OH} = 2 mA, IOVDD 3.3V operation	2.4			
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, input = 0V	–5	0.1	5	µA
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, input = IOVDD	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in sleep mode or low power mode	All external clocks stopped, AVDD = 3.3V		1.37		mA
I_{IOVDD}		All external clocks stopped, IOVDD = 3.3V		0.6		µA
I_{IOVDD}		All external clocks stopped, IOVDD = 1.8V		0.3		
I_{AVDD}	Current consumption with ADC 2-channel and DAC to Line-out 2-channel, operating at f_S 16kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3V		22.8		mA
I_{IOVDD}		IOVDD = 3.3V		0.05		
I_{IOVDD}		IOVDD = 1.8V		0.02		

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear-phase decimation/interpolation filters, with 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{AVDD}	Current consumption with ADC 2-channel and DAC to Line-out 2-channel, operating at f_S 48kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3V		26.7		mA
I_{IOVDD}		IOVDD = 3.3V		0.1		
I_{IOVDD}		IOVDD = 1.8V		0.05		
I_{AVDD}	Current consumption with ADC 2-channel and DAC to Headphone 2-channel, operating at f_S 16kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3V		21.6		mA
I_{IOVDD}		IOVDD = 3.3V		0.06		
I_{IOVDD}		IOVDD = 1.8V		0.03		
I_{AVDD}	Current consumption with ADC 2-channel and DAC to Headphone 2-channel, operating at f_S 48kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3V		26		mA
I_{IOVDD}		IOVDD = 3.3V		0.06		
I_{IOVDD}		IOVDD = 1.8V		0.03		

(1) Ratio of output level with 1kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground or no generator input signal, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.

(2) All performance measurements done with a 20kHz low-pass filter and, where noted, an A-weighted filter. Failure to use such a filter can result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

6.6 Timing Requirements: TDM, I^2S or LJ Interface

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see Figure 6-1 for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period	IOVDD = 1.8V	80			ns
		IOVDD = 3.3V	40			
$t_{H(BCLK)}$	BCLK high pulse duration(1)	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{L(BCLK)}$	BCLK low pulse duration(1)	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{SU(FSYNC)}$	FSYNC setup time	IOVDD = 1.8V	8			ns
		IOVDD = 3.3V	8			
$t_{HLD(FSYNC)}$	FSYNC hold time	IOVDD = 1.8V	8			ns
		IOVDD = 3.3V	8			
$t_{SU(DIN)}$	DIN setup time	IOVDD = 1.8V	8			ns
		IOVDD = 3.3V	8			
$t_{HLD(DIN)}$	DIN hold time	IOVDD = 1.8V	16			ns
		IOVDD = 3.3V	8			
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time, IOVDD = 1.8V			10	ns
		10% - 90% rise time, IOVDD = 3.3V			10	
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time, IOVDD = 1.8V			10	ns
		90% - 10% fall time, IOVDD = 3.3V			10	

(1) To meet the timing specifications, the BCLK minimum high or low pulse duration must be higher than 25ns, if the DOUT data line is latched on the opposite BCLK edge polarity from the one used by the device to transmit the DOUT data at IOVDD = 3.3V.

6.7 Switching Characteristics: TDM, I^2S or LJ Interface

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see Figure 6-1 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(DOUT-BCLK)}$	BCLK to DOUT delay	50% of BCLK to 50% of DOUT, IOVDD = 1.8V			26	ns
		50% of BCLK to 50% of DOUT, IOVDD = 3.3V			19	
$t_{d(DOUT-FSYNC)}$	FSYNC to DOUT delay in TDM or LJ mode	50% of FSYNC to 50% of DOUT, IOVDD = 1.8V			26	ns
		50% of FSYNC to 50% of DOUT, IOVDD = 3.3V			19	
$f_{(BCLK)}$	BCLK output clock frequency; controller mode(1)	IOVDD = 1.8V			12.288	MHz
		IOVDD = 3.3V			24.576	
$t_{d(FSYNC)}$	BCLK to FSYNC delay; controller mode	50% of BCLK to 50% of FSYNC, IOVDD = 1.8V			26	ns
		50% of BCLK to 50% of FSYNC, IOVDD = 3.3V			19	
$t_{H(BCLK)}$	BCLK high pulse duration; controller mode	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{L(BCLK)}$	BCLK low pulse duration; controller mode	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{r(BCLK)}$	BCLK rise time; controller mode	10% - 90% rise time, IOVDD = 1.8V			10	ns
		10% - 90% rise time, IOVDD = 3.3V			10	
$t_{f(BCLK)}$	BCLK fall time; controller mode	90% - 10% fall time, IOVDD = 1.8V			10	ns
		90% - 10% fall time, IOVDD = 3.3V			10	

(1) To meet the timing specifications, the BCLK output clock frequency must be lower than 18.5MHz, if the DOUT data line is latched on the opposite BCLK edge polarity from the one used by the device to transmit DOUT data at IOVDD = 3.3V.

6.8 Timing Diagrams

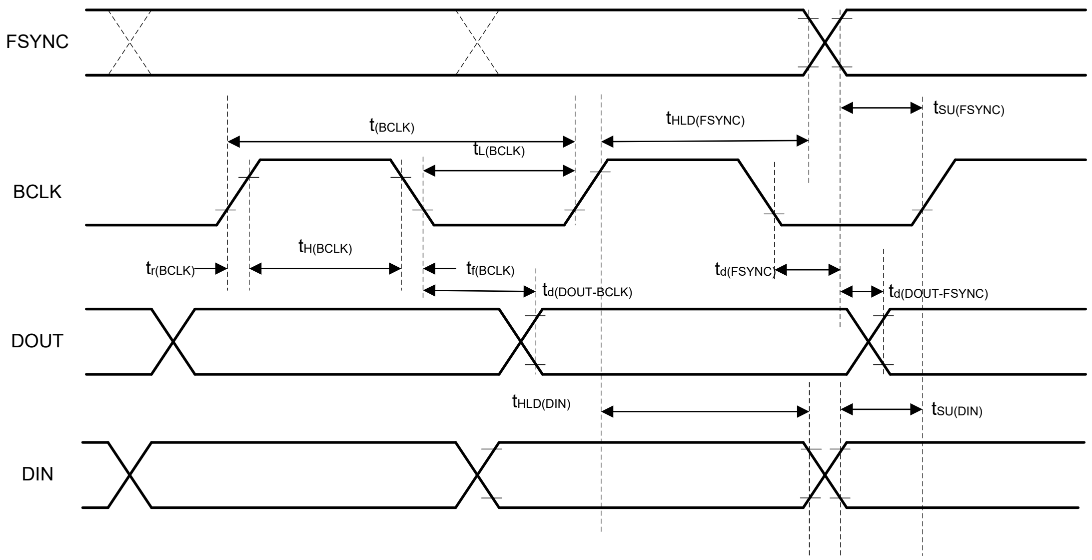
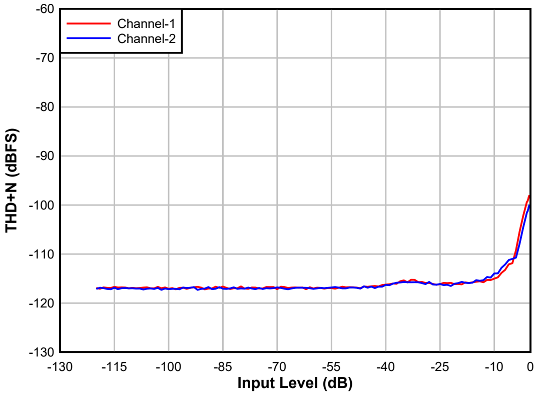


Figure 6-1. TDM, I^2S, and LJ Interface Timing Diagram

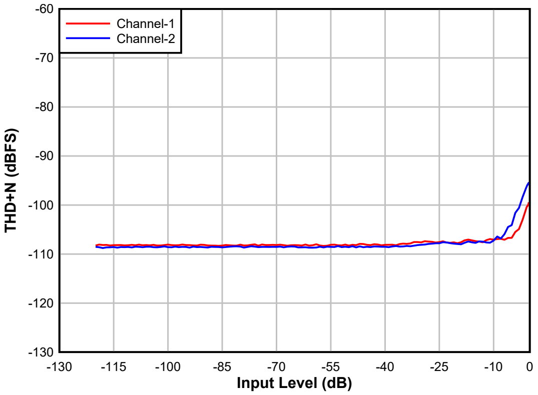
6.9 Typical Characteristics

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear phase decimation/interpolation filter, with AC-coupled line-input in differential configuration and 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted



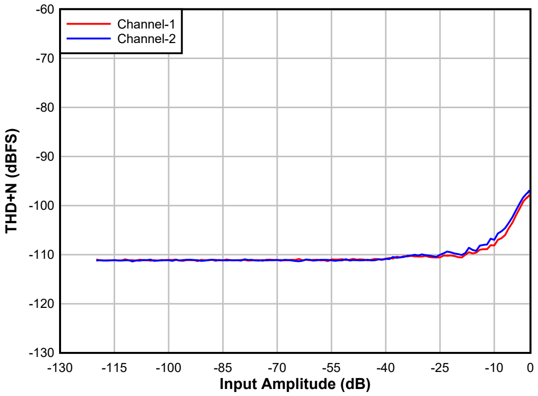
AC-coupled differential line input

Figure 6-2. ADC THD+N Level vs Input



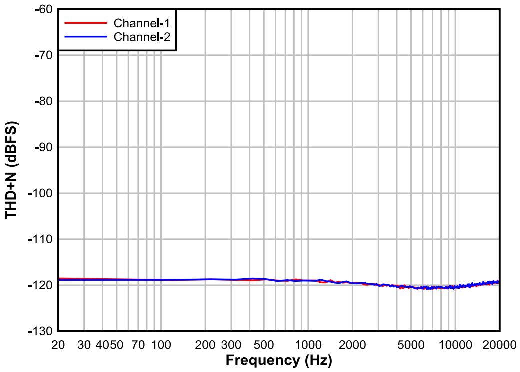
AC-coupled single-ended line input

Figure 6-3. ADC THD+N Level vs Input



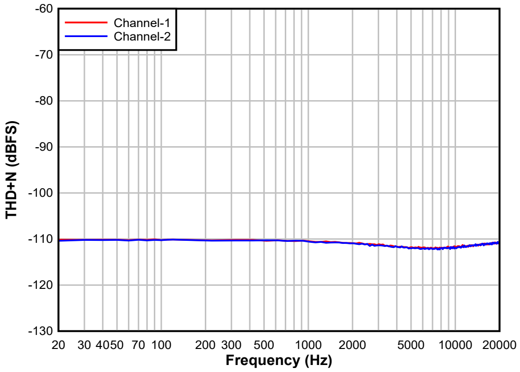
AC-coupled differential line input, AVDD=1.8V

Figure 6-4. ADC THD+N Level vs Input



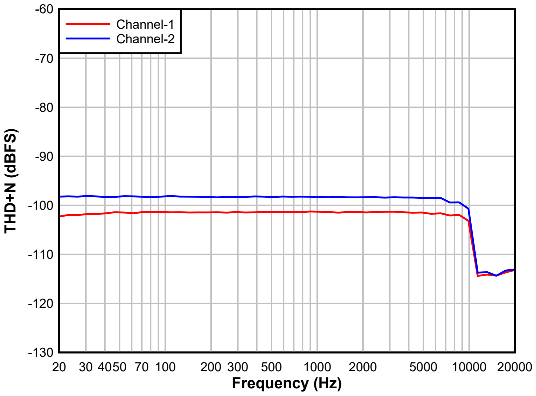
AC-coupled differential line input (-60dBFS)

Figure 6-5. ADC A-weighted DR vs Frequency



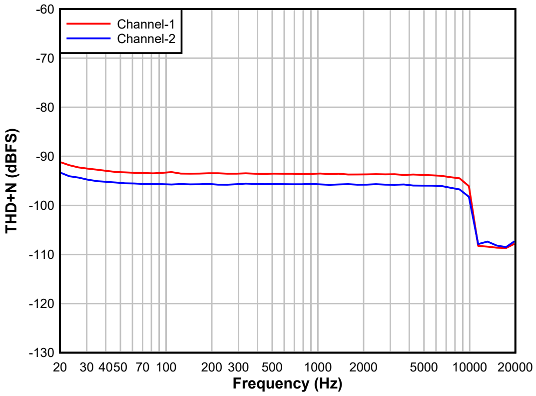
AC-coupled single-ended line input (-60dBFS)

Figure 6-6. ADC A-weighted DR vs Frequency



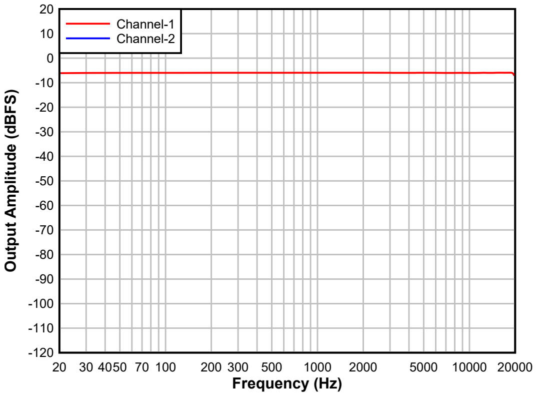
AC-coupled differential line input (-1dBFS)

Figure 6-7. ADC THD+N vs Frequency



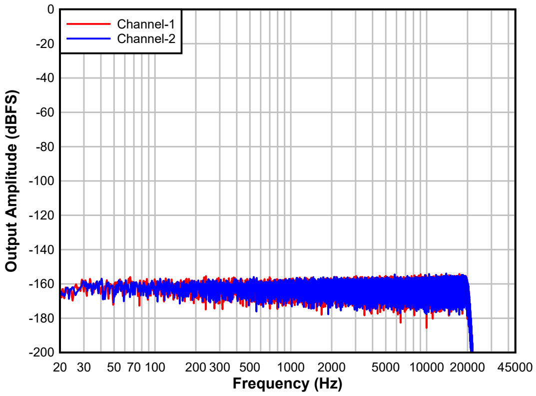
AC-coupled single-ended line input (-1dBFS)

Figure 6-8. ADC THD+N vs Frequency



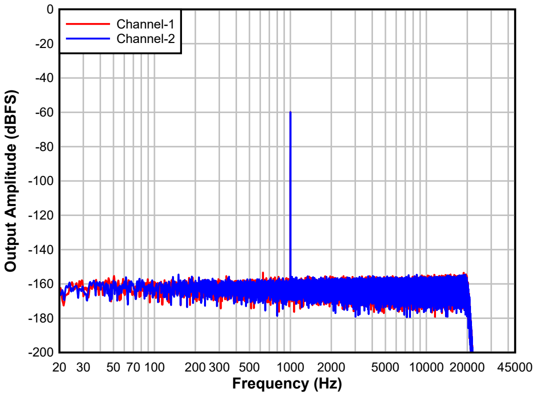
AC-coupled differential line input (-6dBFS)

Figure 6-9. ADC Frequency Response



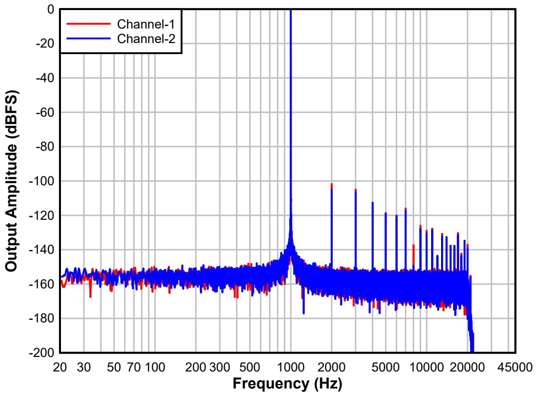
AC-coupled differential line input

Figure 6-10. ADC FFT with Idle Channel Input



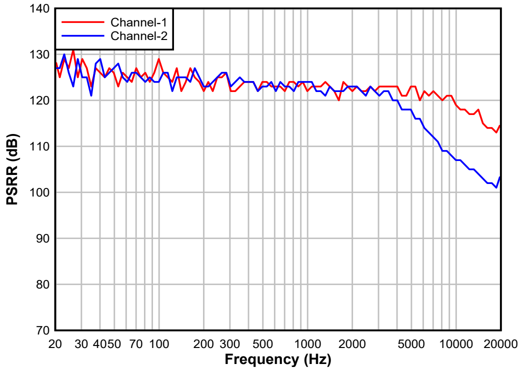
AC-coupled differential line input

Figure 6-11. ADC FFT with -60dBFS Input



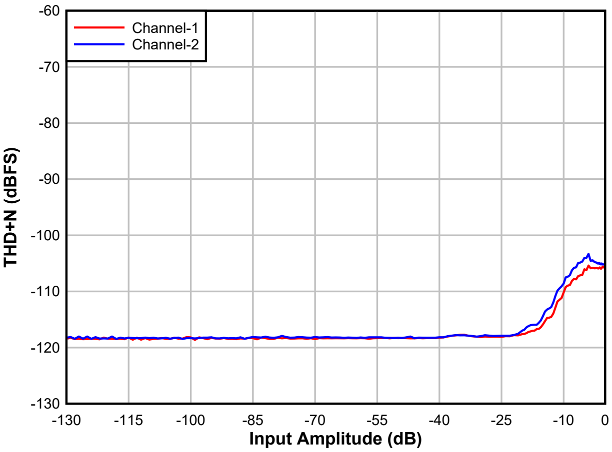
AC-coupled differential line input

Figure 6-12. ADC FFT with -1dBFS Input



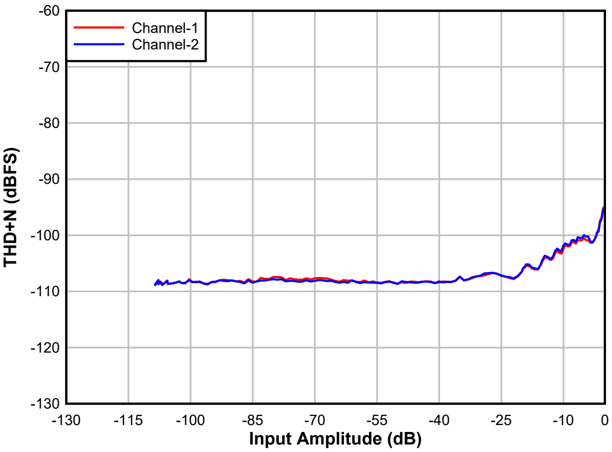
AC-coupled differential line input

Figure 6-13. ADC PSRR vs Frequency



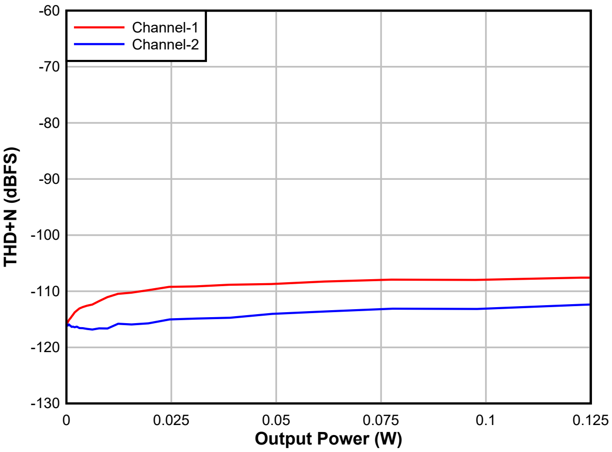
Differential output

Figure 6-14. DAC THD+N Level vs Input



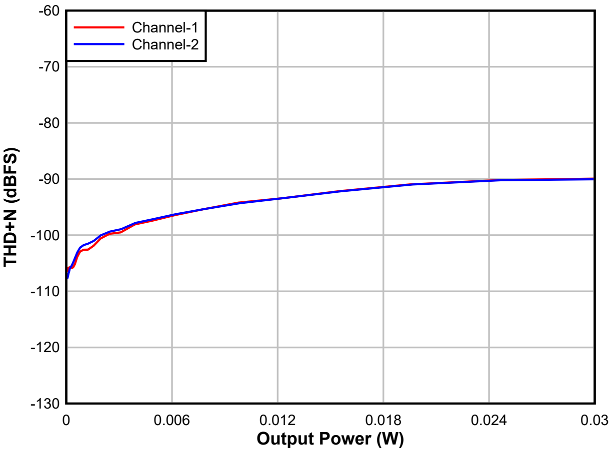
Single-ended output

Figure 6-15. DAC THD+N Level vs Input



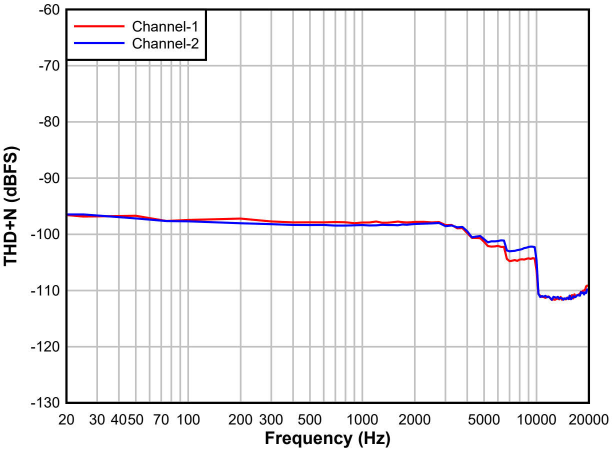
Differential receiver/headphone output, 32Ω load

Figure 6-16. DAC THD+N Level vs Output Power



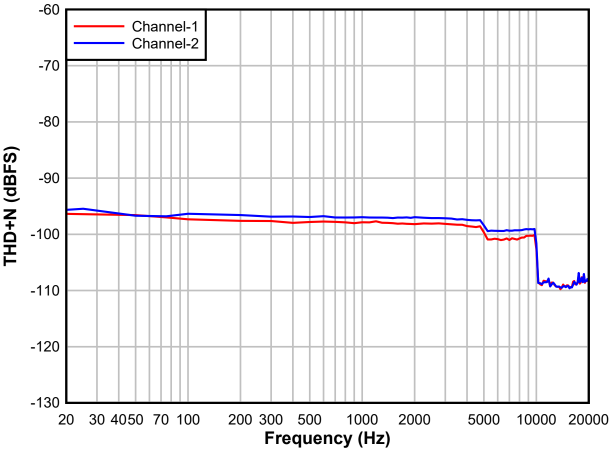
Pseudo-differential output, 32Ω headphone load

Figure 6-17. DAC THD+N Level vs Output Power



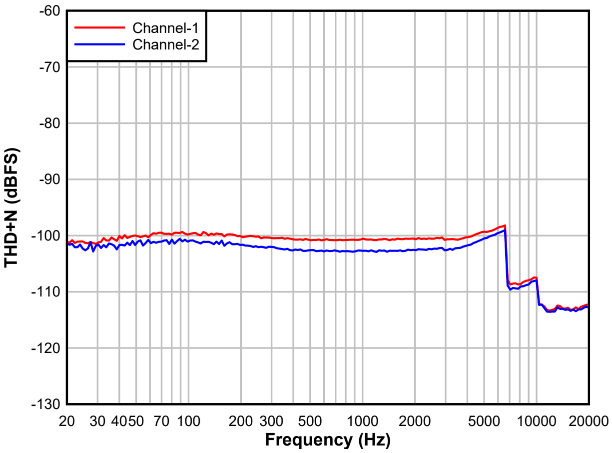
Differential output

Figure 6-18. DAC THD+N Level vs Frequency



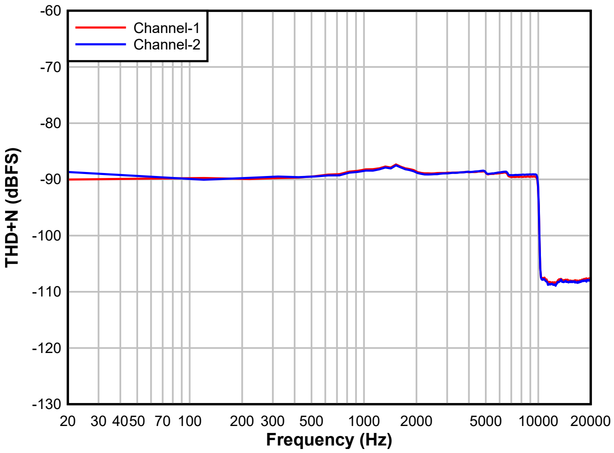
Single-ended output

Figure 6-19. DAC THD+N Level vs Frequency



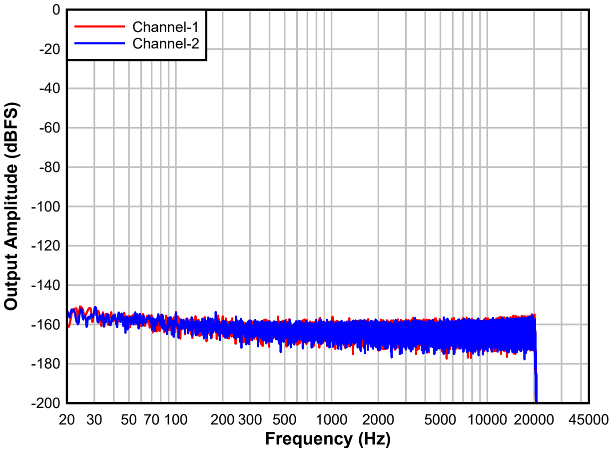
Differential receiver/headphone output, 32Ω load

Figure 6-20. DAC THD+N Level vs Frequency



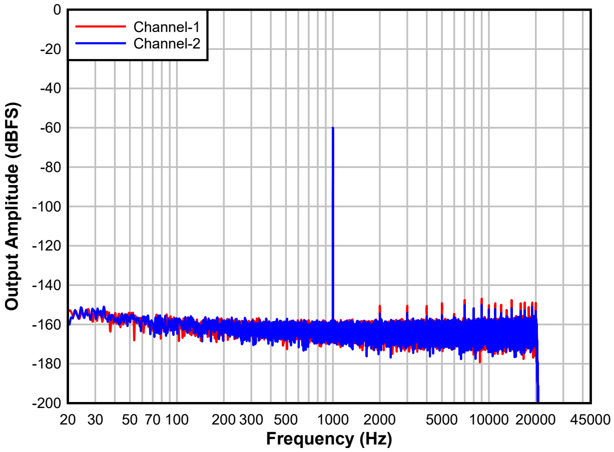
Pseudo-differential output, 32Ω headphone load

Figure 6-21. DAC THD+N Level vs Frequency



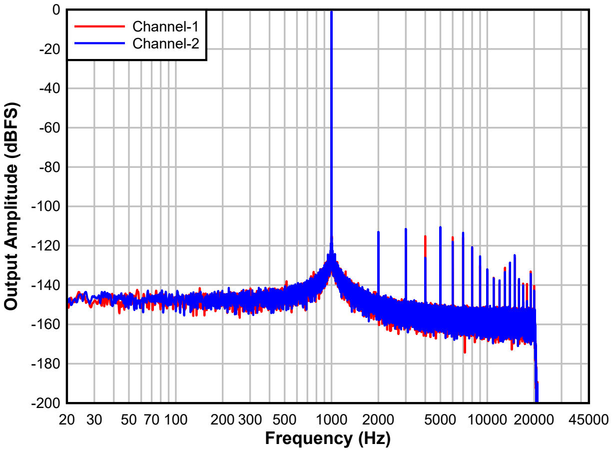
Differential output, idle-channel input

Figure 6-22. DAC FFT



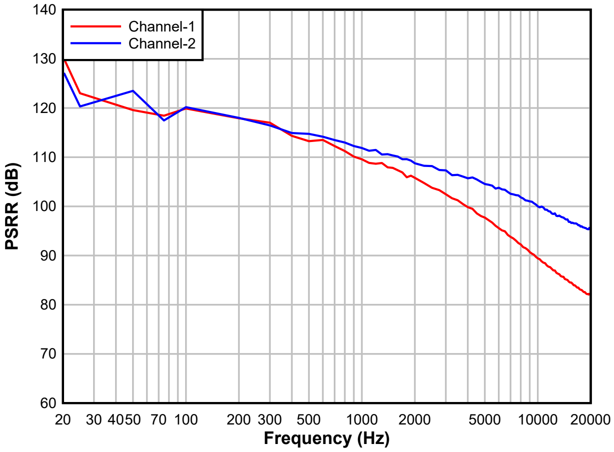
Differential output, -60dBFS input

Figure 6-23. DAC FFT



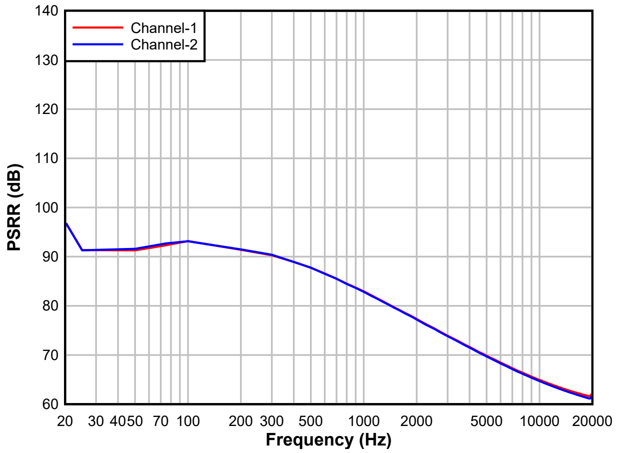
Differential output, -1dBFS input

Figure 6-24. DAC FFT



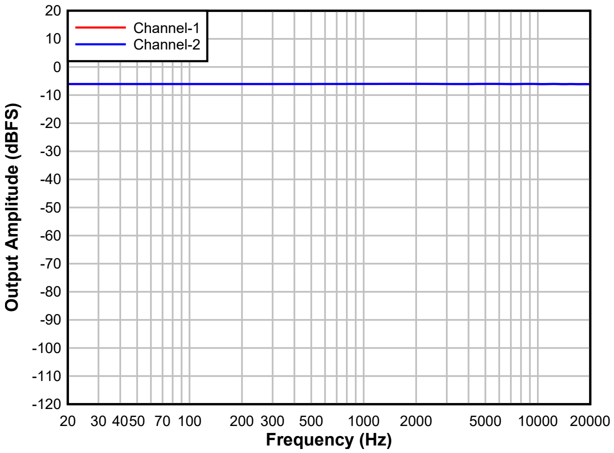
Differential output

Figure 6-25. DAC PSRR vs Frequency



Single-ended output

Figure 6-26. DAC PSRR vs Frequency



Differential output, -6dBFS input

Figure 6-27. DAC Frequency Response

7 Detailed Description

7.1 Overview

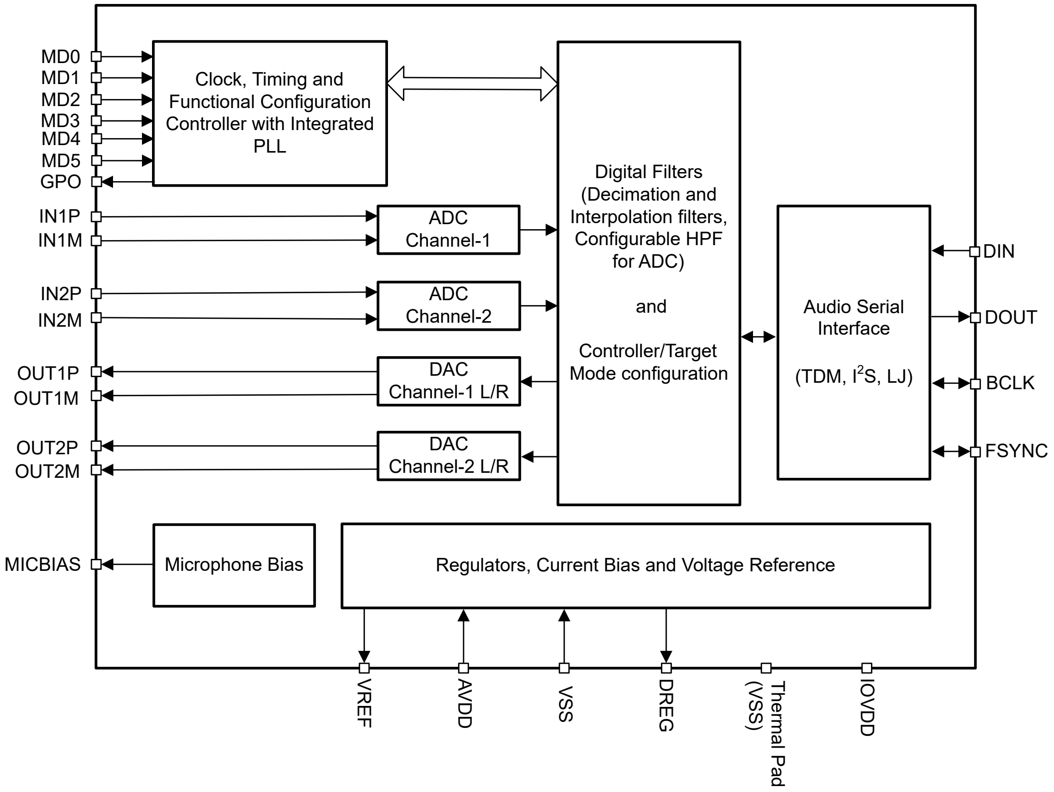
The TAC5242 is from a scalable family of devices. As part of the extended family of devices, the TAC5242 consists of a high-performance, low-power, stereo, audio analog-to-digital converter (ADC) and audio digital-to-analog converter (DAC) with extensive feature integration. This device is optimized for various end-equipments and applications that require low-noise multichannel audio recording and playback and is intended for broad market applications such as ruggedized communication equipment, IP network cameras, professional audio, and multimedia applications. The high dynamic range of this device enables far-field audio recording with high fidelity. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained system designs. Package, performance, and compatible configuration across extended families make this device well-suited for scalable system designs.

The TAC5242 consists of the following blocks:

- Pin or Hardware controlled device configurations
- 2-channel, multi-bit, high-performance delta-sigma (ΔΣ) ADCs
- Configurable single-ended or differential audio inputs
- Low-noise microphone bias output
- High-pass filter (HPF) with selectable cut-off frequency options on ADC signal path
- 2-channel, multibit, high-performance delta-sigma (ΔΣ) DACs
- Configurable single-ended, differential, or pseudo-differential audio outputs
- Linear-phase or Low-latency digital decimation and interpolation filters
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

The device supports a flexible audio serial interface [time-division multiplexing (TDM), I^{2}S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hardware Control

The device supports simple hardware-pin-controlled options to select a specific mode of operation and audio interface for a given system as summarized in Table 7-1. The device is controlled through the MD0 to MD5 pins. MD1 to MD5 pins are connected to either logic low (VSS) or logic high (IOVDD), and the MD0 pin can be connected to AVDD or VSS through different pull-up or pull-down resistors.

Table 7-1. Pin Selectable Configurations Summary

PIN	TARGET MODE	CONTROLLER MODE
MD0	Multi-level analog input for controller/target mode and I^{2}S/TDM/LJ mode selection	
MD1	AVDD supply, word length, and decimation/ interpolation filter type selection	Frame rate and BCLK frequency selection
MD2		
MD3	I^{2}S/LJ Mode: Digital HPF cut-off frequency and input cap quick charge selection for the ADC TDM Mode: Data slot selection	Controller clock input
MD4	ADC input configuration (Differential/Single-ended, AC/DC Coupled) and DAC output configuration (Differential Line-out/ Differential Receiver or Headphone/ Single-ended Line-out/ Pseudo-differential Headphone)	
MD5		

7.3.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAC5242 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus can be operated in target or controller mode through pin control. The ASI supports TDM mode for multi-channel operation, I^{2}S, and Left-Justified (LJ) bus protocols. The data is in MSB-first, two's-complement pulse code modulation (PCM) format, with pin-selectable word-length configuration.

The device supports an audio bus controller or target mode of operation using the hardware pin MD0. In target mode, FSYNC and BCLK work as input pins whereas in controller mode, FSYNC and BCLK work as output pins generated by the device. Table 7-2 shows the controller and target mode selection using the MD0 pin.

Table 7-2. Controller and Target Mode Selection

MD0	CONTROLLER AND TARGET SELECTION
Short to Ground	Target I^{2}S Mode
Short to Ground with 4.7K Ohms	Target TDM Mode
Short to AVDD	Controller I^{2}S Mode
Short to AVDD with 4.7K Ohms	Controller TDM Mode
Short to AVDD with 22K Ohms	Target LJ Mode

In Target mode of operation, the word length for the audio serial interface (ASI) in TAC5242 can be selected through MD1 and MD2 Pins. The TAC5242 also supports 1.8V AVDD operation in target mode with 32-bit word length. Table 7-3 shows the configuration table for setting the word length, AVDD supply voltage, and decimation/interpolation filter type applicable in Target Mode. In controller mode, a fixed word length of 32-bits is supported, the decimation/interpolation filters are configured in the linear phase and the MD1 and MD2 Pins control the system clock configuration described in Table 7-9.

Table 7-3. Word Length, Supply Mode, and Decimation/Interpolation Filter Selection

MD2	MD1	WORD LENGTH, SUPPLY MODE, AND DECIMATION/ INTERPOLATION FILTER SELECTION (Valid for Target Mode only)
Low	Low	AVDD=3.3V, Word Length=32, Linear-phase Filter
Low	High	AVDD=1.8V, Word Length=32, Linear-phase Filter
High	Low	AVDD=3.3V, Word Length=24, Linear-phase Filter

Table 7-3. Word Length, Supply Mode, and Decimation/Interpolation Filter Selection (continued)

MD2	MD1	WORD LENGTH, SUPPLY MODE, AND DECIMATION/ INTERPOLATION FILTER SELECTION (Valid for Target Mode only)
High	High	AVDD=3.3V, Word Length=32, Low-latency phase Filter

The TAC5242 offers slot configuration for target TDM mode of operation. This can be selected through MD3 pin when MD0 is configured in target TDM mode. Table 7-4 shows the slots selected in Target TDM mode of operation based on the MD3 pin. For options on MD3 in other modes of operation, refer to Table 7-1.

Table 7-4. Data Slot Selection for TDM Target Mode

MD3	ADC SLOTS	DAC SLOTS
Low	ADC Data on Slot 0 and 1	DAC Data on Slot 0 and 1
High	ADC Data on Slot 2 and 3	DAC Data on Slot 2 and 3

7.3.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit is transmitted on the rising edge of BCLK and received on the falling edge of the BCLK. Figure 7-1 and Figure 7-2 show the protocol timing for TDM operation with various configurations.

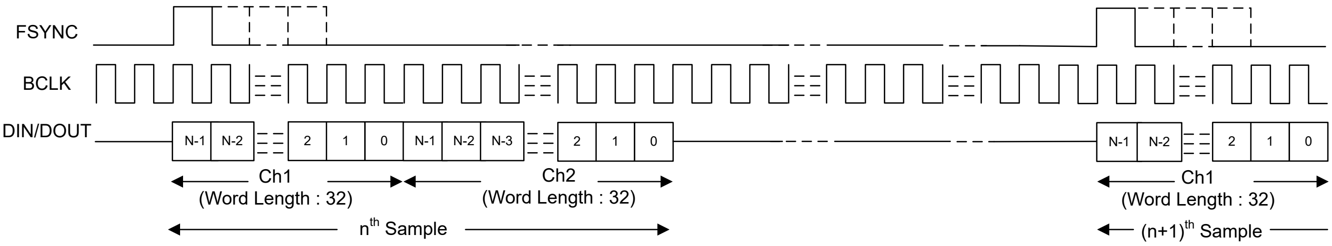


Figure 7-1. TDM Mode Protocol Timing (MD0 shorted to ground with 4.7KOhms) In Target Mode

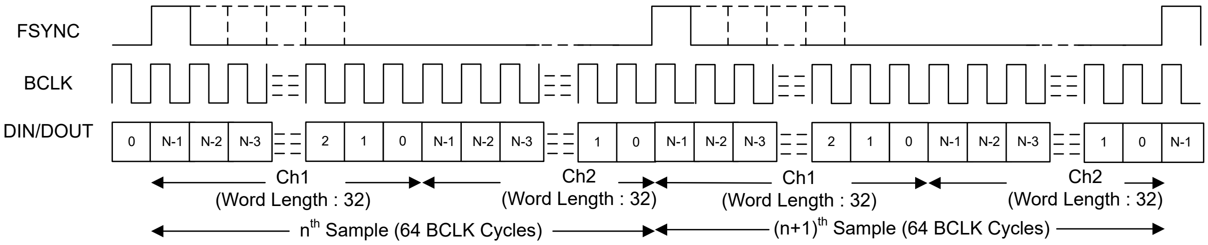


Figure 7-2. TDM Mode Protocol Timing (MD0 shorted to AVDD with 4.7KOhms) In Controller Mode

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active input and output channels times the configured word length of the input and output channel data. The DOUT pin is in a Hi-Z state for the extra unused bit clock cycles. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock but also supports multiples.

7.3.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. In I^2S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK and received on the rising edge of BCLK, in the second cycle after the *falling* edge of FSYNC. The MSB of the right slot 0 is transmitted on the falling edge of BCLK and received on the rising edge of BCLK in the second cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK and received on the rising edge of BCLK. In controller mode, FSYNC is transmitted on the rising edge of BCLK. Figure 7-3 and Figure 7-4 show the protocol timing for I^2S operation in target and controller mode of operation.

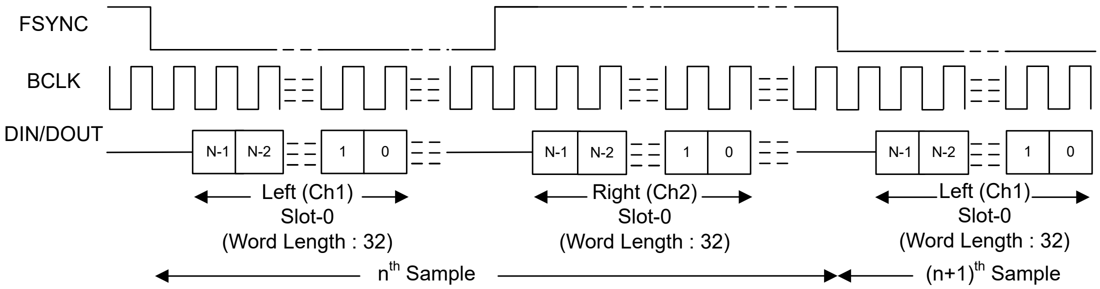


Figure 7-3. I²S Mode Protocol Timing (MD0 shorted to ground) in Target Mode

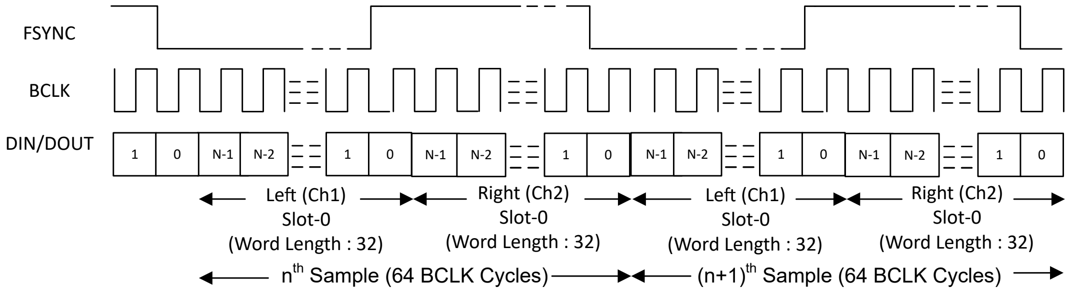


Figure 7-4. I²S Protocol Timing (MD0 shorted to AVDD) In Controller Mode

For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active input and output channels (including left and right slots) times the configured word length of the input and output channel data.

7.3.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. In LJ mode, the MSB of the left slot 0 is transmitted and received in the same BCLK cycle after the *rising* edge of FSYNC. The MSB of the right slot 0 is transmitted and received in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK and received on the rising edge of BCLK. Figure 7-5 illustrates the protocol timing for LJ operation in the target mode of operation.

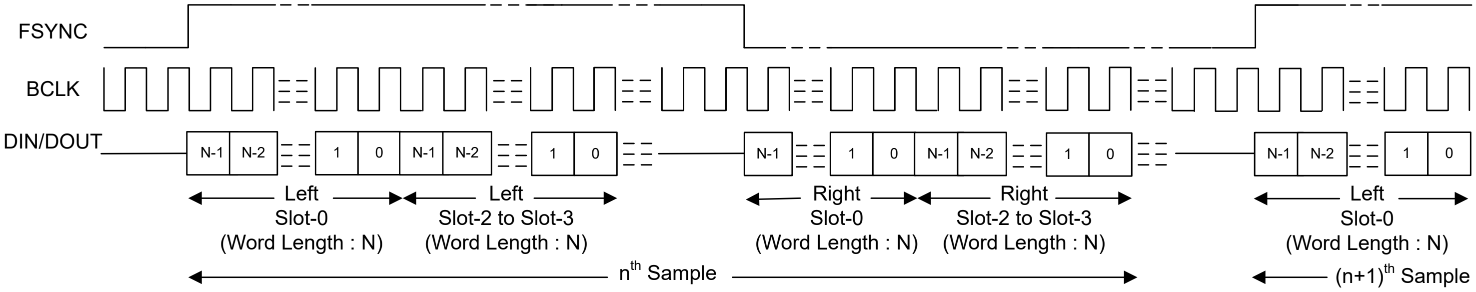


Figure 7-5. LJ Mode Standard Protocol Timing (MD0 shorted to AVDD with 22 kOhm) in Target Mode

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active input and output channels (including left and right slots) times the configured word length of the input and output channel data.

7.3.3 Phase-Locked Loop (PLL) and Clock Generation

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC and DAC modulators and digital filter engine, as well as other control blocks.

In the target mode of operation, the device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. Table 7-5 to Table 7-8 list the supported FSYNC and BCLK frequencies depending on the IOVDD Supply.

Table 7-5. Supported FSYNC (Multiples or Submultiples of 48kHz) and BCLK Frequencies (IOVDD - 3.3V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**

Table 7-6. Supported FSYNC (Multiples or Submultiples of 44.1kHz) and BCLK Frequencies (IOVDD - 3.3V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**

Table 7-7. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies (IOVDD - 1.8V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144

Table 7-7. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies (IOVDD - 1.8V Operation) (continued)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	**Reserved**
128	1.024	2.048	3.072	4.096	6.144	12.288	**Reserved**
192	1.536	3.072	4.608	6.144	9.216	**Reserved**	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	**Reserved**	**Reserved**
384	3.072	6.144	9.216	12.288	**Reserved**	**Reserved**	**Reserved**
512	4.096	8.192	12.288	**Reserved**	**Reserved**	**Reserved**	**Reserved**

Table 7-8. Supported FSYNC (Multiples or Submultiples of 44.1kHz) and BCLK Frequencies (IOVDD - 1.8V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	**Reserved**
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	**Reserved**
192	1.4112	2.8224	4.2336	5.6448	8.4672	**Reserved**	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	**Reserved**	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	**Reserved**	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	**Reserved**	**Reserved**	**Reserved**	**Reserved**

In the controller mode of operation, the device uses the MD3 pin, as the system clock, and CCLK as the reference input clock source. In target mode of operation, the MD3 pin function is described in Table 7-4 and Table 7-11.

The device provides flexibility in FSYNC selection with a supported system clock frequency option of either $256 \times f_S$ or $128 \times f_S$ or a fixed 48/44.1kHz or 96/88.2kHz as configured using the MD1 and MD2 pins. Table 7-9 shows the FSYNC and BCLK selection for the controller mode using the MD1 and MD2 pins.

Table 7-9. System Clock Selection for the Controller Mode

MD2	MD1	SYSTEM CLOCK SELECTION (Valid for Controller Mode Only)		
		FSYNC	BCLK TO FSYNC RATIO	
			I^{2}S MODE	TDM MODE
LOW	LOW	CCLK/256	64	256 for FSYNC ≤ 48kHz, 128 for 48kHz < FSYNC ≤ 96kHz, and 64 for FSYNC > 96kHz
LOW	HIGH	CCLK/128		
HIGH	LOW	96/88.2kHz		128
HIGH	HIGH	48/44.1kHz		256

See Table 7-3 for the MD1 and MD2 pin functions in the target mode of operation. In the controller mode of operation, AVDD = 3.3V and Word-Length = 32 and a linear-phase decimation/interpolation filter is applicable.

7.3.4 Analog Input and Output Configurations

The device supports simultaneous recording of up to two channels using the high-performance stereo ADC. The device consists of two pairs of analog input pins (INxP and INxM) which can be configured in single-ended or differential input mode by setting MD4 and MD5 pins. The input source for the analog pins can be from electret-condenser analog microphones, micro electrical-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board.

The voice or audio signal inputs can be capacitively coupled (AC-coupled) or DC-coupled to the device. For best distortion performance, use of low-voltage coefficient capacitors for AC-coupling is recommended. The typical input impedance for the TAC5242 is 5kΩ for the INxP or INxM pins with ±20% variation. The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power-up. To enable quick charging, the device has a quick charge scheme to speed up the charging of the coupling capacitor at power-up when operating in the I^2S/LJ target mode. This input cap quick charge setting can be enabled by configuring the MD3 pin. The MD3 pin also configures the digital HPF cut-off frequency of the ADC signal path when the device is operating in I^2S/LJ target mode as described in Table 7-11.

For optimal performance, the common-mode variation at the device input should be limited to less than 100mVpp for AC-coupled settings. For applications that cannot avoid large common-mode fluctuations, the device offers the modes to configure the device for higher common-mode tolerance for both single-ended and differential applications.

The device supports playback of two channels using the high-performance stereo DAC. The device consists of two pairs of analog output pins (OUTxP and OUTxM) which can be configured in single-ended or differential input mode by setting MD4 and MD5 pins. The input source for these channels is from TDM/I^2S/LJ interface.

Table 7-10 shows the analog input output configuration modes available with MD4 and MD5 configuration.

Table 7-10. Analog Input and Output Configurations

MD5	MD4	ANALOG INPUT CONFIGURATION	ANALOG OUTPUT CONFIGURATION
Low	Low	Differential input; AC-Coupled only	Differential Output; Line-out only
Low	High	Differential input; AC or DC-Coupled with High Common Mode Tolerance	Differential Output; Receiver/Headphone load or Line-out
High	Low	Single Ended Input on INxP; AC-Coupled only	Single-ended output; Line-out only
High	High	Single Ended Input on INxP; AC or DC-Coupled with High Common Mode Tolerance	Pseudo-differential output with external common-mode sense; Headphone load only

Figure 7-6 to Figure 7-9 show the typical configuration diagrams for the various input configuration modes and Figure 7-10 to Figure 7-12 show the typical configuration diagrams for the various output modes.

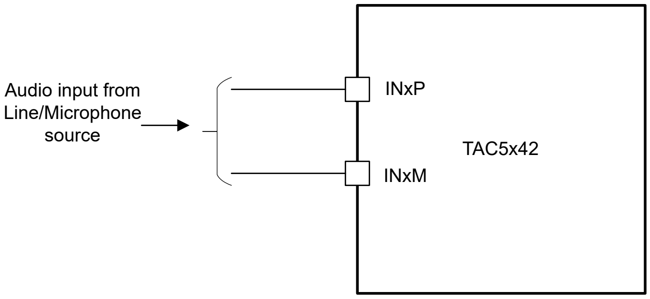


Figure 7-6. DC-Coupled Microphone or Line Differential Input Connection

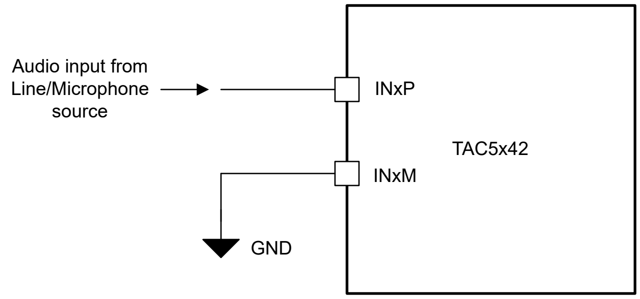


Figure 7-7. DC-Coupled Microphone or Line Single-Ended Input Connection

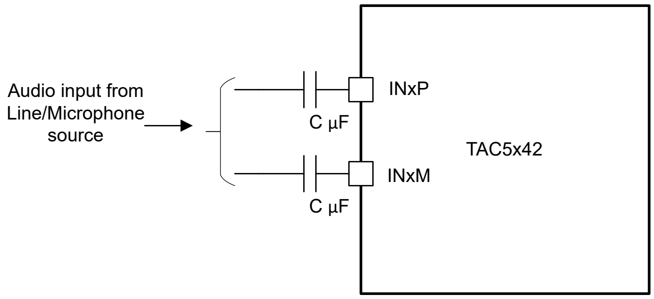


Figure 7-8. AC-Coupled Microphone or Line Differential Input Connection

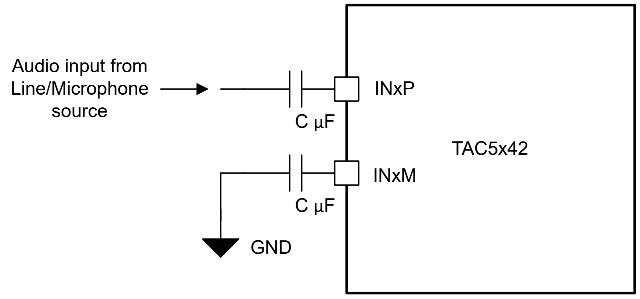


Figure 7-9. AC-Coupled Microphone or Line Single-Ended Input Connection

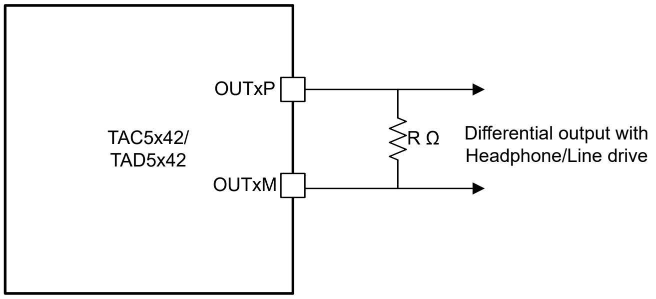


Figure 7-10. Differential Output Connection

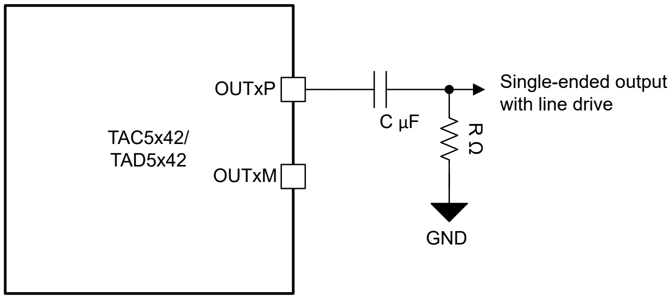


Figure 7-11. Single-ended Output Connection

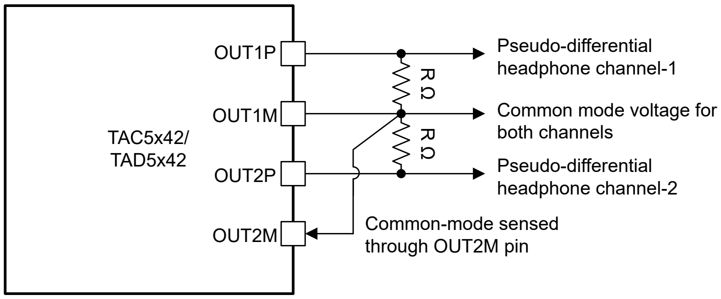


Figure 7-12. Pseudo-differential Output Connection with External Common-Mode Sense

7.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The TAC5242 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1µF capacitor connected from the VREF pin to the analog ground (VSS). The value of this reference voltage, VREF, is set to 2.75V, which in turn supports a 2V_{RMS} differential full-scale input and 2V_{RMS} differential full-scale output to the device. The required minimum AVDD voltage for this VREF voltage is 3V. When the device is configured for 1.8V AVDD supply voltage, the voltage on the VREF pin is 1.375V, which in turn supports a 1V_{RMS} differential full-scale input to the device. Do not connect any external load to a VREF pin.

7.3.6 Integrated Microphone Bias

The device integrates a built-in, low-noise microphone bias pin that outputs a high PSRR, low noise output voltage equal to VREF that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphones. The integrated bias amplifier supports up to 5mA of load current that can be used for multiple microphones. When using this MICBIAS pin for biasing or supplying various microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones.

7.3.7 ADC Signal-Chain

The TAC5242 ADC signal chain is comprised of very low-noise, high-performance, and low-power analog blocks and configurable digital processing blocks. Figure 7-13 shows a conceptual block diagram for the TAC5242 that highlights the key components of the record-path signal chain.

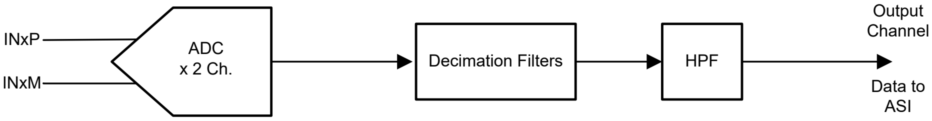


Figure 7-13. ADC Signal-Chain Processing Flowchart

The high performance and flexibility combined with a compact package make the device optimized for a variety of end-equipments and applications that require multichannel audio capture. The ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multi-stage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation followed by a high-pass filter (HPF) with configurable cut-off frequency described further. The TAC5242 supports sample rates of up to 192kHz in both controller and target mode of operation.

7.3.7.1 Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a configurable high-pass filter (HPF) with a –3dB cut-off frequency of 0.000021 × f_S or 0.00025 × f_S. The HPF is not a channel-independent filter but is globally applicable for all the ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter and is efficient enough to filter out possible DC components of the signal. This configuration is only available in Target I^2S or LJ modes of operation. In the Target TDM Mode of operation, MD3 is used to set slots for input and output data streams as described in Table 7-4 and in Controller Mode, MD3 is used as CCLK input as described in Table 7-9, and in these modes, the HPF is by default set to 0.000021 × f_S. Additionally, as a lower frequency filter in digital requires a higher value capacitor as well for low droop at the cutoff frequency, the device also adjusts the input cap quick charge time along with the HPF cut-off with this configuration. Table 7-11 shows the MD3 configuration and –3dB cutoff frequency value and input cap quick charge setting. Figure 7-14 shows a frequency response plot for the HPF filter.

Table 7-11. Input Cap Quick-Charge and HPF HPF Cutoff Frequency Selections for ADC in Target I^2S/LJ Mode

MD3	INPUT CAP QUICK CHARGE	HPF –3dB CUT-OFF FREQUENCY	HPF –3dB CUTT-OFF FREQUENCY @ 48 kHz SAMPLE RATE
Low	Disabled (50ms time)	0.000021 × f_S	1Hz
High	Enabled (12.5ms time)	0.00025 × f_S	12Hz

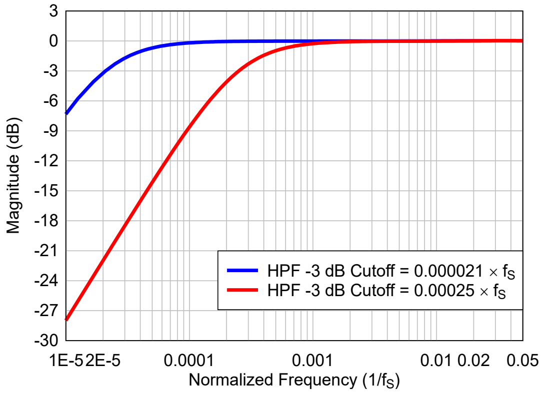


Figure 7-14. HPF Filter Frequency Response Plot

7.3.7.2 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled data from the multibit delta-sigma (ΔΣ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. The decimation filters in the device can be selected to linear-phase or low-latency filters based on the state of the MD2 and MD1 pins according to Table 7-3. This makes the device suitable for a wide variety of audio applications. Following section describes the filter response for different samples rates.

7.3.7.2.1 Linear-phase filters

The linear-phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

7.3.7.2.1.1 Sampling Rate: 8kHz or 7.35kHz

Figure 7-15 and Figure 7-16 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 8kHz or 7.35kHz, and Table 7-12 lists its specifications.

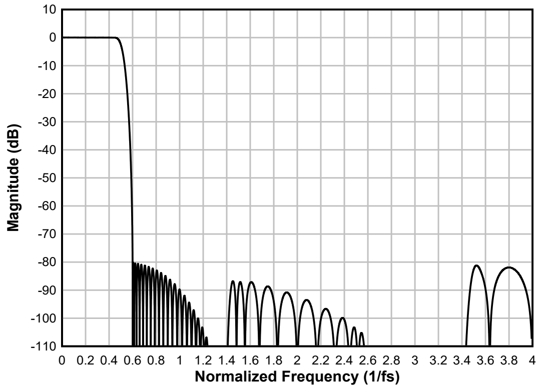


Figure 7-15. Linear-phase Decimation Filter Magnitude Response

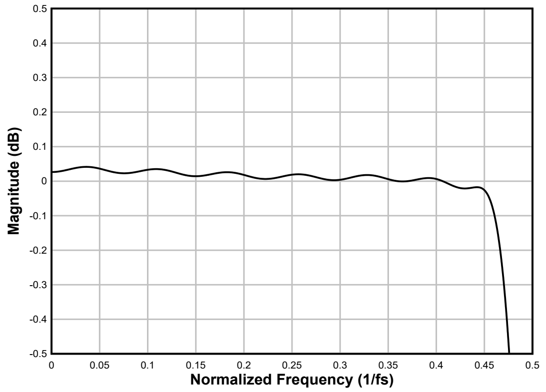


Figure 7-16. Linear-phase Decimation Filter Pass-Band Ripple

Table 7-12. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.2			dB
	Frequency range is 4 × f_S onwards	84.7			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.1		1/f_S

7.3.7.2.1.2 Sampling Rate: 16kHz or 14.7kHz

Figure 7-17 and Figure 7-18 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 16kHz or 14.7kHz, and Table 7-13 lists its specifications.

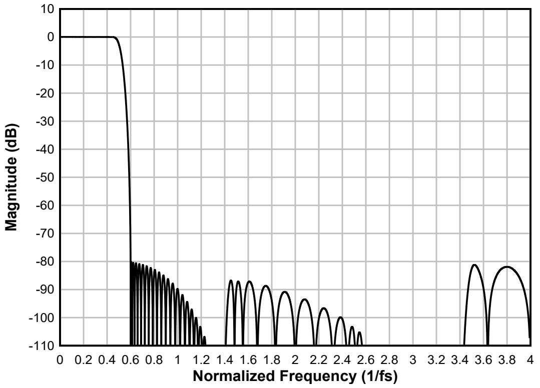


Figure 7-17. Linear-phase Decimation Filter Magnitude Response

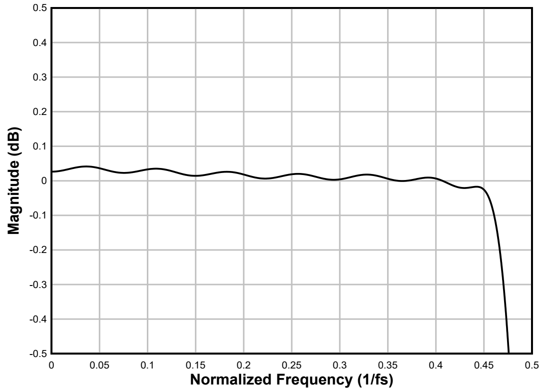


Figure 7-18. Linear-phase Decimation Filter Pass-Band Ripple

Table 7-13. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.2			dB
	Frequency range is 4 × f_S onwards	84.7			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.1		1/f_S

7.3.7.2.1.3 Sampling Rate: 24kHz or 22.05kHz

Figure 7-19 and Figure 7-20 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 24kHz or 22.05kHz, and Table 7-14 lists its specifications.

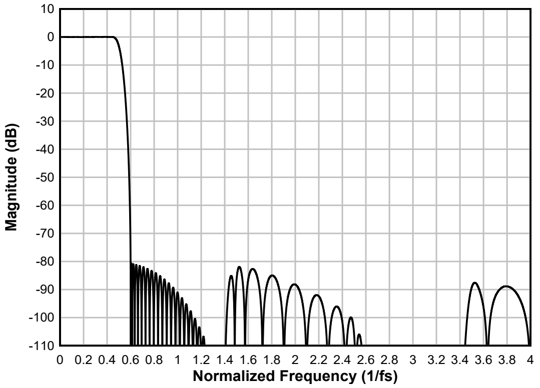


Figure 7-19. Linear-phase Decimation Filter Magnitude Response

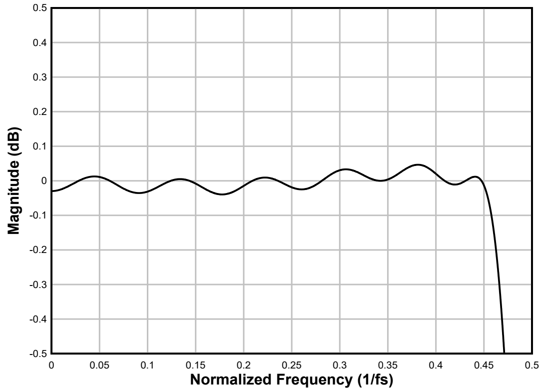


Figure 7-20. Linear-phase Decimation Filter Pass-Band Ripple

Table 7-14. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.6			dB
	Frequency range is 4 × f_S onwards	93			

Table 7-14. Linear-phase Decimation Filter Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay or latency	Frequency range is 0 to 0.455 × f_S		14.7		$1/f_S$

7.3.7.2.1.4 Sampling Rate: 32kHz or 29.4kHz

Figure 7-21 and Figure 7-22 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 32kHz or 29.4kHz, and Table 7-15 lists its specifications.

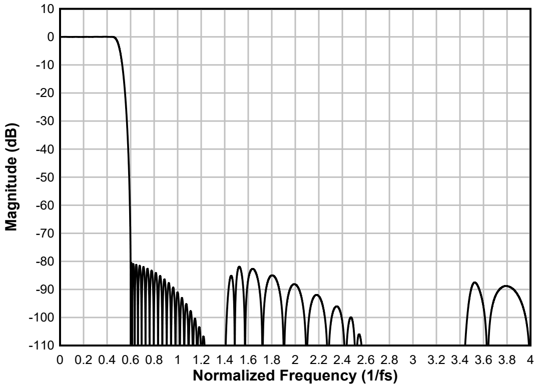


Figure 7-21. Linear-phase Decimation Filter Magnitude Response

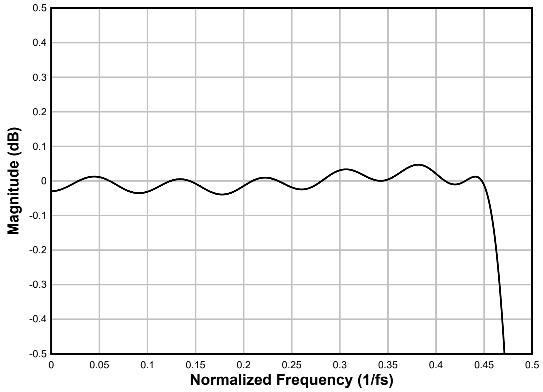


Figure 7-22. Linear-phase Decimation Filter Pass-Band Ripple

Table 7-15. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.6			dB
	Frequency range is 4 × f_S onwards	92.9			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		14.7		$1/f_S$

7.3.7.2.1.5 Sampling Rate: 48kHz or 44.1kHz

Figure 7-23 and Figure 7-24 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 48kHz or 44.1kHz, and Table 7-16 lists its specifications.

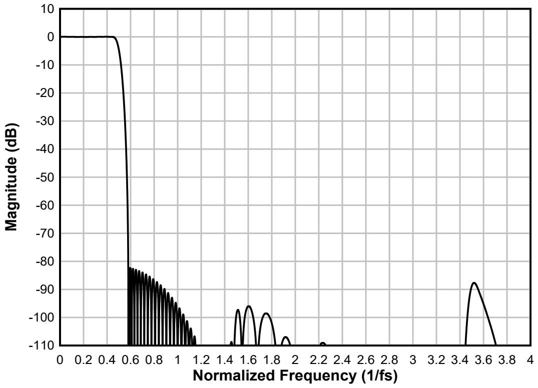


Figure 7-23. Linear-phase Decimation Filter Magnitude Response

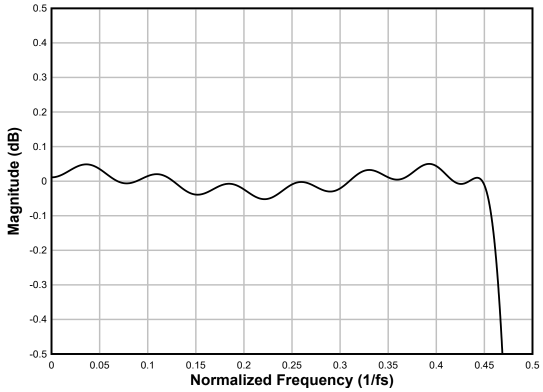


Figure 7-24. Linear-phase Decimation Filter Pass-Band Ripple

Table 7-16. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82.2			dB
	Frequency range is 4 × f_S onwards	98			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17		$1/f_S$

7.3.7.2.1.6 Sampling Rate: 96kHz or 88.2kHz

Figure 7-25 and Figure 7-26 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 96kHz or 88.2kHz, and Table 7-17 lists its specifications.

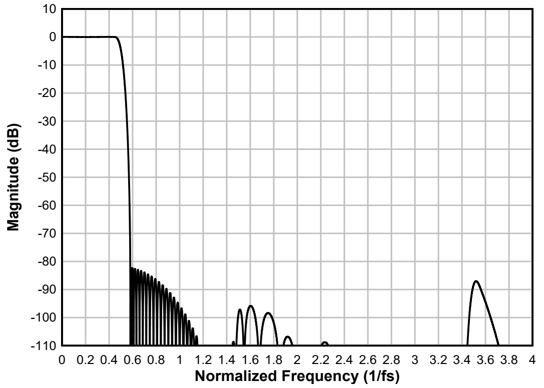


Figure 7-25. Linear-phase Decimation Filter Magnitude Response

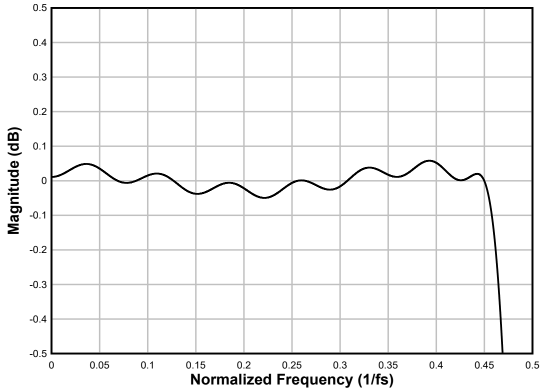


Figure 7-26. Linear-phase Decimation Filter Pass-Band Ripple

Table 7-17. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.06	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82.2			dB
	Frequency range is 4 × f_S onwards	87			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		16.9		$1/f_S$

7.3.7.2.1.7 Sampling Rate: 192kHz or 176.4kHz

Figure 7-27 and Figure 7-28 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 192kHz or 176.4kHz, and Table 7-18 lists its specifications.

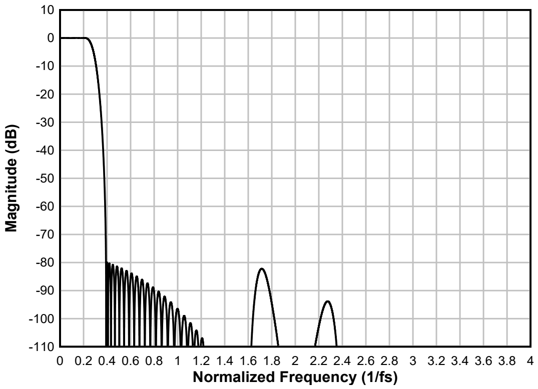


Figure 7-27. Linear-phase Decimation Filter Magnitude Response

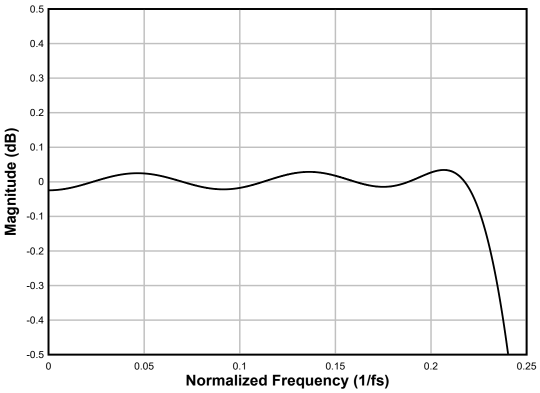


Figure 7-28. Linear-phase Decimation Filter Pass-Band Ripple

Table 7-18. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.223 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.391 × f_S to 4 × f_S	80			dB
	Frequency range is 4 × f_S onwards	82.2			
Group delay or latency	Frequency range is 0 to 0.258 × f_S		11.6		1/f_S

7.3.7.2.2 Low-latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the TAC5242 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the 0.376 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

7.3.7.2.2.1 Sampling Rate: 24kHz or 22.05kHz

Figure 7-29 shows the magnitude response and Figure 7-30 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 24kHz or 22.05kHz. Table 7-19 lists its specifications.

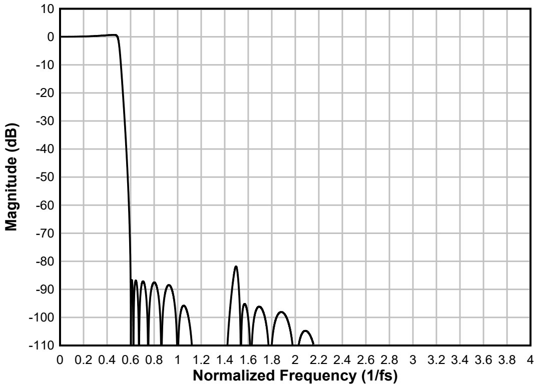


Figure 7-29. Low-latency Decimation Filter Magnitude Response

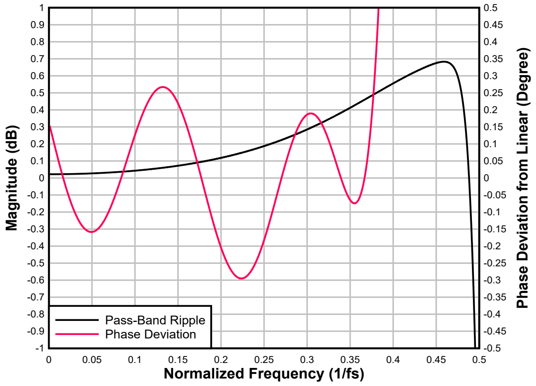


Figure 7-30. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-19. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.492 × f_S	–0.67		–0.67	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	81.8			dB
	Frequency range is 4 × f_S onwards	115			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.5		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.092		0.029	1/f_S
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.3		0.27	Degrees

7.3.7.2.2.2 Sampling Rate: 32kHz or 29.4kHz

Figure 7-31 shows the magnitude response and Figure 7-32 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 32kHz or 29.4kHz. Table 7-20 lists its specifications.

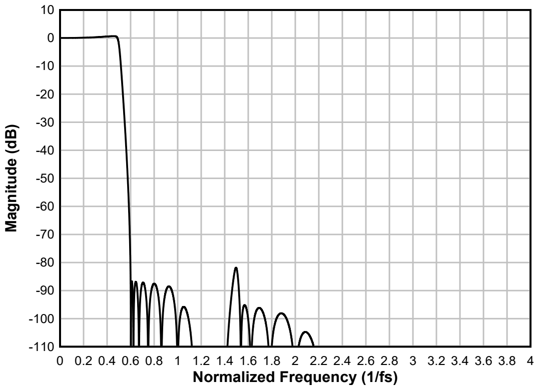


Figure 7-31. Low-latency Decimation Filter Magnitude Response

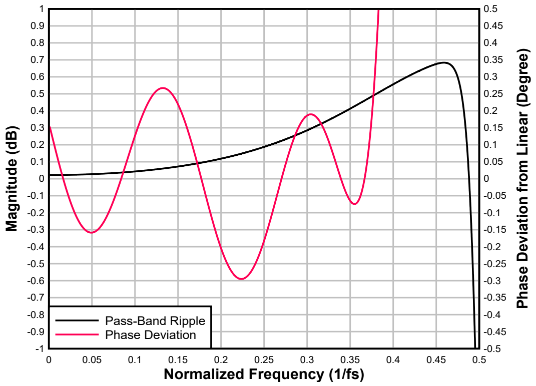


Figure 7-32. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-20. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.492 × f_S	–0.67		–0.67	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	81.8			dB
	Frequency range is 4 × f_S onwards	115			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.5		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.092		0.029	1/f_S
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.3		0.27	Degrees

7.3.7.2.2.3 Sampling Rate: 48kHz or 44.1kHz

Figure 7-33 shows the magnitude response and Figure 7-34 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 48kHz or 44.1kHz. Table 7-21 lists its specifications.

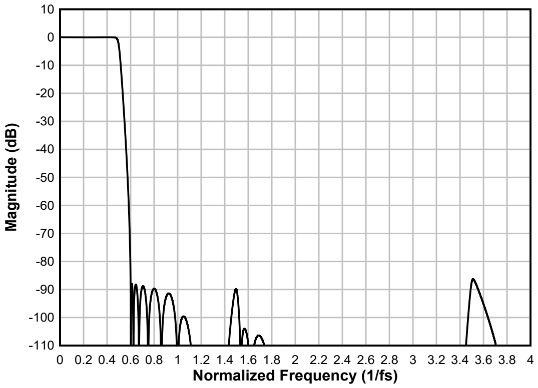


Figure 7-33. Low-latency Decimation Filter Magnitude Response

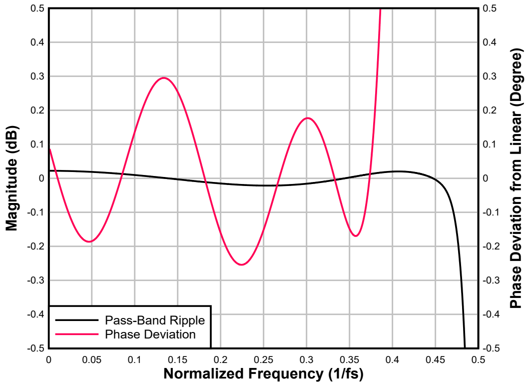


Figure 7-34. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-21. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.456 × f_S	–0.02		–0.02	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	86.3			dB
	Frequency range is 4 × f_S onwards	96.8			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.6		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.086		0.027	1/f_S

Table 7-21. Low-latency Decimation Filter Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.25		0.3	Degrees

7.3.7.2.2.4 Sampling Rate: 96kHz or 88.2kHz

Figure 7-35 shows the magnitude response and Figure 7-36 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 96kHz or 88.2kHz. Table 7-22 lists its specifications.

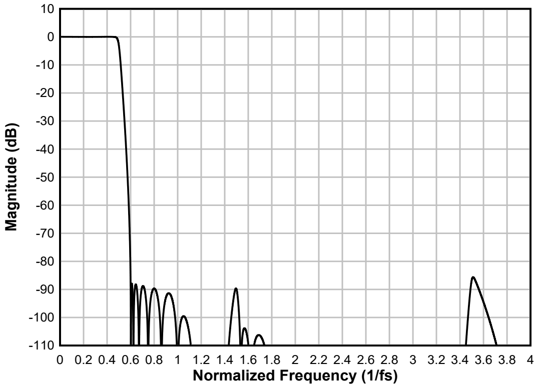


Figure 7-35. Low-latency Decimation Filter Magnitude Response

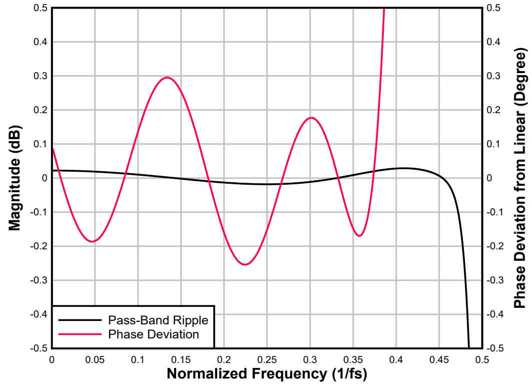


Figure 7-36. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-22. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.456 × f_S	–0.02		0.03	dB
Stop-band attenuation	Frequency range is 0.599 × f_S to 4 × f_S	85.6			dB
	Frequency range is 4 × f_S onwards	95.7			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.6		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.086		0.022	1/f_S
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.25		0.022	Degrees

7.3.7.2.2.5 Sampling Rate: 192kHz or 176.4kHz

Figure 7-37 shows the magnitude response and Figure 7-38 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 192kHz or 176.4kHz. Table 7-23 lists its specifications.

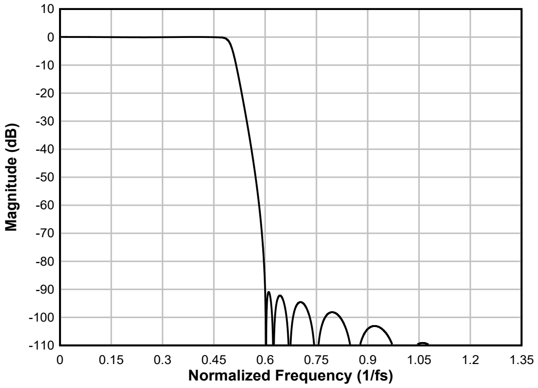


Figure 7-37. Low-latency Decimation Filter Magnitude Response

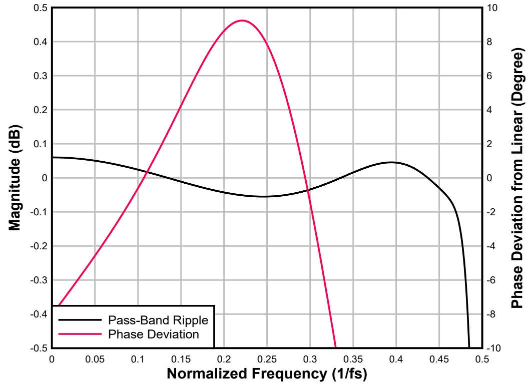


Figure 7-38. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 7-23. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.456 × f_S	–0.06		0.06	dB
Stop-band attenuation	Frequency range is 0.571 × f_S to 1.35 × f_S	90.5			dB
	Frequency range is 1 × f_S onwards	86.9			
Group delay or latency	Frequency range is 0 to 0.327 × f_S		6.8		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.327 × f_S	-0.296		0.829	$1/f_S$
Phase deviation	Frequency range is 0 to 0.327 × f_S	-9.24		9.24	Degrees

7.3.8 DAC Signal-Chain

Figure 7-39 shows the key components of the playback signal chain.

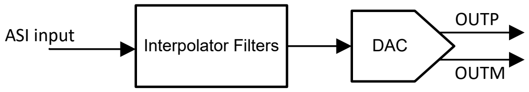


Figure 7-39. DAC Signal-Chain Processing Flowchart

The DAC signal chain offers a highly flexible low-noise playback path for low-noise and high-fidelity audio applications. This low-noise and low-distortion, multi-bit, delta-sigma DAC enables the TAC5242 to achieve a high dynamic range in very low power. Moreover, the DAC architecture has inherent anti-alias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band. The TAC5242 also integrates a high-performance multi-stage digital interpolation filter that sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

7.3.8.1 Digital Interpolation Filters

The device playback channel includes a high dynamic range and a built-in digital interpolation filter to process the input data stream to generate a digital data stream for a multibit delta-sigma (ΔΣ) modulator. The interpolation filters in the device can be selected to linear phase or low-latency filters based on the state of the MD2 and MD1 pins according to Table 7-3. This makes them suitable for a wide variety of audio applications. The following section describes the filter response for different sample rates.

7.3.8.1.1 Linear-phase filters

The linear-phase interpolation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

7.3.8.1.1.1 Sampling Rate: 8kHz or 7.35kHz

Figure 7-40 and Figure 7-41 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 8kHz or 7.35kHz, and Table 7-24 lists its specifications.

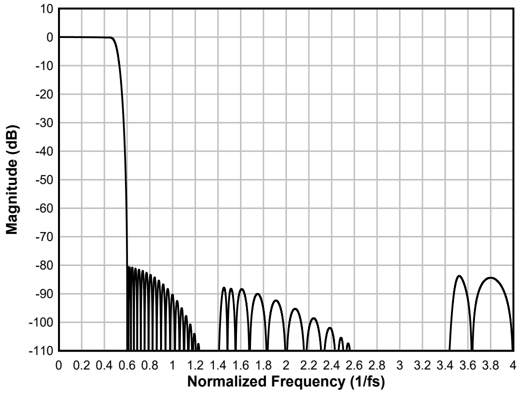


Figure 7-40. Linear-phase Interpolation Filter Magnitude Response

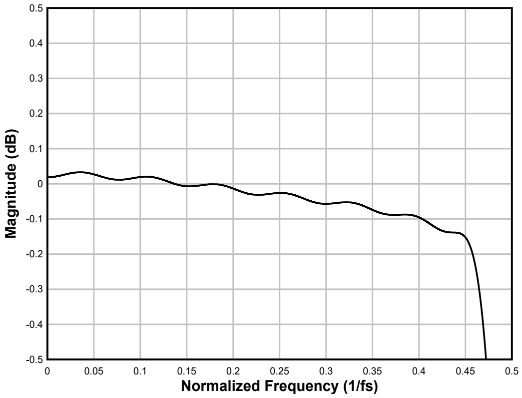


Figure 7-41. Linear-phase Interpolation Filter Pass-Band Ripple

Table 7-24. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.17		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.4			dB
	Frequency range is 4 × f_S to 7.431 × f_S	86.9			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		16		$1/f_S$

7.3.8.1.1.2 Sampling Rate: 16kHz or 14.7kHz

Figure 7-42 and Figure 7-43 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 16kHz or 14.7kHz, and Table 7-25 lists its specifications.

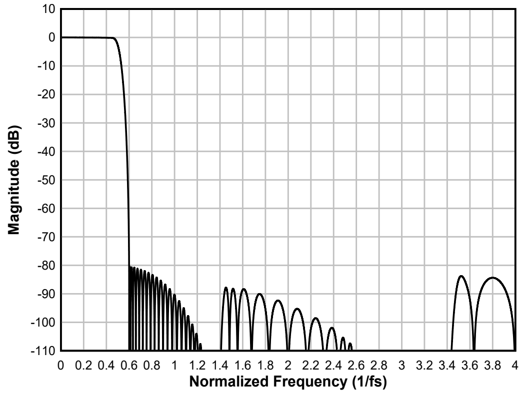


Figure 7-42. Linear-phase Interpolation Filter Magnitude Response

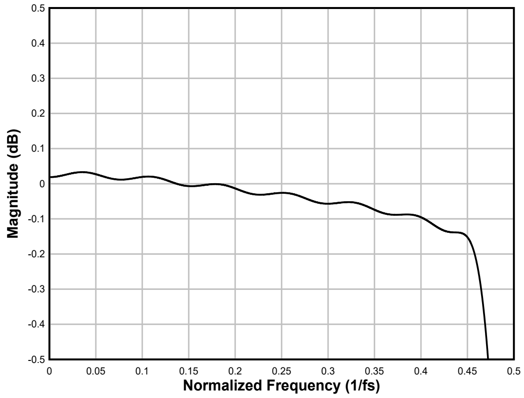


Figure 7-43. Linear-phase Interpolation Filter Pass-Band Ripple

Table 7-25. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.17		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.4			dB
	Frequency range is 4 × f_S to 7.431 × f_S	86.9			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		16		1/f_S

7.3.8.1.1.3 Sampling Rate: 24kHz or 22.05kHz

Figure 7-44 and Figure 7-45 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 24kHz or 22.05kHz, and Table 7-26 lists its specifications.

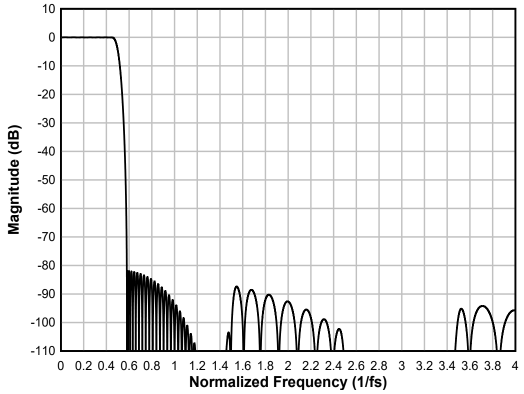


Figure 7-44. Linear-phase Interpolation Filter Magnitude Response

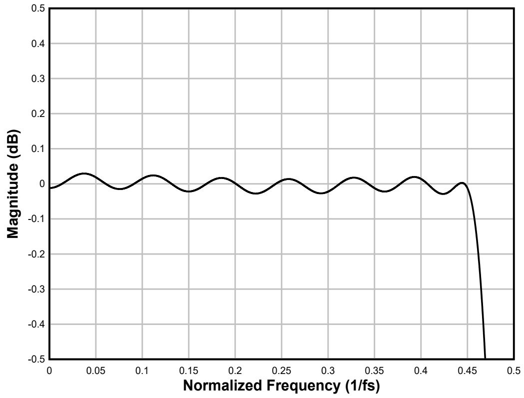


Figure 7-45. Linear-phase Interpolation Filter Pass-Band Ripple

Table 7-26. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.03	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	81.9			dB
	Frequency range is 4 × f_S to 8 × f_S	87.7			

Table 7-26. Linear-phase Interpolation Filter Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay or latency	Frequency range is 0 to 0.455 × f_S		17.6		$1/f_S$

7.3.8.1.1.4 Sampling Rate: 32kHz or 29.4kHz

Figure 7-46 and Figure 7-47 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 32kHz or 29.4kHz, and Table 7-27 lists its specifications.

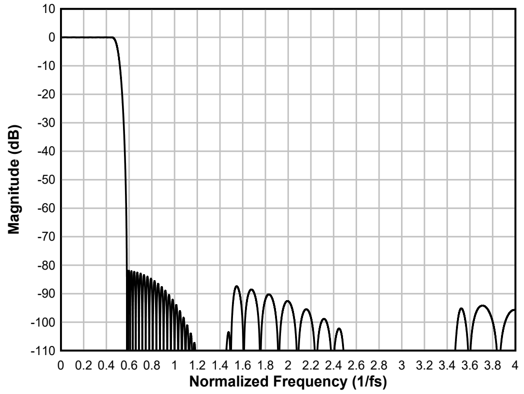


Figure 7-46. Linear-phase Interpolation Filter Magnitude Response

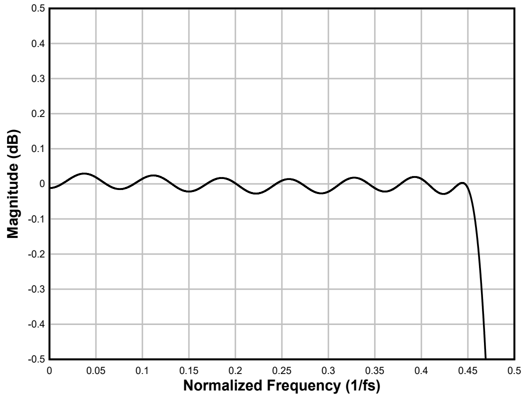


Figure 7-47. Linear-phase Interpolation Filter Pass-Band Ripple

Table 7-27. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.03	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	81.9			dB
	Frequency range is 4 × f_S to 8 × f_S	87.6			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		17.6		$1/f_S$

7.3.8.1.1.5 Sampling Rate: 48kHz or 44.1kHz

Figure 7-48 and Figure 7-49 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 48kHz or 44.1kHz, and Table 7-28 lists its specifications.

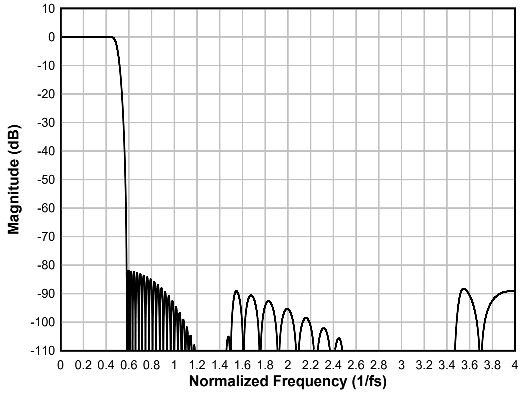


Figure 7-48. Linear-phase Interpolation Filter Magnitude Response

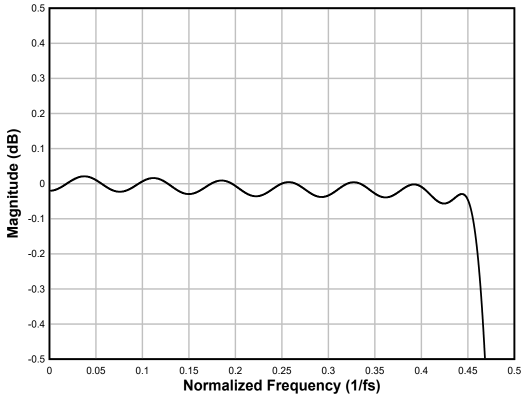


Figure 7-49. Linear-phase Interpolation Filter Pass-Band Ripple

Table 7-28. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.09		0.02	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82			dB
	Frequency range is 4 × f_S to 7.423 × f_S	89.1			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		17.3		1/f_S

7.3.8.1.1.6 Sampling Rate: 96kHz or 88.2kHz

Figure 7-50 and Figure 7-51 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 96kHz or 88.2kHz, and Table 7-29 lists its specifications.

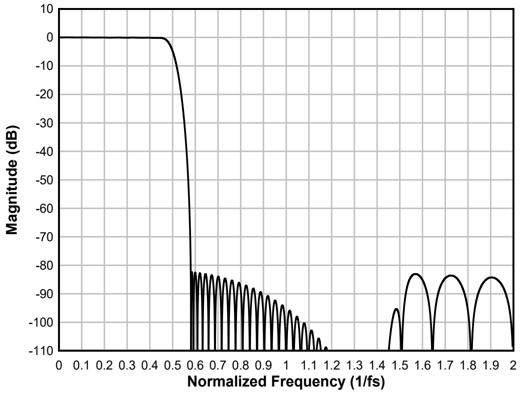


Figure 7-50. Linear-phase Interpolation Filter Magnitude Response

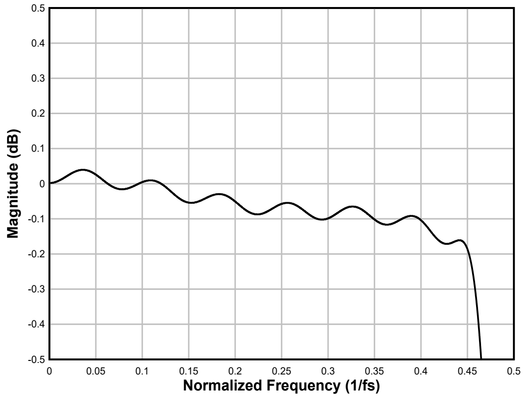


Figure 7-51. Linear-phase Interpolation Filter Pass-Band Ripple

Table 7-29. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.23		0.04	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 2 × f_S	82.4			dB
	Frequency range is 2 × f_S to 3.422 × f_S	85.1			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		16.7		1/f_S

7.3.8.1.1.7 Sampling Rate: 192kHz or 176.4kHz

Figure 7-52 and Figure 7-53 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 192kHz or 176.4kHz, and Table 7-30 lists its specifications.

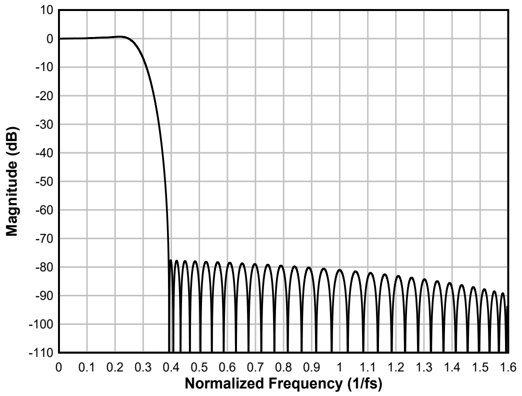


Figure 7-52. Linear-phase Interpolation Filter Magnitude Response

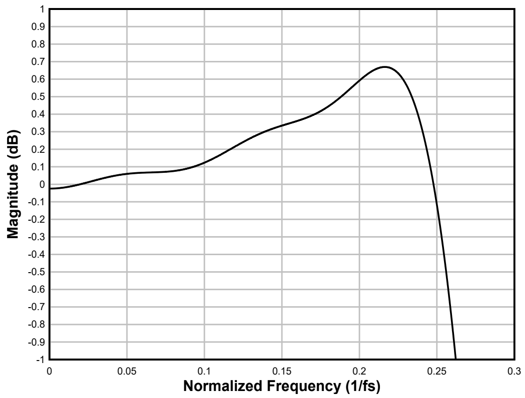


Figure 7-53. Linear-phase Interpolation Filter Pass-Band Ripple

Table 7-30. Linear-phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.258 × f_S	–0.67		0.67	dB
Stop-band attenuation	Frequency range is 0.391 × f_S to 1 × f_S	77.7			dB
	Frequency range is 1 × f_S to 1.612 × f_S	81.1			
Group delay or latency	Frequency range is 0 to 0.258 × f_S		10.7		1/f_S

7.3.8.1.2 Low-latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency interpolation filters on the TAC5242 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the 0.376 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

7.3.8.1.2.1 Sampling Rate: 24kHz or 22.05kHz

Figure 7-54 shows the magnitude response and Figure 7-55 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 24kHz or 22.05kHz. Table 7-31 lists its specifications.

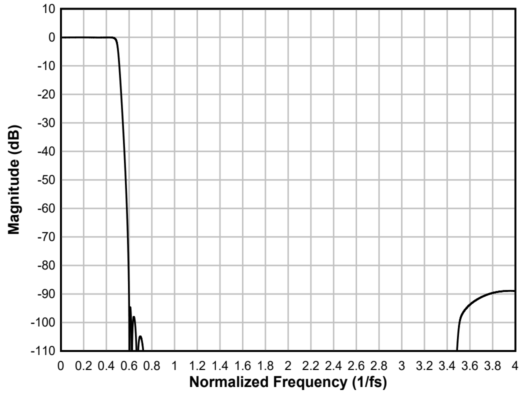


Figure 7-54. Low-latency Interpolation Filter Magnitude Response

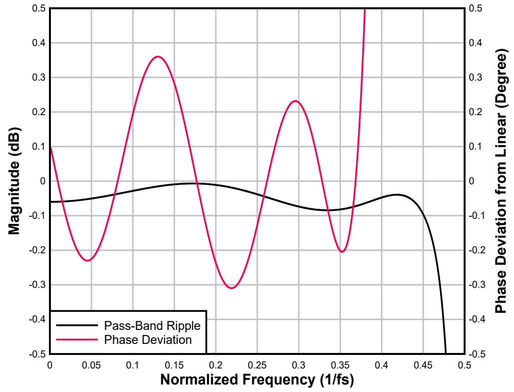


Figure 7-55. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 7-31. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.12		–0.01	dB
Stop-band attenuation	Frequency range is 0.599 × f_S to 4 × f_S	88.9			dB
	Frequency range is 4 × f_S to 7.414 × f_S	89			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		7.19		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.088		0.088	$1/f_S$
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.31		0.36	Degrees

7.3.8.1.2.2 Sampling Rate: 32kHz or 29.4kHz

Figure 7-56 shows the magnitude response and Figure 7-57 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 32kHz or 29.4kHz. Table 7-32 lists its specifications.

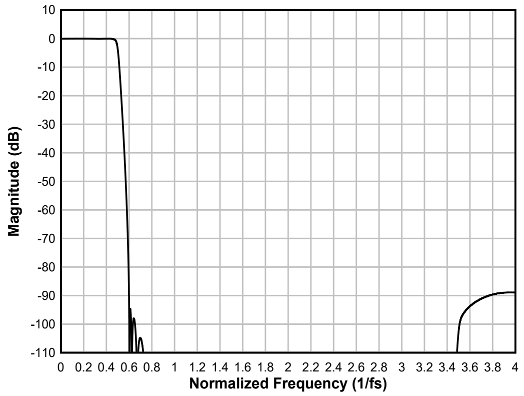


Figure 7-56. Low-latency Interpolation Filter Magnitude Response

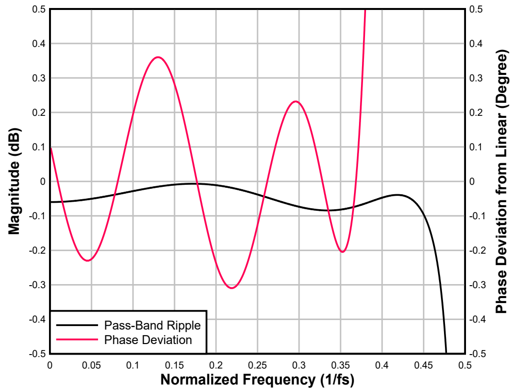


Figure 7-57. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 7-32. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.12		–0.01	dB
Stop-band attenuation	Frequency range is 0.599 × f_S to 4 × f_S	88.9			dB
	Frequency range is 4 × f_S to 7.414 × f_S	89			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		7.19		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.088		0.088	$1/f_S$
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.31		0.36	Degrees

7.3.8.1.2.3 Sampling Rate: 48kHz or 44.1kHz

Figure 7-58 shows the magnitude response and Figure 7-59 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 48kHz or 44.1kHz. Table 7-33 lists its specifications.

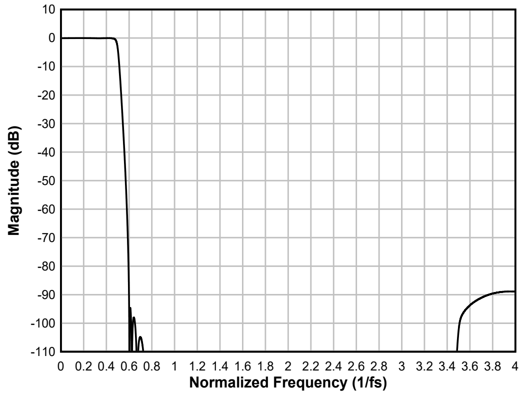


Figure 7-58. Low-latency Interpolation Filter Magnitude Response

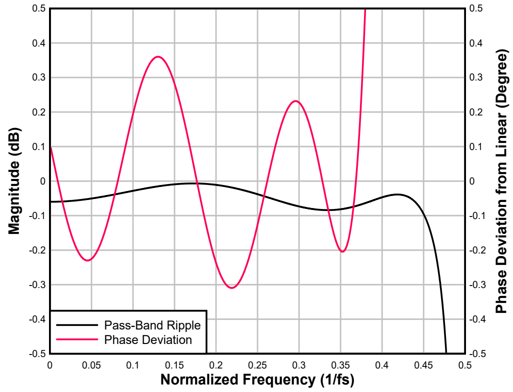


Figure 7-59. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 7-33. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.12		–0.01	dB
Stop-band attenuation	Frequency range is 0.599 × f_S to 4 × f_S	88.9			dB
	Frequency range is 4 × f_S to 7.414 × f_S	89			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		7.19		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.088		0.088	$1/f_S$

Table 7-33. Low-latency Interpolation Filter Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.31		0.36	Degrees

7.3.8.1.2.4 Sampling Rate: 96kHz or 88.2kHz

Figure 7-60 shows the magnitude response and Figure 7-61 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 96kHz or 88.2kHz. Table 7-34 lists its specifications.

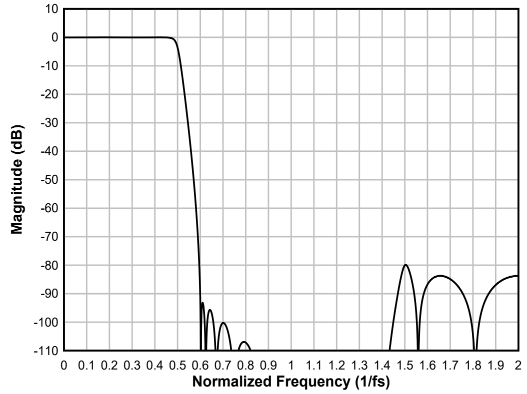


Figure 7-60. Low-latency Interpolation Filter Magnitude Response

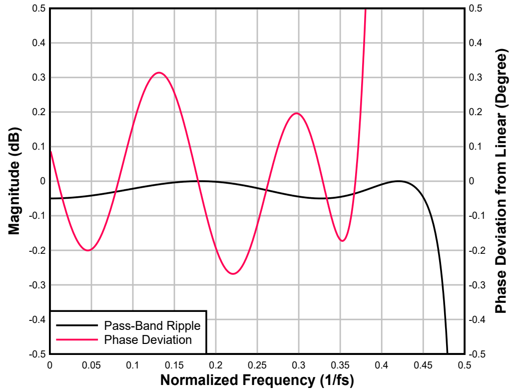


Figure 7-61. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 7-34. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.456 × f_S	–0.07		0	dB
Stop-band attenuation	Frequency range is 0.595 × f_S to 2 × f_S	79.9			dB
	Frequency range is 2 × f_S to 3.405 × f_S	79.9			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.39		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.078		0.022	$1/f_S$
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.268		0.022	Degrees

7.3.8.1.2.5 Sampling Rate: 192kHz or 176.4kHz

Figure 7-62 shows the magnitude response and Figure 7-63 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 192kHz or 176.4kHz. Table 7-35 lists its specifications.

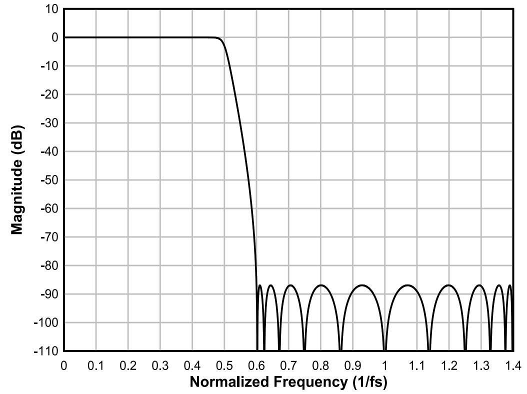


Figure 7-62. Low-latency Interpolation Filter Magnitude Response

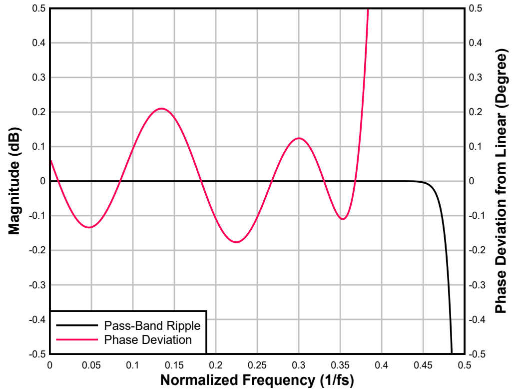


Figure 7-63. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation

Table 7-35. Low-latency Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.005		0	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 1 × f_S	86.9			dB
	Frequency range is 1 × f_S to 1.401 × f_S	86.9			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		5.41		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.055		0.055	$1/f_S$
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.177		0.21	Degrees

7.4 Device Functional Modes

7.4.1 Active Mode

The device wakes up in active mode when AVDD and IOVDD are available. MD0 pin sets the type of audio serial interface and should be configured along with the supplies. Further, configure all other hardware control mode pins (MD1, MD2, MD3, MD4, and MD5) for the desired mode of operation before enabling the clocks for the device.

In active mode, when the audio clocks are available, the device automatically powers up all the ADC and DAC channels and starts receiving and transmitting data over the audio serial interface as per the configurations. If the clocks are stopped, then the device auto-powers down the ADC and DAC channels.

Stopping the clocks or clock error triggers an interrupt on the GPO pin. This is a latched interrupt that can be cleared by power-cycling the device supplies.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TAC5242 is a pin or hardware-controlled, high-performance stereo audio codec that supports sample rates of up to 192kHz on both the record and playback paths. The device can be configured by controlling the Mode pins MD0 to MD5 and can support 1.8V or 3.3V AVDD analog power supply along with flexible digital audio interfaces of I^{2}S/TDM/LJ. The ADC has differential and single-ended input capabilities and can support both line-in and microphone inputs for stereo recording with high dynamic range, and the DAC supports various output configurations like 2-channel differential, single-ended or pseudo-differential with external common-mode sense outputs with options for headphone and line-out drive capabilities.

8.2 Typical Application

8.2.1 Application

Figure 8-1 shows a typical configuration of the TAC5242 for an application using a 2-channel differential AC-coupled microphone operation and a 2-channel differential line-out operation with a Target Mode I^{2}S audio serial data interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

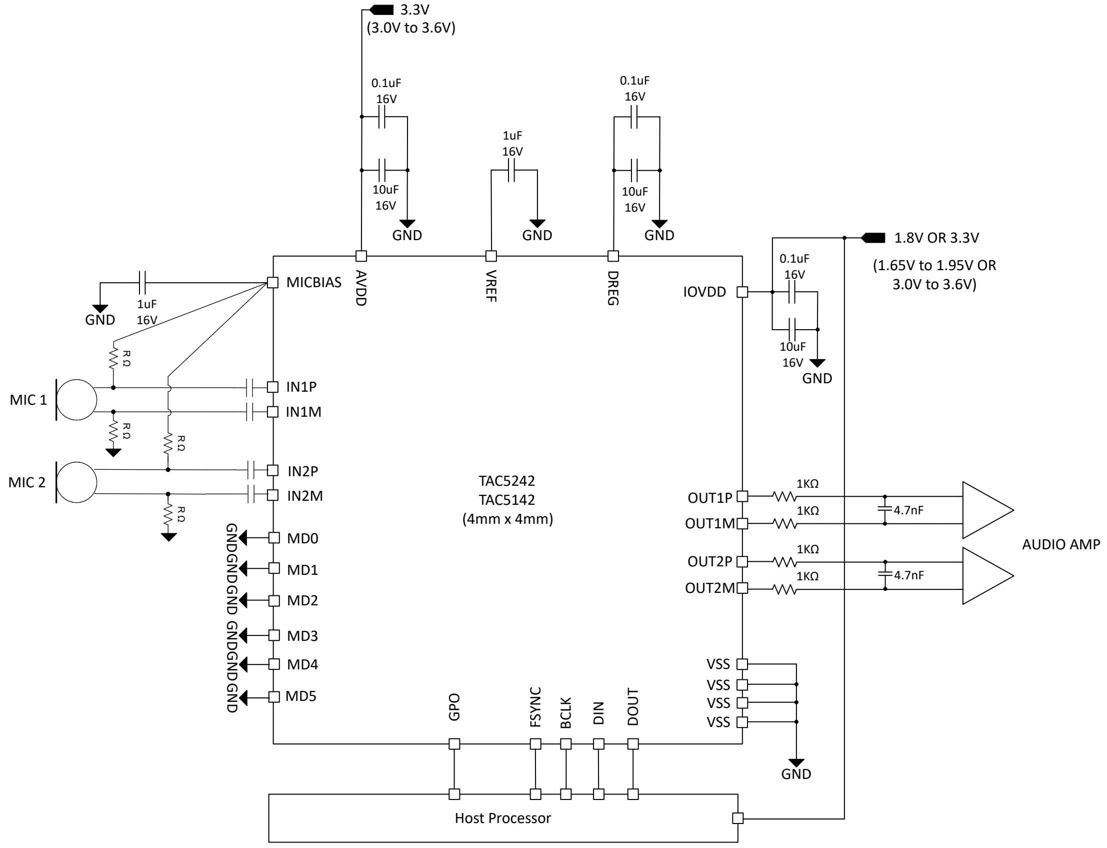


Figure 8-1. Stereo Differential AC-Coupled Microphone with Stereo Differential Line-out in Target I^{2}S Mode, Block Diagram

8.2.2 Design Requirements

Table 8-1 lists the design parameters for this application.

Table 8-1. Design Parameters

PARAMETER	VALUE
AVDD	3.3V
IOVDD	1.8V or 3.3V
AVDD supply current consumption	27mA, with AVDD = 3.3V
IOVDD supply current consumption	0.1mA, with IOVDD = 3.3V
Maximum MICBIAS current	5mA
Load on OUT1M, OUT1P, OUT2M, OUT2P	>600 ohms

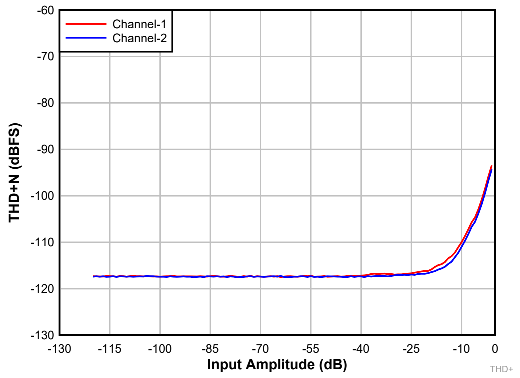
8.2.3 Detailed Design Procedure

This section describes the necessary steps to configure the TAC5242 for this specific application.

1. Audio Serial Interface (ASI) Mode is configured based on the MD0 pin setting which needs to be provided along with the power supplies. Configure MD0 to be either pulled up to AVDD or down to VSS with appropriate resistor values. MD0 is to be grounded for this application case.
2. Apply power to the device:
   a. Power up the IOVDD and AVDD power supplies.
   b. Ensure that the MD0 pin setting is stable as soon as power supplies are up and wait for at least 2ms to allow the device to initialize for this mode of operation.
   c. The device now goes into sleep mode (low-power mode <1.5mA)
3. Configure the Mode pins MD1 to MD5 as per the system requirements:
   a. Pull up to IOVDD or pull down to VSS on MD1 to MD5 pins as per the required configuration. The MD1 to MD5 pins are grounded for this application's use-case.
4. Apply the ASI clocks (BCLK and FSYNC) to wake up the device.
5. To put the device back in sleep mode, stop the clocks:
   a. Wait at least 100ms to allow the device to complete the shutdown sequence.
   b. Change the device configurations by changing MD1 to MD5 pin settings as per requirement.
6. To change the ASI mode, re-configure the MD0 pin and power-cycle the device.
7. Repeat steps 1-6 as required for mode transitions.

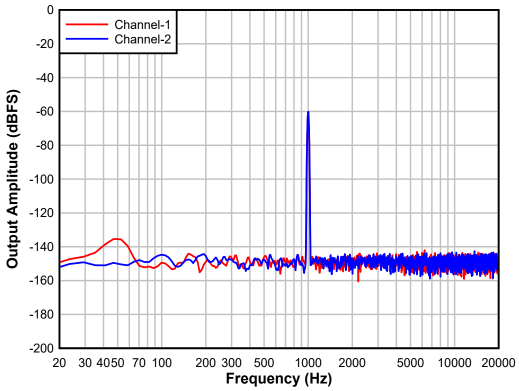
8.2.4 Application Performance Plots

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear phase decimation and interpolation filters, with differential AC-coupled line-input configuration and 1200Ω line-out load in differential configuration; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted



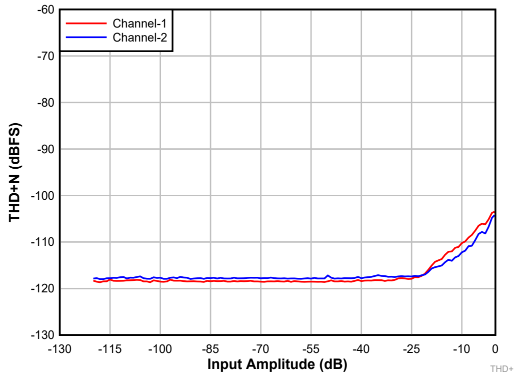
AC-coupled differential line input

Figure 8-2. ADC THD+N Level vs Input



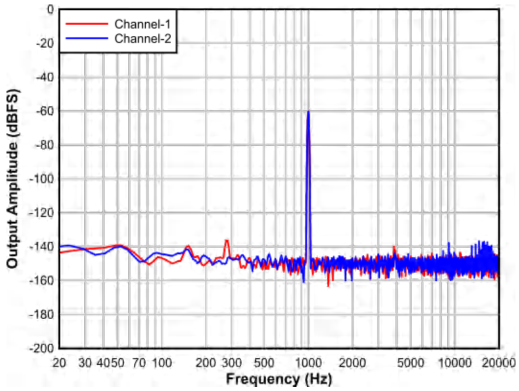
AC-coupled differential line input (-60dBFS)

Figure 8-3. ADC FFT with -60dBFS Input



Differential output

Figure 8-4. DAC THD+N Level vs Input



Differential output (-60dBFS input)

Figure 8-5. DAC FFT with -60dBFS Input

8.3 Power Supply Recommendations

The power supply sequence between the IOVDD and AVDD rails can be applied in any order. MD0 pin should be provided along with the power supplies and should be stable as soon as the supplies are settled to the recommended operating voltage levels. Only initiate the clocks to initialize the device after all the other Mode pins (MD1 to MD5) are also stable.

For the supply power-up requirement, t_1, t_2 and t_3 must be at least 2ms to allow the device to initialize the internal settings. See the *Section 7.3.1* for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement, t_4, t_5 and t_6 must be at least 10ms. This timing (as shown in Figure 8-6) allows the device to ramp down the volume on the record and playback data, power down the analog and digital blocks, and put the device into a low power mode.

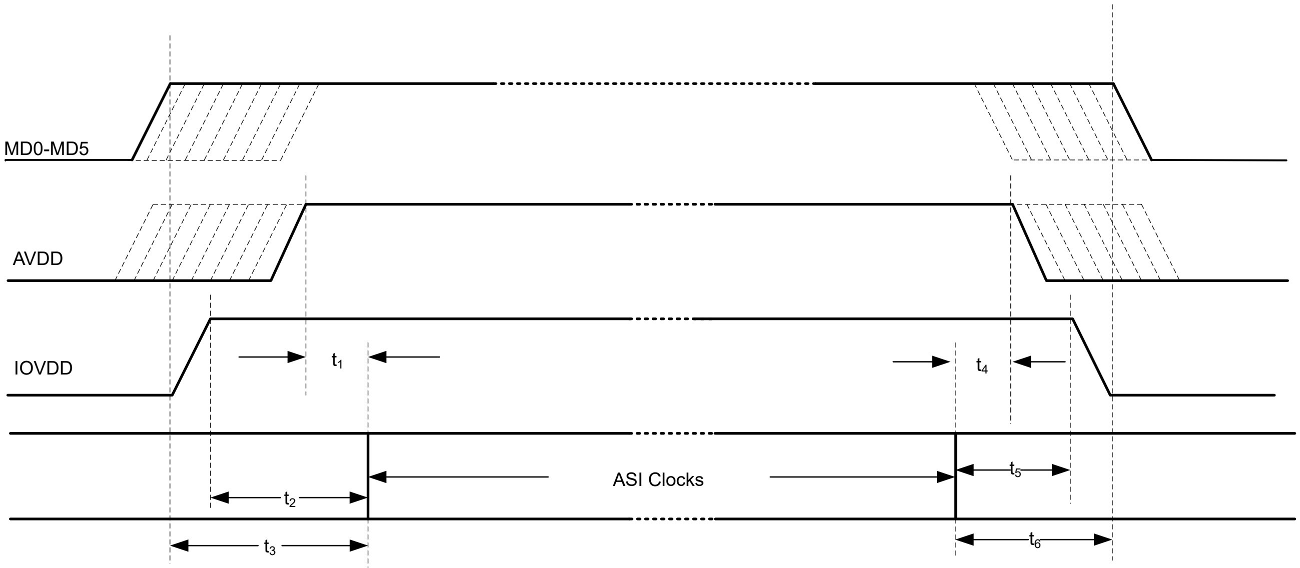


Figure 8-6. Power-Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 0.1V/µs and that the wait time between a power-down and a power-up event is at least 100ms.

The TAC5242 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an internal analog regulator.

8.4 Layout

8.4.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- Use the same ground between VSS and VSSA to avoid any potential voltage difference between them.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- Route the analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- Avoid running high-frequency clock and control signals near INxx and OUTxx pins where possible.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for good performance.
- Directly tap the MICBIAS pin to avoid common impedance when routing the biasing or supply traces for multiple microphones to avoid coupling across microphones.
- Provide a direct connection from the VREF and MICBIAS external capacitor ground terminal to the VSS pin.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

8.4.2 Layout Example

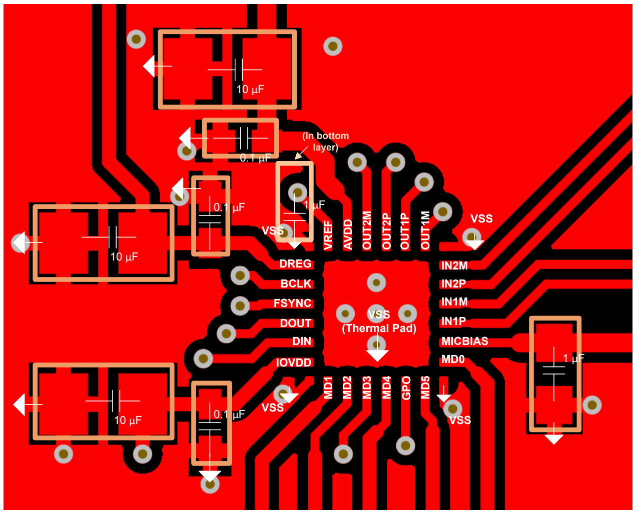


Figure 8-7. Example Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TAx5x42EVM-K Hardware Control Evaluation Module* User's Guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2024) to Revision A (November 2024)	**Page**
• Updated device status to production data.	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAC5242IRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TAC5242
TAC5242IRGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TAC5242

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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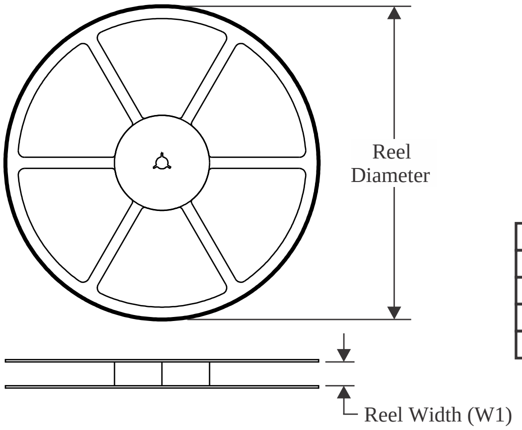
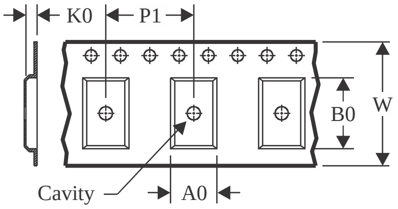
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

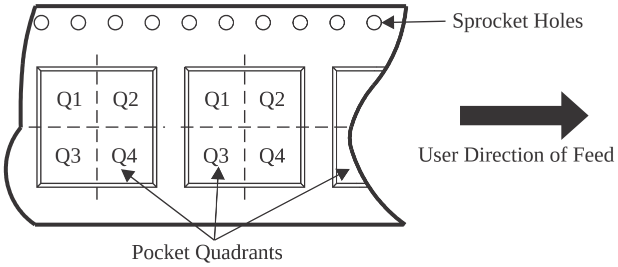


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

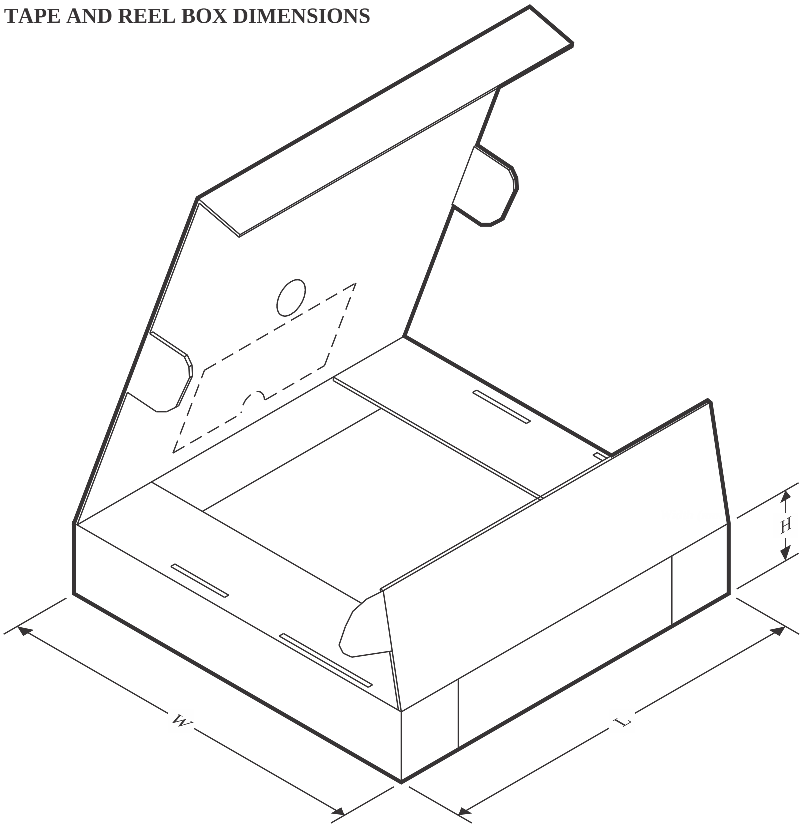
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAC5242IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

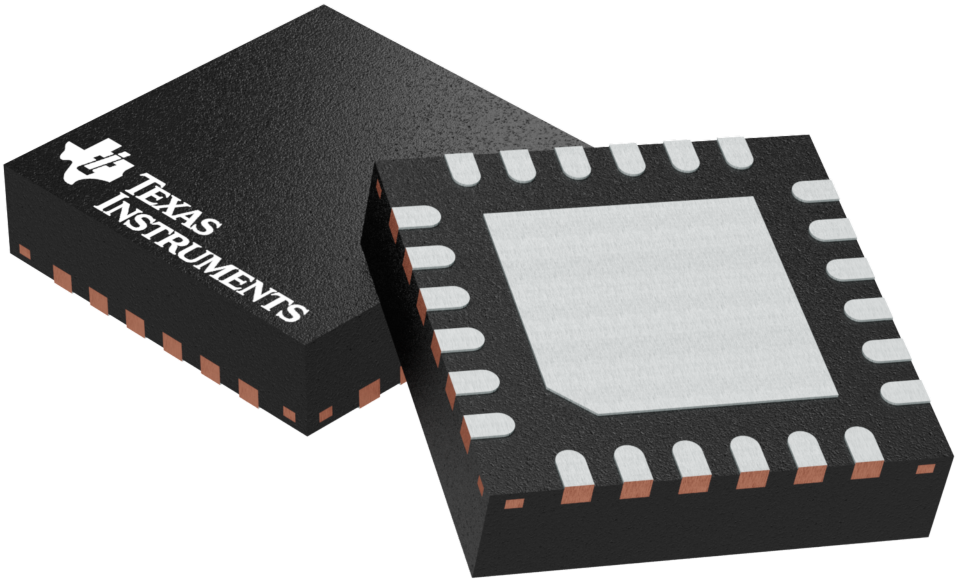
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAC5242IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

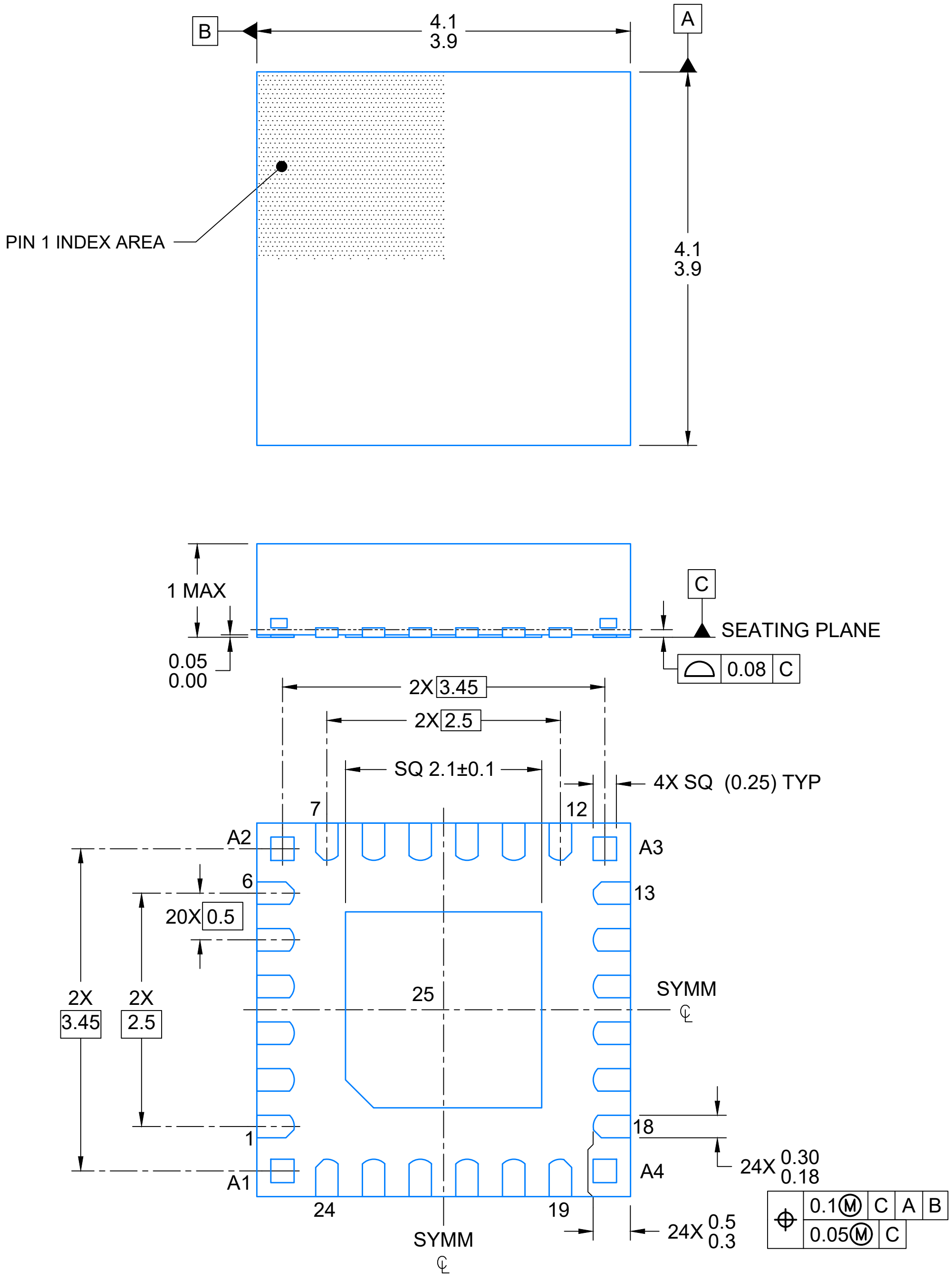


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGE0024R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



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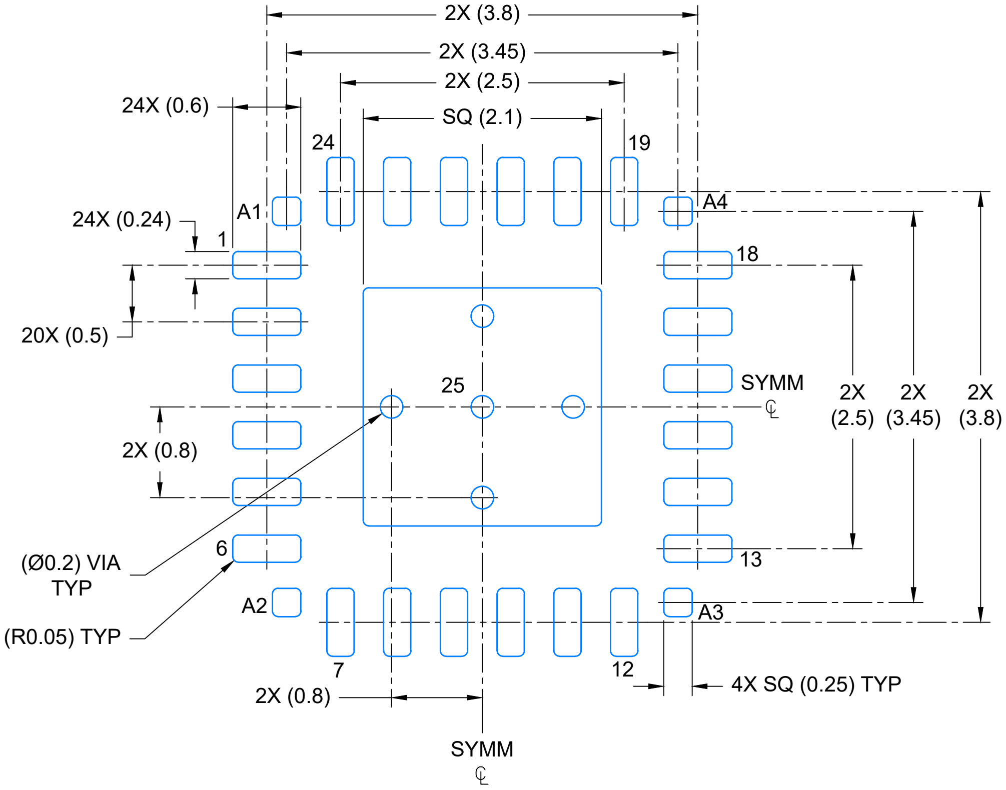
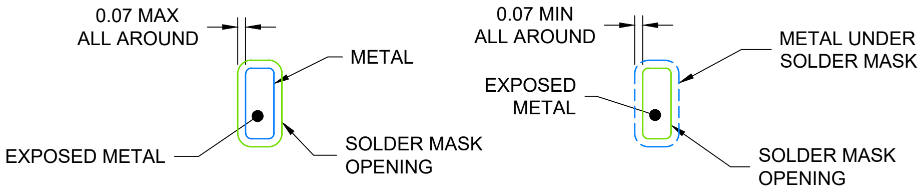
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



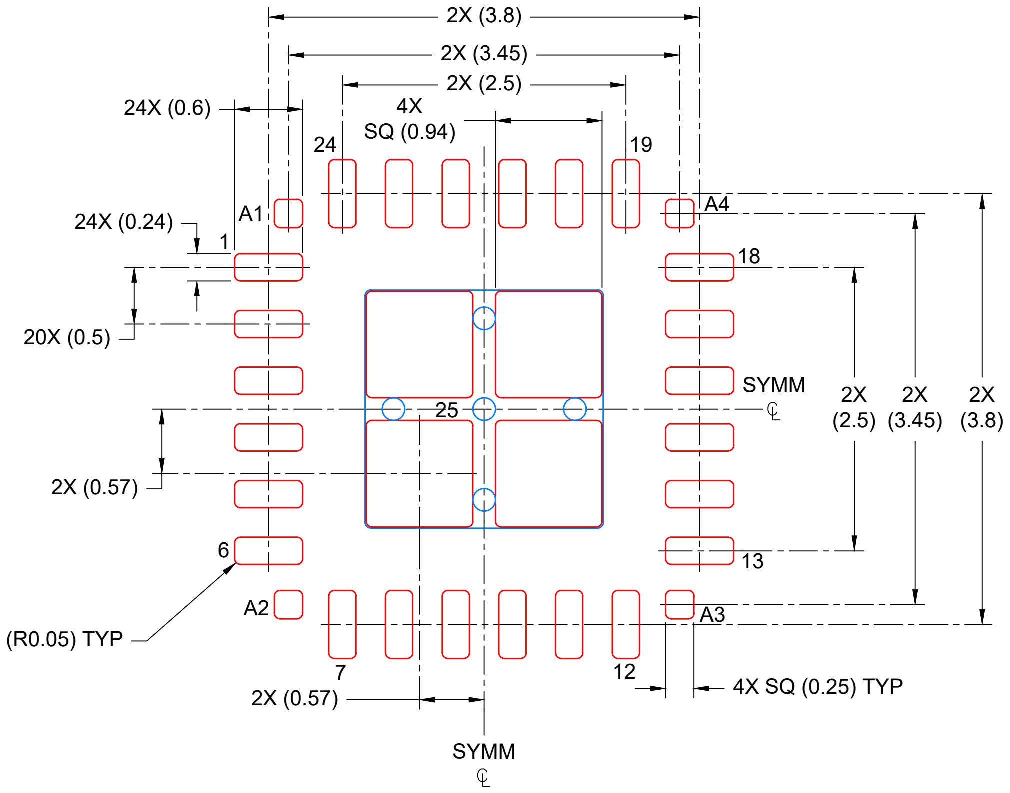
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

4225246/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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