SN75LVPE3410 Quad-Channel PCI-Express 3.0 Linear Redriver

1 Features

- Quad-channel linear equalizer supporting PCIe 1.0/2.0/3.0 up to 8 Gbps interfaces
- CTLE boosts up to 12 dB at 4 GHz helps to extend channel reach
- Ultra-low latency of 70 ps
- Excellent return loss of -17 dB at 4 GHz
- Low additive random jitter of 60 fs (typical) with PRBS data
- Single 3.3-V supply
- Internal voltage regulator provides immunity to supply noise
- Low active power of 124 mW/channel
- No heat sink required
- Pin-strap or SMBus programming
- Support for x2, x4, x8, x16 PCIe bus width with one or multiple SN75LVPE3410
- Automatic receiver detection for PCIe use cases
- Protocol agnostic linear redriver allows seamless support for PCIe link training
- Commercial temperature range of 0°C to 70°C
- 4.0 mm × 6.0 mm, 40 pin WQFN package

2 Applications

- Desktop PC or motherboard
- Notebook PC
- Data storage
- Industrial computer on module

3 Description

The SN75LVPE3410 is a four channel low-power high-performance linear repeater or redriver designed to support PCI Express (PCIe™) Generation 1.0, 2.0 and 3.0.

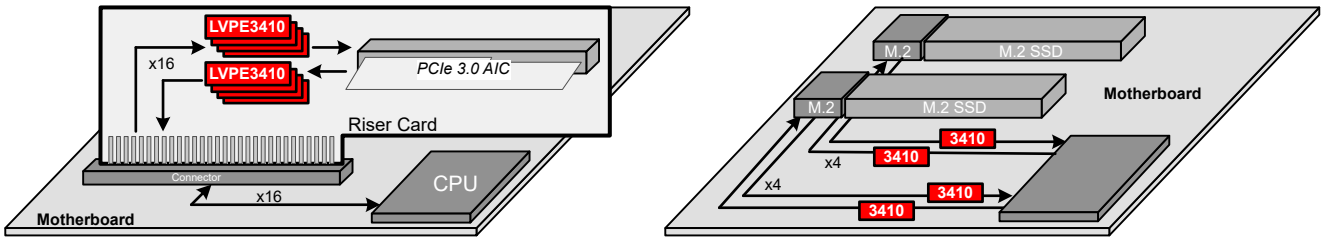
The SN75LVPE3410 receivers deploy continuous time linear equalizers (CTLE) to provide a programmable high-frequency boost. The equalizer can open an input eye that is completely closed due to inter-symbol interference (ISI) induced by an interconnect medium, such as PCB traces. The CTLE receiver is followed by a linear output driver. The linear datapaths of SN75LVPE3410 preserve transmit preset signal characteristics. The linear redriver becomes part of the passive channel that as a whole get link trained for best transmit and receive equalization settings. This transparency in the link training protocol result in best electrical link and lowest possible latency. The programmable equalization of the device along with its linear datapaths maximizes the flexibility of physical placement within the interconnect channel and improves overall channel performance.

The programmable settings can be applied easily through software (SMBus or I^2C) or by using pin control.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN75LVPE3410	RNQ (WQFN, 40)	6 mm × 4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Revision History

DATE	REVISION	NOTES
June 2023	*	Initial Release

5 Pin Configuration and Functions

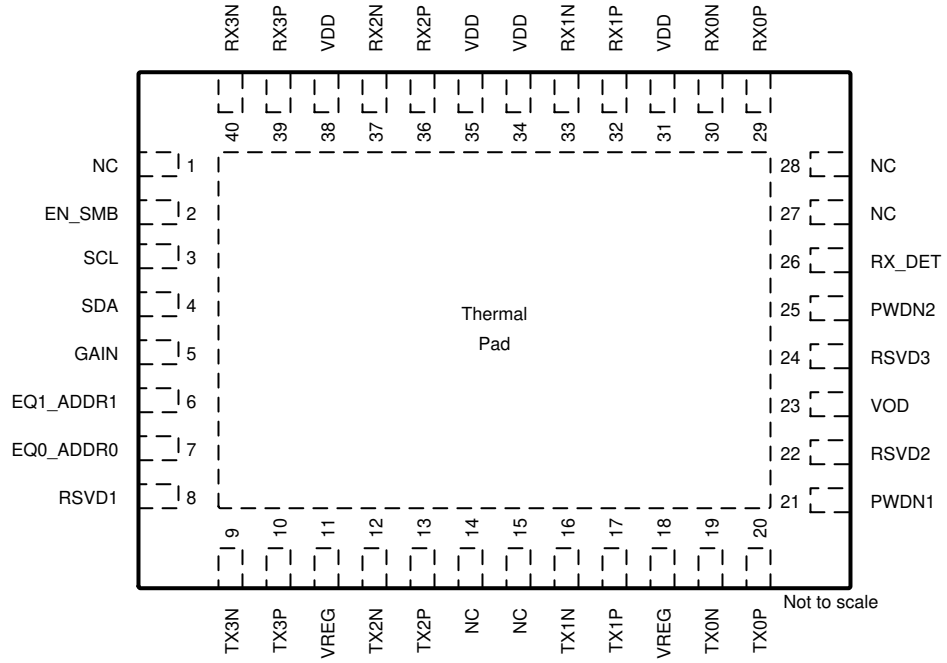


Figure 5-1. RNQ Package, 40-Pin WQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN_SMB	2	I, 4-level	Four-level control input used to select SMBus/I²C or Pin control. L0: **Pin mode** L1: RESERVED L2: RESERVED L3: **I²C or SMBus Target Mode**
EQ0_ADDR0	7	I, 4-level	The 4-Level Control Input pins of SN75LVPE3410 is provided in Table 7-4. In **I²C or SMBus Mode** (EN_SMB = L3), the pins are used to set the I²C or SMBus address of the device. The pin state is read on power up and decoded is provided in Table 7-5. In **Pin mode** (EN_SMB = L0), the pins are decoded at power up to control the CTLE boost setting as provided in Table 7-1.
EQ1_ADDR1	6	I, 4-level	
GAIN	5	I, 4-level	Sets DC gain of CTLE at power up. L0: Reserved L1: Reserved L2: 0 dB (recommended) L3: 3.5 dB
GND	EP	P	EP is the Exposed Pad at the bottom of the WQFN package. It is used as the GND return for the device. The EP should be connected to one or more ground planes through low resistance path. A via array provides a low impedance path to GND, and also improves thermal dissipation.
NC	1, 14, 15, 27, 28	—	No connect
PWDN1	21	I, 3.3 V LVCMOS	Two-level logic controlling the operating state of the redriver. The pin triggers PCIe Rx detect state machine when toggled. High: Power down for channels 0 and 1 Low: Power up, normal operation for channels 0 and 1.
PWDN2	25	I, 3.3 V LVCMOS	Two-level logic controlling the operating state of the redriver. The pin triggers PCIe Rx detect state machine when toggled. High: Power down for channels 2 and 3 Low: Power up, normal operation for channels 2 and 3.
RSVD1	8	—	RESERVED. Can be left unconnected or pulled up to VDD with 4.7k resistor.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
RSVD2	22	—	RESERVED. The pin must be pulled high to VDD with external 4.7k resistor.
RSVD3	24	—	Reserved use for TI. The pin must be left floating (NC).
RX_DET	26	I, 4-level	The RX_DET pin controls the receiver detect function. Depending on the input level, a 50 Ω or >50 kΩ termination to the power rail is enabled. More information is provided in Table 7-3.
RX0N	30	I	Inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 0.
RX0P	29	I	Non-inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 0.
RX1N	33	I	Inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 1.
RX1P	32	I	Non-inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 1.
RX2N	37	I	Inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 2.
RX2P	36	I	Non-inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 2.
RX3N	40	I	Inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 3.
RX3P	39	I	Non-inverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 3.
SCL	3	I/O, 3.3 V LVCMOS, open drain	SMBus / I^2C clock input / open-drain output. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I^2C interface standard. This pin is 3.3 V tolerant.
SDA	4	I/O, 3.3 V LVCMOS, open drain	SMBus / I^2C data input / open-drain clock output. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus interface standard. This pin is 3.3 V tolerant.
TX0N	19	O	Inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 0.
TX0P	20	O	Non-inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 0.
TX1N	16	O	Inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 1.
TX1P	17	O	Non-inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 1.
TX2N	12	O	Inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 2.
TX2P	13	O	Non-inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 2.
TX3N	9	O	Inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 3.
TX3P	10	O	Non-inverting 50 Ω driver outputs. Compatible with AC-coupled differential inputs. Also used for RX detection at power up. Channel 3.
VDD	31, 34, 35, 38	P	Power supply pins. VDD = 3.3 V ±10%. The VDD pins on this device should be connected through a low-resistance path to the board VDD plane. Typical supply decoupling consists of a 0.1 µF capacitor per VDD pin and one 1.0 µF bulk capacitor per device.
VOD	23	I, 4-level	Sets TX VOD setting at power up. L0: –6 dB L1: –3.5 dB L2: 0 dB (recommended) L3: –1.5 dB

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VREG	11, 18	P	Internal voltage regulator output. Must add decoupling caps of 0.1 µF near each pin. The regulator is only for internal use. Do not use to power any external components. Do not route the signal beyond the decoupling capacitors on board.

(1) I = input, O = ouptut, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD_{ABSMAX}	Supply Voltage (VDD)	–0.5	4.0	V
$VIO_{CMOS,ABSMAX}$	3.3 V LVCMOS and Open Drain I/O voltage	–0.5	4.0	V
$VIO_{4LVL,ABSMAX}$	4-level Input I/O voltage	–0.5	2.75	V
$VIO_{HS-RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	–0.5	3.2	V
$VIO_{HS-TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	–0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VDD	Supply voltage, VDD to GND	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
N_{VDD}	Supply noise tolerance	Supply noise, DC to <50 Hz, sinusoidal[1]			250	mVpp
		Supply noise, 50 Hz to 10 MHz, sinusoidal[1]			20	mVpp
		Supply noise, >10 MHz, sinusoidal[1]			10	mVpp
$T_{RampVDD}$	VDD supply ramp time	From 0 V to 3.0 V	0.150		100	ms
T_A	Operating ambient temperature		0		70	C
PW_{LVCMOS}	Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs	PWDN1/2	200			µs
VDD_{SMBUS}	SMBus SDA and SCL Open Drain Termination Voltage	Supply voltage for open drain pull-up resistor			3.6	V
F_{SMBus}	SMBus clock (SCL) frequency in SMBus target mode		10		400	kHz
VID_{LAUNCH}	Source differential launch amplitude		800		1200	mVpp
DR	Data rate	SN75LVPE3410	1		8	Gbps

6.4 Thermal Information

THERMAL METRIC[1]		SN75LVPE3410 RNQ, 40 Pins	UNIT
$R_{\theta JA-High K}$	Junction-to-ambient thermal resistance	31.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
I_{ACTIVE}	Device current consumption when all four channels are active	All four channels enabled with VOD = L2, PWDN1, 2 = L		150	200	mA
$I_{ACTIVE-HALF}$	Device current consumption when two channels are active	Two channels enabled with VOD = L2, PWDN1 or PWDN2 = L		85	112	mA
I_{STBY}	Device current consumption in standby power mode	All four channels disabled, PWDN1, 2 = H		22	33	mA
V_{REG}	Internal regulator output			2.5		V
Control IO						
V_{IH}	High level input voltage	SDA, SCL, PWDN1, PWDN2 pins	2.1			V
V_{IL}	Low level input voltage	SDA, SCL, PWDN1, PWDN2 pins			1.08	V
V_{OH}	High level output voltage	$R_{pull-up}$ = 100 kΩ (SDA, SCL pins)	2			V
V_{OL}	Low level output voltage	I_{OL} = –4 mA (SDA, SCL pins)			0.4	V
I_{IH}	Input high leakage current	V_{Input} = VDD, (SCL, SDA, PWDN1, PWDN2 pins)			10	µA
I_{IL}	Input low leakage current	V_{Input} = 0 V, (SCL, SDA, PWDN1, PWDN2 pins)	-10			µA
$C_{IN-CTRL}$	Input capacitance			1.5		pF
4 Level IOs (EQ0_ADDR0, EQ1_ADDR1, EN_SMB, RX_DET, VOD, GAIN pins)						
I_{IH_4L}	Input high leakage current, 4 level IOs	VIN = 2.5 V			10	µA
I_{IL_4L}	Input low leakage current, 4 level IOs	VIN = GND	-150			µA
Receiver						
Z_{RX-DC}	Rx DC Single-Ended Impedance			50		Ω
$Z_{RX-DIFF-DC}$	Rx DC Differential Impedance			100		Ω
Transmitter						
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	Impedance of Tx during active signaling, VID, diff = 1Vpp			120	Ω
$V_{TX-DC-CM}$	Tx DC common mode Voltage			0.75		V
$I_{TX-SHORT}$	Tx Short Circuit Current	Total current the Tx can supply when shorted to GND			90	mA

6.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss with minimal channel in TI evaluation board	50 MHz to 1.25 GHz		-22		dB
		1.25 GHz to 2.5 GHz		-19		dB
		2.5 GHz to 4.0 GHz		-17		dB
RL_{RX-CM}	Input common-mode return loss with minimal channel in TI evaluation board	50 MHz to 2.5 GHz		-18		dB
		2.5 GHz to 4.0 GHz		-13		dB
XT_{RX}	Receive-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent receiver pairs from 10 MHz to 4 GHz.		-50		dB
GAIN	CTLE block DC gain	Ratio at GAIN = L3 and GAIN = L2, with low frequency CK		3.0		dB
Transmitter						
VOD_{L0-L2}	Ratio of VOD gain L0 to L2	GAIN = L2, with low frequency CK		-6		dB
VOD_{L1-L2}	Ratio of VOD gain L1 to L2	GAIN = L2, with low frequency CK		-3.5		dB
VOD_{L3-L2}	Ration of VOD gain L3 to L2	GAIN = L2, with low frequency CK		-1.5		dB
$RL_{TX-DIFF}$	Output differential return loss with minimal channel in TI evaluation board	50 MHz to 1.25 GHz		-22		dB
		1.25 GHz to 2.5 GHz		-20		dB
		2.5 GHz to 4.0 GHz		-18		dB
RL_{TX-CM}	Output Common-mode return loss with minimal channel in TI evaluation board	50 MHz to 2.5 GHz		-13		dB
		2.5 GHz to 4.0 GHz		-15		dB
XT_{TX}	Transmit-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent transmitter pairs from 10 MHz to 4 GHz.		-50		dB
Device Datapath						
$T_{PLHD/PHLD}$	Input-to-output latency (propagation delay) through a channel	Measured by observing propagation delay during either Low-to-High or High-to-Low transition		70	90	ps
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	Measured between any two lanes within a single transmitter			20	ps
$EQGAIN_{4G}$	High-frequencyuency EQ boost at 4 GHz	Measured with maximum CTLE setting and maximum BW setting (EQ1 = L3, EQ0 = L3). Boost is defined as the gain at 4 GHz relative to 100 MHz.		12		dB
$DCGAIN_{VAR, max}$	Maximum AC/DC gain variation	VOD=L2, GAIN=L2, min EQ setting	-2.5		2.5	dB
LINEARITY	The output AC/DC linearity	VOD = L2.		800		mVpp

6.7 SMBUS/I^{2}C Timing Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Target Mode						
T_{SDA-HD}	Data hold time		0			ns
T_{SDA-SU}	Data setup time		100			ns
T_{SDA-R}	SDA rise time, read operation	Pull-up resistor = 1 kΩ, Cb = 50 pF		120		ns
T_{SDA-F}	SDA fall time, read operation	Pull-up resistor = 1 kΩ, Cb = 50 pF		10		ns

6.8 Typical Characteristics

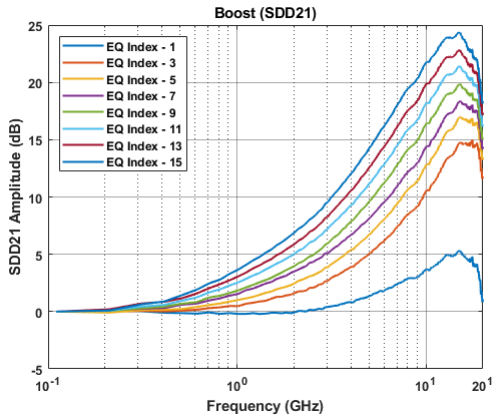


Figure 6-1. Typical EQ Boost vs Frequency for 8 (Out of Available 16) EQ Indices

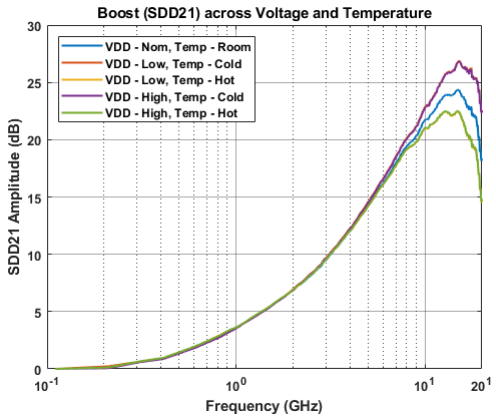


Figure 6-2. EQ Boost vs Frequency with EQ Index 15 (Maximum Setting) for Different Supply Voltage and Temperature Settings

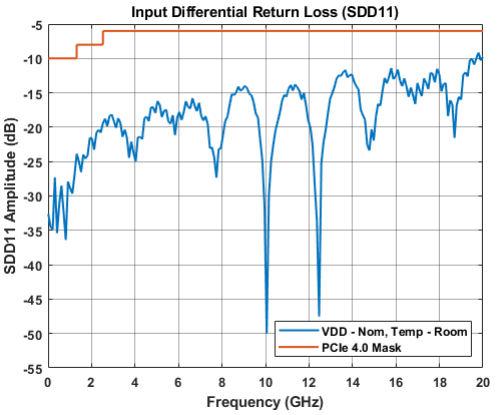


Figure 6-3. Typical Input (RX) Differential Return Loss vs Frequency in TI Evaluation Board with ≅2 dB input and ≅2 dB Output Loss

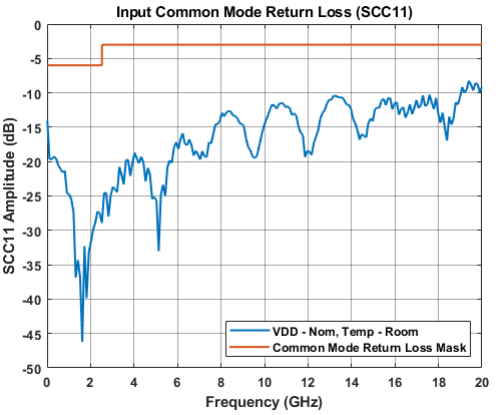


Figure 6-4. Typical Input (RX) Common Mode Return Loss vs Frequency in TI Evaluation Board with ≅2 dB Input and ≅2 dB Output Loss

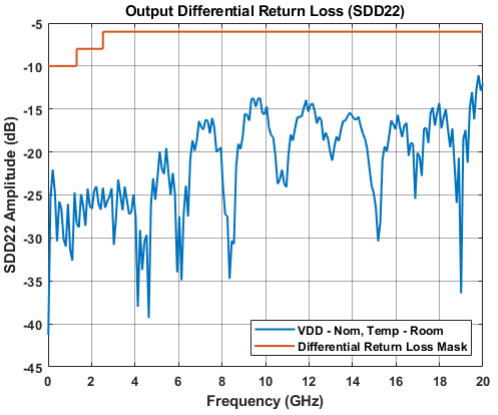


Figure 6-5. Typical Output (TX) Differential Return Loss vs Frequency in TI Evaluation Board with ≅2 dB Input and ≅2 dB Output Loss

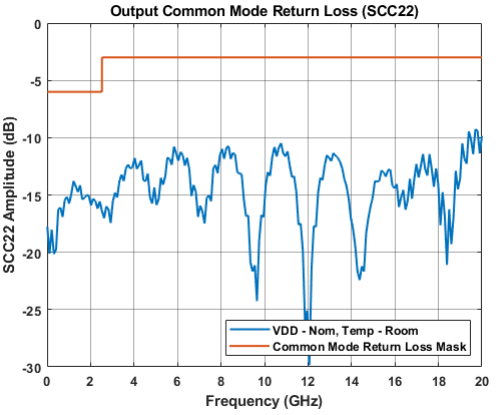


Figure 6-6. Typical Output (TX) Common Mode Return Loss vs Frequency in TI Evaluation Board with ≅2 dB Input and ≅2 dB Output Loss

7 Detailed Description

7.1 Overview

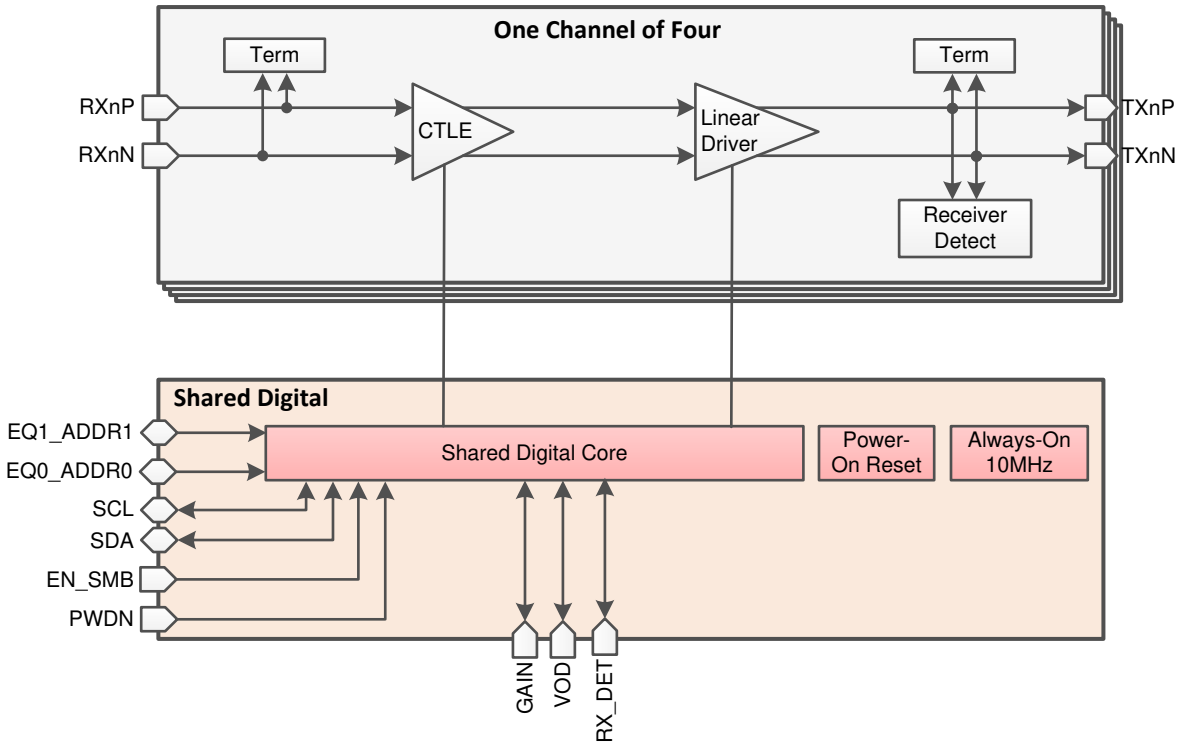
The SN75LVPE3410 is a four-channel multi-rate linear repeater with integrated signal conditioning. The four channels operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective.

The SN75LVPE3410 can be configured two different ways:

Pin Mode – device control configuration is done solely by strap pins. Pin mode is expected to be good enough for many system implementation needs.

SMBus/I^{2}C Target Mode - provides most flexibility. Requires a SMBus/I^{2}C controller device to configure SN75LVPE3410 through writing to its target address.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Linear Equalization

The SN75LVPE3410 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. Table 7-1 shows available equalization boost through EQ0_ADDR0 and EQ1_ADDR1 control pins, when in Pin Control mode (EN_SMB = L0).

Table 7-1. Equalization Control Settings

EQUALIZATION SETTING			TYPICAL EQ BOOST
INDEX	EQ1_ADDR1	EQ0_ADDR0	at 4 GHz
0	L0	L0	–0.3
1	L0	L1	0.4
2	L0	L2	3.3
3	L0	L3	3.8
4	L1	L0	4.9
5	L1	L1	5.2
6	L1	L2	5.4
7	L1	L3	6.5
8	L2	L0	6.7
9	L2	L1	7.7
10	L2	L2	8.7
11	L2	L3	9.1
12	L3	L0	9.4
13	L3	L1	10.3
14	L3	L2	10.6
15	L3	L3	11.8

The equalization of the device can also be set by writing to SMBus/I^2C registers in target mode.

7.3.2 DC Gain

The VOD or GAIN pins can be used to set the overall data-path DC (low frequency) gain of the SN75LVPE3410. For more information, see the *Pin Configuration and Functions* section.

Table 7-2 provides how DC gain of the overall data-paths can be set using GAIN and VOD pins, when in Pin Control mode (EN_SMB = L0).

Table 7-2. DC Gain Settings

Desired DC Gain (dB)	GAIN	VOD
+3.5	L3	L2
0	L2	L2
-1.5	L2	L3
-3.5	L2	L1
-6	L2	L0

It is advised that the DC gain and equalization of the SN75LVPE3410 are set so that the signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively. For most PCIe systems the default DC gain setting 0 dB (GAIN and VOD pins floating) would be sufficient. A DC attenuation, however, can be utilized to apply extra equalization when needed, keeping the data-path linear.

7.3.3 Receiver Detect State Machine

The SN75LVPE3410 deploys an RX detect state machine that governs the RX detection cycle as defined in the PCI express specifications. At power up, after a manually triggered event through PWDN1 and PWDN2 pins (in pin mode), or writing to the relevant I^2C / SMBus register, the redriver determines whether or not a valid PCI express termination is present at the far end of the link. The RX_DET pin of SN75LVPE3410 provides additional flexibility for system designers to appropriately set the device in the desired mode as provided in Table 7-3.

If all four channels of SN75LVPE3410 are used for same PCI express link, the PRWDN1 and PWDN2 pin can be shorted and driven together in a system (for example, by PCIE connector PRSNTx# or fundamental reset PERST# signal).

Table 7-3. Receiver Detect State Machine Settings

PWDN1 and PWDN2	RXDET	COMMENTS
L	L0	PCI Express RX detection state machine is enabled. RX detection is asserted after 2x valid detections. Pre Detect: Hi-Z, Post Detect: 50 Ω.
L	L1	PCI Express RX detection state machine is enabled. RX detection is asserted after 3x valid detections. Pre Detect: Hi-Z, Post Detect: 50 Ω.
L	L2 (Float)	PCI Express RX detection state machine is enabled. RX detection is asserted after 1x valid detection. Pre Detect: Hi-Z, Post Detect: 50 Ω.
L	L3	PCI Express RX detection state machine is disabled. Recommended for non PCI Express interface use case where the SN75LVPE3410 is used as buffer with equalization. Always 50 Ω.
H	X	Manual reset, input is high impedance.

7.4 Device Functional Modes

7.4.1 Active PCIe Mode

The device is in normal operation with PCIe state machine enabled by RX_DET = L0/L1/L2. In this mode PWDN1/PWDN2 pins are driven low in a system (for example, by PCIE connector PRSNTx# or fundamental reset PERST# signal). In this mode, the SN75LVPE3410 redrivers and equalizes PCIe RX or TX signals to provide better signal integrity.

7.4.2 Active Buffer Mode

The device is in normal operation with PCIe state machine disabled by RX_DET = L3. This mode is recommended for non-PCIe use cases. In this mode the device is working as a buffer to provide linear equalization to improve signal integrity.

7.4.3 Standby Mode

The device is in standby mode invoked by PWDN1/PWDN2 = H. In this mode, the device is in standby mode conserving power.

7.5 Programming

7.5.1 Control and Configuration Interface

7.5.1.1 Pin Mode

The SN75LVPE3410 can be fully configured through GPIO/Pin-strap pins. In this mode the device uses 2-level and 4-level pins for device control and signal integrity optimum settings. For contol pin definitions, see *Pin Configuration and Functions*.

7.5.1.1.1 Four-Level Control Inputs

The SN75LVPE3410 has six (GAIN, VOD, EQ1_ADDR1, EQ0_ADDR0, EN_SMB, and RX_DET) 4-level inputs pins that are used to control the device. These 4-level inputs use a resistor divider to help set the four levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better.

Table 7-4. 4-Level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	F (Float)
L3	59 kΩ to GND

7.5.1.2 SMBUS/I²C Register Control Interface

If EN_SMB = L3 (SMBus / I²C control mode), the SN75LVPE3410 is configured through a standard I²C or SMBus interface that may operate up to 400 kHz. The target address of the SN75LVPE3410 is determined by the pin strap settings on the EQ1_ADDR1 and EQ0_ADDR0 pins. The device can be configured for best signal integrity and power settings in the system using the I²C or SMBus interface. The sixteen possible target addresses (8-bit) for the SN75LVPE3410 are provided in Table 7-5.

Table 7-5. SMBUS/I²C Target Address Settings

EQ1_ADDR1 PIN LEVEL	EQ0_ADDR0 PIN LEVEL	8-BIT WRITE ADDRESS (HEX)	7-BIT ADDRESS (HEX)
L0	L0	0x30	0x18
L0	L1	0x32	0x19
L0	L2	0x34	0x1A
L0	L3	0x36	0x1B
L1	L0	0x38	0x1C
L1	L1	0x3A	0x1D
L1	L2	0x3C	0x1E
L1	L3	0x3E	0x1F
L2	L0	0x40	0x20
L2	L1	0x42	0x21
L2	L2	0x44	0x22
L2	L3	0x46	0x23
L3	L0	0x48	0x24
L3	L1	0x4A	0x25
L3	L2	0x4C	0x26
L3	L3	0x4E	0x27

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN75LVPE3410 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

8.2 Typical Applications

The SN75LVPE3410 is a PCI Express linear redriver that can also be configured as interface agnostic redriver by disabling its RX detect feature. The device can be used in wide range of interfaces including PCI Express, SAS and SATA.

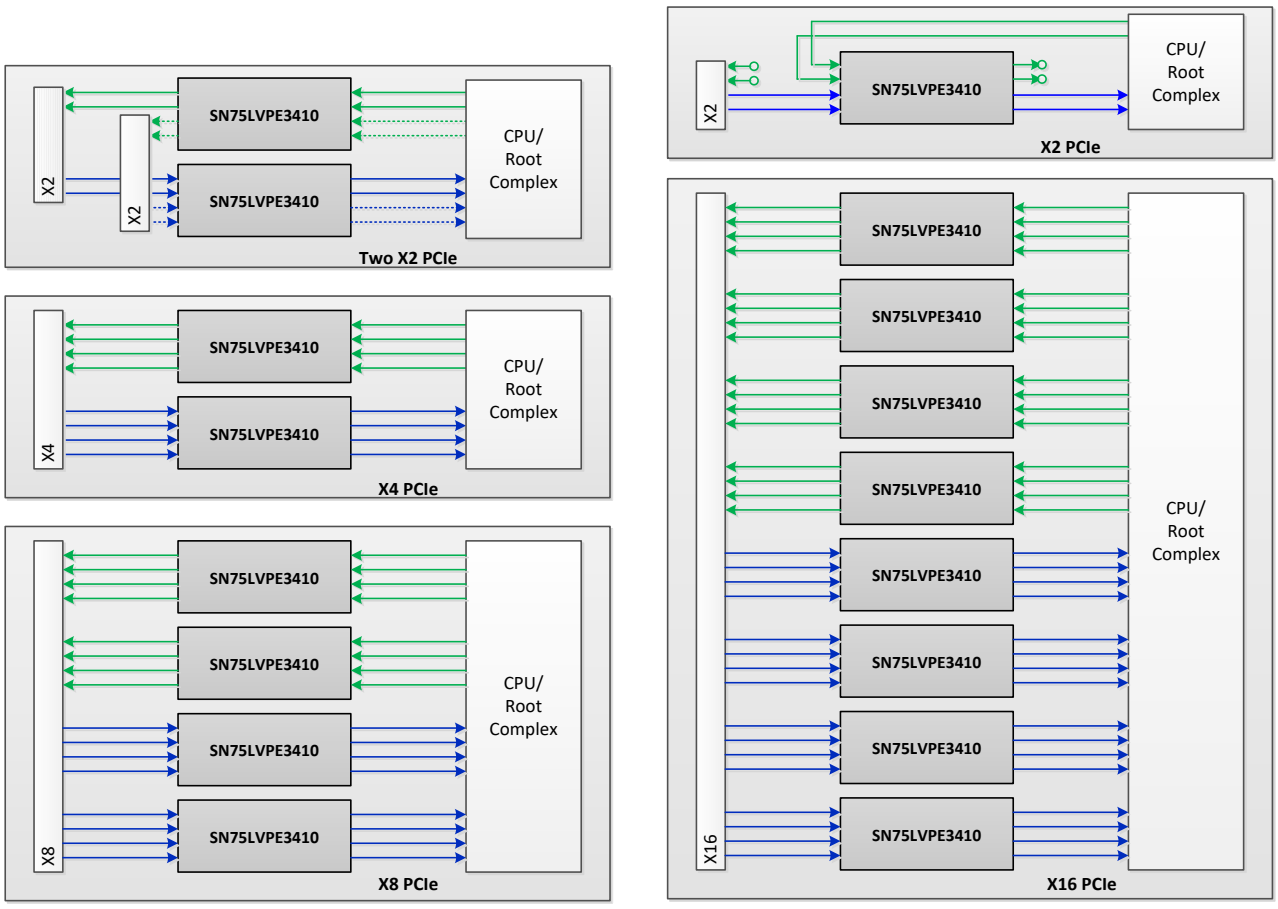


Figure 8-1. PCI Express x2, x4, x8, and x16 Use Cases Using SN75LVPE3410

The SN75LVPE3410 is a protocol agnostic 4-channel linear redriver with PCI Express receiver-detect capability. Its protocol agnostic nature allows it to be used in PCI Express x2, x4, x8, and x16 applications. Figure 8-1 shows how a number of SN75LVPE3410 devices can be used to obtain signal conditioning for PCI Express buses of varying widths. Note all four channels of the SN75LVPE3410 flow in same direction. Therefore, if the device is used for x2 configuration, careful layout consideration is needed. In x2 configuration, the two-channel grouping can be used for PCIe receiver detect. PWDN1 pin puts channels 1 and 2, and PWDN2 pin puts channels 3 and 4 into standby.

8.2.1 PCIe x4 Lane Configuration

The SN75LVPE3410 can be used in server or motherboard applications to boost transmit and receive signals to increase the reach of the host or root complex processor to PCI Express slots or connectors. The following design recommendations can be used in any lane configuration. Figure 8-2 shows a simplified schematic for x4 configuration.

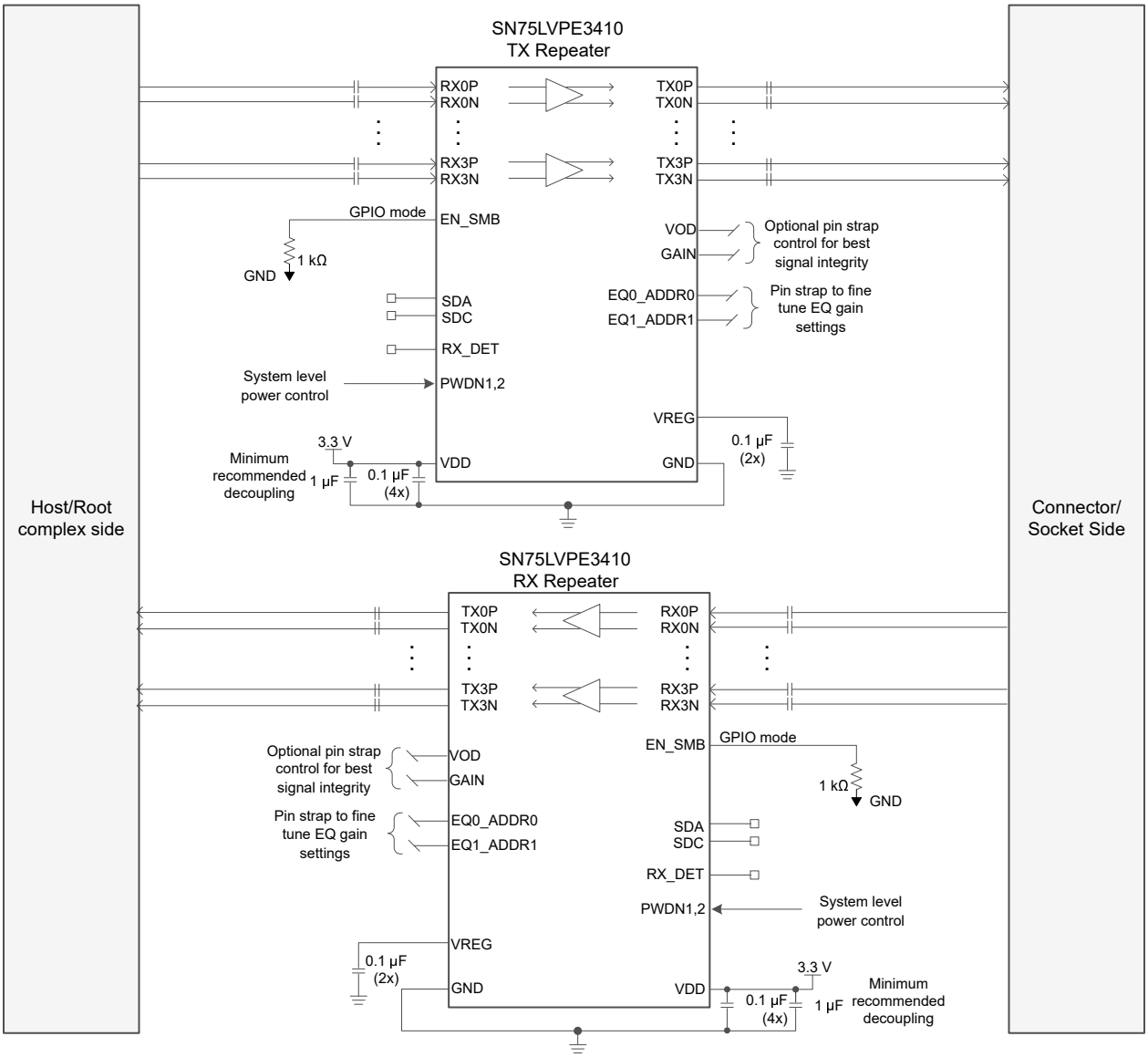


Figure 8-2. Simplified Schematic for PCIe x4 Lane Configuration

8.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Use 85 Ω impedance traces when interfacing with PCIe CEM connectors. Length matching on the P and N traces should be done on the single-ended segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- AC-coupling capacitors of 220 nF are recommended, set the maximum body size to 0402, and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

8.2.1.2 Detailed Design Procedure

In PCIe Gen 3.0 applications, the specification requires Rx-Tx link training to establish and optimize signal conditioning settings at 8 Gbps, respectively. In link training, the Rx partner requests a series of FIR – pre-shoot and de-emphasis coefficients (10 Presets) from the Tx partner. The Rx partner includes 7-levels (6 dB to 12 dB) of CTLE followed by a single tap DFE. The link training would pre-condition the signal, with an equalized link between the root-complex and endpoint.

Note that there is no link training in PCIe Gen 1.0 (2.5 Gbps) or PCIe Gen 2.0 (5.0 Gbps) applications. The SN75LVPE3410 is placed in between the Tx and Rx. It helps extend the PCB trace reach distance by boosting the attenuated signals with its equalization, which allows the user to recover the signal by the downstream Rx more easily.

For operation in Gen 3.0 links, the SN75LVPE3410 transmit outputs are designed to pass the Tx Preset signaling onto the Rx for the PCIe Gen 3.0 link to train and optimize the equalization settings. The suggested setting for the SN75LVPE3410 are VOD = 0 dB and DC GAIN = 0 dB. Adjustments to the EQ setting should be performed based on the channel loss to optimize the eye opening in the Rx partner. The available EQ gain settings are provided in Table 7-1.

The Tx equalization presets or CTLE and DFE coefficients in the Rx can also be adjusted to further improve the eye opening.

Figure 8-3 shows an example for SN75LVPE3410 Typical Connection Schematic.

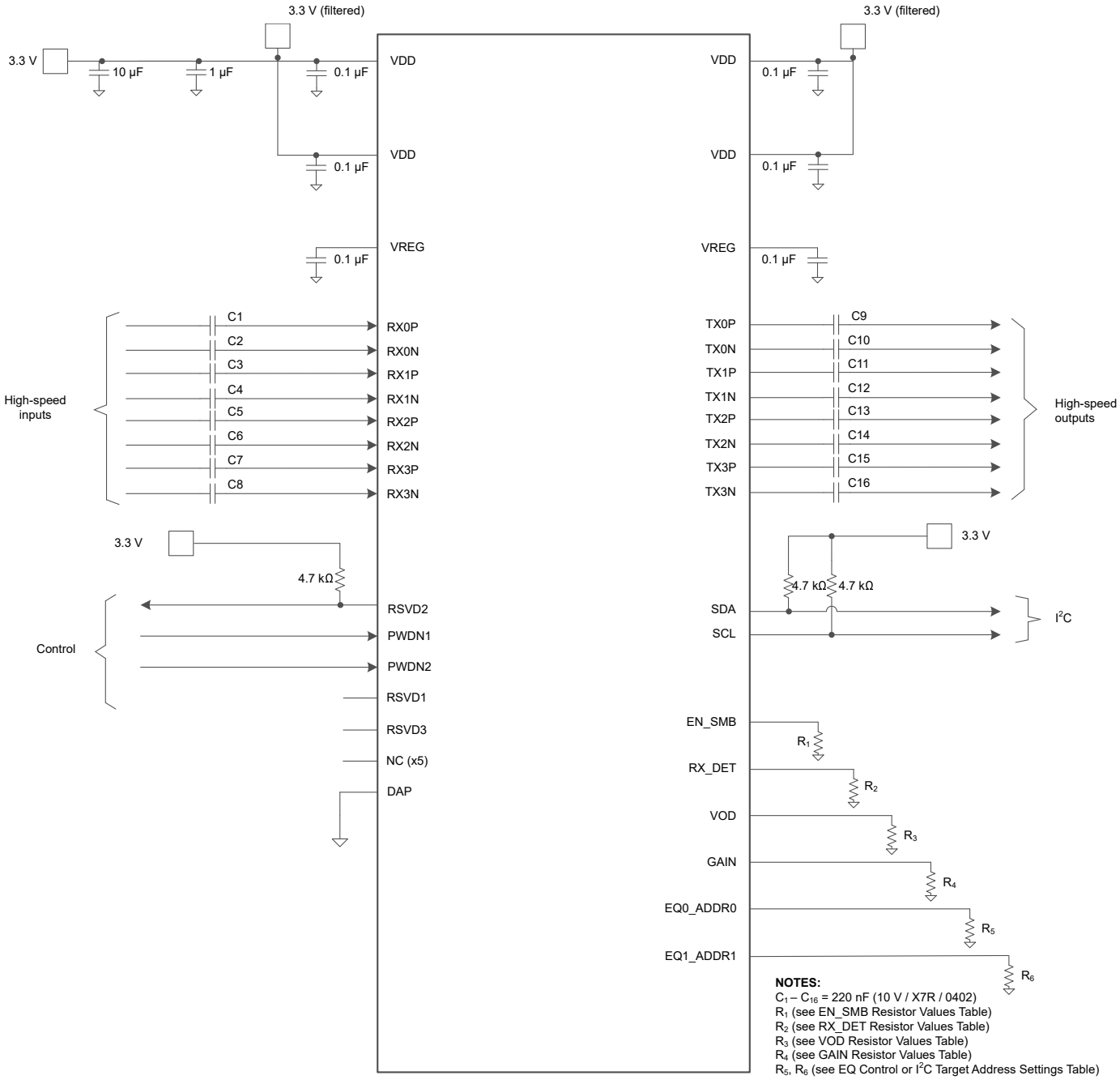


Figure 8-3. SN75LVPE3410 Typical Connection Schematic

8.2.1.3 Application Curves

The SN75LVPE3410 is a linear redriver that can be used to extend channel reach of a PCIe link. Normally, PCIe-compliant TX and RX are equipped with signal-conditioning functions and can handle channel losses of up to 22 dB at 4 GHz. With the SN75LVPE3410, the total channel loss between a PCIe root complex and an end point can be up to 32 dB at 4 GHz.

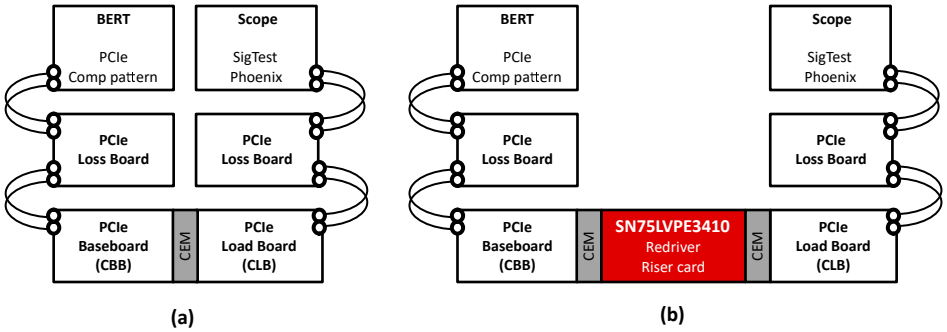


Figure 8-4. Test Setup to Demonstrate PCIe 3.0 Link Reach Extension Using SN75LVPE3410 - (a) Baseline Setup, (b) With Redriver

Figure 8-4 shows a test setup to demonstrate reach extension capability of SN75LVPE3410 as PCIe 3.0 redriver. Table 8-1 provides the test results. As can be seen SN75LVPE3410 provide reach extension such a way that a PCIe 3.0 link with 34 dB total loss passes sigtest compliance requirements. Figure 8-5 shows eye diagram from PCIe 3.0 sigtest tool.

Table 8-1. PCIe 3.0 Link Reach Extension Using SN75LVPE3410

Setup	Total Link Loss	Minimum Eye Width	Composite Eye Height	PCIe 3.0 Sigtest Result
Baseline setup - no redriver	22 dB	62 ps	88 mV	Pass
Link with redriver	34 dB	37 ps	141 mV	Pass

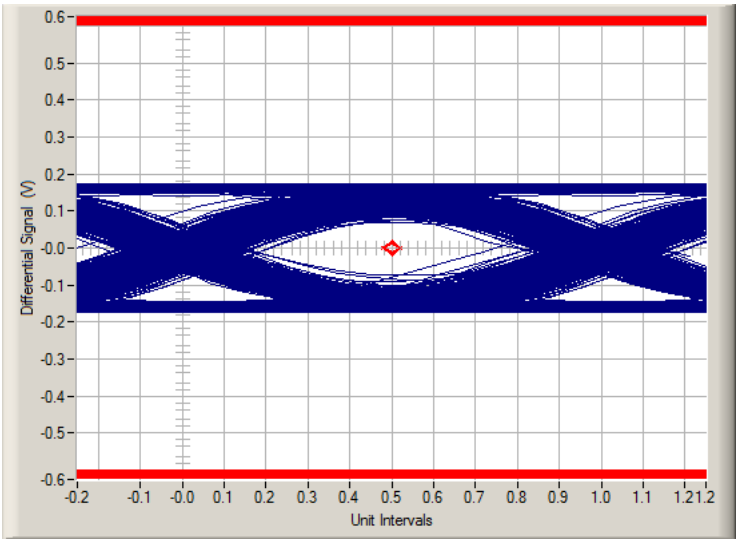


Figure 8-5. PCIe 3.0 Sigtest Eye Diagram with 34 dB Total Loss Using SN75LVPE3410

8.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the *Recommended Operating Conditions* for DC voltage, AC noise, and start-up ramp time.
2. The SN75LVPE3410 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1 µF capacitor per VDD pin, one 1.0 µF bulk capacitor per device, and one 10 µF bulk capacitor per power bus that delivers power to one or more SN75LVPE3410 devices. The local decoupling (0.1 µF) capacitors must be connected as close to the VDD pins as possible and with minimal path to the SN75LVPE3410 ground pad.

8.4 Layout

8.4.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VDD pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most/all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

8.4.2 Layout Example

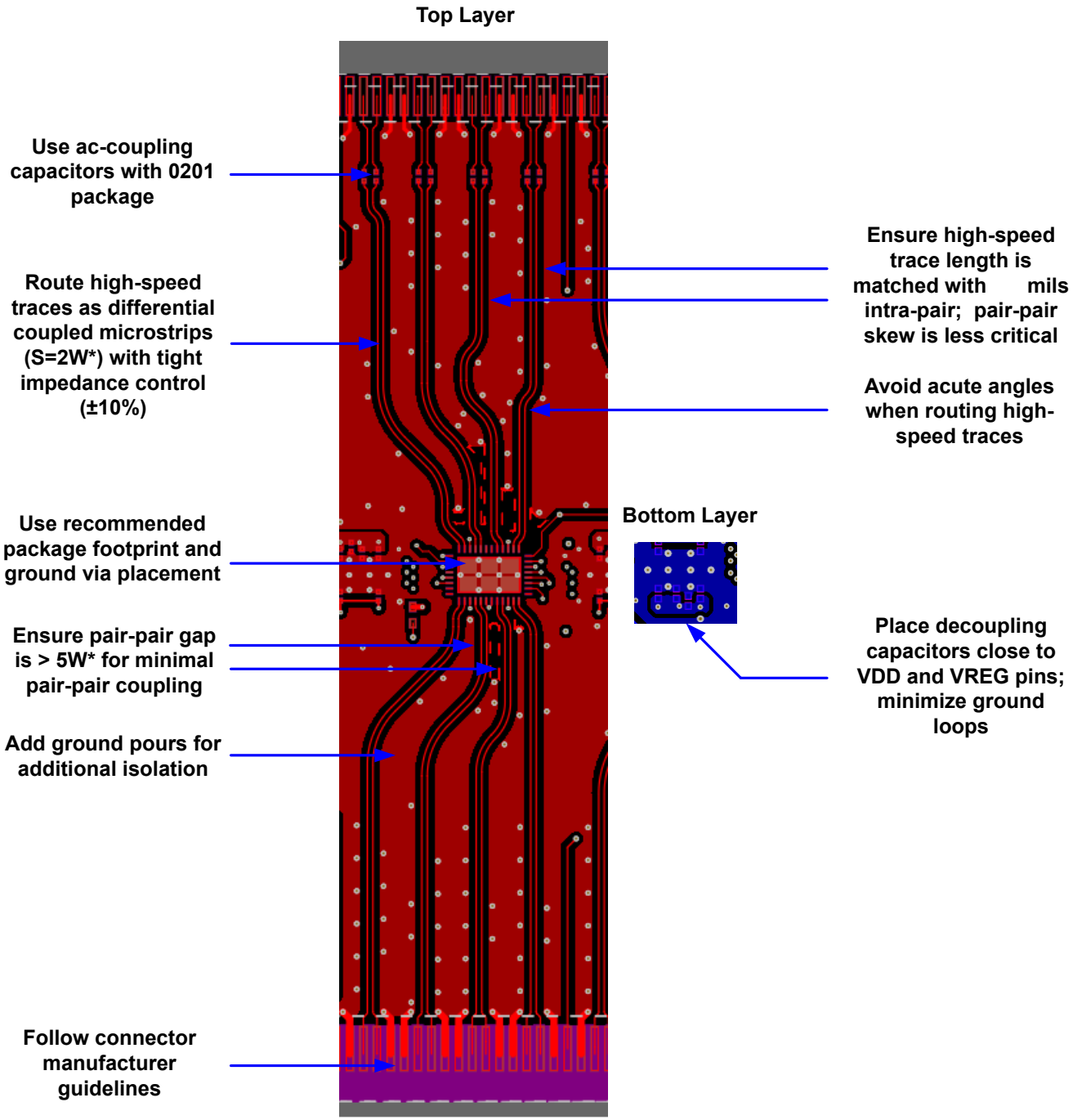


Figure 8-6. SN75LVPE3410 Layout Example - Sub-Section of a PCIe Riser Card With CEM Connectors

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DS160PR410 Programming Guide* user's guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVPE3410RNQR	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	PX410
SN75LVPE3410RNQR.A	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	PX410
SN75LVPE3410RNQR.B	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	PX410
SN75LVPE3410RNQT	Active	Production	WQFN (RNQ) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	PX410
SN75LVPE3410RNQT.A	Active	Production	WQFN (RNQ) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	PX410
SN75LVPE3410RNQT.B	Active	Production	WQFN (RNQ) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	PX410

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

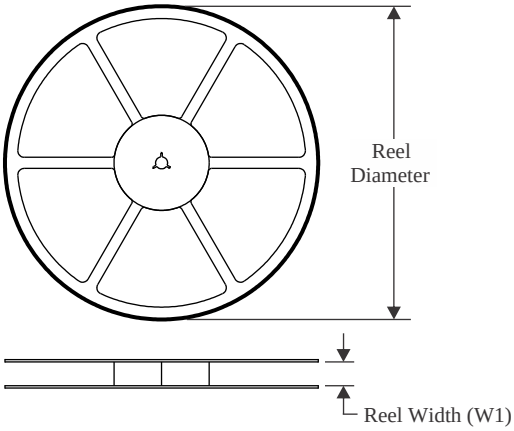
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

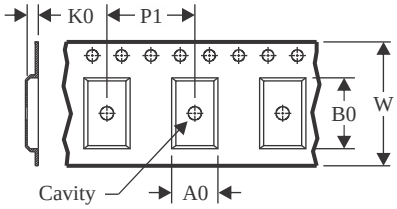
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

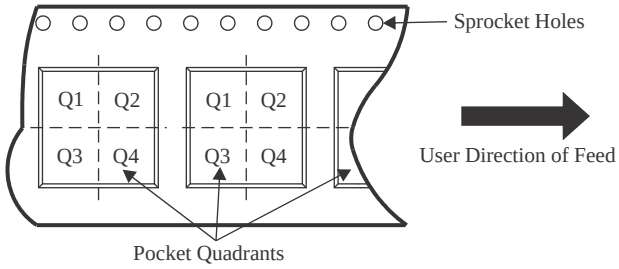


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

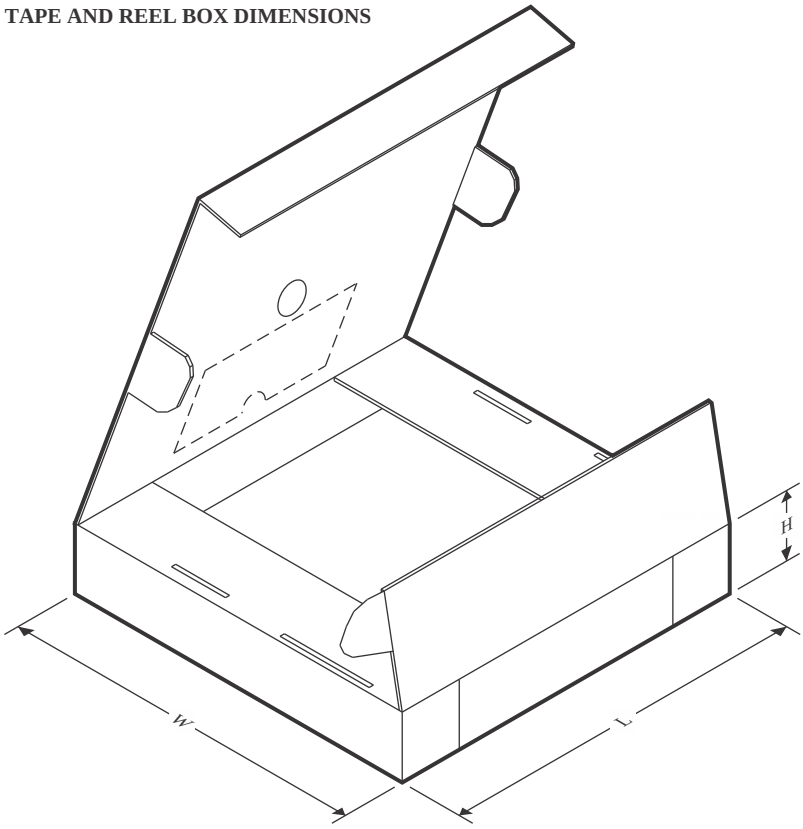
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVPE3410RNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
SN75LVPE3410RNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

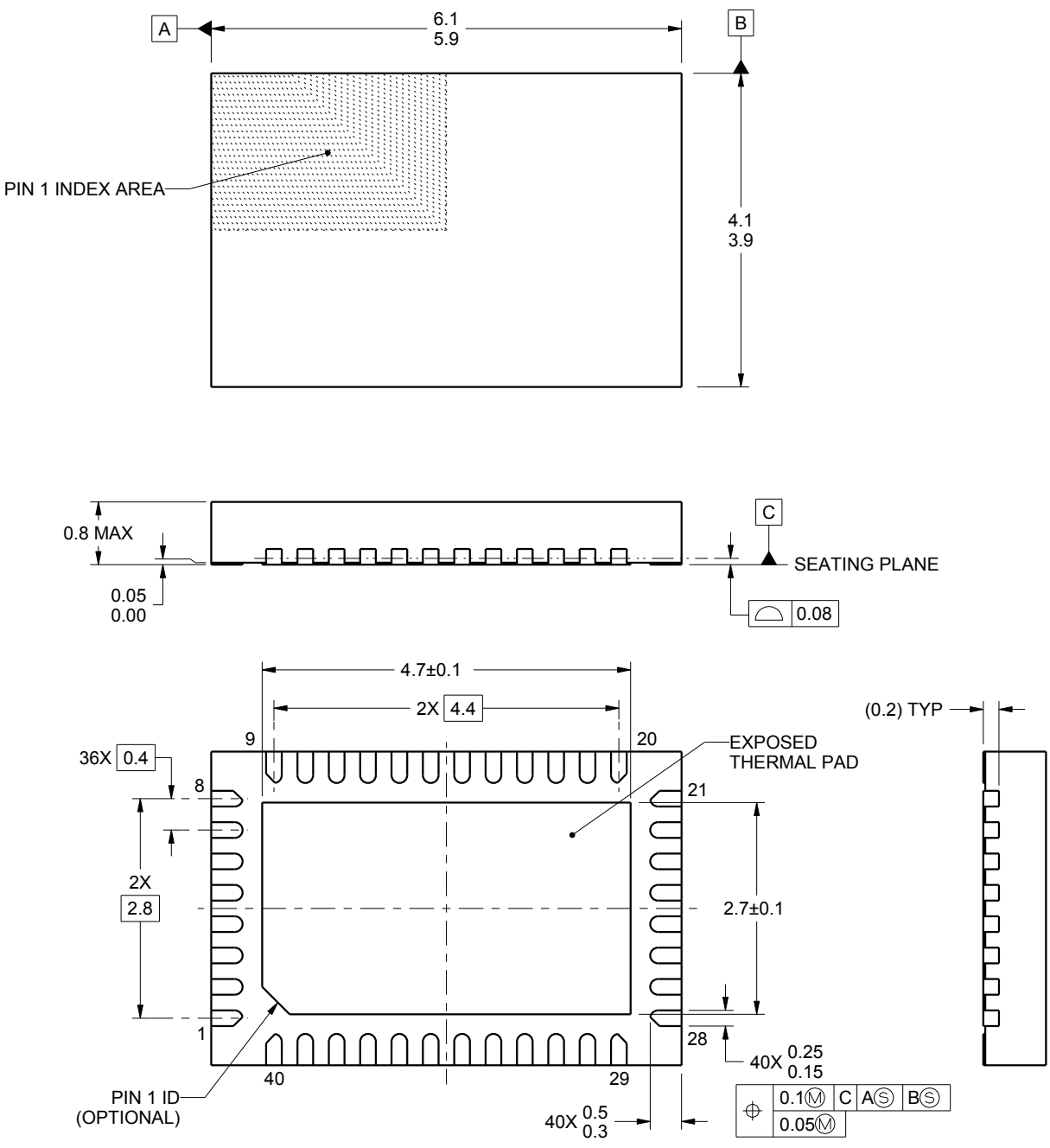
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVPE3410RNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
SN75LVPE3410RNQT	WQFN	RNQ	40	250	210.0	185.0	35.0

PACKAGE OUTLINE

RNQ0040A

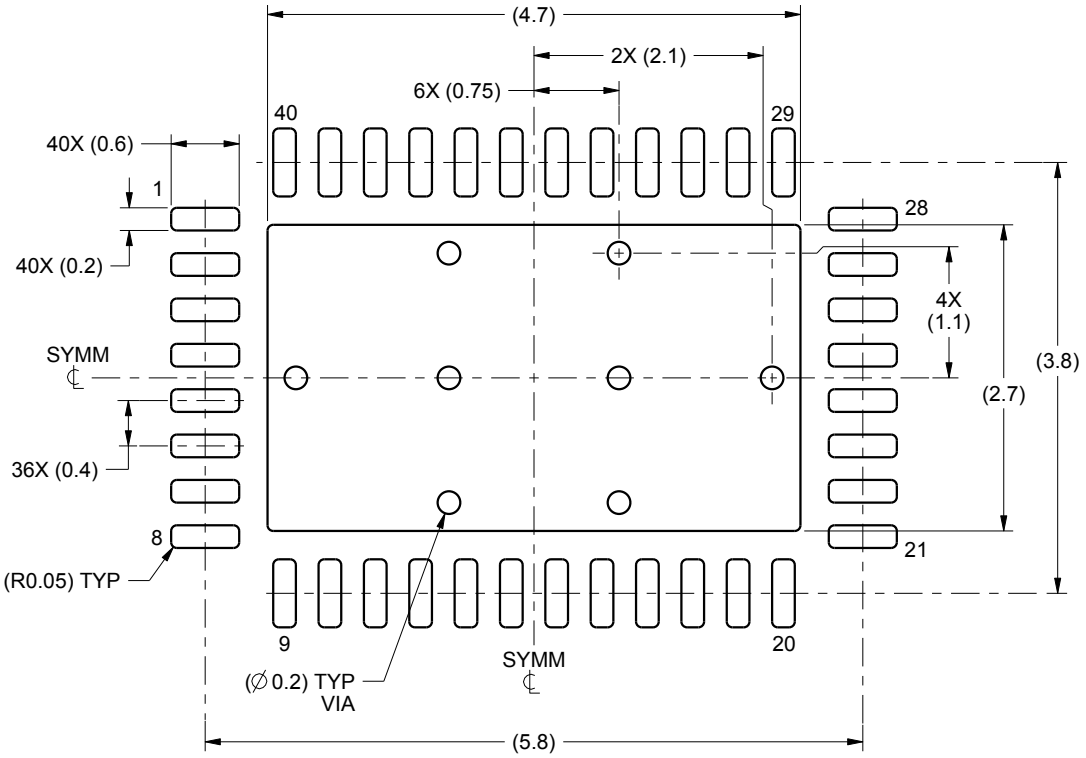
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

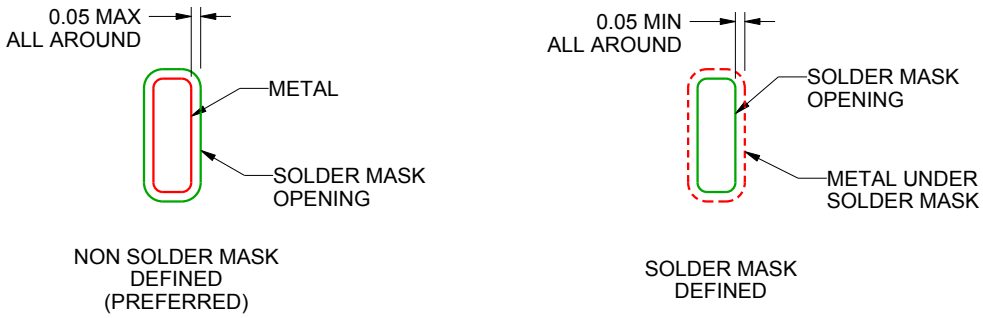


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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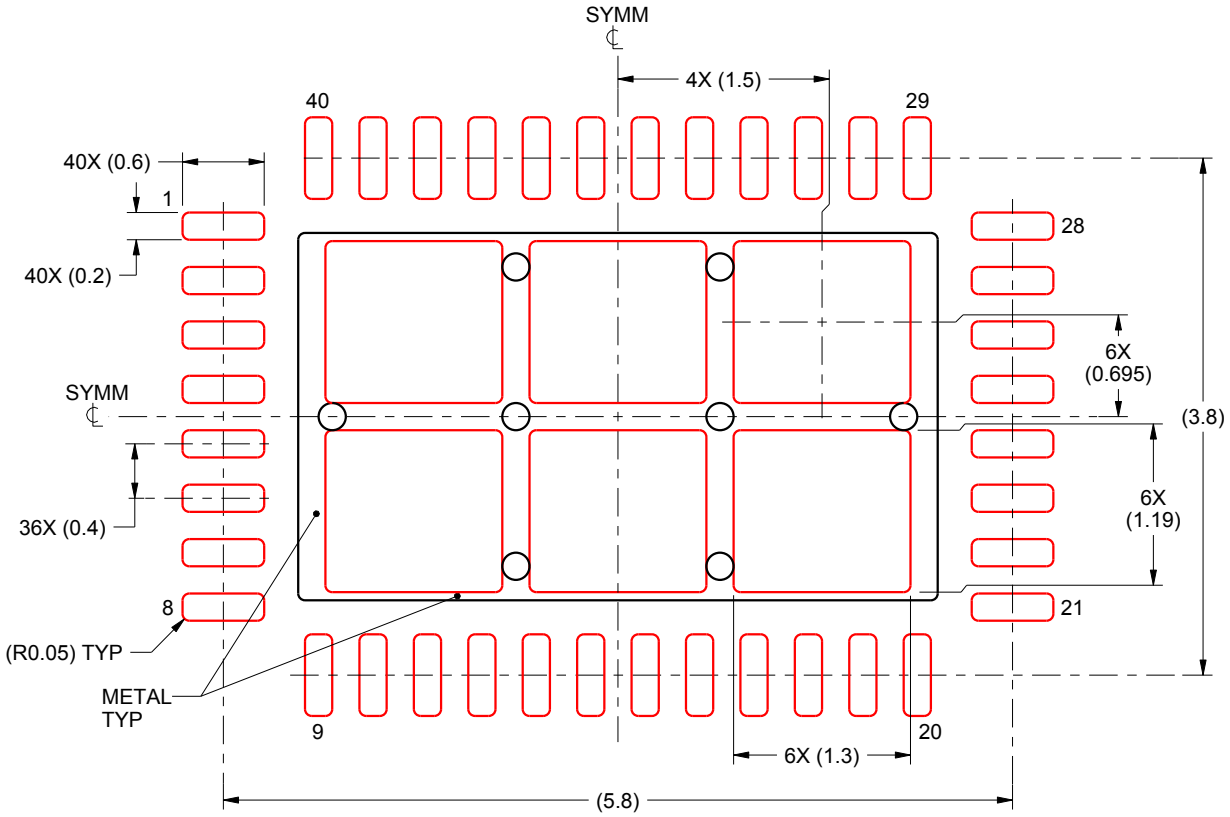
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222125/B 01/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025