SN75LVPE3101 Dual-Channel PCI Express 3.0 Linear Redriver

1 Features

- Supports PCI Express 3.0, SATA Express, and SATA Gen3
- Ultra low-power architecture:
  - Active: < 330mW
  - Shutdown: < 700µW
- 16 settings for up to 14dB at 4GHz of linear equalization
- Hot-plug capable
- Temperature range: –40°C to 85°C (industrial)
- ESD HBM rating: ±5kV
- Available in single 3.3V supply
- Available in 4mm × 4mm VQFN

2 Applications

- Desktop PC or motherboard
- Notebook PCs
- Data storage
- Industrial computer on module

3 Description

The SN75LVPE3101 is a dual-channel PCI Express (PCIe) 3.0 x1 redriver. The device offers low power consumption on a 3.3V supply and is designed to support PCIe 1.0, 2.0, and 3.0 data rates.

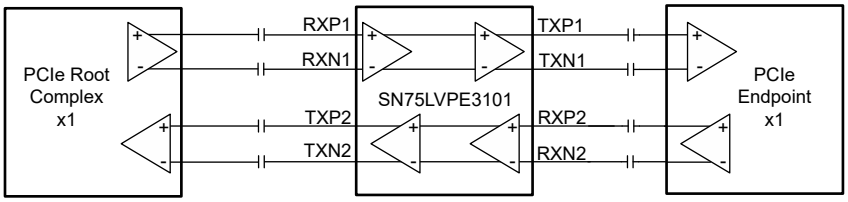
The SN75LVPE3101 implements a linear equalizer, supporting up to 14dB of loss due to inter-symbol interference (ISI). When PCIe signals travel across a printed circuit board (PCB) or cable, signal integrity degrades due to loss and inter-symbol interference. The linear equalizer compensates for the channel loss, and thereby, extends the channel length and enables systems to pass PCIe compliance. The dual channel implementation and small package size provides flexibility in the placement of the SN75LVPE3101 in the PCIe 3.0 data path.

The SN75LVPE3101 is available in a 24-pin 4mm × 4mm VQFN.

Device Information

PART NUMBER(1)	TEMPERATURE	PACKAGE
SN75LVPE3101	T_A = –40°C to 85°C	RGE (VQFN, 24)

(1) For all available packages, see Section 10.



Simplified Schematic

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4 Pin Configuration and Functions

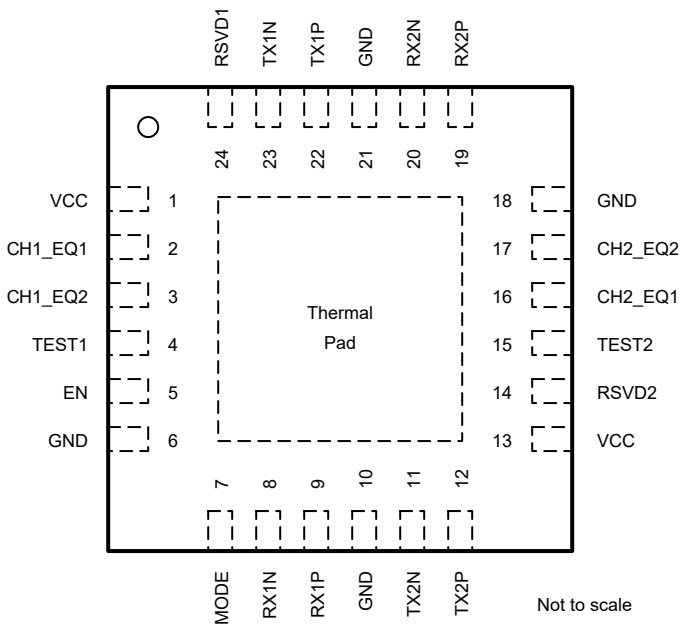

Figure 4-1. RGE Package 24-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE	INTERNAL PULLUP PULLDOWN	DESCRIPTION
NAME	NO.			
CH1_EQ1	2	I (4-level)	PU (approx 45K) PD (approx 95K)	CH1_EQ1. Configuration pin used to control RX EQ level for RX1P/N. The state of this pin is sampled after the rising edge of EN. Refer to Figure 5-1 for details of timing. This pin along with CH1_EQ2 allows for up to 16 equalization settings.
CH1_EQ2	3	I (4-level)		CH1_EQ2. Configuration pin used to control RX EQ level for RX1P/N. The state of this pin is sampled after the rising edge of EN. Refer to Figure 5-1 for details of timing. This pin along with CH1_EQ1 allows for up to 16 equalization settings.
CH2_EQ1	16	I (4-level)		CH2_EQ1. Configuration pin used to control RX EQ level for RX2P/N. The state of this pin is sampled after the rising edge of EN. Refer to Figure 5-1 for details of timing. This pin along with CH2_EQ2 allows for up to 16 equalization settings.
CH2_EQ2	17	I (4-level)		CH2_EQ2. Configuration pin used to control RX EQ level for RX2P/N. The state of this pin is sampled after the rising edge of EN. Refer to Figure 5-1 for details of timing. This pin along with CH2_EQ1 allows for up to 16 equalization settings.
EN	5	I (2-level)	PU (approx 400K)	EN. Places SN75LVPE3101 into shutdown mode when asserted low. Normal operation when pin is asserted high. When in shutdown, the receiver terminations of the device are high impedance and the TX/RX channels are disabled.
GND	6, 10, 18, 21	GND	—	Ground
MODE	7	I	PU (approx 45 K) PD (approx 95K)	MODE. The state of this pin is sampled after the rising edge of EN. Connect to GND through 20kΩ resistor.
RSVD1	24	O	—	RSVD1. Leave the pin unconnected.
RSVD2	14	I	PU (approx 400K)	RSVD2. Leave the pin unconnected.
RX1N	8	90Ω Differential Input	—	Inverting differential high-speed input for Channel 1
RX1P	9			Noninverting differential high-speed input for Channel 1
RX2N	20	90Ω Differential Input	—	Inverting differential high-speed input for Channel 2
RX2P	19			Noninverting differential high-speed input for Channel 2
TEST1	4	I	PU (approx 45K) PD (approx 95K)	TEST1. Must connect to GND directly or through 1kΩ resistor.

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Table 4-1. Pin Functions (continued)

PIN		TYPE	INTERNAL PULLUP PULLDOWN	DESCRIPTION
NAME	NO.			
TEST2	15	I	PU (approx 45K) PD (approx 95K)	TEST2. Must connect to GND directly or through 1kΩ resistor.
TX1N	23	90Ω Differential Output	—	Inverting differential high-speed output for Channel 1
TX1P	22			Noninverting differential high-speed output for Channel 1
TX2N	11	90Ω Differential Output	—	Inverting differential high-speed output for Channel 2
TX2P	12			Noninverting differential high-speed output for Channel 2
VCC	1, 13	Power	—	3.3V (±10%) supply
Thermal pad			—	Thermal pad. Recommend connecting to a solid ground plane.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage Range	–0.3	4	V
V_{IO}	Differential voltage for RX1P/N and RX2P/N	–2.5	2.5	V
	Voltage at RX pins	–0.5	4	V
	Voltage on control pins	–0.5	4	V
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±5000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{PSN}	Supply noise on V_{CC} pins			100	mV
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		105	°C

5.4 Thermal Information

THERMAL METRIC(1)		SN75LVPE3101 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
P_{ACTIVE_1200mV}	Device power consumption when all channels are active	All channels enabled , V_{CC} = 3.3V; EN = 1;		330		mW
$P_{SHUTDOWN}$	Shutdown power when EN = 0.	VCC = 3.3V; EN = 0		0.7		mW
4-level Inputs (TEST[2:1], MODE, CH1_EQ[2:1], CH2_EQ[2:1])						
V_{TH}	Threshold "0" / "R"	V_{CC} = 3.3V		0.55		V
	Threshold "R" / "F"	V_{CC} = 3.3V		1.65		V
	Threshold "F" / "1"	V_{CC} = 3.3V		2.8		V
I_{IH}	High-level input current	V_{CC} = 3.6V; V_{IN} = 3.6V	20		80	µA
I_{IL}	Low-level input current	V_{CC} = 3.6V; V_{IN} = 0V	–160		–40	µA
R_{PU}	Internal pullup resistance			45		kΩ
R_{PD}	Internal pulldown resistance			95		kΩ
EN, RSVD2						
V_{IH}	High-level input voltage	V_{CC} = 3.3V	1.7		3.6	V
V_{IL}	Low-level input voltage	V_{CC} = 3.3V	0		0.7	V
I_{IH}	High-level input current	V_{CC} = 3.6V; V_{IN} = 3.6V	–10		10	µA
I_{IL}	Low-level input current	V_{CC} = 3.6V; V_{IN} = 0V	–15		15	µA
R_{PU_EN}	Internal pullup resistance for EN and RSVD2			400		kΩ
High-Speed Receiver Interface (RX1P/N and RX2P/N)						
$R_{L\_100\ MHz}$	RX Differential return loss at 100MHz to 2.5GHz	SDD11, 100MHz to 2.5GHz		–18		dB
$R_{L\_5\ GHz}$	RX Differential return loss at 5GHz	SDD11, 5GHz		–14		dB
$R_{L\_10\ GHz}$	RX Differential return loss from 5GHz to 10GHz	SDD11, 5GHz to 10GHz		–6		dB
R_{L_CM}	RX common-mode return loss	SCC11, 0.5GHz to 5GHz		–12		dB
X-Talk	Differential crosstalk between TX and RX signal pairs			–50		dB
$E_{ACGAIN\_4\ GHz}$	Maximum AC equalization gain	50mVpp CP10 at 4GHz; V_{CC} = 3.3V		14		dB
$E_{ACGAIN\_5\ GHz}$	Maximum AC equalization gain	50mVpp CP10 at 5GHz; V_{CC} = 3.3V		16		dB
E_{DC_GAIN0}	DC gain at 0dB setting	200mVpp VID at 100MHz		0.7		dB
V_{DIFF_IN}	Input differential peak-peak voltage swing range			1200		mV
$V_{RX\text{-}DC\text{-}CM}$	RX DC common-mode voltage			0		V
$R_{RX\text{-}DC\text{-}CM}$	RX DC common-mode impedance	Measured at connector; Present when far-end termination is detected on TXP/N	18		30	Ω
$R_{RX\text{-}DC\text{-}DIFF}$	RX DC differential impedance	Measured at connector; Present when far-end termination is detected on TXP/N	72		120	Ω
$Z_{RX\text{-}DC\text{-}DIFF}$	DC Input CM Input Impedance V > 0 during RESET or power down.	1. RX DC CM Impedance with RX terminations not powered. 2. Measured over the range 0mV to 500mV with respect to GND. 3. Only DC input CM Input impedance V > 0 is specified.	35			kΩ
$V_{RX\text{-}SIGNAL\text{-}DET}$	Input differential peak-to-peak signal detect assert level	At 10Gbps; No loss input channel and PRBS7 pattern.		85		mV
$V_{RX\text{-}IDLE\text{-}DET}$	Input differential peak-to-peak signal detect deassert level	At 10Gbps; No loss input channel and PRBS7 pattern.		60		mV

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over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RX-CM-AC-P}$	Peak RX AC common-mode voltage	Measured at package pin.			150	mV
High-Speed Transmitter Interface (TX1P/N and TX2P/N)						
$R_{L\_TX\_100\ MHz}$	TX Differential return loss at 100MHz to 2.5GHz	SDD22, 100MHz to 2.5GHz		–20		dB
$R_{L\_TX\_2.5\ GHz}$	TX Differential return loss at 5GHz	SDD22, 5GHz		–16		dB
$R_{L\_TX\_10\ GHz}$	TX Differential return loss from 5GHz to 10GHz	SDD22, 5GHz to 10GHz		–8.5		dB
$R_{L\_TX\_CM}$	TX common-mode return loss	SCC22, 0.5GHz to 5 GHz		–6.7		dB
$V_{TX-DIFFPP-1200}$	Differential peak-to-peak TX voltage swing linear dynamic range at 100MHz	100MHz; Measured at –1dB compression point = 20 × log(VOD/ VOD_linear)		1000		mV
	Differential peak-to-peak TX voltage swing linear dynamic range at 5GHz	5GHz; Measured at –1dB compression point = 20 × log(VOD/VOD_linear)		1300		mV
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during RX Detection.	Measured at package pins.			600	mV
$V_{TX-DC-CM}$	TX DC common-mode voltage		0	1.85	2.05	V
$V_{TX-CM-AC-PP-ACTIVE}$	Transmitter AC common mode peak-peak voltage when active. Maximum mismatch from TXP+TXN for both time and amplitude.	CHx_EQ setting matches input channel insertion loss			116	mV
$V_{TX-IDLE-DIFF-AC-PP}$	AC electrical idle differential peak-to-peak output voltage		0		10	mV
$R_{TX-DC-CM}$	TX DC common-mode impedance		18		30	Ω
$R_{TX-DC-DIFF}$	TX DC differential impedance		72		120	Ω
$I_{TX-SHORT}$	Transmitter short-circuit current limit.				107	mA
$C_{AC-COUPLING}$	External AC-coupling capacitor on differential pairs.		75		265	nF

5.6 Timing Requirements

over operating free-air temperature and voltage range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
t_{d_pg}	Internal power good asserted high when V_{CC} is at 2.5V			5	µs
t_{VCC_RAMP}	V_{CC} supply ramp requirement	0.1		50	ms

5.7 Switching Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DIFF_DLY}	Differential propagation delay	V_{CC} = 3.0V; EN = 1			150	ps
t_{PWRUP_ACTIVE}	Time from assertion of EN to device active and performing Rx. Detect on both ports	V_{CC} = 3.0V; EN = 1			8	ms
$t_{TX\_RISE\_FALL}$	Transmitter rise/fall time	V_{CC} = 3.3V; EN = 1; 10Gbps; 20% to 80% of differential output; 1200mVpp linear range setting; Fast Input rise/fall time		27		ps
$t_{RF\_MISMATCH}$	Transmitter rise/fall mismatch	V_{CC} = 3.3V; EN = 1; 10Gbps; 20% to 80% of differential output; 1200mVpp linear range setting; 1000mVpp VID		0.6		ps

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over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TX_DJ}	Transmitter residual deterministic jitter	V_{CC} = 3.3V; EN = 1; 10Gbps; 1200mVpp linear range setting; Input channel loss of 12dB; Output channel loss of 1.5dB; Optimized EQ		0.05		UI

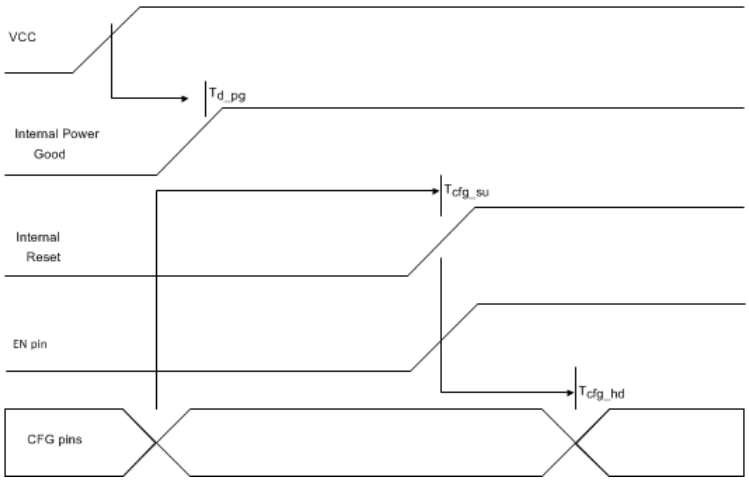

Figure 5-1. Power-Up Diagram

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5.8 Typical Characteristics

V_{CC} = 3.3V, 25°C, 200mVpp V_{ID} sine wave, Z_O = 100Ω, RGE package

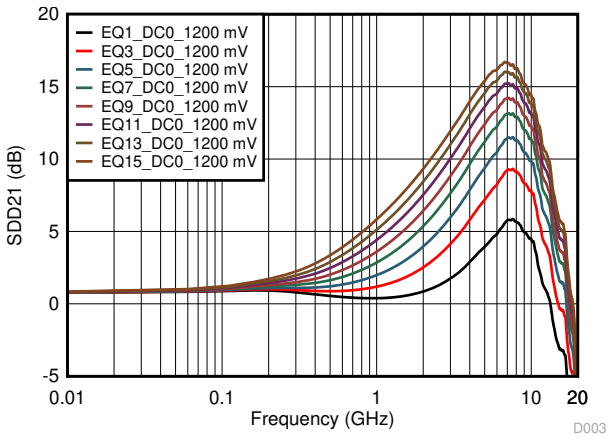


Figure 5-2. 1200mV DC0 Gain Odd EQ Settings Curves

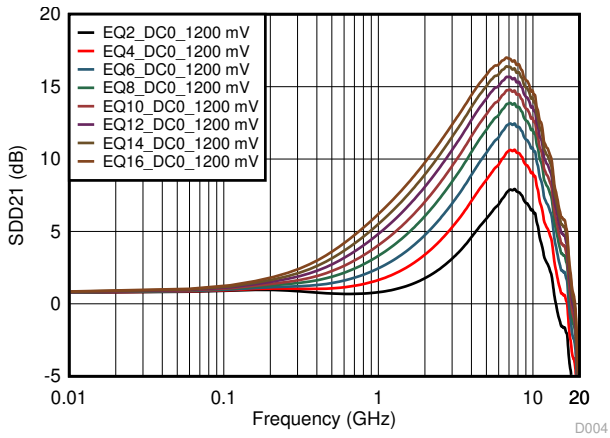


Figure 5-3. 1200mV DC0 Even EQ Settings Curves

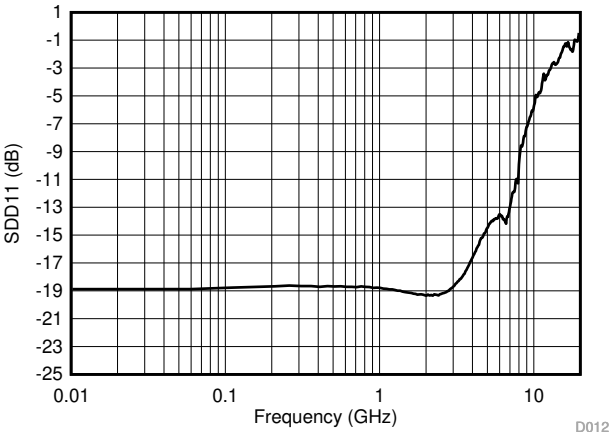


Figure 5-4. SDD11 Return Loss

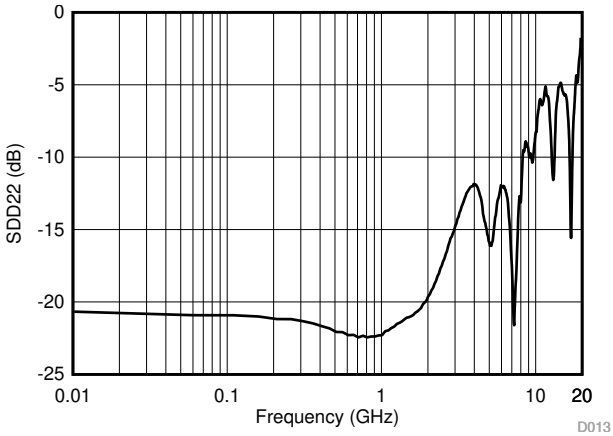


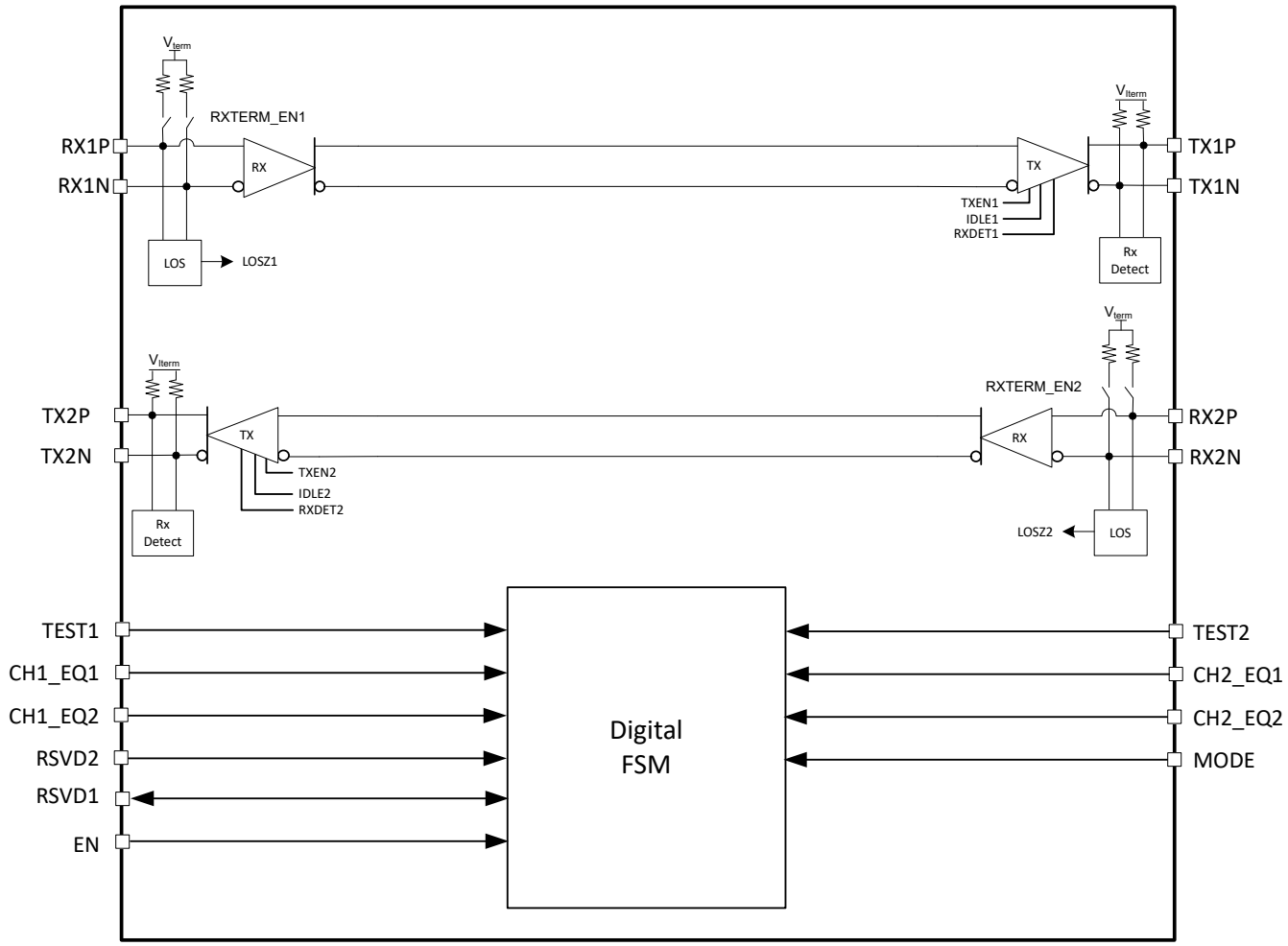
Figure 5-5. SDD22 Return Loss

6 Detailed Description

6.1 Overview

The SN75LVPE3101 is a PCIe 3.0 x1 redriver. As signals traverse through a channel (like FR4 trace) the amplitude of the signal is attenuated. The attenuation varies depending on the frequency content of the signal. Depending the length of the channel, this attenuation can be large enough to result in signal integrity issues at a PCIe 3.0 receiver. By placing a SN75LVPE3101 between PCIe 3.0 root complex and endpoint, the attenuation effect of the channel can be eliminated or minimized. The result is a PCIe 3.0-compatible eye at the receiver of the endpoint. With up to 16 receiver equalization settings, the SN75LVPE3101 can support many different channel loss combinations. The SN75LVPE3101 ultra-low power architecture offers low power consumption on a single 3.3V supply. The SN75LVPE3101 settings are configurable through pins.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 4-Level Control Inputs

The SN75LVPE3101 has (MODE, CH1_EQ1, CH1_EQ2, CH2_EQ1, and CH2_EQ2) 4-level inputs pins that are used to control the equalization gain and the output voltage swing dynamic range. These 4-level inputs use a resistor divider to help set the four valid levels and provide a wider range of control settings. These resistors together with the external resistor connection combine to achieve the desired voltage level.

Table 6-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 kΩ 5% to GND.
F	Float (leave pin open)
1	Tie 1 kΩ 5% to V_{CC}.

Note

To conserve power, the SN75LVPE3101 disables the internal pullup and pull-down resistors of the 4-level input after the state of 4-level pins are sampled on the rising edge of the EN pin. A change of state for any four level input pin is not applied to the SN75LVPE3101 until after the EN pin transitions from low to high.

6.3.2 Linear Equalization

With a linear equalizer, the SN75LVPE3101 can electrically shorten a particular channel allowing for longer run lengths.

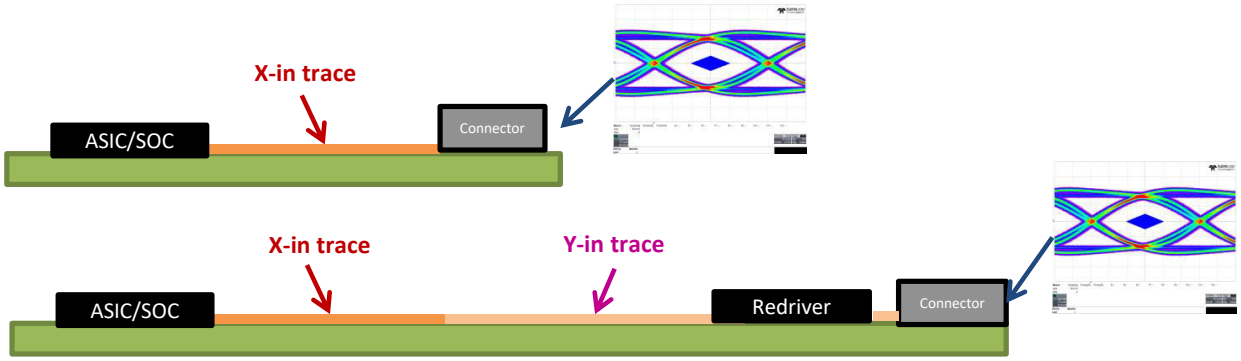

Figure 6-1. Linear Equalizer

With a SN75LVPE3101, a longer trace can be made to have similar insertion loss as a shorter trace. For example, a long trace of X + Y inches can be made to have similar loss characteristics of a shorter trace of X inches.

The receiver equalization level for each channel is determined by the state of the CHx_EQ1 and CHx_EQ2 pins, where x = 1 or 2.

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Table 6-2. EQ Configuration Options

EQ SETTING #	CHx_EQ2 PIN LEVEL	CHx_EQ1 PIN LEVEL	EQ GAIN at 2.5 GHz / 4 GHz / 5 GHz (dB)
1	0	0	1.0 / 2.3 / 3.6
2	0	R	2.1 / 4.0 / 5.5
3	0	F	3.0 / 5.2 / 6.8
4	0	1	4.0 / 6.4 / 8.1
5	R	0	4.6 / 7.2 / 9.0
6	R	R	5.5 / 8.2 / 10.0
7	R	F	6.2 / 9.0 / 10.8
8	R	1	6.9 / 9.8 / 11.6
9	F	0	7.3 / 10.2 / 11.9
10	F	R	7.9 / 10.9 / 12.6
11	F	F	8.4 / 11.4 / 13.1
12	F	1	9.0 / 12.0 / 13.7
13	1	0	9.4 / 12.3 / 14.1
14	1	R	9.9 / 12.8 / 14.6
15	1	F	10.3 / 13.2 / 14.9
16	1	1	10.7 / 13.6 / 15.3

6.3.3 PCIe/SATA/SATA Express Redriver Operation

When operating in a PCI Express (PCIe) Gen3, SATA Gen3, or SATA Express application, the SN75LVPE3101 enables both channels (upstream and downstream) receiver and transmitter paths upon detecting far-end termination on both TX1 and TX2. Both upstream and downstream paths remain enabled until the EN pin is deasserted low. In this mode, the SN75LVPE3101 is transparent to PCIe link power management (L0s, L1) and SATA interface power states. When far-end termination is detected on both TX1 and TX2, the SN75LVPE3101 power is at $P_{(ACTIVE\_1200mV)}$ regardless of the PCIe or SATA power state. To save power during system S3/S4/S5 states, TI recommends to deassert the EN pin to conserve power.

6.4 Device Functional Modes

6.4.1 Shutdown Mode

The device enters Shutdown mode when the EN pin is low and V_{CC} is active and stable. Shutdown mode is the lowest power state of the SN75LVPE3101. While in Shutdown mode, the SN75LVPE3101 receiver terminations are disabled.

6.4.2 Disconnect Mode

Next to Shutdown mode, the Disconnect mode is the lowest power state of the SN75LVPE3101. The SN75LVPE3101 enters Disconnect mode when exiting Shutdown mode. In the Disconnect state, the SN75LVPE3101 periodically checks for far-end receiver termination on both TX1 and TX2. When the far-end receiver termination is detected on both ports, the SN75LVPE3101 transitions to Active mode.

6.4.3 Active Mode

Active mode is the highest power state of the SN75LVPE3101. Any time high-speed traffic is received, the SN75LVPE3101 remains in Active mode. The SN75LVPE3101 only exits Active mode if electrical idle is detected on both RX1 and RX2. While in Active mode, the SN75LVPE3101 high-speed receivers and transmitters are powered and active.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The SN75LVPE3101 is a linear redriver designed specifically to compensation for ISI jitter caused by attenuation through a passive medium like traces and cables. The SN75LVPE3101 has two independent channels, therefore the device can be optimized to correct ISI in both the upstream and downstream direction through 16 different equalization choices. Designers can place the SN75LVPE3101 between two port partners to correct signal integrity issues, resulting in a more robust system.

7.2 Typical SATA, PCIe and SATA Express Application

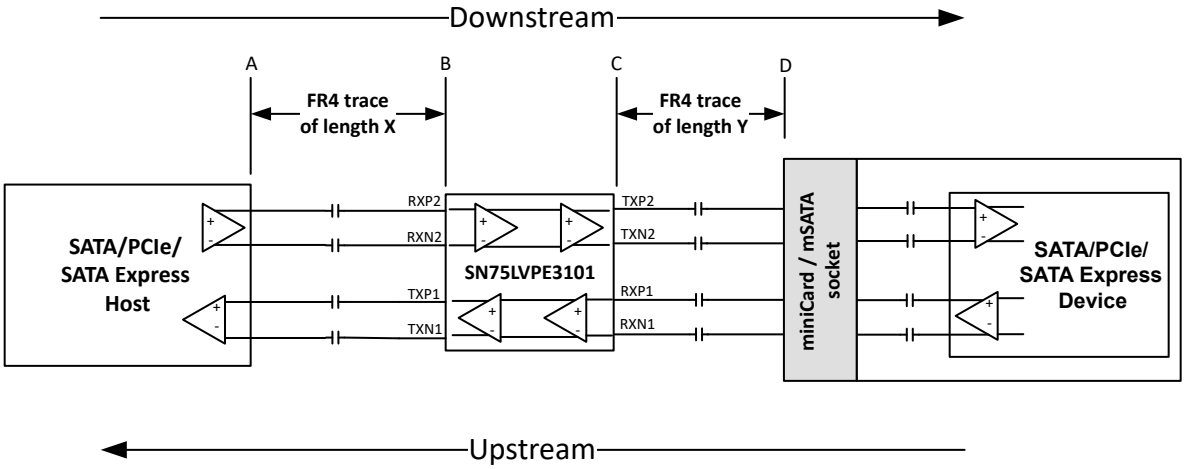

Figure 7-1. SATA/PCIe/SATA Express Typical Application

7.2.1 Design Requirements

For this design example, use the parameters shown in Table 7-1.

Table 7-1. Design Parameters

PARAMETER	VALUE
VCC supply (3 V to 3.6 V)	3.3 V
PCIe Support Required (Yes/No)	Yes
SATA Express Support Required (Yes/No)	Yes
SATA Support Required (Yes/No)	Yes, then ferrite beads (FB1 and FB2) and 49.9 Ω required. No, then ferrite bead (FB1 and FB2) and 49.9 Ω not required.
TX1, TX2, RX2 AC-coupling Capacitor (176 nF to 265 nF)	220 nF ±10%
RX1 AC-coupling Capacitor (297 nF to 363 nF)	Optional. But if implemented suggest 330 nF ±10%
A to B FR4 Length (inches)	8
A to B FR4 Trace Width (mils)	4
C to D FR4 length (inches)	2
C to D FR4 Trace Width (mils)	4

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7.2.2 Detailed Design Procedure

In this example, the SN75LVPE3101 has a DC gain fixed at 0dB and a linearity range fixed at 1200mV. The SN75LVPE3101 performs far-end receiver termination detection and enables both upstream and downstream paths when far-end termination is detected on both TX1 and TX2.

The AC-coupling capacitor range defined for a SATA device is a lot smaller than the AC-coupling capacitor range defined for SATA Express and PCI Express (PCIe) as indicated by Figure 7-2. While the SN75LVPE3101 can usually detect the receiver termination of the PCIe and SATA Express device, a SATA 12nF (maximum) AC-coupling capacitor prevents the SN75LVPE3101 from detecting the SATA device receiver termination. To correct this problem, a ferrite bead along with 49.9Ω resistor must be placed between C_{TX2} and the miniCard/mSATA socket. These components can be isolated from the high-speed channel when PCIe or SATA Express is active by using an NFET as shown in Figure 7-4. TI recommends to enable the NFET whenever a SATA device is present. The ferrite bead chosen must present at least 600Ω impedance at 100MHz so as to not impact high-speed signaling. TI recommends to use Murata BLM03AG601SN1 or BLM03HD601SN1D or a ferrite bead with similar characteristics from a different vendor. For applications which only require support for PCIe and SATA Express and do not need to support SATA, the ferrite beads and 49.9Ω resistors are not needed.

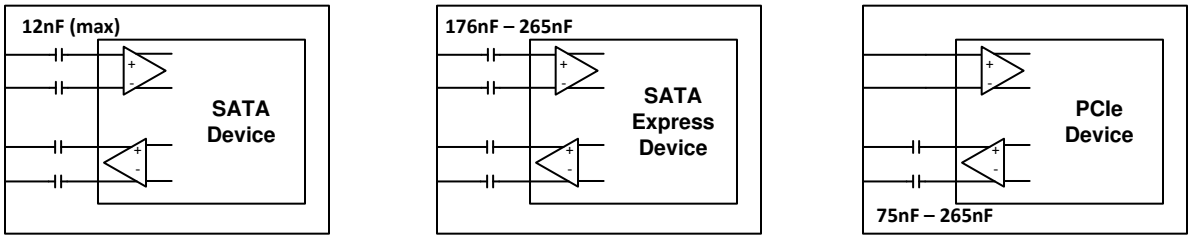

Figure 7-2. AC-Coupling Capacitor Implementation for SATA, SATA Express, and PCIe Devices

The SN75LVPE3101 power is at $P_{(ACTIVE\_1200mV)}$ when both the upstream and downstream paths are enabled. To save system power in system S3/S4/S5 states, TI recommends to control the SN75LVPE3101 EN pin. Any time the system enters a low power state (S3, S4, or S5), TI recommends to deassert the EN pin. While the EN pin is deasserted, the SN75LVPE3101 consumes $P_{(SHUTDOWN)}$. Assertion of this pin is necessary any time the system exits a lower power state.

The SN75LVPE3101 compensates for channel loss in both the upstream (C to D) and downstream direction (A to B). Configure the CH1_EQ[2:1] and CH2_EQ[2:1] pins to the equalization setting that matches as close possible to the channel insertion loss. In this particular example, CH2_EQ[2:1] is for path A to B which is the channel between the PCIe/SATA/SATA Express host and the SN75LVPE3101, and CH1_EQ[2:1] is for path C to D which is the channel between the SN75LVPE3101 and the miniCard/mSATA socket.

In this particular example, the channel A-B has a trace length of 8 inches with a 4mil trace width. This particular channel has about 0.83dB per inch of insertion loss at 5GHz. This equates to approximately 6.7dB of loss for the entire 8 inches of trace as depicted in Figure 7-3. An additional 1.5dB of loss is added due to package of the PCIe/SATA/SATA Express host, SN75LVPE3101, and the AC-coupling capacitor. This brings the entire channel loss at 5GHz to 6.7dB + 1.5dB = 8.2dB. The channel A-B for this example is connected to SN75LVPE3101 RX2P/N input and therefore CH2_EQ[2:1] pins are used for adjusting SN75LVPE3101 RX2P/N equalization settings. Set the CH2_EQ[2:1] pins such that SN75LVPE3101 equalization is between 5dB and 8dB. A value closer to 5dB may be best if the host has transmitter de-emphasis.

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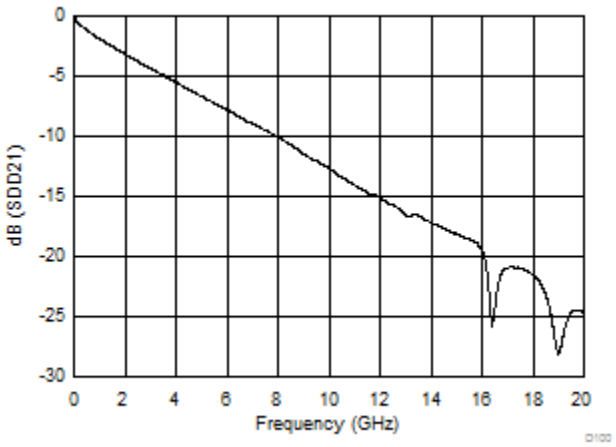

Freq = 5GHz dB(SDD21) = –6.666

Figure 7-3. Insertion Loss for 8in FR4 Trace Lenght and 4mil FR4 Trace Width

Use a similar method for the upstream path (C to D). In this particular example, C to D has a trace length of 2 inches with a 4mil trace width. This equates to approximately 1.5dB at 5GHz. The SATA/SATA Express/PCIe device has a channel loss that can be added to the C to D channel loss. For this example, assume a value of 5dB is acceptable to compensate for C to D channel loss as well as loss associated with the SATA/SATA Express/PCIe device. Set the CH1_EQ[2:1] pins such that the SN75LVPE3101 equalization is 5dB.

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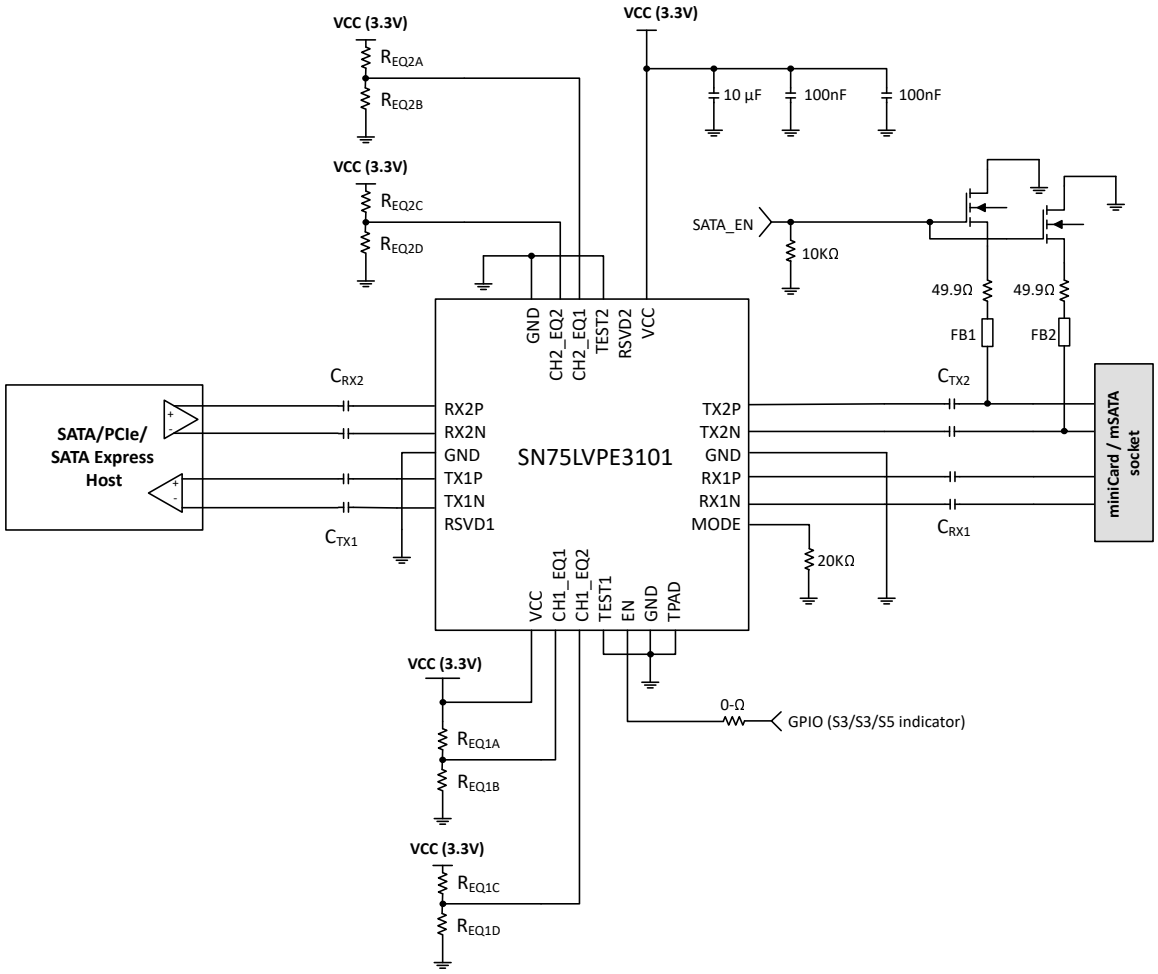

Figure 7-4. Example SATA/PCIe/SATA Express Schematic

7.2.3 Application Curves

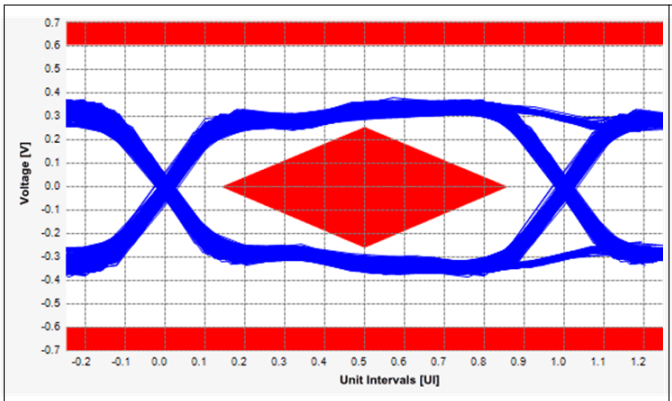

Figure 7-5. PCIe Gen1 TX Eye Diagram

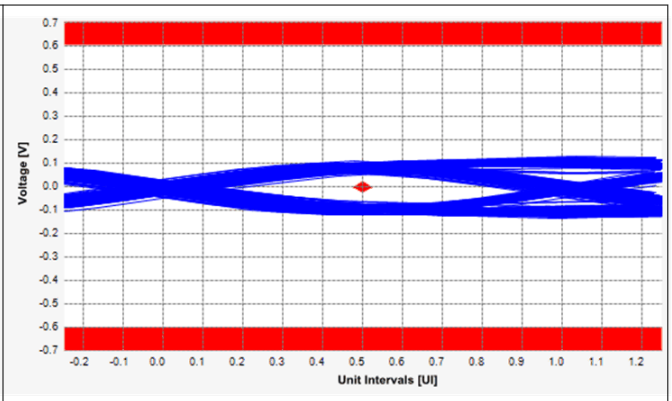

Figure 7-6. PCIe Gen 3 TX Eye Diagram

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7.3 Power Supply Recommendations

The SN75LVPE3101 has two V_{CC} supply pins. TI recommends to place a 100nF decoupling capacitor near each of the V_{CC} pins. TI also recommends to have at least one bulk capacitor of at least 10µF on the V_{CC} plane near the SN75LVPE3101.

7.4 Layout

7.4.1 Layout Guidelines

- Route RXP/N and TXP/N pairs with controlled differential impedance. The differential impedance of the high speed traces depend on the specific design. PCIe allows differential impedances ranging from 70Ω to 100Ω, with 85Ω typically recommended for Card ElectroMechanical (CEM) specification interoperability.
- Keep away from other high speed signals.
- In PCIe applications, maintaining polarity through the SN75LVPE3101 is not necessary. Therefore, TI recommends connecting polarity in such a way that produces the best routing.
- Keep intra-pair routing to within 2 mils.
- Intra-pair length matching must be near the location of mismatch.
- Inter-pair length matching is not necessary.
- Separate each pair at least by 3 times the signal trace width.
- Keep the use of bends in differential traces to a minimum. When bends are used, make sure the number of left and right bends are as equal as possible and the angle of the bend ≥ 135 degrees. This minimizes any length mismatch causes by the bends; and therefore, minimize the impact bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of vias must be kept to a minimum. TI recommends keeping the vias count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do NOT route differential pairs over any plane split.
- When using through-hole high-speed connectors, TI recommends to route differential pairs on bottom layer to minimize the stub created by the through-hole connector.
- Adding test points causes impedance discontinuity; and therefore, negatively impact signal performance. If test points are used, place the test points in series and symmetrically. The test points must not be placed in a manner that causes a stub on the differential pair.

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7.4.2 Layout Example

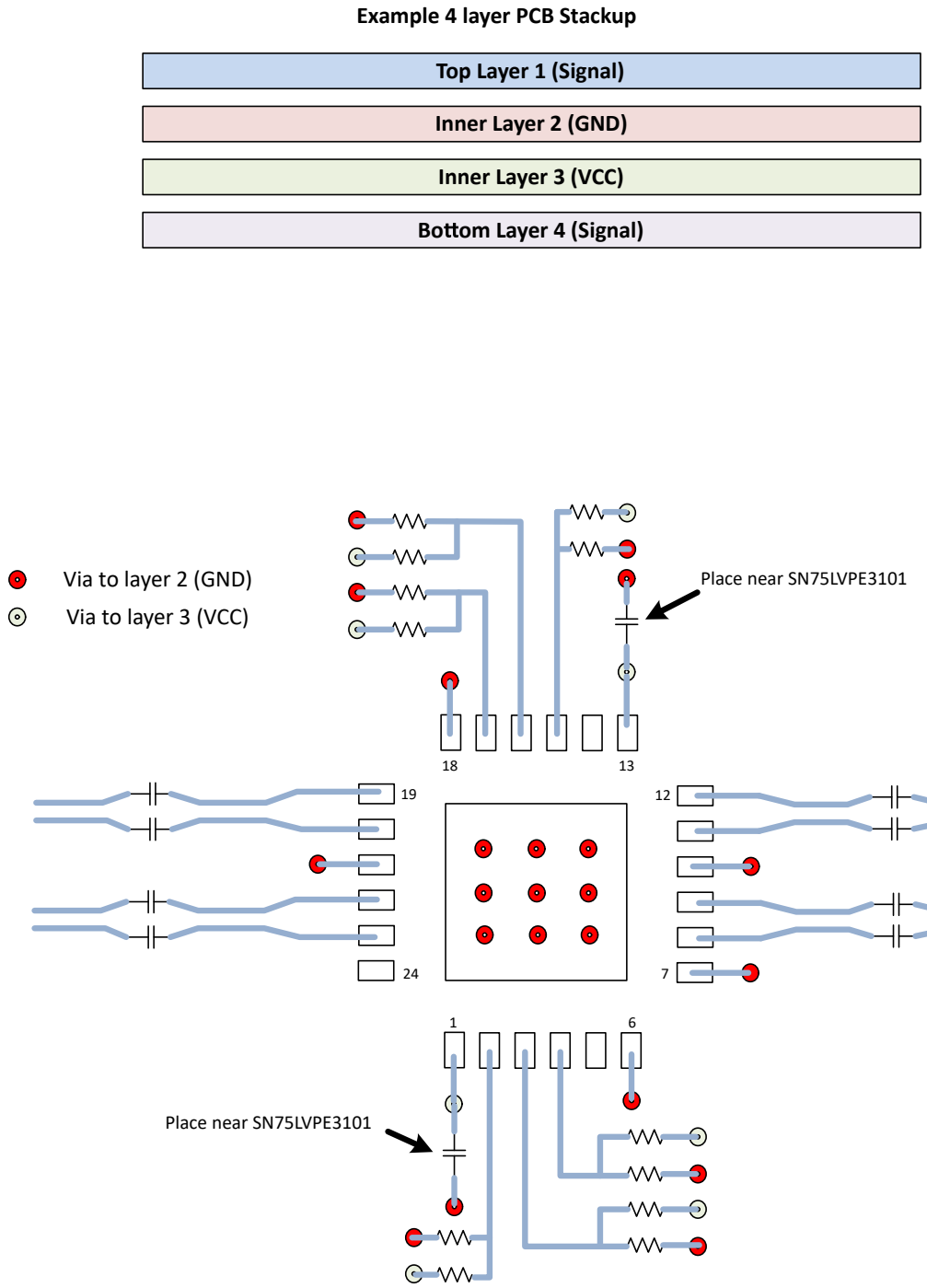

Figure 7-7. Example Layout

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8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVPE3101RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PX101
SN75LVPE3101RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PX101
SN75LVPE3101RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PX101
SN75LVPE3101RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PX101

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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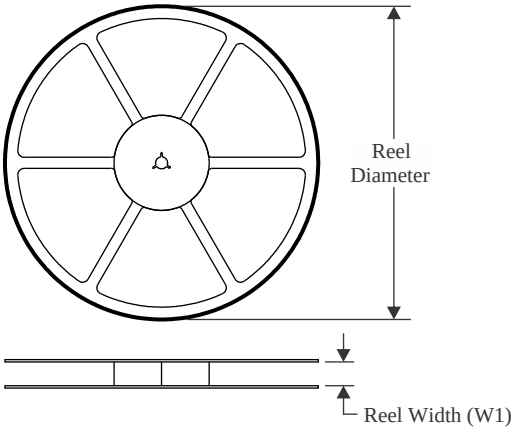
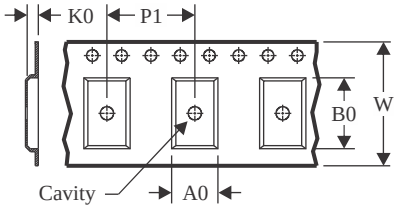
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

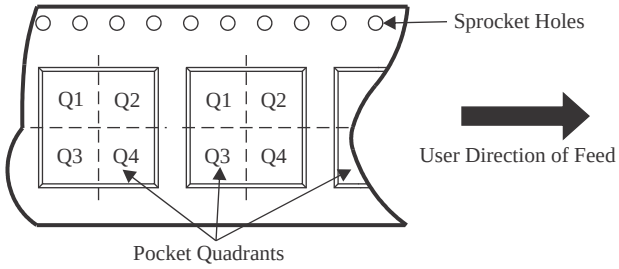


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

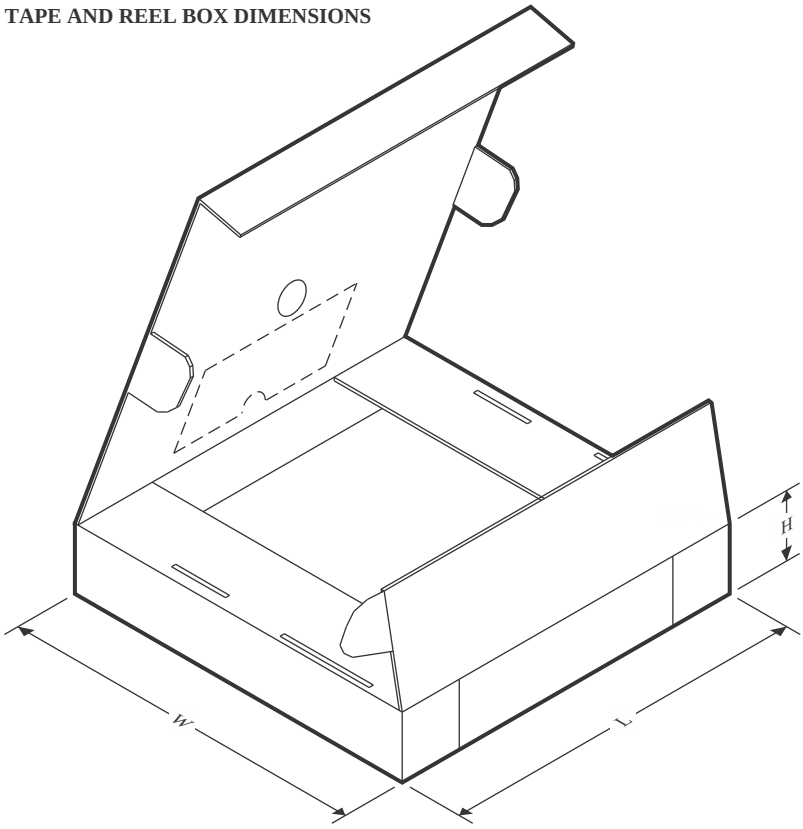
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVPE3101RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN75LVPE3101RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



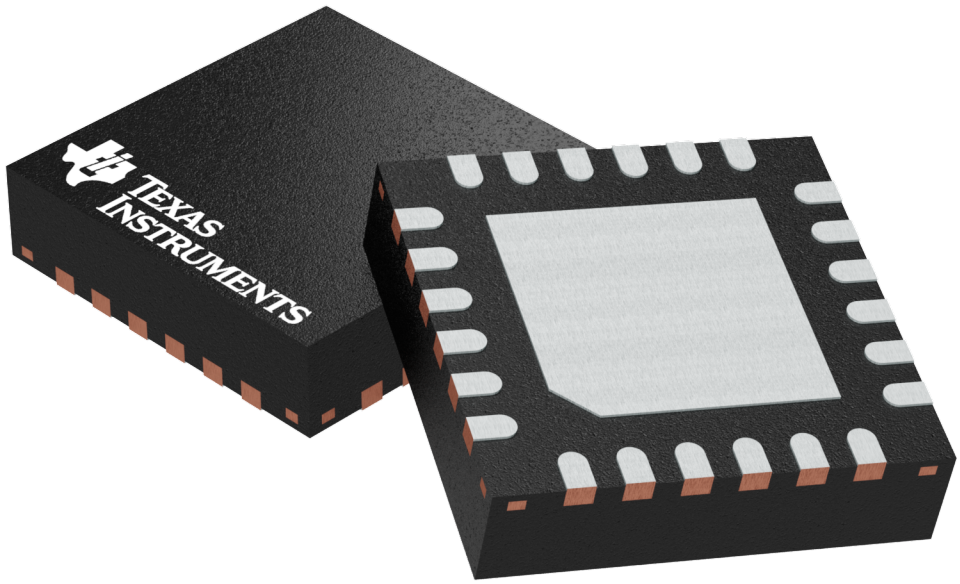
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVPE3101RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
SN75LVPE3101RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

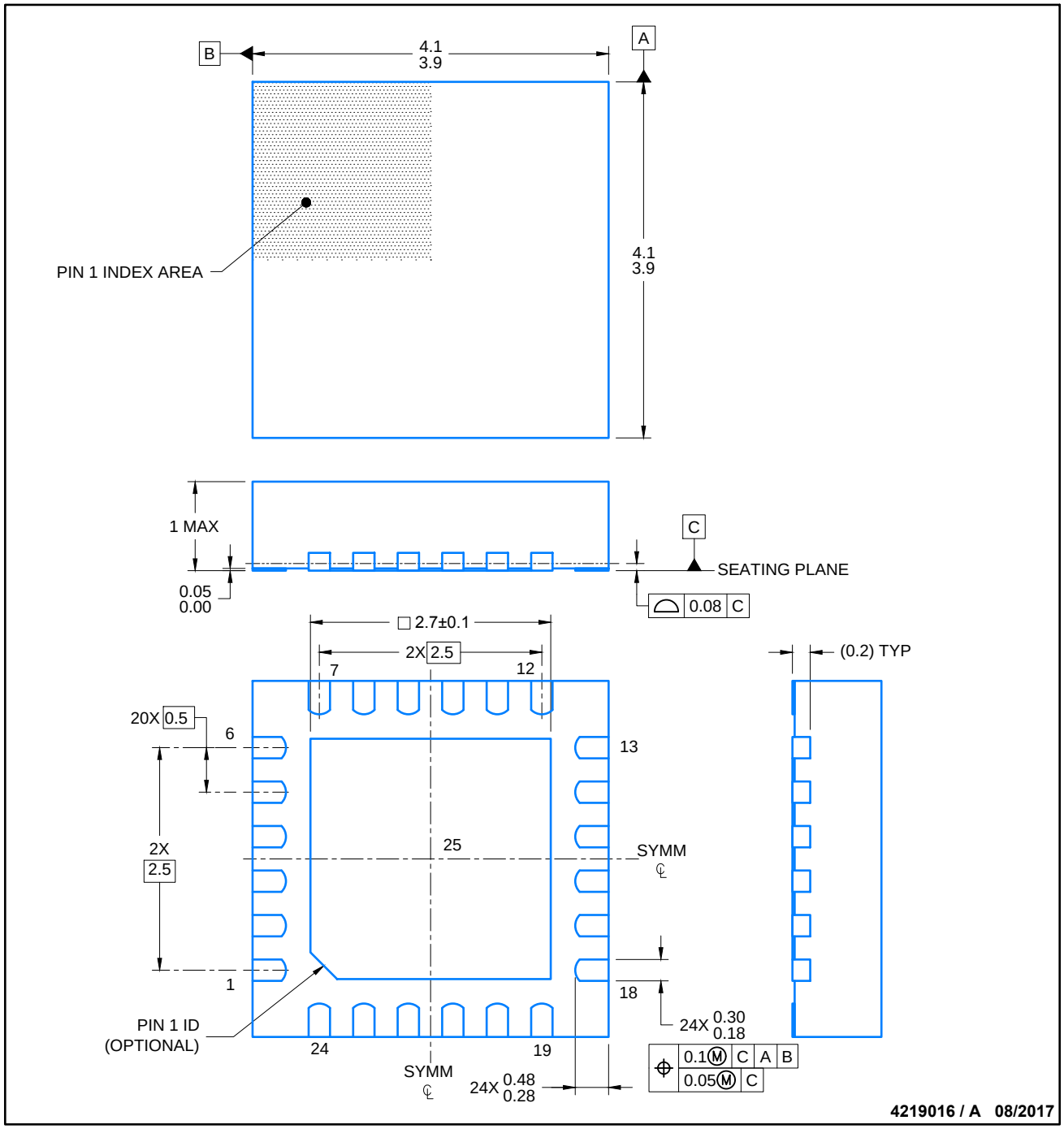
4204104/H

PACKAGE OUTLINE

RGE0024H

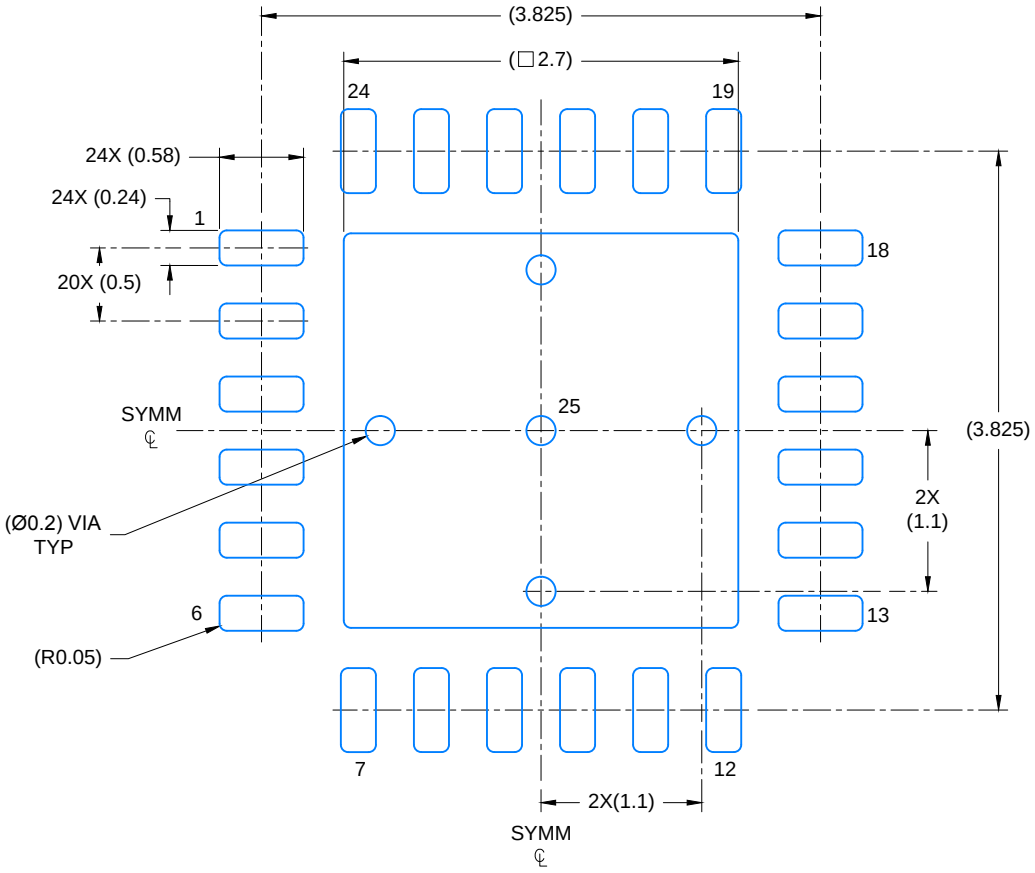
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



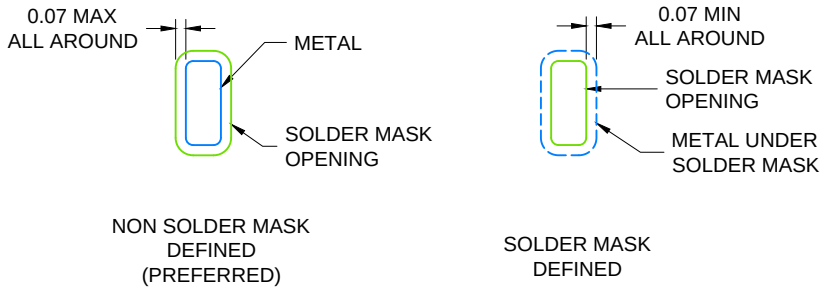
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

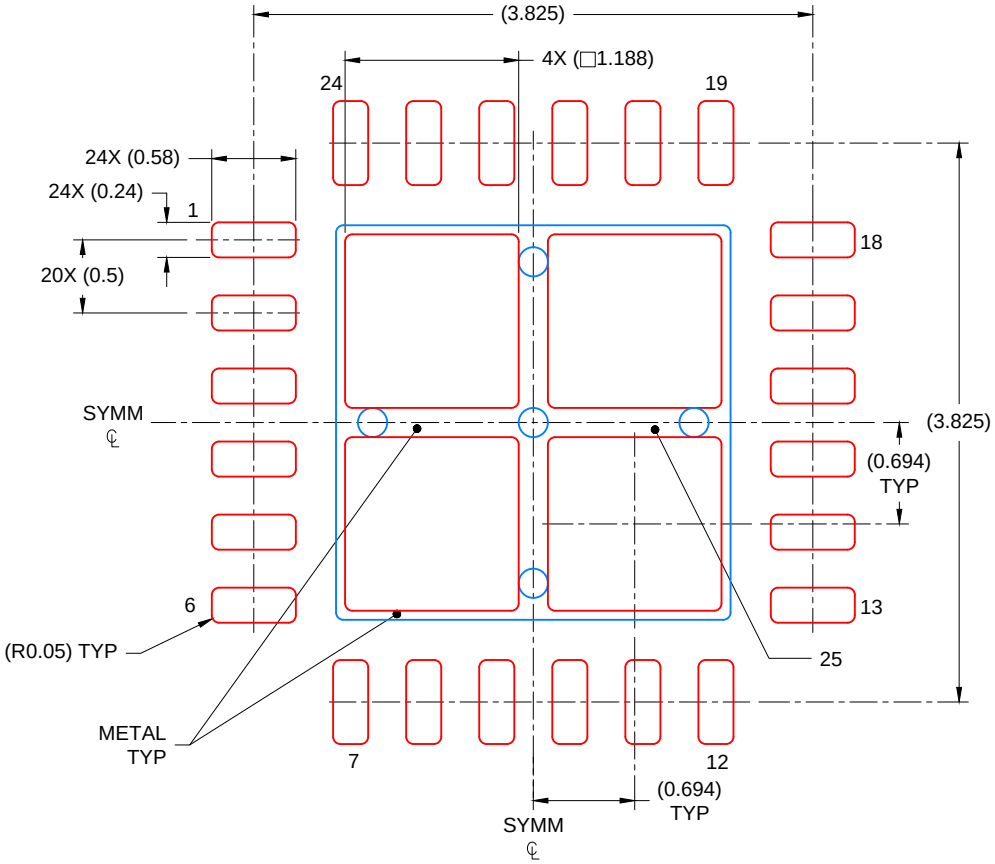


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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