SN75DP130 DisplayPort™ 1:1 Redriver With Link Training

1 Features

- Supports DP v1.1a and DP v1.2 Signaling Including HBR2 Data Rates to 5.4 Gbps
- Supports HDMI 1.4b With TMDS Clock Frequencies up to 340 MHz
- Glueless Interface to AMD, Intel, and NVIDIA Graphics Processors
- Auto-Configuration Through Link Training
- Output Signal Conditioning With Tunable Voltage Swing and Pre-Emphasis Gain
- Highly Configurable Input Variable Equalizer
- Two Device Options Including a Dual Power Supply Configuration for Lowest Power
- 2-kV ESD HBM Protection
- Temperature Range: 0°C to 85°C
- 48-Pin 7-mm × 7-mm VQFN Package

2 Applications

- Notebook PCs
- Desktop PCs
- PC Docking Stations
- PC Standalone Video Cards

3 Description

The SN75DP130 device is a single channel DisplayPort™ (DP) re-driver that regenerates the DP high-speed digital link. The device complies with the VESA DisplayPort Standard Version 1.2, and supports a 4-lane Main Link interface signaling up to HBR2 rates at 5.4 Gbps per lane. This device also supports DP++ Dual-Mode, offering TMDS signaling for DVI and full HDMI Version 1.4a support.

The device compensates for PCB-related frequency loss and switching-related loss to provide the optimum DP electrical performance from source to sink. The Main Link signal inputs feature configurable equalizers with selectable boost settings. At the Main Link output, four primary levels of differential output voltage swing (VOD) and four primary levels of pre-emphasis are available. A secondary level of boost adjustment, programmed through I^2C, for fine-tuning the Main Link output. The device can monitor the AUX channel and automatically adjust the output signaling levels and input equalizers in response to Link Training commands. Additionally, the SN75DP130 output signal conditioning and EQ parameters are fully programmable through the I^2C interface.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75DP130	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simple Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2013) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (January 2013) to Revision D — **Page**

- Power-Down Sequence deleted: 1. De-assert EN to the device ... 38
- Power-Up Sequence deleted: 1. Assert RSTN and de-assert EN to the device ... 38
- Power-Up Sequence deleted: 5. Assert EN a minimum of 10 µs after RSTN has been de-asserted. ... 38
- Deleted the EN time line from Figure 34 ... 38

Changes from Revision B (October 2011) to Revision C — **Page**

- Added text to RSTN description in PIN FUNCTIONS ... 5
- Added RSTN pin row to V_{IH} in RECOMMENDED OPERATING CONDITIONS ... 7
- Added RSTN pin row to V_{IL} in RECOMMENDED OPERATING CONDITIONS ... 7
- Added rows to Device power under normal operation in POWER DISSIPATION table ... 8
- Changed in Table 1 13.9 to 113.9 ... 13
- Deleted unnecessary tie dot in Block Diagram ... 17
- Changed Table 3 ... 20
- Changed Figure 17 ... 21
- Changed Figure 18 ... 23
- Changed SN75DP130 Local I^2C Control and Status Registers ... 26
- Added DP130 POWER SEQUENCING section ... 38

Changes from Revision A (September 2011) to Revision B **Page**

- Deleted pins 37 an 43 from GND in the PIN FUNCTIONS table 6

Changes from Original (April 2011) to Revision A **Page**

- Changed pin numbers in PIN FUNCTIONS table, VDDD_DREG and NC 6

5 Description (continued)

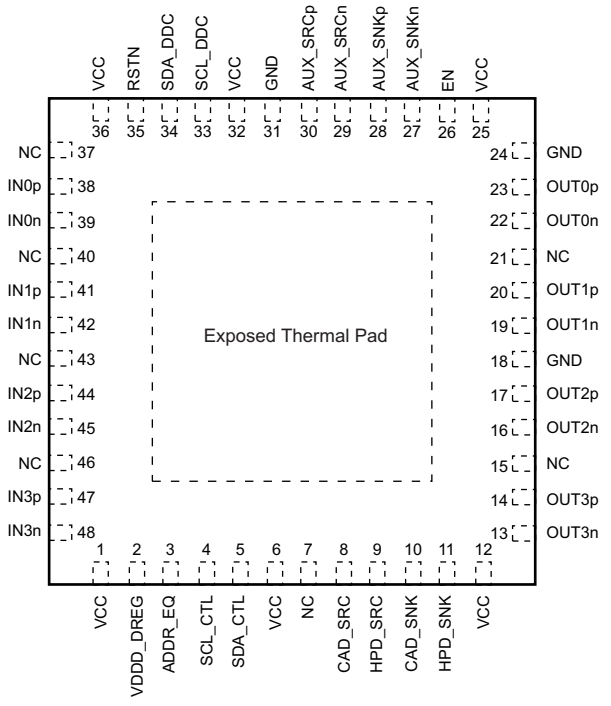
The SN75DP130 is optimized for mobile applications, and contains activity detection circuitry on the Main Link input that transitions to a low-power Output Disable mode in the absence of a valid input signal. Other low-power modes are supported, including a standby mode with typical dissipation of approximately 2 mW when no video sink (for example, monitor) is connected.

The device is characterized for an extended operational temperature range from 0°C to 85°C.

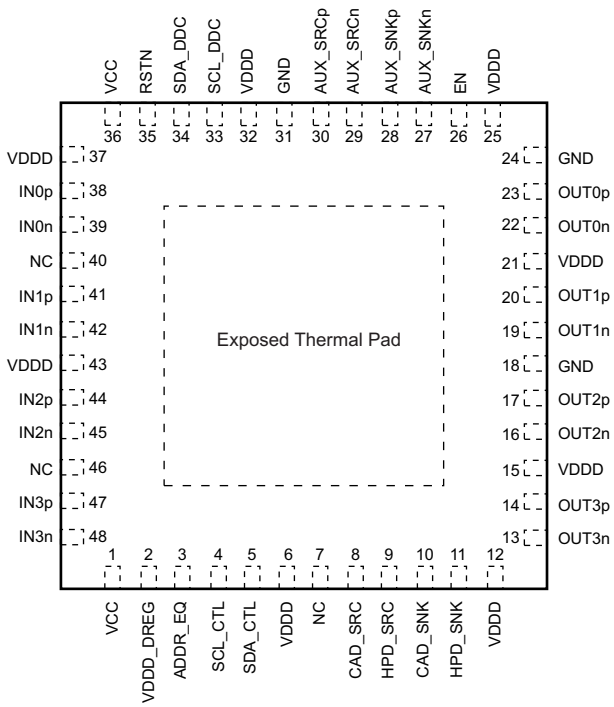
The SN75DP130 offers separate AUX and DDC source interfaces that connect to one AUX sink channel. This minimizes component count when implemented with a graphics processor (GPU) comprising separate DDC and AUX interfaces. For GPUs with combined DDC/AUX, the device can operate as a FET switch to short-circuit the AUX channel AC coupling caps while connected to a TMDS sink device. Other sideband circuits such as Hot Plug Detect (HPD) are optimized to reduce external components, providing a seamless connection to Intel, AMD, and NVIDIA graphics processors.

6 Pin Configuration and Functions

SN75DP130SS RGZ Package
48-Pin VQFN Single Supply
Top View



SN75DP130DS RGZ Package
48-Pin VQFN Dual Supply
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
MAIN LINK TERMINALS			
IN0n	39	Input (100-Ω diff)	DisplayPort Main Link Lane 0 Differential Input
IN0p	38		
IN1n	42		DisplayPort Main Link Lane 1 Differential Input
IN1p	41		
IN2n	45		DisplayPort Main Link Lane 2 Differential Input
IN2p	44		
IN3n	48		DisplayPort Main Link Lane 3 Differential Input
IN3p	47		
OUT0n	22	Output (100-Ω diff)	DisplayPort Main Link Lane 0 Differential Output
OUT0p	23		
OUT1n	19		DisplayPort Main Link Lane 1 Differential Output
OUT1p	20		
OUT2n	16		DisplayPort Main Link Lane 2 Differential Output
OUT2p	17		
OUT3n	13		DisplayPort Main Link Lane 3 Differential Output
OUT3p	14		
AUX CHANNEL AND DDC DATA TERMINALS			
AUX_SRCn	29	I/O (100-Ω diff)	Source Side Bidirectional DisplayPort Auxiliary Data Channel. If the AUX_SNK channel is used for monitoring only, these signals are not used and may be left open.
AUX_SRCp	30		
AUX_SNKn	27	I/O (100-Ω diff)	Sink Side Bidirectional DisplayPort Auxiliary Data Channel.
AUX_SNKp	28		
SDA_DDC	34	I/O	Bidirectional I^2C Display Data Channel (DDC) for TMDS mode. These signals may be used together with AUX_SNK to form a FET switch to short-circuit the AC coupling capacitors during TMDS operation in a DP++ Dual-Mode configuration. These terminals include integrated 60-kΩ pullup resistors
SCL_DDC	33		
HPD, CAD, AND CONTROL TERMINALS			
HPD_SRC	9	O	Hot Plug Detect Output to the DisplayPort Source.
HPD_SNK	11	I	DisplayPort Hot Plug Detect Input from Sink. This device input is 5-V tolerant.
			Note: Pull this input high during compliance testing or use I^2C control interface to go into compliance test mode and control HPD_SNK and HPD_SRC by software.
CAD_SRC	8	O	DP Cable Adapter Detect Output. This output typically drives the GPU CAD input.
CAD_SNK	10	I	DisplayPort Cable Adapter Detect Input. This input tolerates a 5-V supply with a supply impedance higher than 90kΩ. A device internal zener diode limits the input voltage to 3.3 V. An external 1MΩ resistor to GND is recommended. This terminal is used to select DP mode or TMDS mode in a DP++ Dual-Mode application.
SCL_CTL	4	I/O	Bidirectional I^2C interface to configure the SN75DP130. This interface is active independent of the EN input but inactive when RSTN is low.
SDA_CTL	5		
RSTN	35	I	Active Low Device Reset. This input includes a 150-kΩ resistor to the VDDD core supply. An external capacitor to GND is recommended on the RSTN input to provide a power-up delay (see the V_{IL} and V_{IH} specifications in *Recommended Operating Conditions*).
			This signal is used to place the SN75DP130 into Shutdown mode for the lowest power consumption. When the RSTN input is asserted, all outputs (excluding HPD_SRC and CAD_SRC) are high-impedance, and inputs (excluding HPD_SNK and CAD_SNK) are ignored; all I^2C and DPCD registers are reset to their default values.
			At power up, the RSTN input must not be de-asserted until the VCC and VDDD supplies have reached at least the minimum recommended supply voltage level (see Figure 34 for timing requirements).
EN	26	I	Device Enable. This input incorporates an internal pullup of 200 kΩ.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
ADDR_EQ	3	3-level Input	I^2C Target Address Select and EQ Configuration Input. If the I^2C bus is used, this input setting selects the I^2C target address, as described in Figure 19. This input also configures the input EQ to the device, as described in Table 3.
SUPPLY AND GROUND TERMINALS			
VDDD	SN75DP130DS 6, 12, 15, 21, 25, 32, 37, 43		Digital low voltage core and Main Link supply for SN75DP130DS device option. Nominally 1.1 V.
VCC	SN75DP130SS 1, 6, 12, 25, 32, 36		3.3-V Supply
	SN75DP130DS 1, 36		
VDDD_DREG	2		SN75DP130SS: Digital voltage regulator decoupling; install 1 µF to GND. SN75DP130DS: Treat same as VDDD; this pin will be most noisy of all VDDD terminals and needs a decoupling capacitor nearby.
GND	18, 24, 31, and Exposed Thermal Pad		Ground. Reference GND connections include the device package exposed thermal pad.
NC	SN75DP130SS 7, 15, 21, 37, 40, 43, 46		No Connect. These terminals may be left unconnected, or connect to GND.
	SN75DP130DS 7, 40, 46		

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.3	4	V
	V_{DDD}, V_{DDD_DREG}	–0.3	1.3	
Voltage	Main link I/O differential voltage	–0.3	1.3	V
	HPD_SNK	–0.3	5.5	
	All other terminals	–0.3	4	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{DDD}	Digital core and Main Link supply voltage		0.97	1.05	1.2	V
T_A	Operating free-air temperature		0		85	°C
T_{CASE}	Case temperature				103.1	°C
$V_{IH(HPD)}$	High-level input voltage HPD_SNK		1.9		5.5	V
V_{IH}	High-level input voltage for device control signals		1.9		3.6	V
		RSTN pin (typical hysteresis of 80 mV)		0.75		
V_{IL}	Low-level input voltage for device control signals		0		0.8	V
		RSTN pin (typical hysteresis of 80 mV)		0.3		
MAIN LINK TERMINALS						
V_{ID}	Peak-to-peak input differential voltage; RBR, HBR, HBR2		0.3		1.40	Vpp
d_R	Data rate				5.4	Gbps
C_{AC}	AC coupling capacitance (each input and each output line)		75		200	nF
R_{tdiff}	Differential output termination resistance		80	100	120	Ω
V_{Oterm}	Output termination voltage (AC coupled)		0		2	V
$t_{SK(in\ HBR2)}$	Intra-pair skew at the input at 5.4 Gbps	When used as re-driver in DP source			20	ps
		When used as receiver equalizer in DP sink			100	
$t_{SK(in\ HBR)}$	Intra-pair skew at the input at 2.7 Gbps				100	ps
$t_{SK(in\ RBR)}$	Intra-pair skew at the input at 1.62 Gbps				300	ps
AUX CHANNEL DATA TERMINALS						
V_{I-DC}	DC input voltage	AUX_SRCp and AUX_SNKp in DP mode	–0.5	0.3	0.4	V
		AUX_SRCn and AUX_SNKn in DP mode	2	3	3.6	
		AUX_SRCp/n and AUX_SNKp/n in TMDS mode	–0.5		3.6	
V_{ID}	Differential input voltage amplitude (DP mode only)		300		1400	mV_{PP}
$d_{R(AUX)}$	Data rate (before Manchester encoding)		0.8	1	1.2	Mbps
$d_{R(FAUX)}$	Data rate Fast AUX (300ppm frequency tolerance)			720		Mbps
t_{jccin_adj}	Cycle-to-cycle AUX input jitter adjacent cycle (DP mode only)				0.05	UI
t_{jccin}	Cycle-to-cycle AUX input jitter within one cycle (DP mode only)				0.1	UI
C_{AC}	AUX AC coupling capacitance (DP mode only)		75		200	nF
V_{srcCMM}	AUX source common mode voltage (only applies to DP mode) CAD = V_{IL}; measured on AUX source and sink before AC coupling caps		0		2000	mV
DDC AND I^2C TERMINALS						
V_I	Input voltage		–0.5		3.6	V
d_R	Data rate				100	kbps
V_{IH}	High-level input voltage		0.7 V_{CC}			V
V_{IL}	Low-level input voltage				0.3 V_{CC}	V
f_{SCL}	SCL clock frequency standard I^2C mode				100	kHz
$t_{w(L)}$	SCL clock low period standard I^2C mode		4.7			µs
$t_{w(H)}$	SCL clock high period standard I^2C mode		4			µs
C_{bus}	Total capacitive load for each bus line				400	pF

7.4 Thermal Information

THERMAL METRIC[1]		SN75DP130 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	21.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.7	
ψ_{JT}	Junction-to-top characterization parameter, high-k board	1.2	
ψ_{JB}	Junction-to-board characterization parameter, high-k board	11.9	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	6.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Power Dissipation

See *SN75DP130 Power Sequencing*.

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
P_N	Device power under normal operation	SN75DP130SS; 4 DP Lanes.		468	828	mW
		SN75DP130DS; 4 DP Lanes.		174	304	
		SN75DP130SS; 2 DP Lanes		252	450	
		SN75DP130DS; 2 DP Lanes.		102	178	
		SN75DP130SS; 1 DP Lanes		144	252	
		SN75DP130DS; 1 DP Lanes.		66	112	
P_{SD}	Shutdown mode power dissipation	SN75DP130SS; 4 DP Lanes.			14.4	mW
		SN75DP130DS; 4 DP Lanes.			7.2	
P_{SBY}	Standby mode power dissipation	SN75DP130SS; 4 DP Lanes.			14.4	mW
		SN75DP130DS; 4 DP Lanes.			7.2	
P_{D3}	D3 power down mode dissipation	SN75DP130SS; 4 DP Lanes.			54	mW
		SN75DP130DS; 4 DP Lanes.			46	
P_{OD}	Output disable (squelch) mode current	SN75DP130SS; 4 DP Lanes.		126	180	mW
		SN75DP130DS; 4 DP Lanes.		58	88	

(1) Test conditions correspond to Power Supply test conditions in *Electrical Characteristics*

7.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$I_{CCDP1HBR2}$	Supply Current 1 DP Lanes	Maximum conditions: IN/OUT at 5.4 Gbps PRBS,V_{OD} = 510 mVpp, P_E = 6 dB; AUX at 1 Mbps PRBS, V_{ID} = 1000 mVpp; EQ = 3.5 dB Typical Conditions: IN/OUT at 5.4 Gbps PRBS,V_{OD} = 510 mVpp, P_E = 0dB AUX and I^2C Idle; EQ = 5 3dB		40	70	mA
$I_{CCDP2HBR2}$	Supply Current 2 DP Lanes			70	125	mA
$I_{CCDP4HBR2}$	Supply Current 4 DP Lanes			130	230	mA
$I_{CCDP1HBR}$	Supply Current 1 DP Lanes	Main Link at 2.7Gbps PRBS, V_{OD} = 510 mVpp, P_E = 0 dB; AUX and I^2C Idle; EQ at 3 dB fixed gain		40		mA
$I_{CCDP2HBR}$	Supply Current 2 DP Lanes			70		mA
$I_{CCDP4HBR}$	Supply Current 4 DP Lanes			130		mA
I_{CCTMDS}	Supply Current TMDS Mode	Main Link at 2.5 Gbps PRBS, V_{ID} = V_{OD} = 600 mVpp; AUX Idle			170	mA
I_{SD}	Shutdown supply current	Shutdown mode		3	4	mA
I_{SBY}	Standby supply current	Standby mode		3	4	mA
I_{D3}	D3 supply current	D3 power-down mode		10	15	mA
I_{OD}	Squelch supply current	Output disable (Squelch) mode		35	50	mA
MAIN LINK						
$V_{OD(L0)}$	Output differential voltage swing	$V_{PRE(L0)}$; 675 Mbps D10.2 Test Pattern; BOOST = 01	238	340	442	mV_{PP}
$V_{OD(L1)}$			357	510	663	
$V_{OD(L2)}$			484	690	897	
$V_{OD(L3)}$			700	1000	1300	
$V_{OD(TMDS)}$		675 Mbps D10.2 Test Pattern; BOOST = 01	420	600	780	
$\Delta V_{OD(L0L1)}$	Output peak-to-peak differential voltage delta	ΔV_{ODn} = 20×log($V_{ODL(n+1)}$ / $V_{ODL(n)}$) measured in compliance with PHY CTS1.1D15 section 3.2 at test point TP2 using special CTS test board	1.7	3.5	5.3	dB
$\Delta V_{OD(L1L2)}$			1.6	2.5	3.5	
$\Delta V_{OD(L2L3)}$			0.8	3.5	6	
$V_{PRE(L0)}$	Driver output pre-emphasis (default)	All V_{OD} options		0	0.25	dB
$V_{PRE(L1)}$		V_{OD} = $V_{OD(L0)}$, $V_{OD(L1)}$, or $V_{OD(L2)}$; BOOST = 01		3.5		
$V_{PRE(L2)}$		V_{OD} = $V_{OD(L0)}$ or $V_{OD(L1)}$; BOOST = 01		6		
$V_{PRE(L3)}$		V_{OD} = $V_{OD(L0)}$; BOOST = 01		9.5		
$V_{PRE(BOOST)}$	Output V_{PRE} boost	BOOST = 10		10%		dB
		BOOST = 00		–10%		
$\Delta V_{PRE(L1L0)}$	Pre-emphasis delta	Measured in compliance with PHY CTS1.1D15 section 3.3 at test point TP2 using special CTS test board	2			dB
$\Delta V_{PRE(L2L1)}$			1.6			
$\Delta V_{PRE(L3L2)}$			1.6			
$\Delta V_{ConsBit}$	Nontransition bit voltage variation	See CTS spec section 3.3.5			30%	
$A_{EQ(HBR)}$	Equalizer gain for RBR/HBR	See Table 3 for EQ setting details; Max value represents the typical value for the maximum configurable EQ setting			9	dB
$A_{EQ(HBR2)}$	Equalizer gain for HBR2				18	dB
$A_{EQ(TMDS)}$	Equalizer gain for TMDS				3	dB
R_{OUT}	Driver output impedance			50		Ω
R_{IN}	Input termination impedance		40	50	60	Ω
V_{Iterm}	Input termination voltage	AC coupled; self-biased	0		2	V
$V_{OCM(SS)}$	Steady state output common-mode voltage		0		2	V

(1) Values are V_{DD} supply measurements; V_{CC} supply (DS package option) measurements are 5 mA (typical) and 8 mA (max), with zero current in shutdown and standby modes.

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{OCM(SS)}$	Change in steady state output common-mode voltage between logic levels	Tested in compliance to section 3.10 in CTS 1.1a		10		mV_{PP}
$V_{OCM(PP)}$	Output common-mode noise	HBR2		20		mV_{RMS}
				30		
$V_{SQUELCH}$	Squelch threshold voltage	Programable through I^2C; default at 80 mVpp typical		80		mV_{PP}
$I_{TXSHORT}$	Short circuit current limit	Main Link outputs shorted to GND			50	mA
HPD_SRC, CAD_SRC						
V_{OH}	High-level output voltage	I_{OH} = 500 µA	2.7		3.6	V
V_{OL}	Low-level output voltage	I_{OH} = 500 µA	0		0.1	V
R_{outCAD}	CAD series output resistance[2]	EN = RSTN = V_{CC}; HPD_SNK = CAD_SNK = V_{CC}		150		Ω
R_{outHPD}	HPD series output resistance	EN = RSTN = V_{CC}; HPD_SNK = CAD_SNK = V_{CC}		150		Ω
I_{LEAK}	Leakage current [3]	V_{CC} = 0 V, V(pin) = 1.2 V; RSTN			20	µA
		V_{CC} = 0 V, V(pin) = 3.3 V; SCL/SDA_CTL, AUX_SNKp/n			20	
		V_{CC} = 0 V, V(pin) = 3.3 V; HPD_SNK			40	
		V_{CC} = 0 V, V(pin) = 3.3 V; AUX_SRCp/n			60	
HPD_SNK						
I_H	High-level input current	V_{IH} = 1.9 V (leakage includes the 130-kΩ pull-down resistor)	–30		30	µA
I_L	Low-level input current	V_{IL} = 0.8 V (leakage includes the 130-kΩ pull-down resistor)	–30		30	µA
V_{TH+}	Positive going input threshold voltage			1.4		V
R_{pdHPD}	HPD input termination to GND	V_{CC} = 0 V	100	130	160	kΩ
CAD_SNK						
I_H	High-level input current	V_{IH} = 1.9 V	–1		1	µA
I_L	Low-level input current	V_{IL} = 0.8 V	–1		1	µA
V_{TH+}	Positive going input threshold voltage			1.4		V
AUX/DDC/I^2C						
V_{PASS}	DDC mode passthrough voltage	V_{CAD_SNK} = V_{IH}; I_O = 100 µA	1.9			V
C_{IO}	I/O capacitance	V_{IO} = 0 V; f(test) = 1 MHz		10		pF
r_{ON}	On resistance AUX_SRCn to AUX_SNKn in DP mode	V_{CC} = 3 V w/ V_I = 2.85 V or V_{CC} = 3.6 V w/ V_I = 3.4 V; I_O = 5 mA		5	10	Ω
	On resistance SCL/SDA_DDC to AUX_SNK in TMDS mode	I_O = 3 mA		15	30	
	On resistance AUX_SRC to AUX_SNK in TMDS mode	I_O = 3 mA		10	20	
Δr_{ON}	On resistance variation with input signal voltage change in DP mode	V_{CC} = 3.6 V, I_O = 5 mA, V_I = 2.6 to 3.4 V, V_{CC} = 3 V, I_O = 5 mA, V_I = 0 to 0.4 V			5	Ω
$V_{ID(HYS)}$	Differential input hysterisis	By design (simulation only)		50		mV
I_H	High-level input current	V_I = V_{CC}	–5		5	µA

(2) A series output resistance of 100kΩ may be added in series to the CAD_SRC output to mimic a cable adapter.
(3) Applies to failsafe inputs: RSTN, SDA_CTL, SCL_CTL, SDA_DDC, SCL_DDC, AUX_SNK P/N, AUX_SRC P/N, HPD_SNK

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_L	Low-level input current	V_I = GND; CAD_SNK = V_{IH}	–5		5	µA
		V_I = GND; At DDC inputs			80	
V_{AUX+}	Voltage on the Aux+ for PHY-CTS 3.19	1M (5%) pullup to V_{CC} and 100-kΩ pulldown to GND on AUX+; V_{CC} = 3.3 V	0		0.4	V
V_{AUX-}	Voltage on the Aux- for PHY-CTS 3.18	100 kΩ pullup to V_{CC} and 1M (5%) pulldown to GND on AUX-; V_{CC} = 3.3 V	2.4		3.6	V
$\|S_{1122}\|$	Differential line insertion loss	V_{ID} = 400 mV, AC coupled; p-channel biasing 0.3 V and N-channel 3 V; 360-MHz sine wave; CAD_SNK = V_{IL}		1.6	3	dB
R_{DDC}	Switcheable pul-lup resistor on DDC at source side (SCL_DDC, SDA_DDC)	CAD_SNK = V_{IH}	48	60	72	kΩ

7.7 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MAIN LINK						
t_{PD}	Propagation delay time	See Figure 10		300		ps
$t_{SK(1)}$	Intra-pair output skew	Signal input skew = 0ps; d_R = 2.7 Gbps, V_{PRE} = 0 dB, 800 mVp-p, D10.2 clock pattern at device input; See Figure 11			20	ps
$t_{SK(2)}$	Inter-pair output skew				100	ps
Δt_{jit}	Total peak-to-peak residual jitter	$V_{OD(L0)}$; $V_{PRE(L0)}$; EQ = 8 dB; clean source; minimum input and output cabling; 1.62 Gbps, 2.7 Gbps, and 5.4 Gbps PRBS7 data pattern.			15	ps
t_{sq_enter}	Squelch entry time	Time from active DP signal turned off to ML output off with noise floor minimized	10		120	µs
t_{sq_exit}	Squelch exit time	Time from DP signal on to ML output on	0		1	µs
HPD/CAD						
$t_{PD(HPD)}$	Propagation delay HPD_SNK to HPD_SRC	V_{CC} = 3 V; See Figure 1			50	ns
$t_{PD(CAD)}$	Propagation delay CAD_SNK to CAD_SRC				50	ns
$t_{T(HPD)}$	HPD logic shut off time	V_{CC} = 3 V; See Figure 2			400	ms
AUX/DDC/I^2C						
$t_{sk(AUX)}$	Intra-pair skew	V_{ID} = 400 mV, AC coupled; p-channel biasing 0.3V and N-channel 3 V; See Figure 13			400	ps
$t_{PLH(DP)}$	Propagation delay time, low to high	CAD = V_{IL}; 1-Mbps pattern;See Figure 14			3	ns
$t_{PHL(DP)}$	Propagation delay time, high to low				3	ns
$t_{PLH(DDC)}$	Propagation delay time, low to high	CAD = V_{IH}; 100-kbps pattern			50	ns
$t_{PHL(DDC)}$	Propagation delay time, high to low				50	ns
$t_{PU(AUX)}$	Main Link D3 wake-up time	V_{ID} = 0.1 V, V_{ICMM} = 2-V source side (before AC coupling caps)			50	µs
I^2C						
Refer to the I^2C-Bus Specification, Version 2.1 (January 2000); SN75DP130 meets the switching characteristics for standard mode transfers up to 100 kbps.						

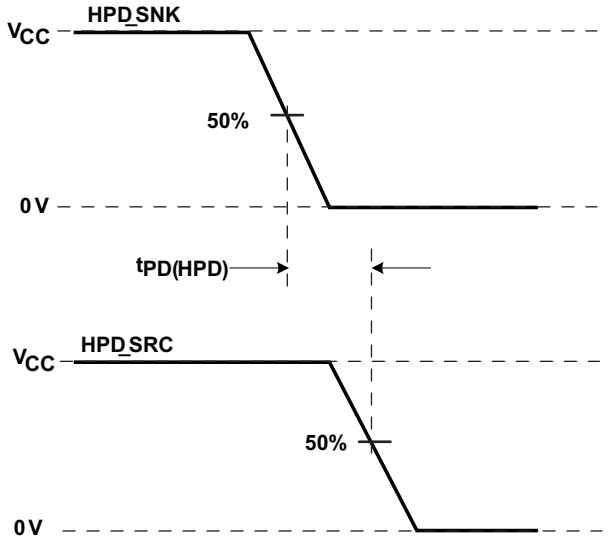


Figure 1. HPD Timing Diagram 1

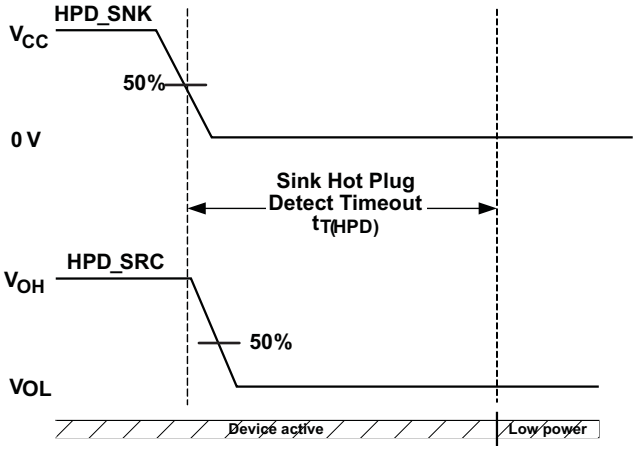
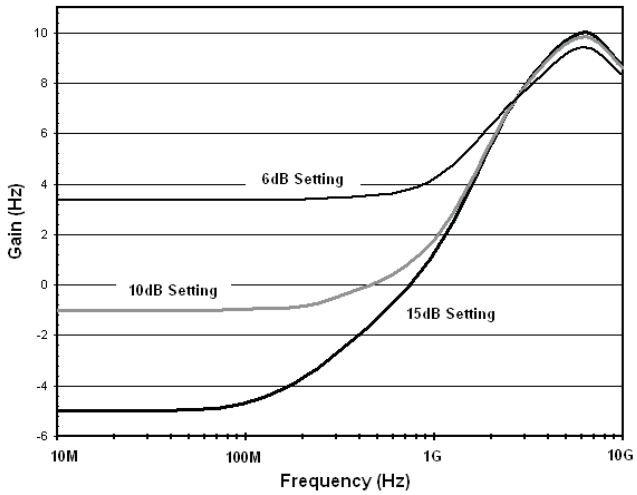


Figure 2. HPD Timing Diagram 2

7.8 Typical Characteristics

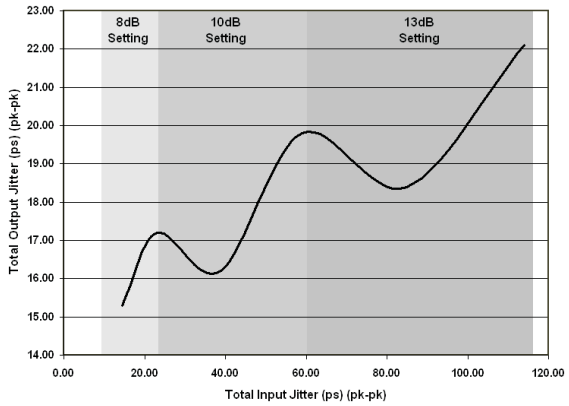
Table 1. Characterization Test Board Trace Lengths Related to Input Jitter

INPUT MODE	TRACE LENGTH (INCHES)	TOTAL INPUT JITTER (ps)	RECOMMENDED EQ SETTING
Display Port HBR2	2	14.4	8
	6	23.1	8
	10	38.8	10
	14	58.9	10
	18	84.8	13
	22	113.9	13
TMDS 3.4 Gbps	2	15.8	6
	6	21.3	6
	10	33.2	6
	14	49.9	13
	18	70.5	13
	22	91.5	13



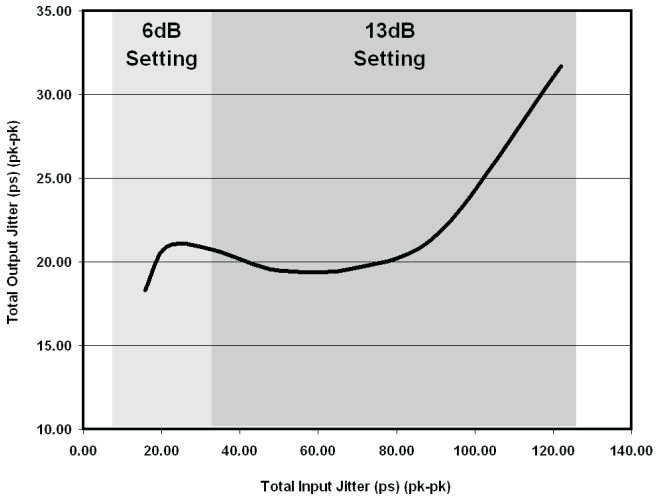
Gain represents SN75DP130 design simulation.

Figure 3. Typical EQ Gain Curves



DisplayPort output jitter measured at the surface mount pins connected to the main link output channels on the SN75DP130 characterization test board; input jitter generated from test board with variable input trace lengths using 4 mil traces of lengths 2 inches to 22 inches generating the typical input jitter as represented in Table 1.

Figure 4. DisplayPort Sink Jitter Performance With Optimal EQ Settings



DisplayPort output jitter measured at the surface mount pins connected to the main link output channels on the SN75DP130 characterization test board; input jitter generated from test board with variable input trace lengths using 4 mil traces of lengths 2 inches to 22 inches generating the typical input jitter as represented in Table 1.

Figure 5. TMDS Sink jitter Performance With Optimal EQ Settings

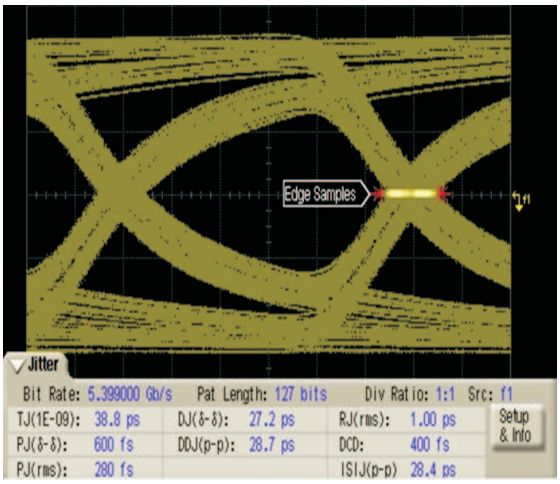


Figure 6. Main Link Input With 10-Inch Trace; DisplayPort Sink

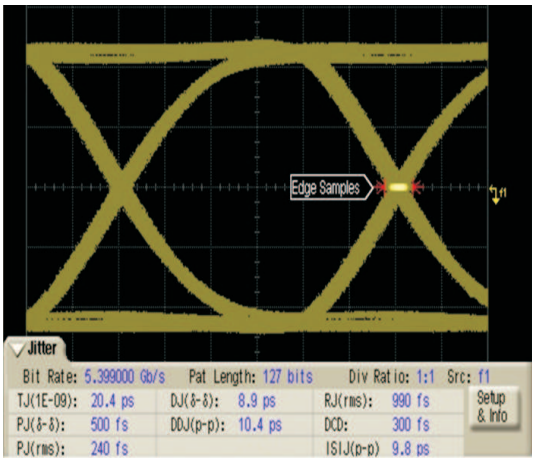


Figure 7. SN75DP130 Output; 10-Inch Input Trace; 13-dB EQ Setting; DP Sink

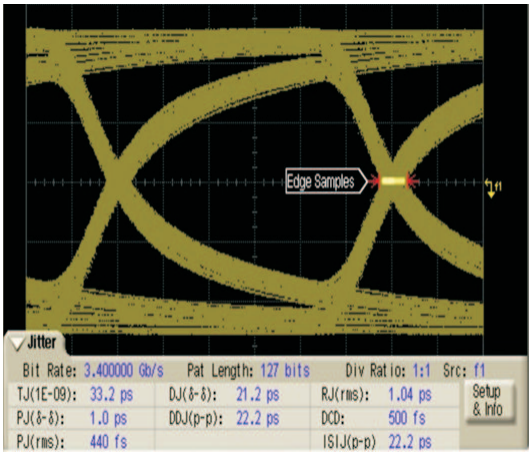


Figure 8. Main Link Input With 10-Inch Trace; TMDS Sink

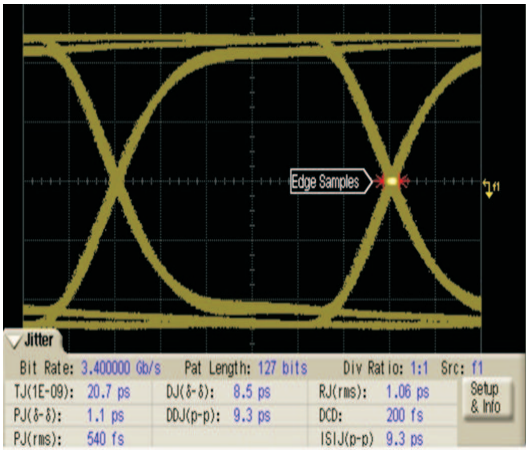


Figure 9. SN75DP130 Output; 10-Inch Input Trace; 13-dB EQ Setting; TMDS Sink

8 Parameter Measurement Information

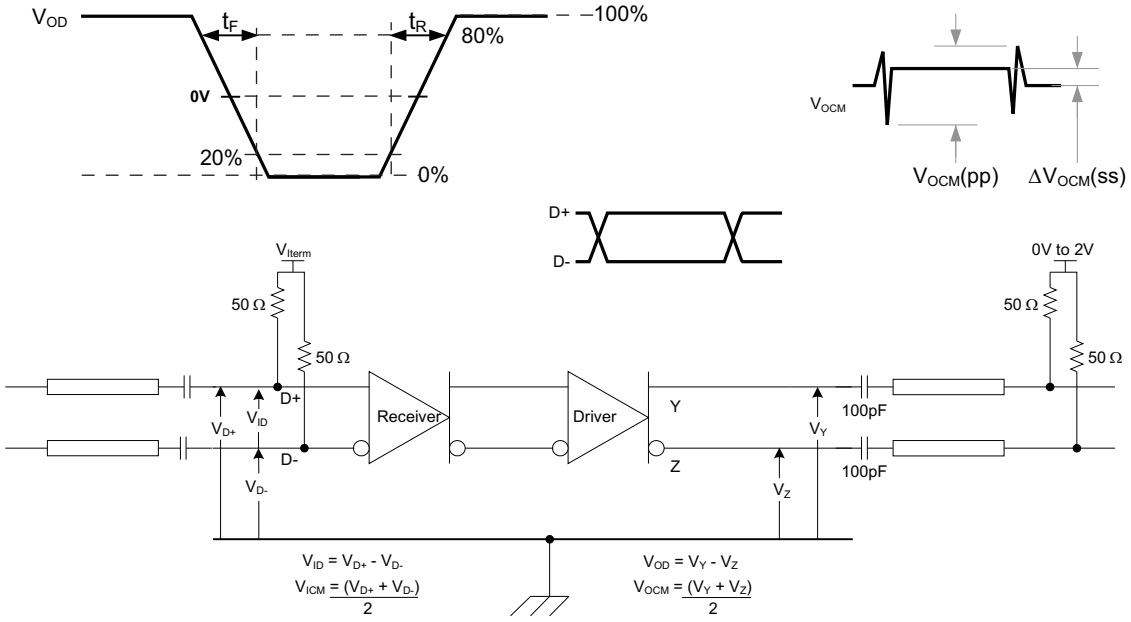


Figure 10. Main Link Test Circuit

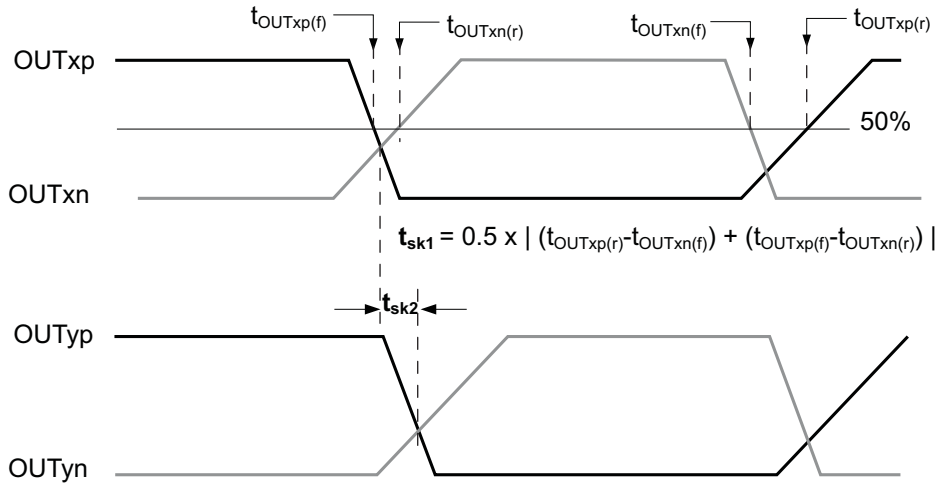


Figure 11. Main Link Skew Measurements

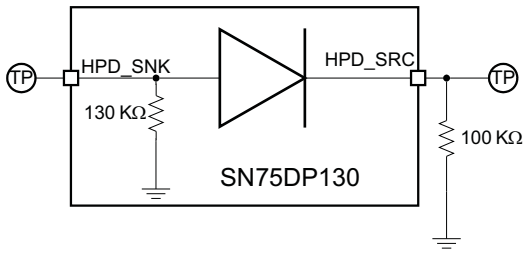


Figure 12. HPD Test Circuit

Parameter Measurement Information (continued)

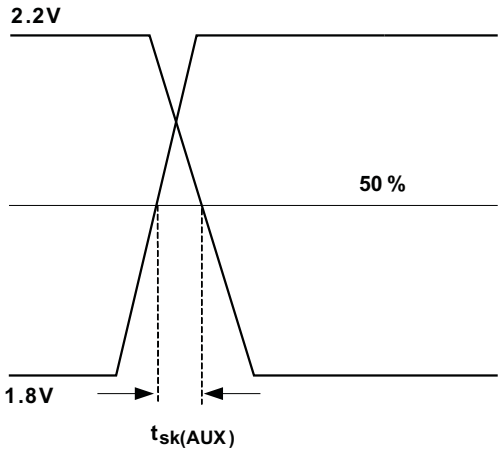


Figure 13. AUX Skew Measurement

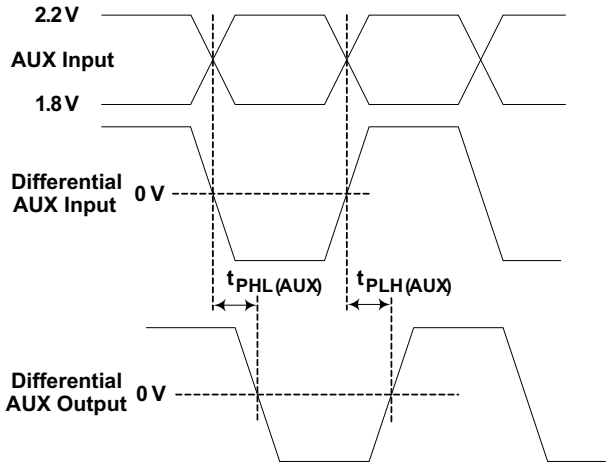


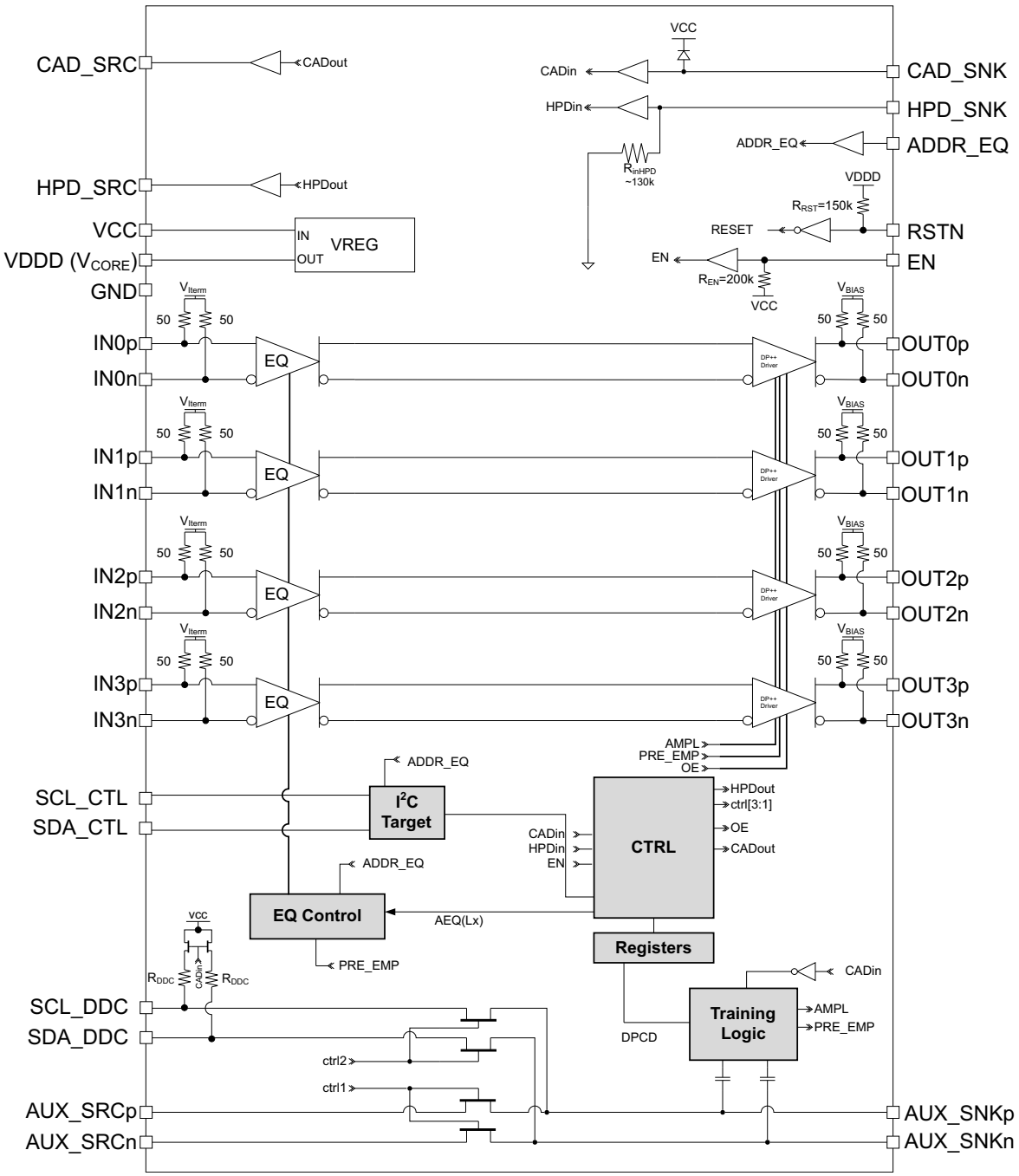
Figure 14. AUX Delay Measurement

9 Detailed Description

9.1 Overview

The SN75DP130 DisplayPort (DP) re-driver that regenerates the DP high-speed digital link. The device complies with the VESA DisplayPort Standard Version 1.2, and supports a 4-lane main link interface signaling up to HBR2 rates at 5.4 Gbps per lane. The device compensates for ISI loss across a transmission line to provide the optimum DP electrical performance from source to sink. The SN75DP130 is typically used in source applications either on a motherboard or in a docking station. With its large amount of equalization gain and ability to adjust its outputs levels, the DP130 can also be used in a sink application.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Reset Signal

The SN75DP130 RSTN input gives control over the device reset and to place the device into shutdown mode. When RSTN is low, all DPCD registers are reset to their default values, and all Main Link lanes are disabled. When the RSTN input returns to a high logic level, the device comes out of the shutdown mode. To turn on the Main Link, it is necessary to either program the DPCD registers through the local I^2C interface or to go through a full sequence of Link Training between DP source and DP sink.

It is critical to reset the digital logic of the SN75DP130 after the V_{DDD} supply is stable (that is, V_{DDD} has reached the minimum recommended operating voltage). This is achieved by asserting the RSTN input from low to high. A system may provide a control signal to the RSTN signal that transitions low to high after the V_{DDD} supply is stable, or implement an external capacitor connected between RSTN and GND, to allow delaying the RSTN signal during power up. The implementations are shown in Figure 15 and Figure 16.

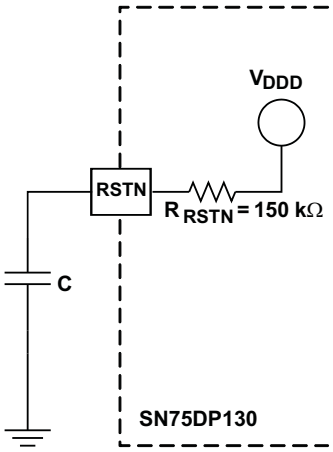


Figure 15. External Capacitor Controlled RSTN

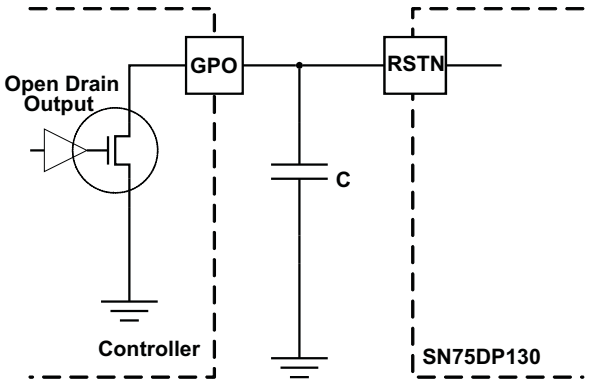


Figure 16. RSTN Input from Active Controller

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{DDD} supply where a slower ramp-up results in a larger value external capacitor.

Refer to the latest reference schematic for the SN75DP130 device and/or consider approximately 200-nF capacitor as a reasonable first estimate for the size of the external capacitor.

When implementing a RSTN input from an active controller, it is recommended to use an open-drain driver if the RSTN input is driven. This protects the RSTN input from damage of an input voltage greater than V_{DDD}.

9.3.2 Hot Plug Detect and Cable Adapter Detect

The SN75DP130 generates the Hot Plug Detect (HPD_SRC) signal to indicate to the source that a sink has been detected. A low HPD_SNK signal input indicates no sink device is connected. When HPD_SNK is high, the CAD_SNK signal indicates whether a DP sink (CAD_SNK=low) or a TMDS sink (CAD_SNK=high).

A sink device can request a source device interrupt by pulling the HPD_SNK signal low for a duration of 0.5 ms to 1 ms. The interrupt passes through the SN75DP130. If the HPD_SNK signal goes low for longer than 2 ms, the DP source determines that the sink device is disconnected. To conserve power, the SN75DP130 will go into a power saving Standby mode after the HPD signal went low for a duration of $t_{T(HPD)}$.

In the TMDS mode the AUX training logic is disabled and the Main Link transmits with a fixed output voltage swing of 600mVpp; the pre-emphasis level is set to 0 dB. Output swing and pre-emphasis level are also adjustable by I^2C interface. In TMDS mode all four Main Link output lanes are enabled.

Through the local I^2C interface it is also possible to force the device to ignore HPD_SNK and CAD_SNK, and control HPD_SRC and CAD_SRC directly.

9.3.3 AUX and DDC Configuration

The SN75DP130 offers an AUX source channel (AUX_SRC), AUX sink channel (AUX_SNK), a selectable DDC interface (SDA_DDC/SCL_DDC) for TMDS mode, and a local I^2C control interface (SCL_CTL / SDA_CTL). Upon power-up, the SN75DP130 enables the connection between the AUX_SNK to the appropriate source interface based on CAD_SNK. Table 2 describes the switching logic, including the programmability through the local I^2C interface.

The DDC interface incorporates 60-kΩ pull-up resistors on SDA_DDC and SCL_DDC, which are turned on when CAD_SNK is high (TMDS mode) but turned off when CAD_SNK is low (DP mode).

Table 2. AUX and DDC Interface Configurations

HPD_SNK	I^2C REGISTER BIT 04.0	I^2C REGISTER BIT 04.1	CAD_SNK	AUX_SNK	AUX_SRC	DDC	AUX MONITOR	COMMENT
0	X	X	X	OFF	OFF	OFF	inactive	no sink detected; low power mode
1	0 (default; works for Intel, NVIDIA, and AMD)	0 (default)	0	ON	ON	OFF	active	DP sink detected; AUX_SNK connects to AUX_SRC
			1	ON	OFF	ON	inactive	TMDS cable adapter detected; DDC connects to AUX_SNK
	1 (NVIDIA, AMD special mode)		0	OFF	ON	OFF	active	DP sink detected; AUX_SNK disconnected from AUX_SRC; AUX_SNK monitors AUX training
			1	ON	ON	OFF	inactive	TMDS cable adapter detected; AUX_SNK connects to AUX_SRC and can be used to short AC coupling caps
	0	1	0	ON	ON	OFF	active	DP sink detected; AUX_SNK connects to AUX_SRC
			1				inactive	TMDS cable adapter detected; AUX_SRC connects to AUX_SNK
	1		undetermined					mode not recommended

9.3.4 Main Link Configuration

The EQ input stage is self-configuring based on Link Training. A variety of EQ settings are available through external pin configuration to accommodate for different PCB loss and GPU settings, and the I^2C interface may be used to fully customize EQ configuration lane-by-lane beyond the input pin configurability options, as described in Table 3.

Table 3. Main Link EQ Configurations

EQ_I2C_ENABLE (reg 05.7)	ADDR_EQ	CAD_SNK(1) VIL = DP VIH = TMDS	LINK TRAINING ON/OFF (reg 04.2)	LINK TRAINING AEQ(Lx)(2) LANE 0 to 2	LINK TRAINING AEQ(Lx)(2) LANE 3	DESCRIPTION
0 (default)	VIL	VIL	1 (default)	AEQ(L0) = 8 dB at 2.7 GHz AEQ(L1) = 6 dB at 2.7 GHz AEQ(L2) = 3.5 dB at 2.7 GHz AEQ(L3) = 0 dB at 2.7 GHz	same as Lane 0 to 2	automatic low-range EQ gain based on link training; DP mode
			0	AEQ(Lx) = 6 dB at 2.7 GHz		DP mode; fixed EQ
		VIH	x	EQ(Lx) = 6 dB at 2.7 GHz	3 dB at 1.35 GHz	TMDS mode; fixed EQ
	VIM	VIL	1	AEQ(Lx) = 8 dB at 2.7 GHz	same as Lane 0 to 2	DP mode; fixed EQ
			0	AEQ(Lx) = 8 dB at 2.7 GHz		DP mode; fixed EQ
		VIH	x	EQ(Lx) = 8 dB at 2.7 GHz	3 dB at 1.35 GHz	TMDS mode; fixed EQ
	VIH	VIL	1	AEQ(L0) = 15 dB at 2.7 GHz AEQ(L1) = 13 dB at 2.7 GHz AEQ(L2) = 10 dB at 2.7 GHz AEQ(L3) = 6 dB at 2.7 GHz	same as Lane 0 to 2	automatic high-range EQ gain based on link training; DP mode
			0	AEQ(Lx) = 13 dB at 2.7 GHz		DP mode; fixed EQ
		VIH	x	EQ(Lx) = 13 dB at 2.7 GHz	3 dB at 1.35 GHz	TMDS mode; fixed EQ
1	x	VIL	1	AEQ(Lx) = 0 dB at 2.7 GHz AEQ(Lx) I^2C programmable	same as Lane 0 to 2	DP mode; EQ fully programmable for each training level; EQ disabled by default
			0	AEQ(L1) = 0 dB at 2.7 GHz AEQ(L1) I^2C programmable		DP mode; EQ fully programmable by AEQ(L1) levels; default AEQ(L1) EQ setting at 6 dB At 2.7 GHz
		VIH	x		3 dB at 1.35 GHz	TMDS mode; fixed EQ

(1) Setting CAD_TEST_MODE (Reg 17.0) forces the SN75DP130 into a TMDS test mode even if no external CAD signal is present
(2) EQ setting is adjusted based on the output pre-emphasis level setting; the EQ setting is indifferent to the level of V_{OD}.

9.3.5 Link Training and DPCD

The SN75DP130 monitors the auxiliary interface access to DisplayPort Configuration Data (DPCD) registers during Link Training in DP mode to select the output voltage swing V_{OD}, output pre-emphasis, and the EQ setting of the Main Link. The AUX monitor for SN75DP130 supports Link Training in 1Mbps Manchester mode, and is disabled during TMDS mode (CAD_SNK=VIH).

The AUX channel is further monitored for the DisplayPort D3 standby command.

The DPCD registers monitored by SN75DP130 are listed in Figure 17. Bit fields not listed are reserved and values written to reserved fields are ignored.

Figure 17. DPCD Registers Used by the SN75DP130 AUX Monitor

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R/W	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. DPCD Registers Used by the SN75DP130 AUX Monitor

Address	Field	Type	Description
00100h	LINK_BW_SET	RW	Bits 7:0 = Link Bandwidth Setting Write Values: 06h – 1.62 Gbps per lane 0Ah – 2.7 Gbps per lane (default) 14h – 5.4 Gbps per lane *Note: any other value is reserved; the SN75DP130 will revert to 5.4 Gbps operation when any other value is written* Read Values: 00h – 1.62 Gbps per lane 01h – 2.7 Gbps per lane (default) 02h – 5.4 Gbps per lane
00101h	LANE_COUNT_SET	RW	Bits 4:0 = Lane Count Write Values: 00h – All lanes disabled (default) 01h – One lane enabled 02h – Two lanes enabled 04h – Four lanes enabled *Note: any other value is invalid and disables all Main Link output lanes* Read Values: 00h – All lanes disabled (default) 01h – One lane enabled 03h – Two lanes enabled 0Fh – Four lanes enabled
00103h	TRAINING_LANE0_SET	RW	Write Values: Bits 1:0 = Output Voltage V_{OD} Level 00 – Voltage swing level 0 (default) 01 – Voltage swing level 1 10 – Voltage swing level 2 11 – Voltage swing level 3 Bits 4:3 = Pre-emphasis Level 00 – Pre-emphasis level 0 (default) 01 – Pre-emphasis level 1 10 – Pre-emphasis level 2 11 – Pre-emphasis level 3 *Note: the following combinations are not allowed for bits [1:0]/[4:3]: 01/11, 10/10, 10/11, 11/01, 11/10, 11/11; setting to any of these invalid combinations disables all Main Link lanes until the register value is changed back to a valid entry* Read Values: Bits 1:0 = Output Voltage V_{OD} Level 00 – Voltage swing level 0 (default) 01 – Voltage swing level 1 10 – Voltage swing level 2 11 – Voltage swing level 3 Bits 3:2 = Pre-emphasis Level 00 – Pre-emphasis level 0 (default) 01 – Pre-emphasis level 1 10 – Pre-emphasis level 2 11 – Pre-emphasis level 3

Table 4. DPCD Registers Used by the SN75DP130 AUX Monitor (continued)

Address	Field	Type	Description
00104h	TRAINING_LANE1_SET	RW	Sets the V_{OD} and pre-emphasis levels for lane 1
00105h	TRAINING_LANE2_SET	RW	Sets the V_{OD} and pre-emphasis levels for lane 2
00106h	TRAINING_LANE3_SET	RW	Sets the V_{OD} and pre-emphasis levels for lane 3
0010F	TRAINING_LANE0_1_SET2	RW	Write Values: Bits 1:0 = Lane 0 Post Cursor 2 00 – IN0 expects post cursor2 level 0; OUT0 transmits at post cursor 2 level 0 01 – IN0 expects post cursor2 level 1; OUT0 transmits at post cursor 2 level 0 10 – IN0 expects post cursor2 level 2; OUT0 transmits at post cursor 2 level 0 11 – IN0 expects post cursor2 level 3; OUT0 transmits at post cursor 2 level 0 Bits 5:4 = Lane 1 Post Cursor 2 00 – IN1 expects post cursor2 level 0; OUT1 transmits at post cursor 2 level 0 01 – IN1 expects post cursor2 level 1; OUT1 transmits at post cursor 2 level 0 10 – IN1 expects post cursor2 level 2; OUT1 transmits at post cursor 2 level 0 11 – IN1 expects post cursor2 level 3; OUT1 transmits at post cursor 2 level 0 Read Values: Bits 1:0 = Lane 0 Post Cursor 2 00 – IN0 expects post cursor2 level 0; OUT0 transmits at post cursor 2 level 0 01 – IN0 expects post cursor2 level 1; OUT0 transmits at post cursor 2 level 0 10 – IN0 expects post cursor2 level 2; OUT0 transmits at post cursor 2 level 0 11 – IN0 expects post cursor2 level 3; OUT0 transmits at post cursor 2 level 0 Bits 3:2 = Lane 1 Post Cursor 2 00 – IN1 expects post cursor2 level 0; OUT1 transmits at post cursor 2 level 0 01 – IN1 expects post cursor2 level 1; OUT1 transmits at post cursor 2 level 0 10 – IN1 expects post cursor2 level 2; OUT1 transmits at post cursor 2 level 0 11 – IN1 expects post cursor2 level 3; OUT1 transmits at post cursor 2 level 0
0110F	TRAINING_LANE2_3_SET2	RW	Bit definition identical to that of TRAINING_LANE_0_1_SET2 but for lanes 2 (IN2/OUT2) and lane 3 (IN3/OUT3)
00600h	SET_POWER	RW	Bits 1:0 = Power Mode Write Values: 01 – Normal mode (default) 10 – Power down mode; D3 Standby Mode The Main Link and all analog circuits are shut down and the AUX channel is monitored during the D3 Standby Mode. The device exits D3 Standby Mode by access to this register, when CAD_SNK goes high, or if DP_HPD_SNK goes low for longer than $t_{T(HPD)}$, which indicates that the DP sink was disconnected, or that the PRIORITY control has selected the HDMI/DVI sink. *Note: setting the register to the invalid combination 0600h[1:0] = 00 or 11 is ignored by the device and the device remains in normal mode* Read Values: 00 – Normal mode (default) 01 – Power-down mode; D3 Standby Mode

9.3.6 Equalization

The SN75DP130 includes a flexible continuous time linear equalizer (CTLE) to compensate for trace or cable loss at its input. When the SN75DP130 is in DP mode, the equalization is self-configuring based on link training commands that are monitored on the AUX channel. The host can configure the desired equalization values, on a lane-by-lane basis, through I^2C control. These I^2C equalization values are then automatically implemented based on the results of link training.

When the SN75DP130 is in TMDS mode, the equalization applied is based on external pin settings and I^2C settings. (See Table 3 for details.)

9.3.7 Configurable Outputs

The SN75DP130 driver on each channel provides flexibility in setting output voltage swing as well as driver de-emphasis. Four levels of output voltage swing and four levels of de-emphasis settings are independently available. Channel equalization coupled with output configurability allows for optimizing the device output eyes across a wide range of channel environments.

9.3.8 Squelch

The SN75DP130 incorporates selectable output signal squelch for conditions when the device input signal does not meet preset thresholds. Main link lane 0 incorporates an activity detector which is enabled through I^2C control. The activity detection threshold is selectable, through I^2C, from four predefined values ranging from 40 mVpp to 250 mVpp. When squelch is enabled and the activity monitor determines that the lane O input signal falls below the selected threshold, the device output drivers are disabled.

9.4 Device Functional Modes

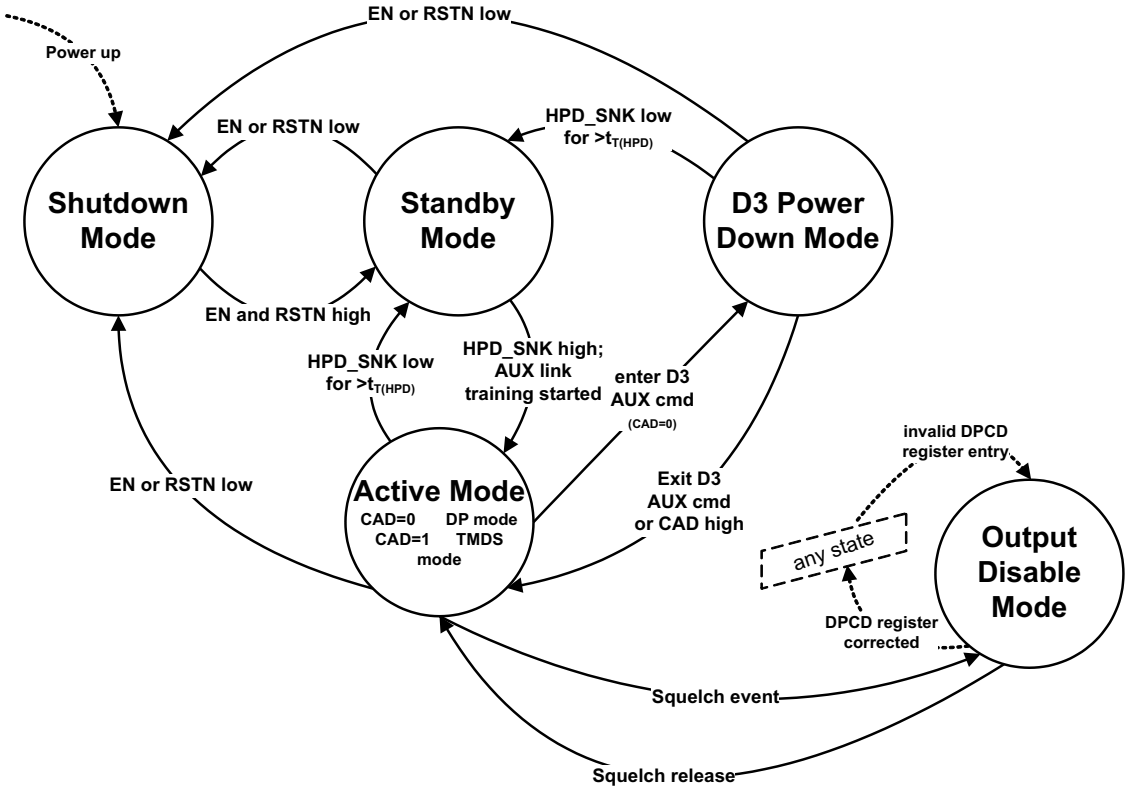


Figure 18. SN75DP130 Operating Modes Flow Diagram

Device Functional Modes (continued)

Table 5. Description of SN75DP130 Operating Modes

MODE	CHARACTERISTICS	CONDITIONS
Shutdown Mode	Least amount of power consumption (most circuitry turned off); HPD_SRC reflects HPD_SNK state; all other outputs are high-impedance; if RSTN is high local I^2C IF remains active; if RSTN is low local I^2C interface is turned off, all other inputs are ignored, and AUX DPCD is reset. (EN=low does not reset DPCD)	EN or RSTN is low; Power on default mode
Standby Mode	Low power consumption (I^2C interface is active; AUX monitor is inactive); Main Link outputs are disabled;	EN and RSTN are high; HPD_SNK low longer than $t_{T(HPD)}$
D3 Power Down Mode	Low power consumption (I^2C interface is active; AUX monitor active in DP mode); Main Link outputs are disabled;	EN and RSTN are high; AUX cmd requested DP sink to enter D3 power saving mode
Active Mode	Data transfer (normal operation); The device is either in TMDS mode (CAD_SNK=high) or DP mode (CAD_SNK=low); In DP mode, the AUX monitor is actively monitoring for Link Training; the output signal swing and input equalization setting depend on the Link Training or I^2C settings; the AUX SRC channel is active; the AUX SNK and DDC are active unless disabled through I^2C interface. At power-up all Main Link outputs are disabled by default. AUX Link Training is necessary to overwrite the DPCD registers to enable Main Link outputs. In TMDS mode the output signal swing is 600mVpp unless this setting is adjusted by overwriting according registers through I^2C interface. Transactions on the AUX lines will be ignored.	EN and RSTN are high; HPD_SNK is high; HPD_SNK can also be low for less than $t_{Z(HPD)}$ (e.g., sink interrupt request to source)
Compliance Test Mode	Through I^2C registers the device can be forced into ignoring HPD_SNK and CAD_SNK, HPD_SRC and CAD_SRC are programmable; output swing, pre-emphasis and EQ setting are programmable; automatic power down features can be disabled	EN and RSTN is high; I^2C selects HPD and/or CAD test mode
Output Disable Mode	DPCD write commands on the AUX bus detected by the SN75DP130 will also write to the local DPCD register. The DPCD register should always be written with a valid entry. If register 101h or 103h is written with a forbidden value, the SN75DP130 disables the Main Link output signals, forcing the DP sink to issue an interrupt. The DP source can now retrain the link using valued DPCD register values. As soon as all DPCD registers contain a valid entry, the SN75DP130 switches back into the appropriate mode of operation.	EN and RSTN are high; DPCD register 101h or 103h entry is invalid

Table 6. Description of Operating Mode Transitions

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → Standby	Activate SN75DP130	EN and RSTN both transitioned high
Standby → Active	Turn on Main Link (DP sink plugged in)	HPD_SNK input asserts high
Active → D3 Power Down	DP source requests temporary power down for power savings	Receive D3 entry command on AUX
Active → Output Disable	Squelch event; inactive video stream	Main Link monitor detects the inactive video stream
D3 Power Down → Active	Exit temporary power down	Receive D3 exit command on AUX, or CAD_SNK input is asserted (high)
D3 Power Down → Standby	Exit temporary power down (DP sink unplugged)	HPD_SNK de-asserted to low for longer than $t_{T(HPD)}$
Active → Standby	Turn off Main Link (DP sink unplugged)	HPD_SNK de-asserted to low for longer than $t_{T(HPD)}$
Any → Shutdown	Turn off SN75DP130	EN or RSTN transitions low
Any → Output Disable	DPCD register access error condition	Invalid DPCD register access
Output Disable → Active	Squelch released; video stream reactivated	Main Link monitor detects active video stream
Output Disable → Any	DPCD register error condition is corrected	Appropriate operating mode is re-entered

9.5 Programming

9.5.1 I²C Interface Overview

The SN75DP130 I²C interface is enabled when EN and RSTN are input high. The SCL_CTL and SDA_CTL terminals are used for I²C clock and I²C data respectively. The SN75DP130 I²C interface conforms to the two-wire serial interface defined by the I²C Bus Specification, Version 2.1 (January 2000), and supports the standard mode transfer up to 100 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for SN75DP130 is factory preset to 01011xx with the two least significant bits being determined by the ADDR_EQ 3-level control input. Figure 19 clarifies the SN75DP130 target address.

Figure 19. SN75DP130 I²C Target Address Description

7 (MSB)	6	5	4	3	2	1	0 (W/R)
0	1	0	1	1	ADDR1	ADDR0	0/1

Note: ADDR_EQ = LOW: ADDR[1:0] = 00: W/R=58/59
ADDR_EQ = V_{CC}/2: ADDR[1:0] = 01: W/R=5A/5B;
ADDR_EQ = HIGH: ADDR[1:0] = 10: W/R=5C/5D

The following procedure is followed to write to the SN75DP130 I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SN75DP130 7-bit address and a zero-value "W/R" bit to indicate a write cycle
2. The SN75DP130 acknowledges the address cycle
3. The master presents the sub-address (I²C register within SN75DP130) to be written, consisting of one byte of data, MSB-first
4. The SN75DP130 acknowledges the sub-address cycle
5. The master presents the first byte of data to be written to the I²C register
6. The SN75DP130 acknowledges the byte transfer
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SN75DP130
8. The master terminates the write operation by generating a stop condition (P)

The following procedure is followed to read the SN75DP130 I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN75DP130 7-bit address and a one-value "W/R" bit to indicate a read cycle
2. The SN75DP130 acknowledges the address cycle
3. The SN75DP130 transmit the contents of the memory registers MSB-first starting at register 00h.
4. The SN75DP130 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer
5. If an ACK is received, the SN75DP130 transmits the next byte of data
6. The master terminates the read operation by generating a stop condition (P)

   No sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I²C master terminates the read operation.

Refer to *SN75DP130 Local I²C Control and Status Registers* for SN75DP130 local I²C register descriptions. Reads from reserved fields not described return zeros, and writes are ignored.

9.6 Register Maps

9.6.1 SN75DP130 Local I²C Control and Status Registers

Figure 20. Local I²C Control and Status Registers

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R/W	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Offset = 01h

Bit	Field	Type	Description
1	AUTO_POWERDOWN_DISABLE	RW	0 – The SN75DP130 automatically enters Standby mode based on HPD_SNK (default) 1 – The SN75DP130 will not automatically enter Standby mode
0	FORCE_SHUTDOWN_MODE	RW	0 – SN75DP130 is forced to Shutdown mode 1 – Shutdown mode is determined by EN input, normal operation (default)

Table 8. Offset = 02h

Bit	Field	Type	Description
7:0	TI_TEST	RW	This field defaults to zero value, and should not be modified.

Table 9. Offset = 03h

Bit	Field	Type	Description
5:4	SQUELCH_SENSITIVITY	RW	Main Link squelch sensitivity is selected by this field, and determines the transitions to and from the Output Disable mode. 00 – Main Link IN0p/n squelch detection threshold set to 40mVpp 01 – Main Link IN0p/n squelch detection threshold set to 80mVpp (default) 10 – Main Link IN0p/n squelch detection threshold set to 160mVpp 11 – Main Link IN0p/n squelch detection threshold set to 250mVpp
3	SQUELCH_ENABLE	RW	0 – Main Link IN0p/n squelch detection enabled (default) 1 – Main Link IN0p/n squelch detection disabled

Table 10. Offset = 04h

Bit	Field	Type	Description
3	TI_TEST	RW	This field defaults to zero value, and should not be modified.
2	LINK_TRAINING_ENABLE	RW	0 – Link Training is disabled. V_{OD} and Pre-emphasis are configured through the I²C register interface; the EQ is fixed when this bit is zero. 1 – Link Training is enabled (default)
1:0	AUX_DDC_MUX_CFG	RW	See Table 6 for details on the programming of this field. 00 – AUX_SNK is switched to AUX_SRC for DDC source side based on CAD_SNK (default) 01 – AUX_SNK is switched to AUX_SRC based on the CAD_SNK input, and used to short-circuit AC coupling capacitors in the TMDS operating mode. 10 – AUX_SNK is switched to AUX_SRC side based on the HPD_SNK inptu, while the DDC source interface remains disabled. 11 – Undefined operation

Table 11. Offset = 05h

Bit	Field	Type	Description
7	EQ_I2C_ENABLE	RW	0 – EQ settings controlled by device inputs only (default) 1 – EQ settings controlled by I^2C register settings
6:4	AEQ_L0_LANE0_SET	RW	This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)
2:0	AEQ_L1_LANE0_SET	RW	This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: ● I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled ● I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)

Table 12. Offset = 06h

Bit	Field	Type	Description
6:4	AEQ_L2_LANE0_SET	RW	This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)
2:0	AEQ_L3_LANE0_SET	RW	This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2)010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2)100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)

Table 13. Offset = 07h

Bit	Field	Type	Description
6:4	AEQ_L0_LANE1_SET	RW	This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)
2:0	AEQ_L1_LANE1_SET	RW	This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: ● I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled ● I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)

Table 14. Offset = 08h

Bit	Field	Type	Description
6:4	AEQ_L2_LANE1_SET	RW	This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)
2:0	AEQ_L3_LANE1_SET	RW	This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)

Table 15. Offset = 09h

Bit	Field	Type	Description
6:4	AEQ_L0_LANE2_SET	RW	This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)
2:0	AEQ_L1_LANE2_SET	RW	This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: ● I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled ● I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)

Table 16. Offset = 0Ah

Bit	Field	Type	Description
6:4	AEQ_L2_LANE2_SET	RW	This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)
2:0	AEQ_L3_LANE2_SET	RW	This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)

Table 17. Offset = 0Bh

Bit	Field	Type	Description
6:4	AEQ_L0_LANE3_SET	RW	This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)
2:0	AEQ_L1_LANE3_SET	RW	This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ mode: ● I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)

Table 18. Offset = 0Ch

Bit	Field	Type	Description
6:4	AEQ_L2_LANE3_SET	RW	This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)
2:0	AEQ_L3_LANE3_SET	RW	This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)

Table 19. Offset = 15h

Bit	Field	Type	Description
4:3	BOOST	RW	Controls the output pre-emphasis amplitude when the DisplayPort sink is selected; allows to reduce or increase all pre-emphasis settings by ~10%. Setting this field will impact V_{OD} when pre-emphasis is disabled. This setting also impacts the output in TMDS mode for the DisplayPort sink connection when the DisplayPort sink CAD_SNK input is high. 00 – Pre-emphasis reduced by ~10%; V_{OD} reduced by 10% if pre-emphasis is disabled. 01 – Pre-emphasis nominal (default) 10 – Pre-emphasis increased by ~10%; V_{OD} increased by 10% if pre-emphasis is disabled. 11 – Reserved
2	DP_TMDS_VOD	RW	Sets the target output swing in TMDS mode when the DisplayPort sink is selected, where CAD_SNK input is high. 0 – Low TMDS output swing (default) 1 – High TMDS output swing
1:0	DP_TMDS_VPRE	RW	Controls the output pre-emphasis in TMDS mode when the DisplayPort sink is selected, where CAD_SNK input is high. 00 – No TMDS pre-emphasis(default) 01 – Low TMDS pre-emphasis 10 – High TMDS pre-emphasis 11 – Reserved

Table 20. Offset = 17h

Bit	Field	Type	Description
3	HPD_TEST_MODE	RW	0 – Normal HPD mode. HPD_SRC reflects the status of HPD_SNK (default) 1 – Test mode. HPD_SNK is pulled high internally, and the HPD_SRC output is driven high and the Main Link is activated, depending on the squelch setting. This mode allows execution of 17h certain tests on SN75DP130 without a connected display sink.
1	CAD_OUTPUT_INVERT	RW	0 – CAD_SRC output high means TMDS cable adapter detected (default) 1 – CAD_SRC output low means TMDS cable adapter detected
0	CAD_TEST_MODE	RW	0 – Normal CAD mode. CAD_SRC reflects the status of CAD_SNK, based on the value of CAD_OUTPUT_INVERT (default) 1 – Test mode. CAD_SRC indicates TMDS mode, depending on the value of CAD_OUTPUT_INVERT; CAD_SNK input is ignored. This mode allows execution of certain tests on SN75DP130 without a connected TMDS display sink.

Table 21. Offset = 18h – 1Ah

Bit	Field	Type	Description
7:0	TI_TEST	RW	These registers shall not be modified.

Table 22. Offset = 1Bh

Bit	Field	Type	Description
7	I2C_SOFT_RESET	WO	Writing a one to this register resets all I^2C registers to default values. Writing a zero to this register has no effect. Reads from this register return zero.
6	DPCD_RESET	WO	Writing a one to this register resets the DPCD register bits (corresponding to DPCD addresses 103h – 106h, the AEQ_Lx_LANEy_SET bits). Writing a zero to this register has no effect. Reads from this register return zero.

Table 23. Offset = 1Ch

Bit	Field	Type	Description
3:0	DPCD_ADDR_HIGH	RW	This value maps to bits 19:16 of the 20-bit DPCD register address accessed through the DPCD_DATA register.

Table 24. Offset = 1DH

Bit	Field	Type	Description
7:0	DPCD_ADDR_MID	RW	This value maps to bits 15:8 of the 20-bit DPCD register address accessed through the DPCD_DATA register.

Table 25. Offset = 1Eh

Bit	Field	Type	Description
7:0	DPCD_ADDR_LOW	RW	This value maps to bits 7:0 of the 20-bit DPCD register address accessed through the DPCD_DATA register.

Table 26. Offset = 1Fh

Bit	Field	Type	Description
7:0	DPCD_DATA	RW	This register contains the data to write into or read from the DPCD register addressed by DPCD_ADDR_HIGH, DPCD_ADDR_MID, and DPCD_ADDR_LOW.

Table 27. Offset = 20h

Bit	Field	Type	Description
7:1	DEV_ID_REV.	RO	This field identifies the device and revision. 0000000 – SN75DP130 Revision 0
0	BIT_INVERT	R/W	The value read from this field is the inverse of that written. Default read value is zero.

Table 28. Offset = 21h

Bit	Field	Type	Description
7:0	TI_TEST	R/W	These registers shall not be modified.

Table 29. Offset = 22h – 27h

Bit	Field	Type	Description
7:0	TI_TEST_RESERVED	RO	These read only registers are reserved for test; writes are ignored.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN75DP130 offers separate AUX and DDC source interfaces that connect to a single AUX sink channel. This minimizes component count when implemented with a graphics processor (GPU) comprising separate DDC and AUX interfaces. For GPUs with combined DDC/AUX, the device can operate as a FET switch to short circuit the AUX channel AC coupling caps while connected to a TMDS sink device.

The configuration shown in Figure 21 supports a GPU with separate DDC and AUX interfaces, and overcomes the need for an external AUX to DDC switch. This circuit provides back current protection into the GPU AUX, HPD, and CAD inputs.

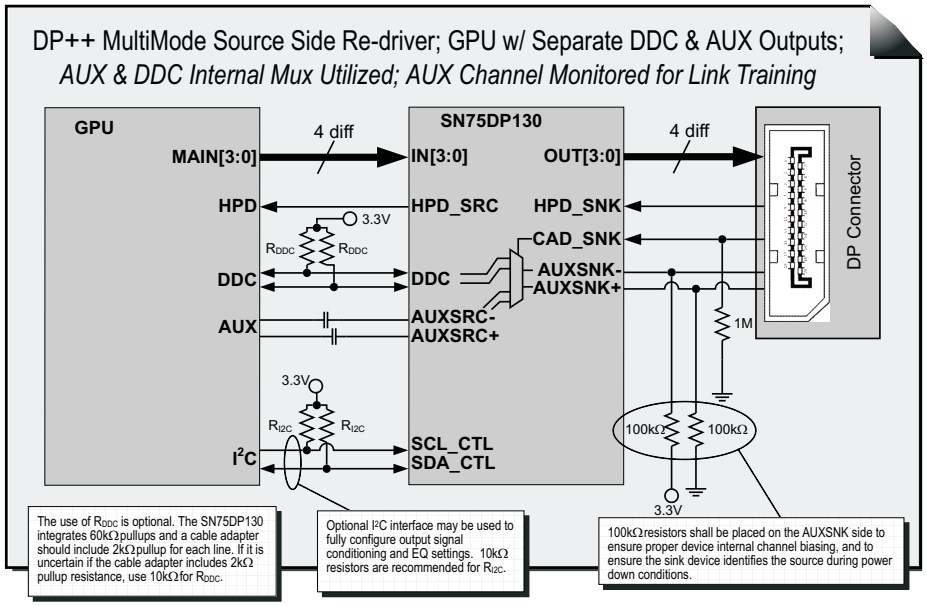


Figure 21. DP++ Dual-Mode in a Split AUX/DDC Configuration

Application Information (continued)

The configuration shown in Figure 22 is preferred to avoid very long AUX signal stub lines. Furthermore, this configuration provides isolation between the DP connector and the GPU.

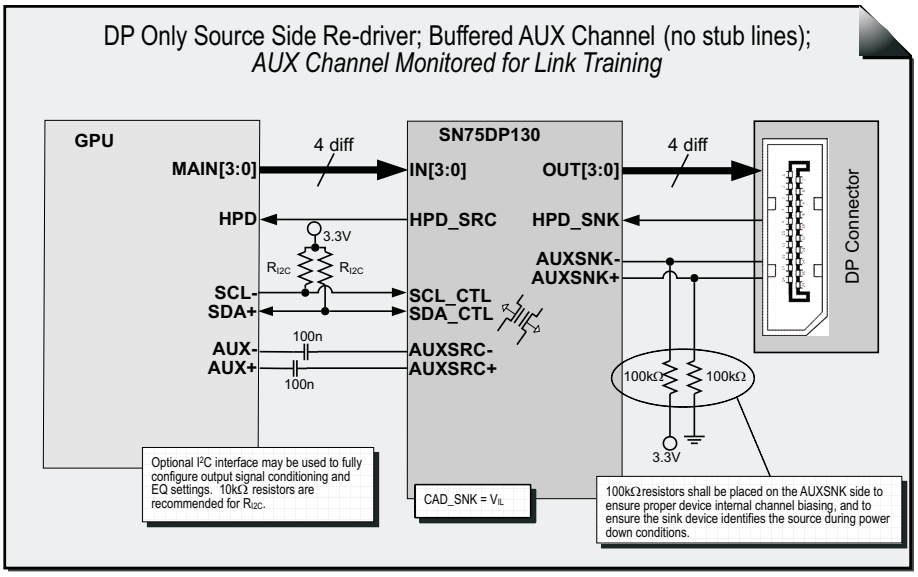


Figure 22. DP Only Configuration with AUX Pass Through

The configuration shown in Figure 23 enables the SN75DP130 in DP++ Dual-Mode with the AUX input only monitoring the AUX channel. Use this setting when AUX stub lines can be kept short and minimum AUX attenuation is desired. For DP v1.1a, the stub length shall not exceed 4cm each, and for DP v1.2 with FAUX support each stub line shall be shorter than 1cm.

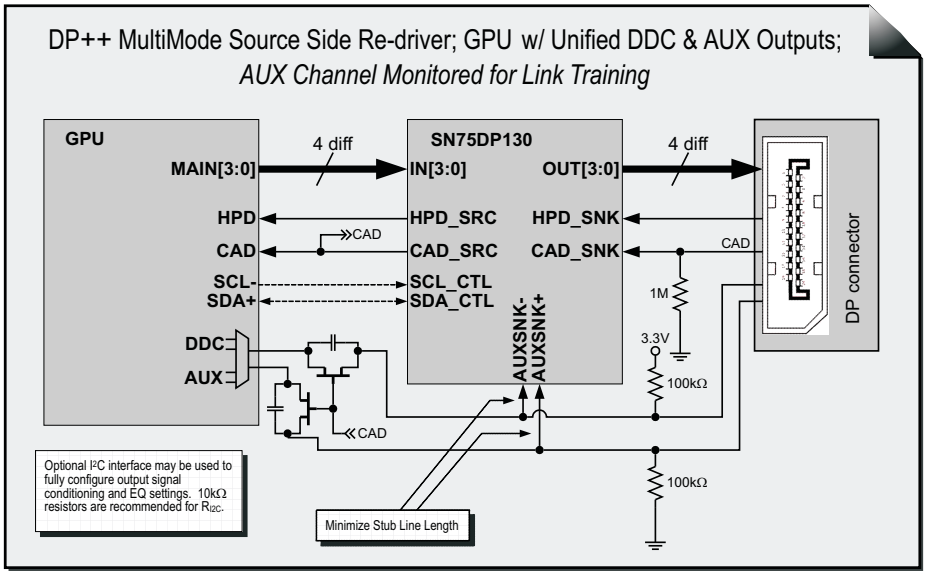


Figure 23. DP++ Dual-Mode Configuration with AUX Monitor

Application Information (continued)

The alternate configuration shown in Figure 24 allows a reduced BOM by eliminating the need for external FET switches while routing AUX and DDC externally, which eliminates any insertion loss cases of AUX is brought through the SN75DP130. For DP v1.2 with FAUX support each stub line shall be shorter than 1cm.

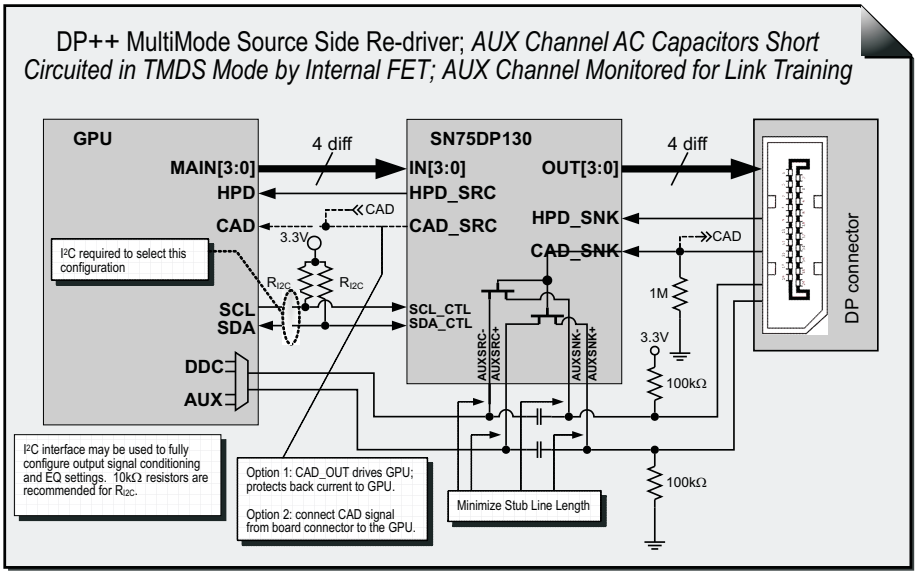


Figure 24. Alternate Low-BOM DP++ Dual-Mode Configuration

The previous application examples were specifically concerned with source side implementations of the SN75DP130. Even though source applications (notebook, docking station, and so forth) are the primary target application for the DP130A, the DP130A can also be used in a sink application, such as a DisplayPort monitor. The reader is referred to SLLA349 (*Implementation Guide: DP130 in a Sink*) for a detailed discussions of the implementation guidelines for sink applications.

10.2 Typical Application

The configuration shown in Figure 25 supports a GPU with unified AUX/DDC interfaces. This circuit provides back current protection into the GPU AUX, HPD, and CAD inputs.

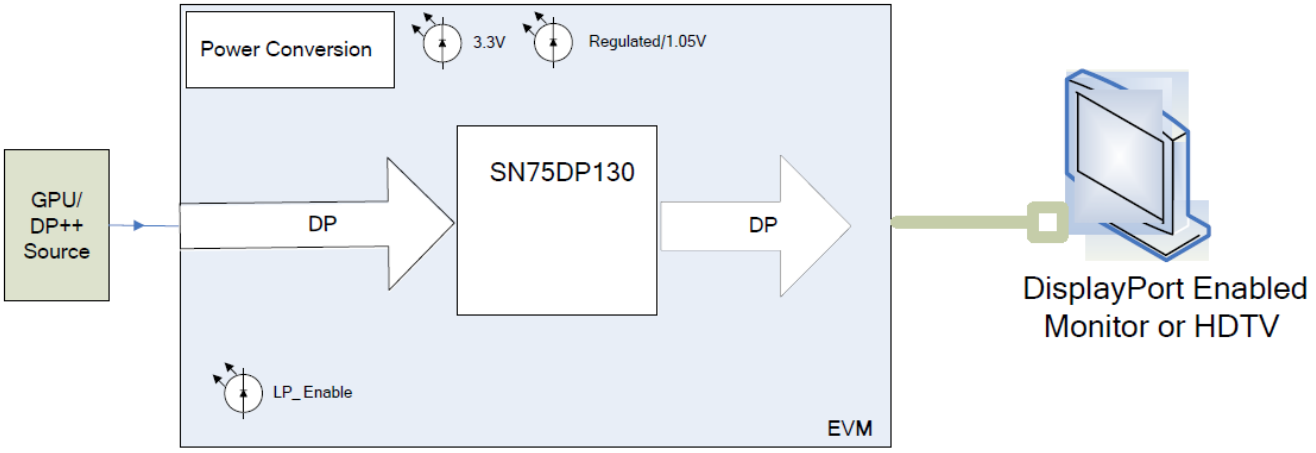


Figure 25. Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 30 as the input parameters.

Table 30. Design Parameters

DESIGN PARAMETERS	VALUE
VCC power supply	3.3 V
VDD power supply	1.1 V
DP single-ended impedance	50 Ω

10.2.2 Detailed Design Procedure

10.2.2.1 Logic I²C Interface

The internal registers of the SN75DP130 are accessed through the SCL_CTL pin and 3 SDA_CTL pin. The 7-bit I²C slave address of the DP130 is determined by the ADDR_EQ pin 4.

Table 31. I²C Slave Address Selection

ADDR_EQ	7-BIT I²C SLAVE ADDRESS	READ SLAVE ADDRESS	WRITE SLAVE ADDRESS
Low (VIL)	7'b0101100	'h59	'h58
VCC/2 (VIM)	7'b0101101	'h5B	'h5A
High (VIH)	7'b0101110	'h5D	'h5C

10.2.2.2 CAD Sink Over Ride

For testing and debug purposes, leave a place holder on the CAD_SNK input in order to have the option to independently set the DP130 in DP or TMDS mode. A 2k pull-up on this place holder will set the DP130 in TMDS mode independent of the Sink.

10.2.2.3 HPD Sink Over Ride

For testing and debug purposes, leave a place holder on the HPD_SNK input in order to have the option to force the presence of the sink. A 2k pull-up on this place holder will provide an indication of the sink presence.

10.2.3 Application Curves

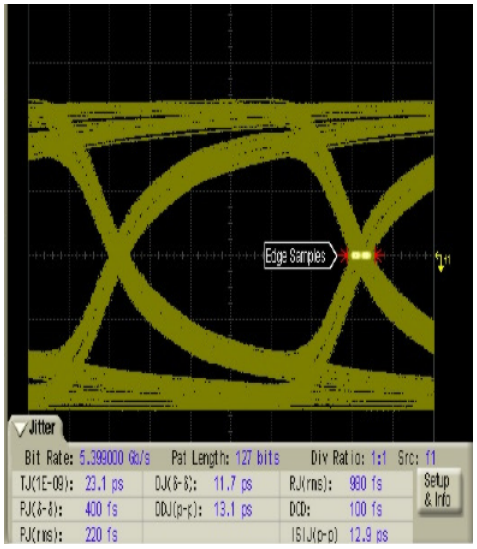


Figure 26. Input Into DP130

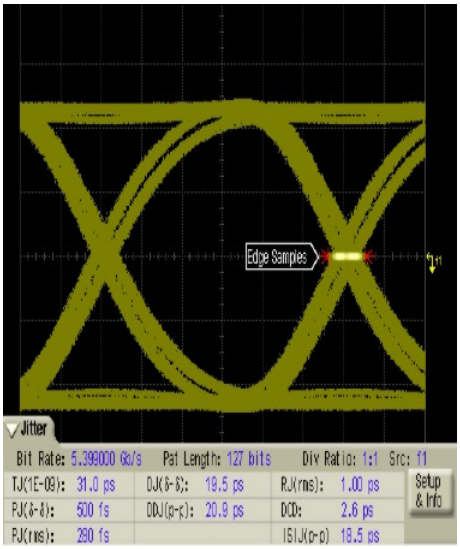


Figure 27. Eye Diagram (EQ = 3.5 dB)

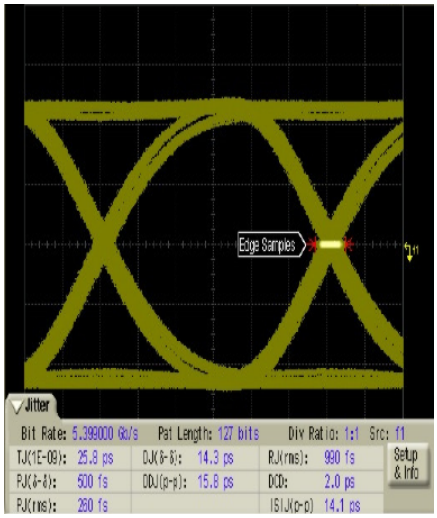


Figure 28. Eye Diagram (EQ = 6 dB)

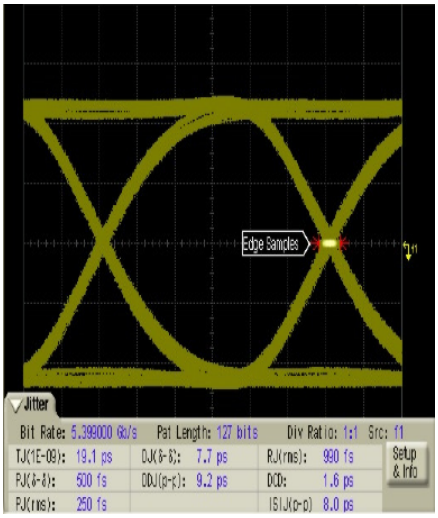


Figure 29. Eye Diagram (EQ = 8 dB)

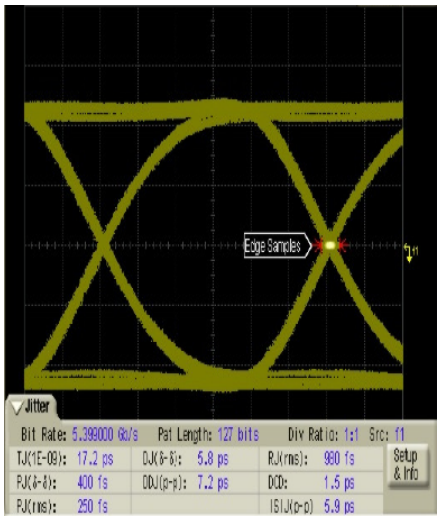


Figure 30. Eye Diagram (EQ = 10 dB)

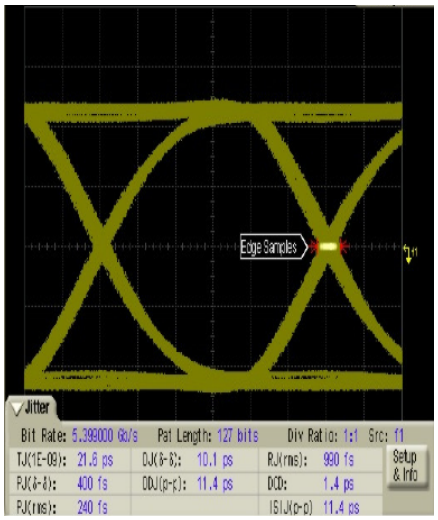


Figure 31. Eye Diagram (EQ = 13 dB)

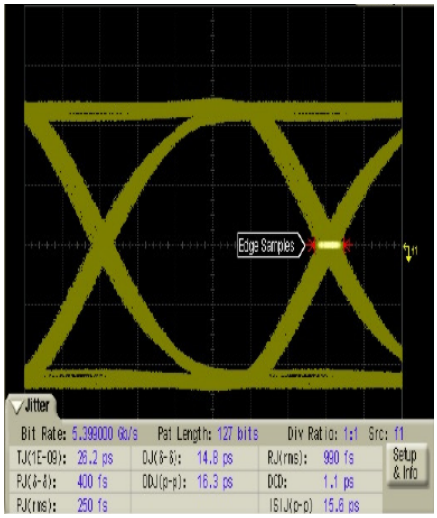


Figure 32. Eye Diagram (EQ = 15 dB)

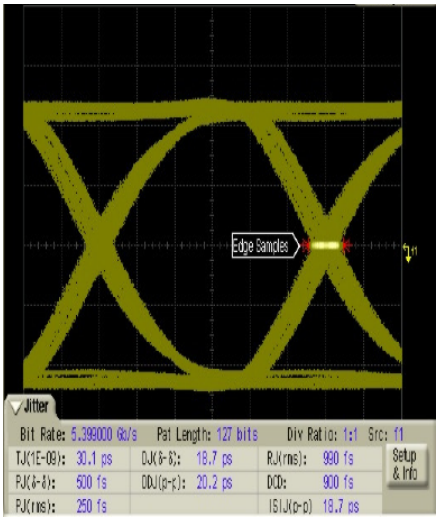


Figure 33. Eye Diagram (EQ = 18 dB)

11 Power Supply Recommendations

11.1 SN75DP130 Power Sequencing

The following power-up and power-down sequences describe how the RSTN signal is applied to the SN75DP130. See *Power Dissipation*.

11.1.1 Power-Up Sequence:

1. Apply V_{cc} with less than a 10-ms ramp time for the SN75DP130 and for the SN75DP130, apply V_{ddd} then V_{cc} (both having less than 10-ms ramp time) devices. V_{ddd} must be asserted first and stable for greater than 10 µs before V_{cc} is applied.
2. RSTN must remain asserted until V_{cc}/V_{ddd} voltage has reached minimum recommended operation for more than 100 µs.
3. De-assert RSTN (Note: This RSTN is a 1.05-V interface and is internally connected to V_{ddd_dreg} through a 150-kΩ resistor).
4. Device will be available for operation approximately 400 ms after a valid reset.

11.1.2 Power-Down Sequence:

1. Assert RSTN to the device.
2. Remove V_{cc} and V_{ddd}.

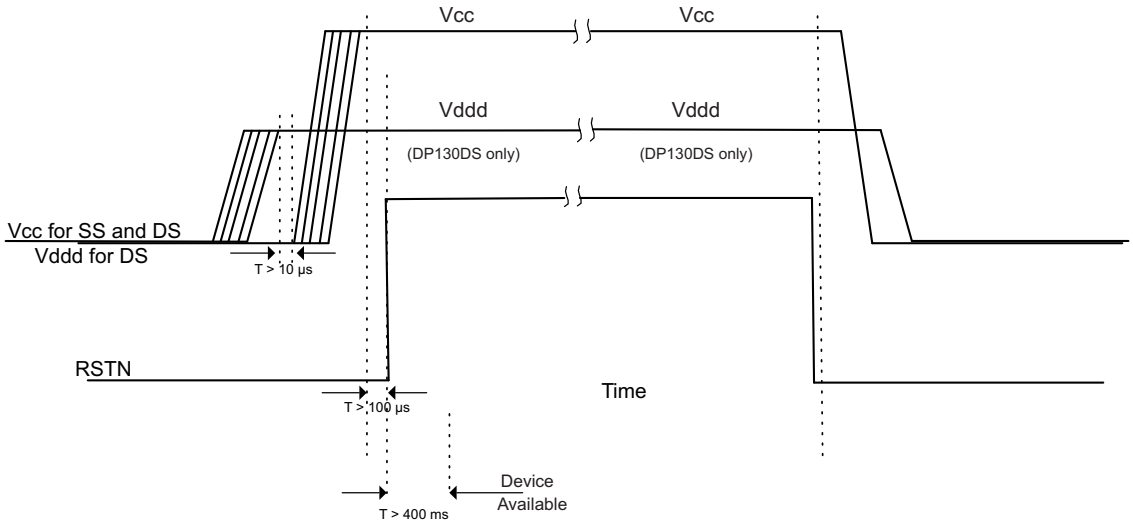


Figure 34. Power-Up and Power-Down Sequence

SN75DP130 Power Sequencing (continued)

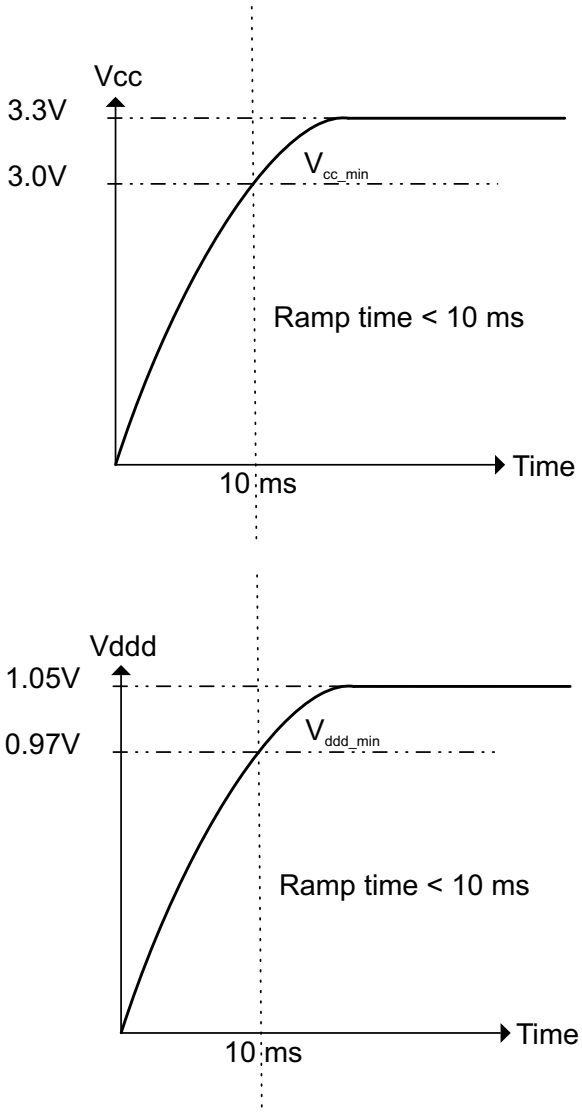


Figure 35. V_{CC}/V_{DDD} Ramp Recommendation

SN75DP130 Power Sequencing (continued)

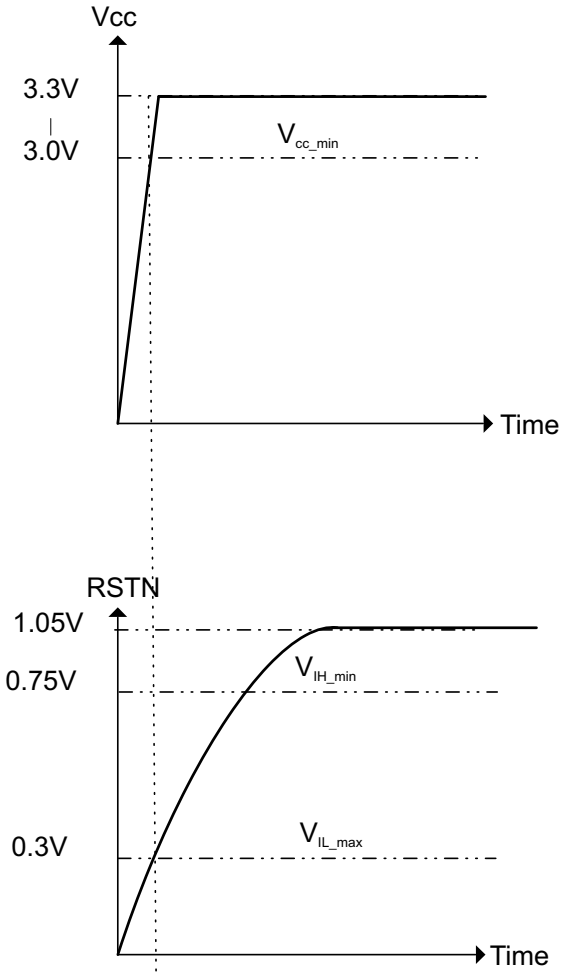


Figure 36. RSTN Voltage Thresholds

12 Layout

12.1 Layout Guidelines

- Decoupling with small current loops is recommended.
- TI recommends placing the decoupling capacitor as close as possible to the device and on the same side of the PCB.
- Choose the capacitor such that the resonant frequency of the capacitor does not align closely with 5.4 GHz.
- Also provide several GND vias to the thermal pad to minimize the area of current loops.

12.1.1 Layer Stack

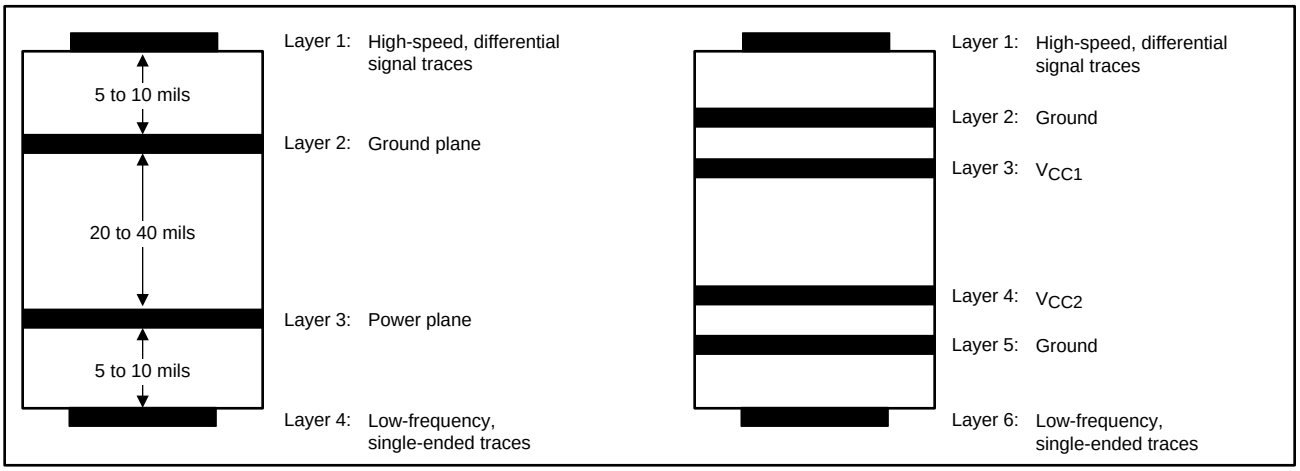


Figure 37. Recommended 4- or 6-Layer (0.062") Stack for a Receiver PCB Design

Routing the high-speed differential signal traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the DisplayPort connectors to the repeater inputs and from the repeater output to the subsequent receiver circuit.

Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.

Routing the fast-edged control signals on the bottom layer by prevents them from cross-talking into the high-speed signal traces and minimizes EMI.

If the receiver requires a supply voltage different from the one of the repeater, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. Finally, a second power/ground system provides added isolation between the signal layers.

Layout Guidelines (continued)

12.1.2 Differential Traces

Guidelines for routing PCB traces are necessary when trying to maintain signal integrity and lower EMI. Although there seems to be an endless number of precautions to be taken, this section provides only a few main recommendations as layout guidance.

1. Reduce intra-pair skew in a differential trace by introducing small meandering corrections at the point of mismatch.
2. Reduce inter-pair skew, caused by component placement and IC pinouts, by making larger meandering correction along the signal path. Use chamfered corners with a length-to-trace width ratio of between 3 and 5. The distance between bends should be 8 to 10 times the trace width.
3. Use 45-degree bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45-degree bend is seen as a smaller discontinuity.
4. When routing around an object, route both trace of a pair in parallel. Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur.
5. Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b), the resulting discontinuity, however, is limited to a far narrower area.
6. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.
7. Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise they will cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.
8. Use the smallest size possible for signal trace vias and DisplayPort connector pads as they have less impact on the 100-Ω differential impedance. Large vias and pads can cause the impedance to drop below 85 Ω.
9. Use solid power and ground planes for 100-Ω impedance control and minimum power noise.
10. For 100-Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
11. Keep the trace length between the DisplayPort connector and the DisplayPort device as short as possible to minimize attenuation.
12. Use good DisplayPort connectors whose impedances meet the specifications.
13. Place bulk capacitors (for example, 10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
14. Place smaller 0.1-µF or 0.01-µF capacitors at the device.

12.2 Layout Example

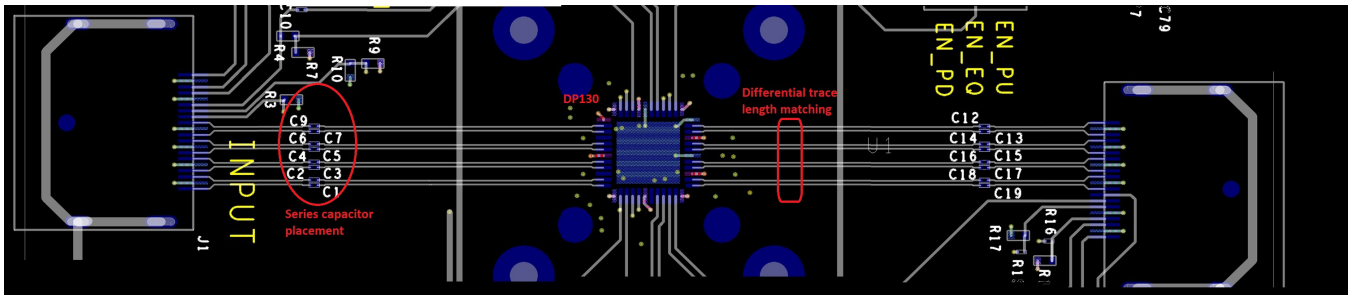


Figure 38. Layout Example

13 Device and Documentation Support

13.1 Trademarks

DisplayPort is a trademark of VESA Standards Association.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75DP130DSRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130DS
SN75DP130DSRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130DS
SN75DP130DSRGZRG4.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	-	Call TI	Call TI	0 to 85	
SN75DP130DSRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130DS
SN75DP130DSRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130DS
SN75DP130SSRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	0 to 85	DP130SS
SN75DP130SSRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130SS
SN75DP130SSRGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130SS
SN75DP130SSRGZRG4.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130SS
SN75DP130SSRGZRG4.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130SS
SN75DP130SSRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	0 to 85	DP130SS
SN75DP130SSRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130SS
SN75DP130SSRGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP130SS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

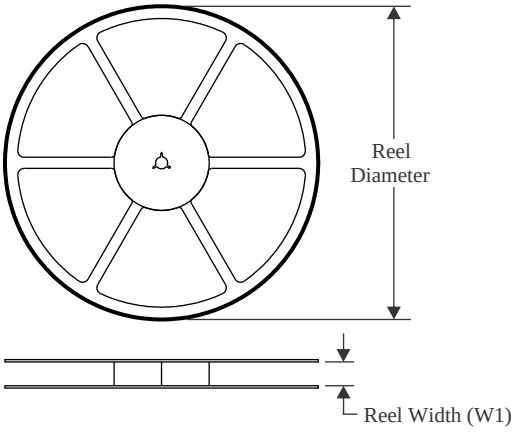
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

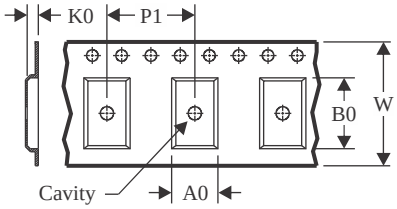
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

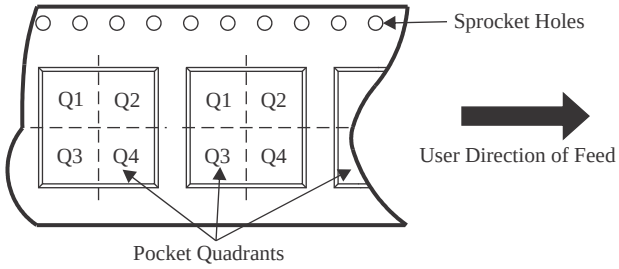


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

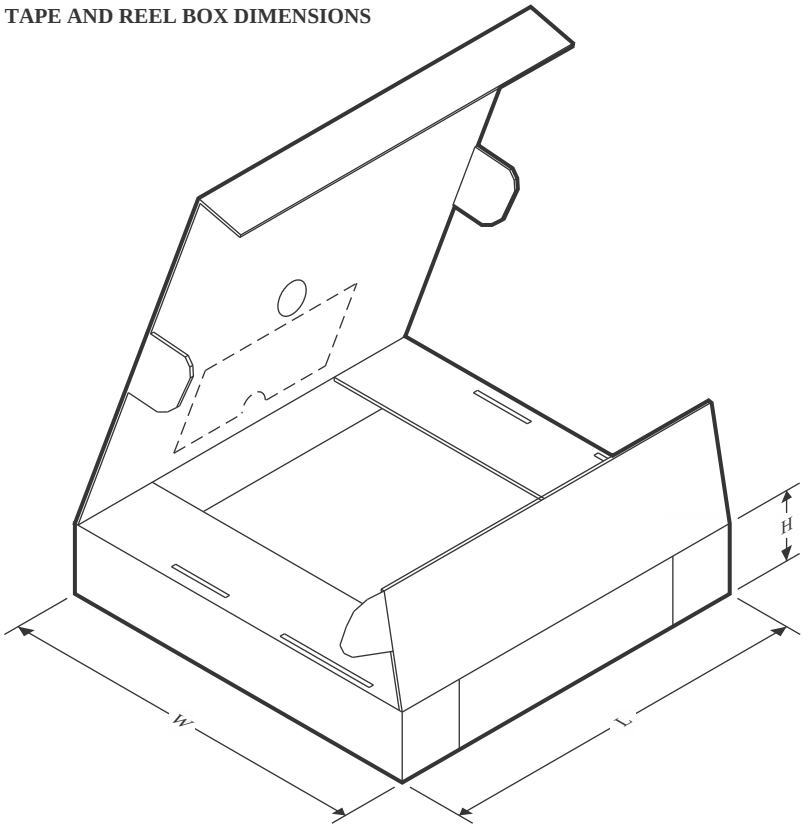
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP130DSRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
SN75DP130DSRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
SN75DP130SSRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
SN75DP130SSRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP130DSRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN75DP130DSRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
SN75DP130SSRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN75DP130SSRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

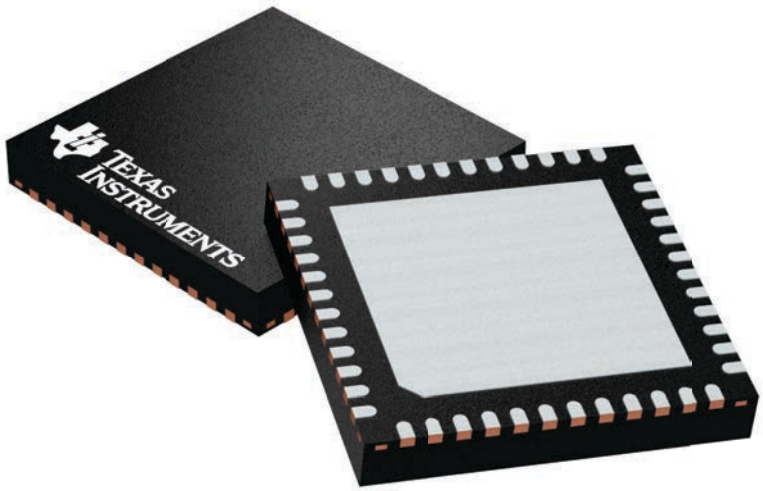
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

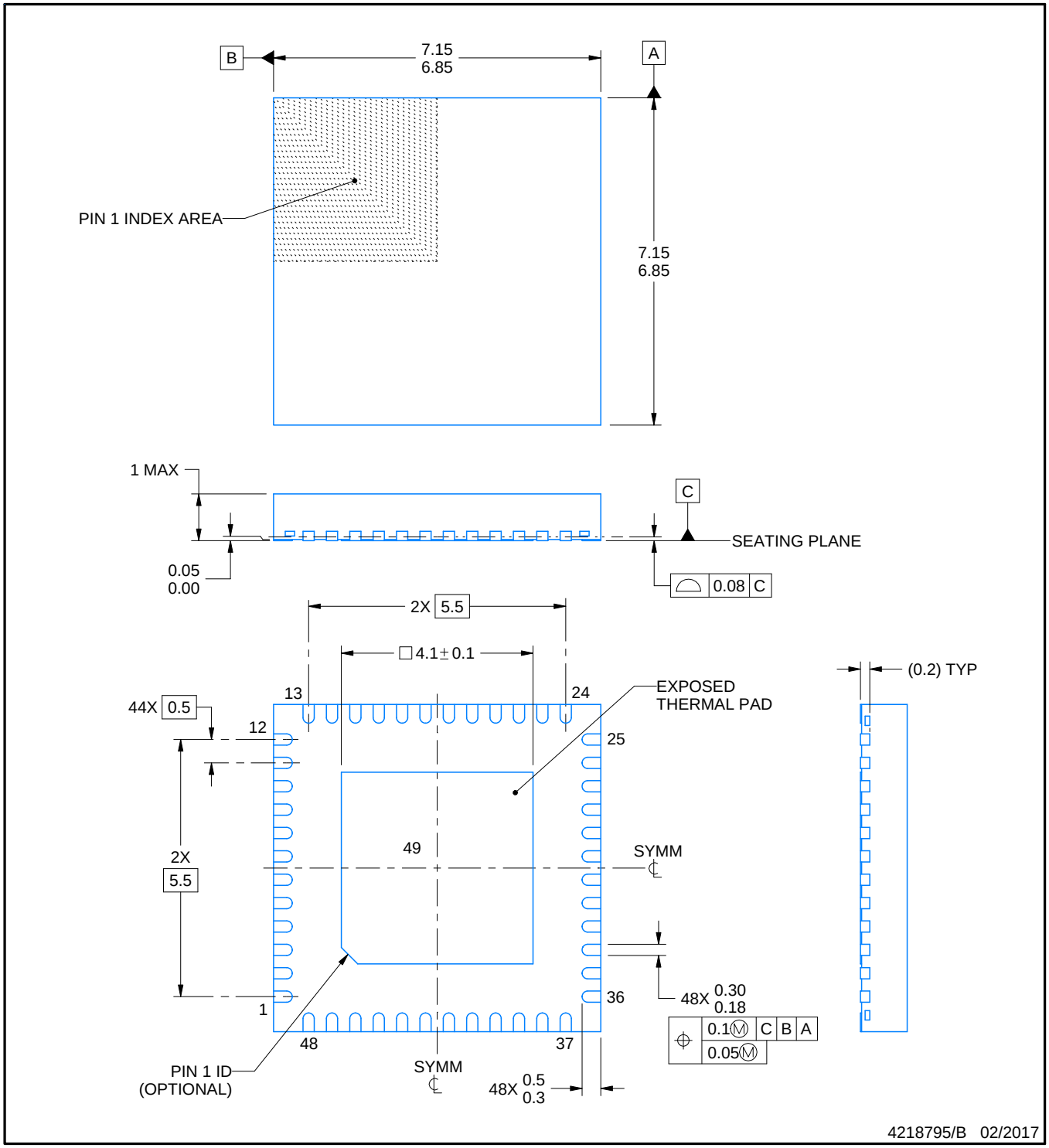
4224671/A

RGZ0048B

PACKAGE OUTLINE

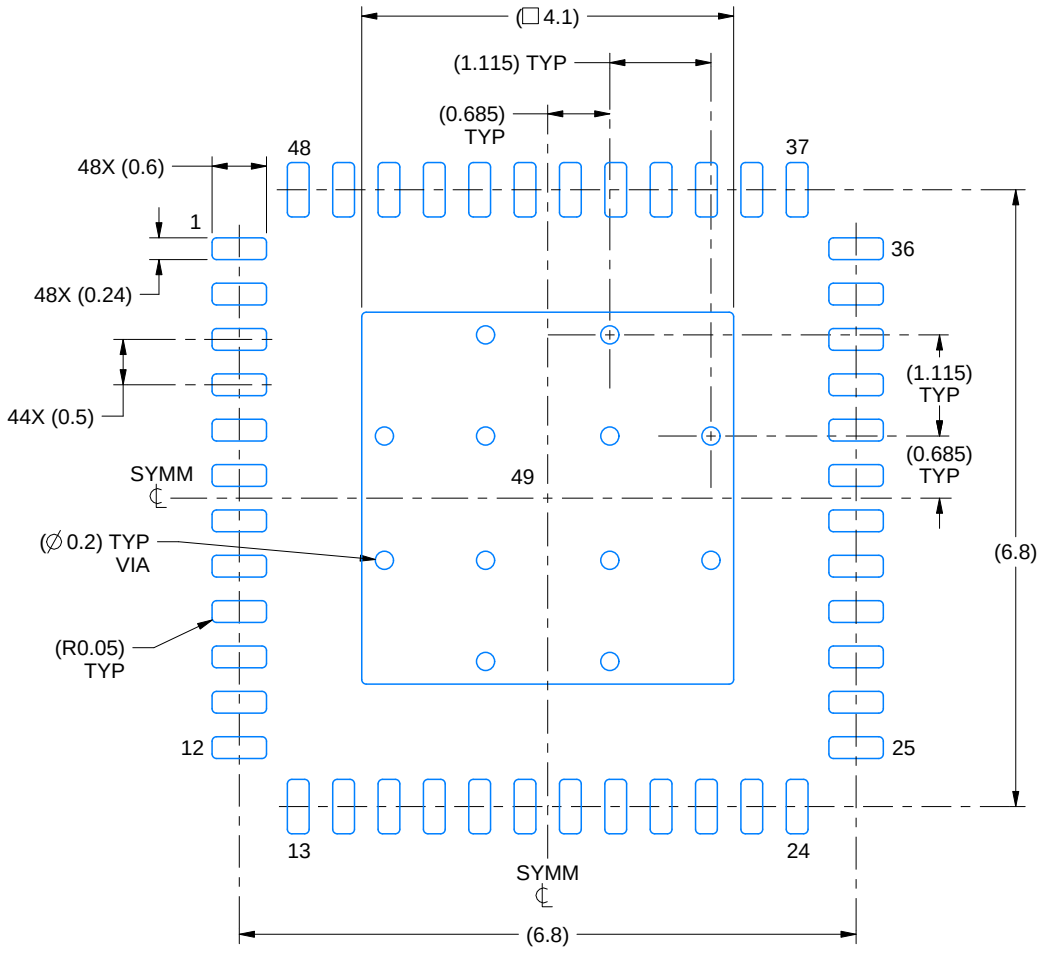
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

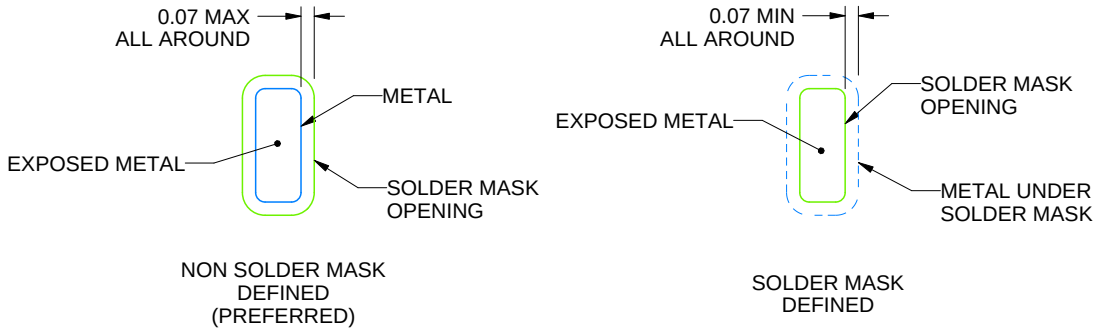


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

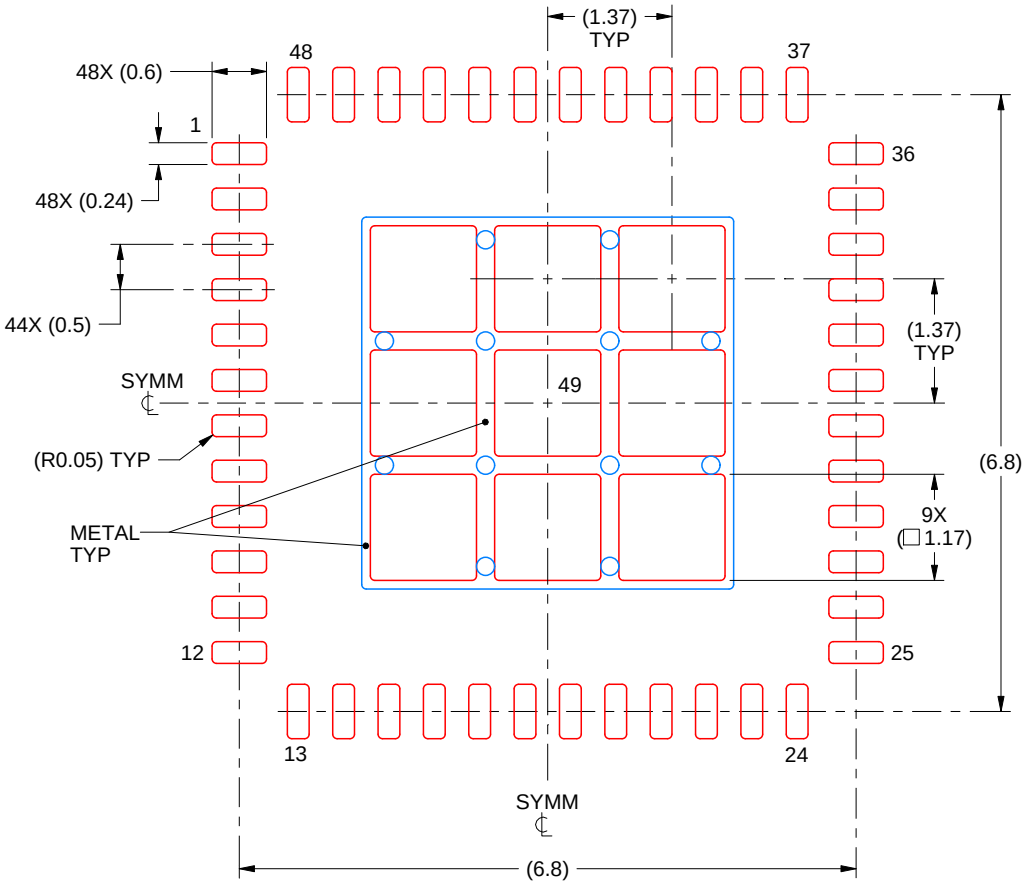


SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

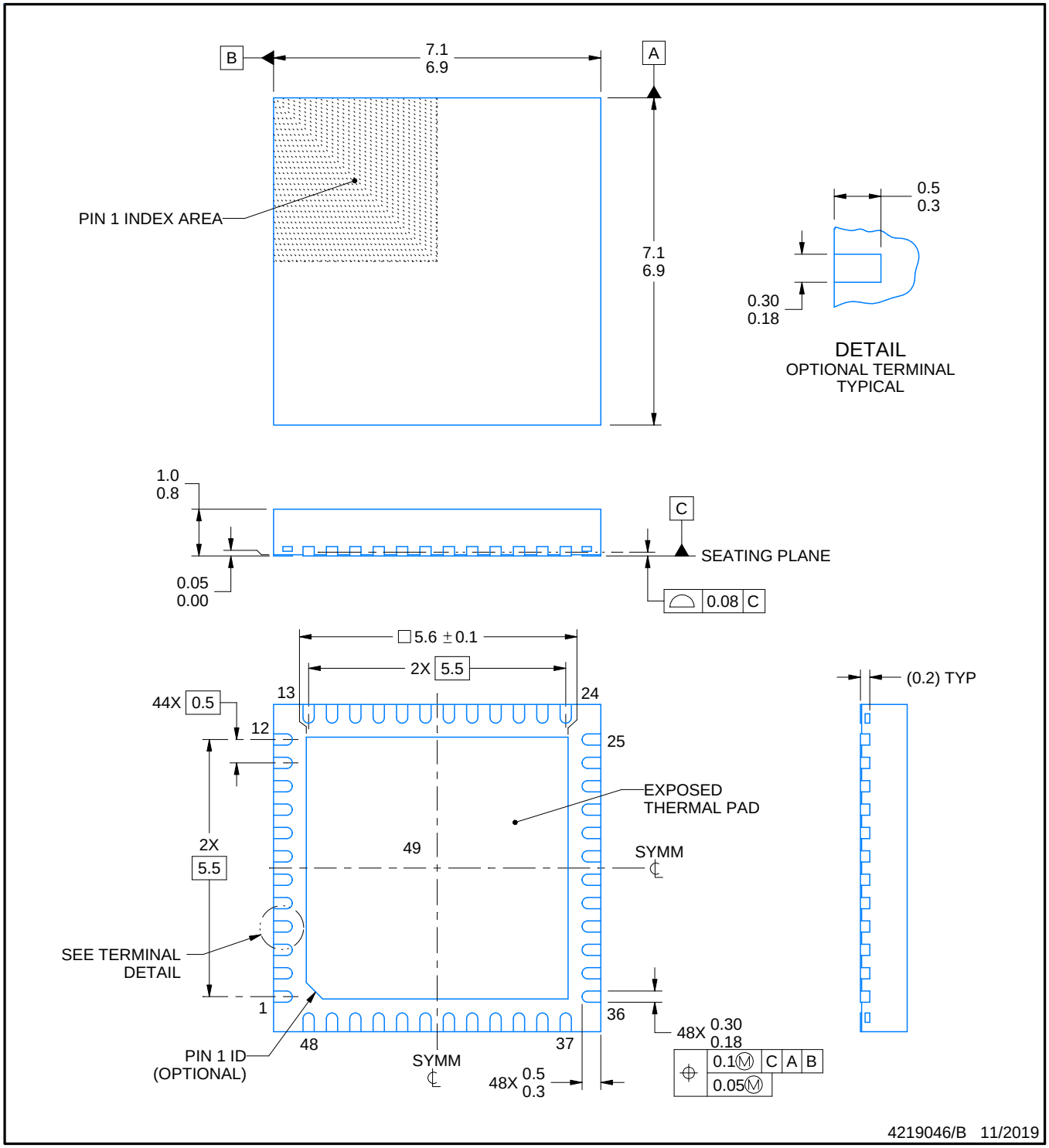
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RGZ0048D

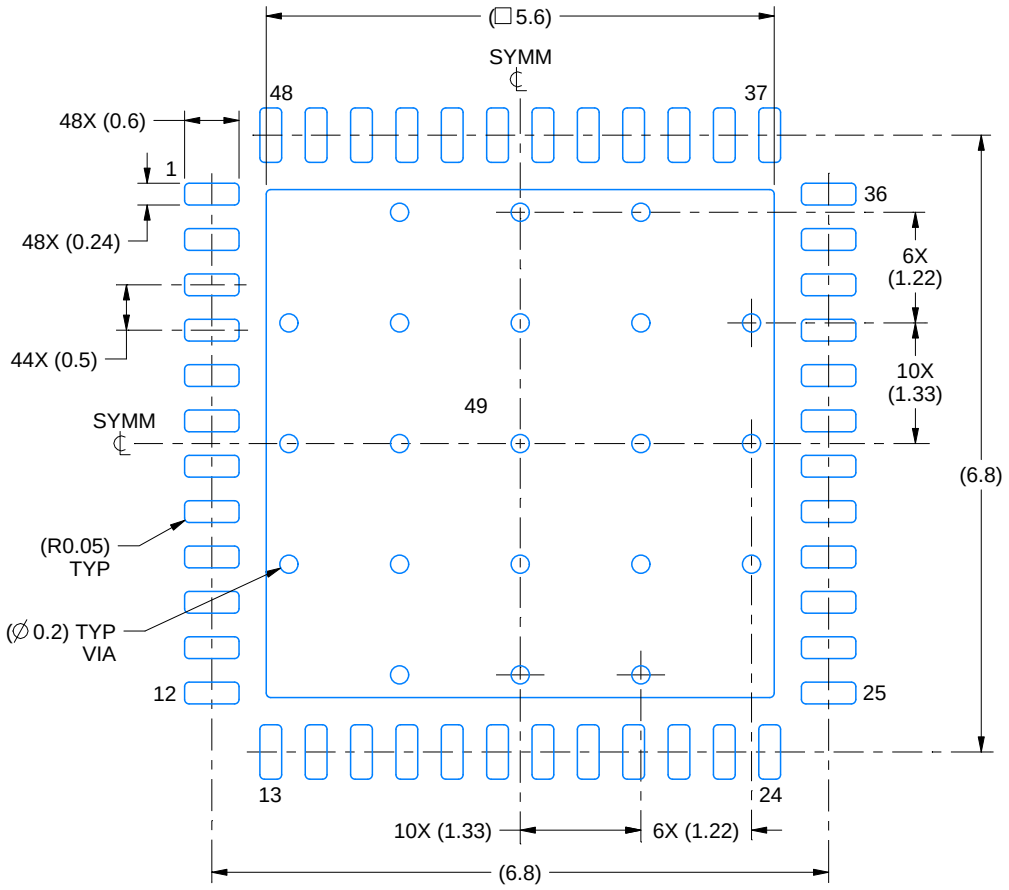
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

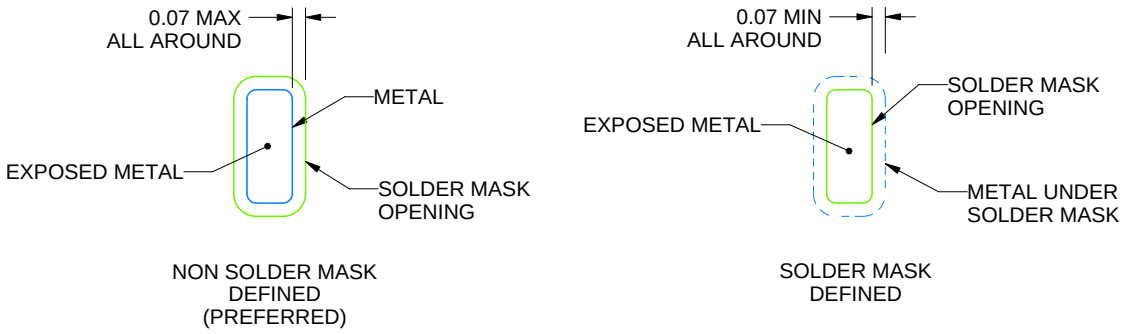


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

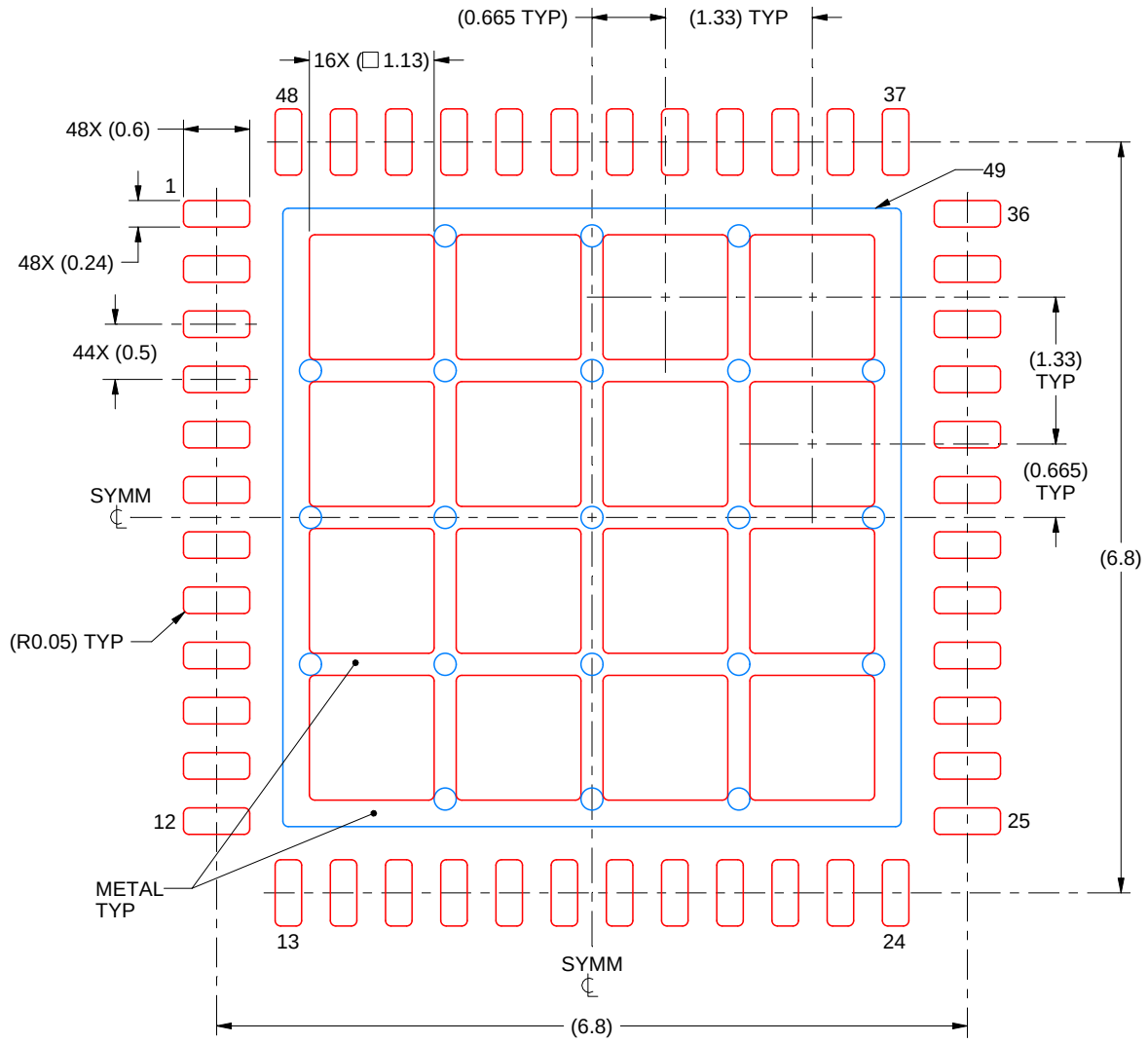


SOLDER MASK DETAILS

4219046/B 11/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4219046/B 11/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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