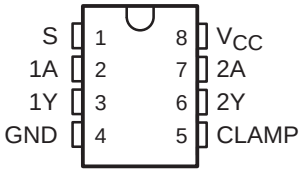
- **Characterized for Use to 300 mA**
- **No Output Latch-Up at 55 V (After Conducting 300 mA)**
- **High-Voltage Outputs (100 V Typ)**
- **Output Clamp Diodes for Transient Suppression (300 mA, 70 V)**
- **TTL- or MOS-Compatible Diode-Clamped Inputs**
- **pnp Transistor Inputs Reduce Input Current**
- **Standard Supply Voltage**
- **Suitable for Hammer-Driver Applications**
- **Plastic DIP (P) With Copper-Lead Frame Provides Cooler Operation and Improved Reliability**

**D OR P PACKAGE**
**(TOP VIEW)**

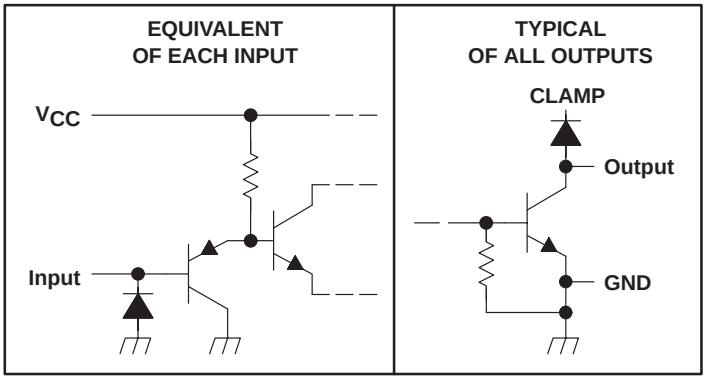



## description

The SN75476 through SN75478 are dual peripheral drivers designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, and SN75478 provide AND, NAND, and OR drivers respectively. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs for inductive transient protection.

The SN75476, SN75477, and SN75478 drivers are characterized for operation from 0°C to 70°C.

## schematics of inputs and outputs




## Function Tables

**SN75476**
**(each AND driver)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| H | H | H |
| L | X | L |
| X | L | L |

**SN75477**
**(each NAND driver)**

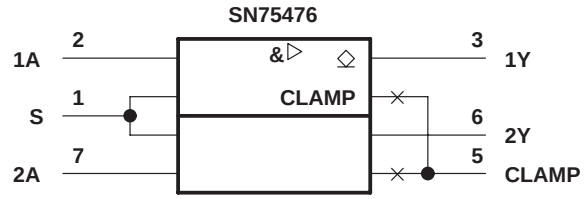
| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| H | H | L |
| L | X | H |
| X | L | H |

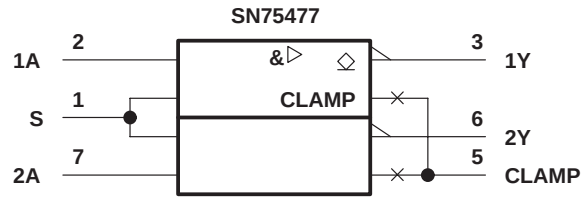
**SN75478**
**(each OR driver)**

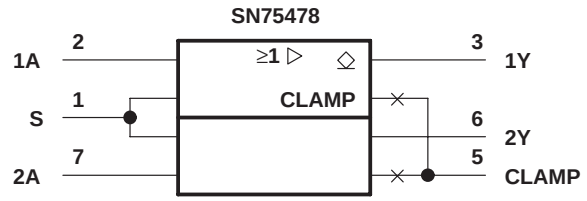
| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| H | X | H |
| X | H | H |
| L | L | L |

H = high level, L = low level
X = irrelevant

## logic symbols†

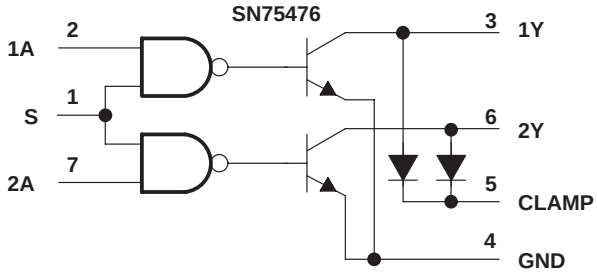


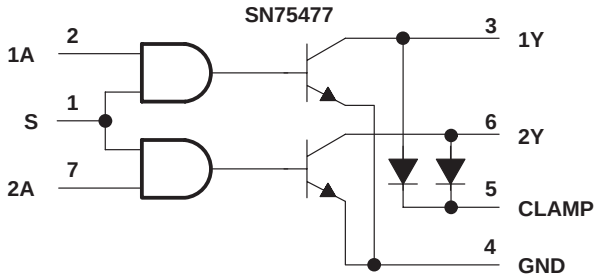




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

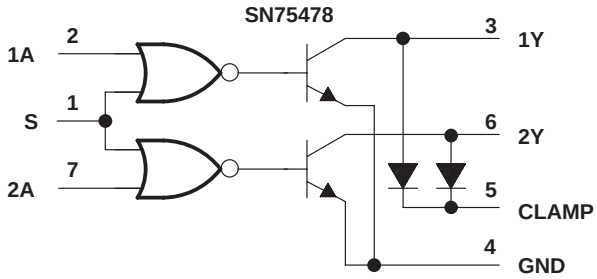
## logic diagrams (positive logic)




Positive Logic: $Y = AS$ or $\overline{\overline{A}+\overline{S}}$




Positive Logic: $Y = \overline{AS}$ or $\overline{A}+\overline{S}$




Positive Logic: $Y = A+S$ or $\overline{\overline{A}\,\overline{S}}$

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage, $V_I$ . . . . . 5.5 V
Continuous output current (see Note 2) . . . . . 400 mA
Peak output current: $t_w \leq 10$ ms, duty cycle $\leq 50\%$ . . . . . 500 mA
$t_w \leq 30$ ns, duty cycle $\leq 0.002\%$ . . . . . 3 A
Output clamp current, $I_{OK}$ . . . . . 400 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$ . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network GND.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous power dissipation ratings.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | V |
| High-level input voltage, $V_{IH}$ | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | | $I_I$ = –12 mA | | | –0.95 | –1.5 | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = 4.5 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = 100 mA | | 0.16 | 0.3 | V |
| | | | | $I_{OL}$ = 175 mA | | 0.22 | 0.5 | |
| | | | | $I_{OL}$ = 300 mA | | 0.33 | 0.6 | |
| $V_{O(BR)}$ | Output breakdown voltage | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = 100 μA | 70 | 100 | | V |
| $V_{R(K)}$ | Output clamp reverse voltage | | $V_{CC}$ = 4.5 V, | $I_R$ = 100 μA | 70 | 100 | | V |
| $V_{F(K)}$ | Output clamp forward voltage | | $V_{CC}$ = 4.5 V, | $I_F$ = 300 mA | 0.8 | 1.15 | 1.6 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = 4.5 V, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $V_{OH}$ = 70 V | | 1 | 100 | μA |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | 0.01 | 10 | μA |
| $I_{IL}$ | Low-level input current | A input | $V_{CC}$ = 5.5 V, | $V_I$ = 0.8 V | | –80 | –110 | μA |
| | | S input | | | | –160 | –220 | |
| $I_{CCH}$ | Supply current, outputs high | SN75476 | $V_{CC}$ = 5.5 V | $V_I$ = 5 V | | 10 | 17 | mA |
| | | SN75477 | | $V_I$ = 0 | | 10 | 17 | |
| | | SN75478 | | $V_I$ = 5 V | | 10 | 17 | |
| $I_{CCL}$ | Supply current, outputs low | SN75476 | $V_{CC}$ = 5.5 V | $V_I$ = 0 | | 54 | 75 | mA |
| | | SN75477 | | $V_I$ = 5 V | | 54 | 75 | |
| | | SN75478 | | $V_I$ = 0 | | 54 | 75 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

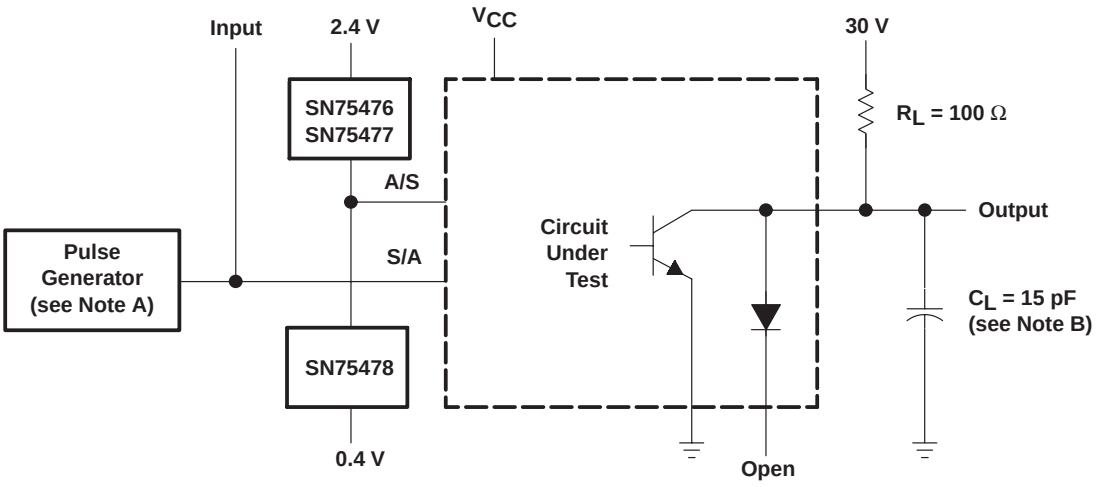
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 15 pF, See Figure 1 | $R_L$ = 100 Ω, | | 200 | 350 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 200 | 350 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | | 50 | 125 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | | 90 | 125 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, See Figure 2 | $I_O$ ≈ 300 mA, | $V_S$–18 | | | mV |

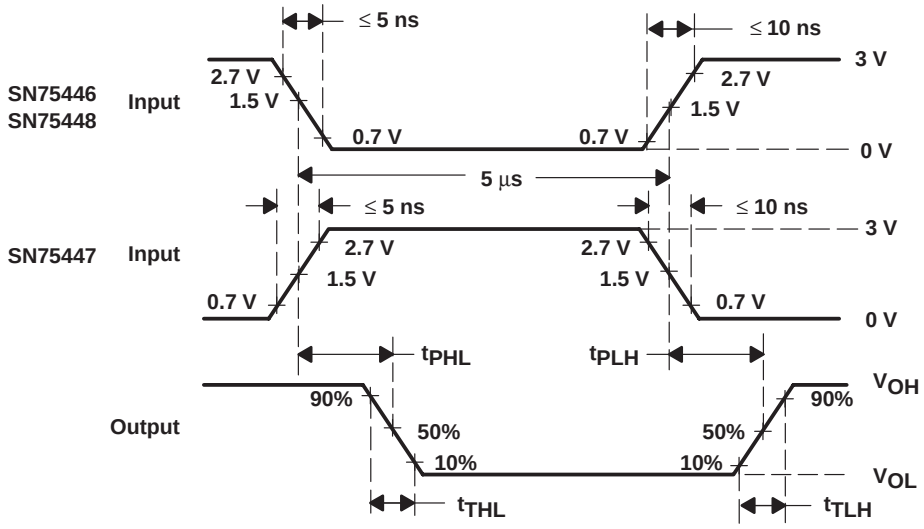


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

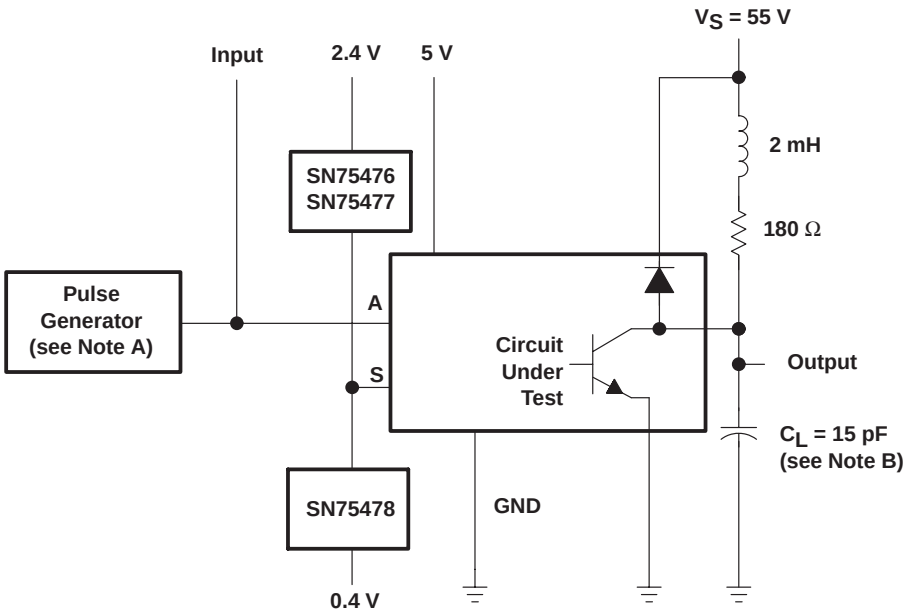



VOLTAGE WAVEFORMS

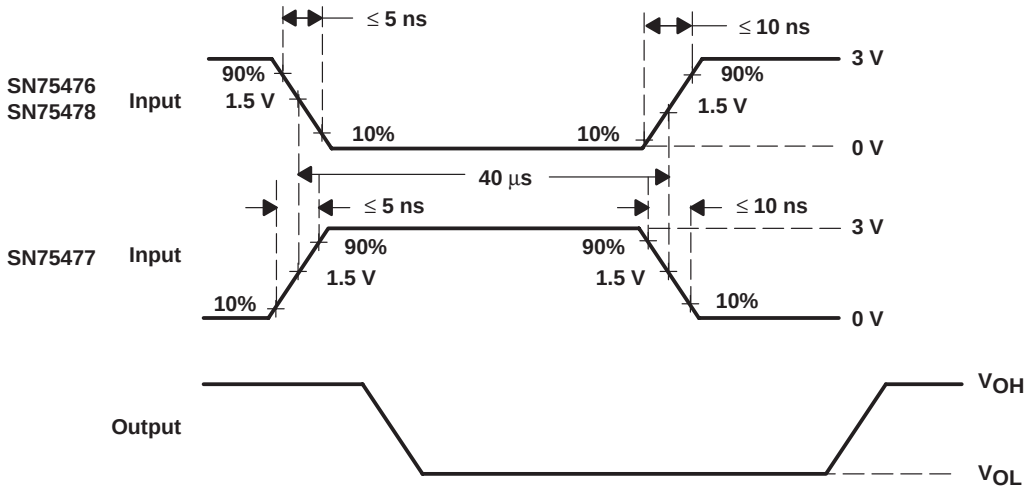
NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics**

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 2. Latch-Up Test Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN75477D | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 |
| SN75477D.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 |
| SN75477DE4 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 |
| SN75477DR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 |
| SN75477DR.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 |
| SN75477DRE4 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75477 |
| SN75477P | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75477P |
| SN75477P.A | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75477P |
| SN75477PE4 | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75477P |
| SN75478P | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75478P |
| SN75478P.A | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75478P |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

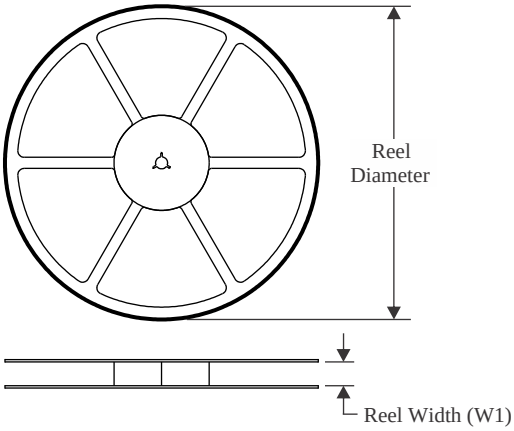
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

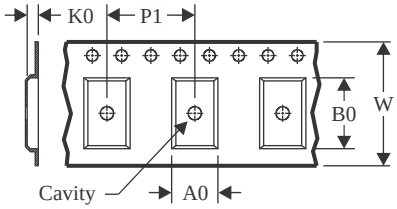
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

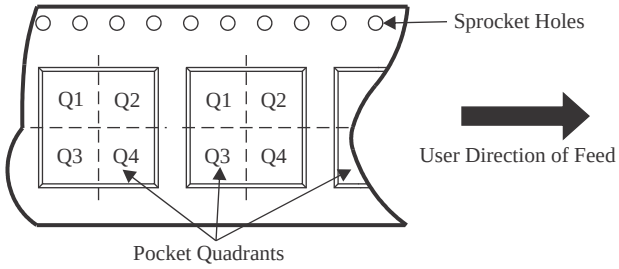



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

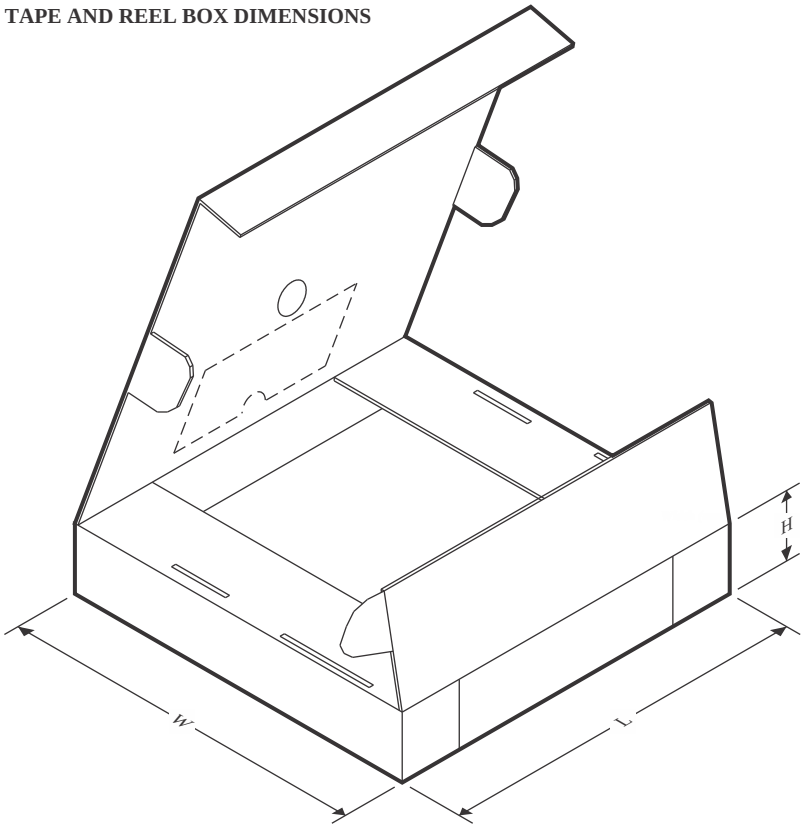
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75477DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

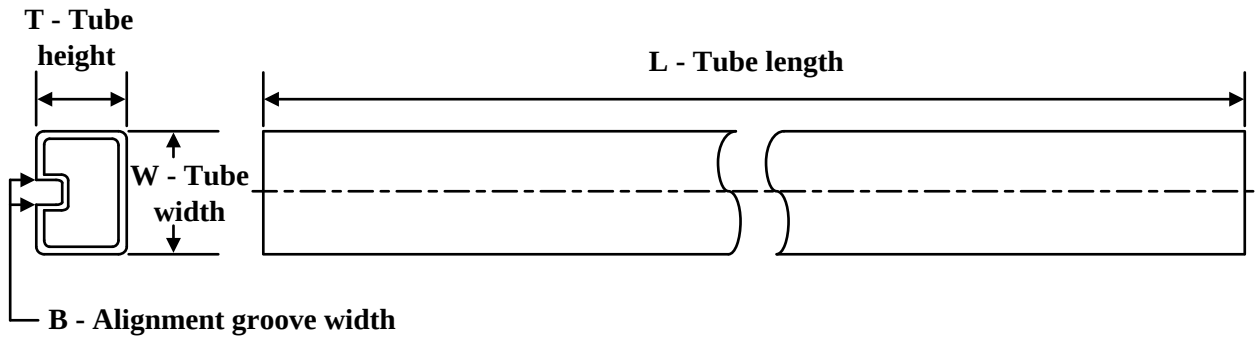
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

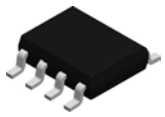
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75477DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN75477D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75477D.A | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75477DE4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75477P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75477P.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75477PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75478P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75478P.A | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |

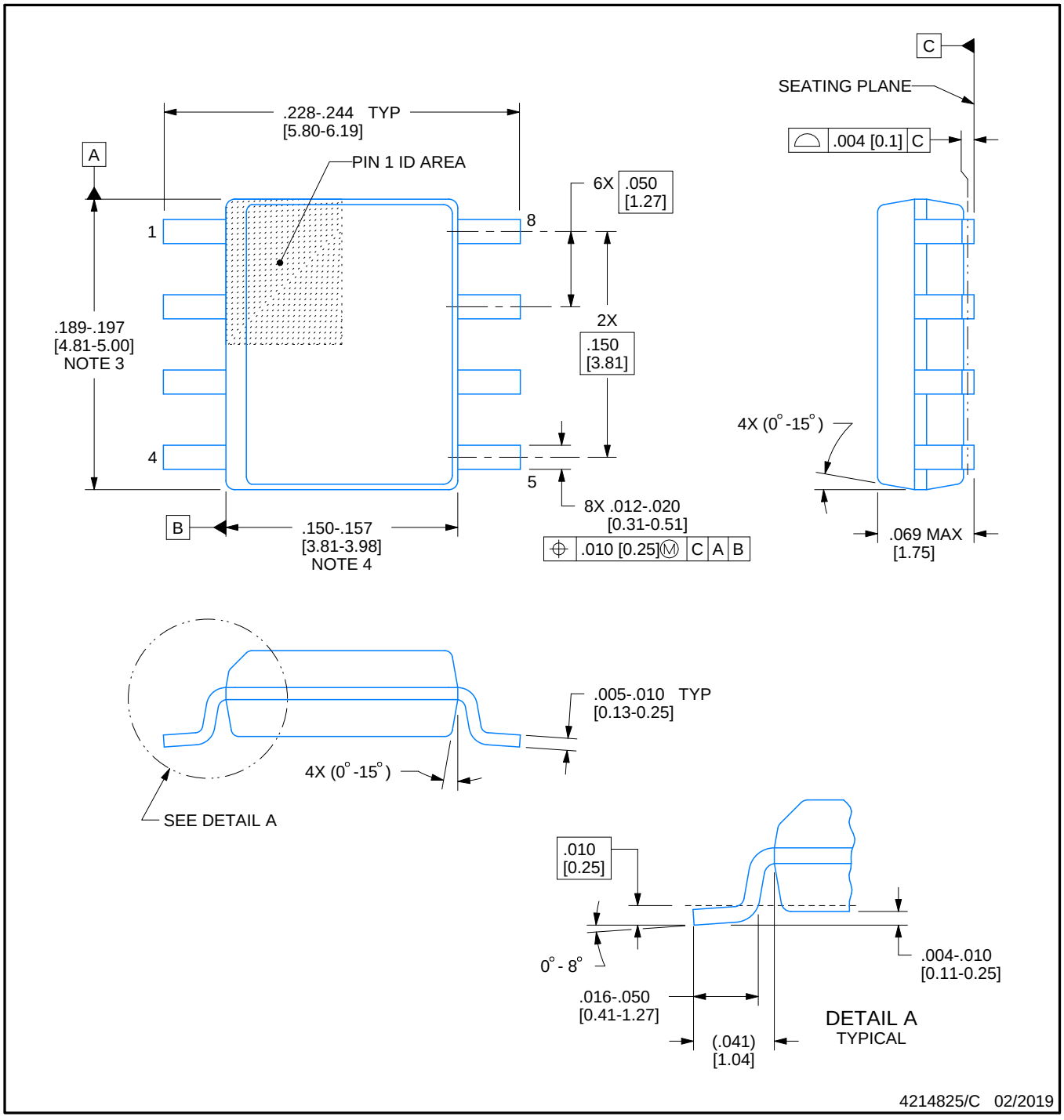


# PACKAGE OUTLINE

## D0008A

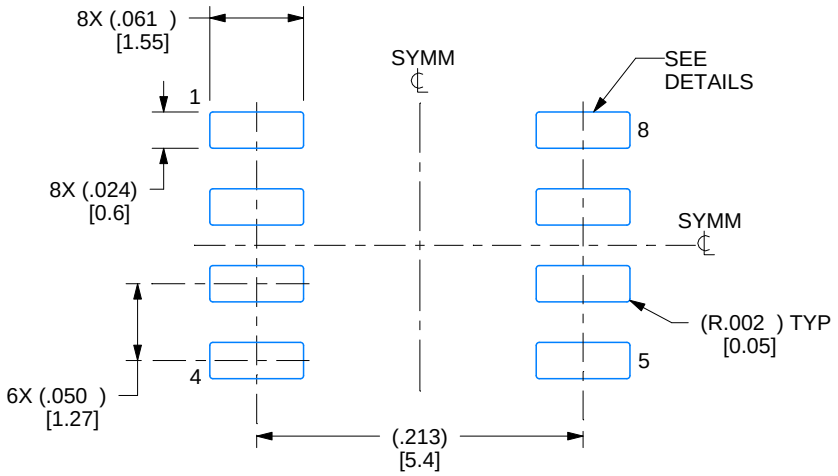
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

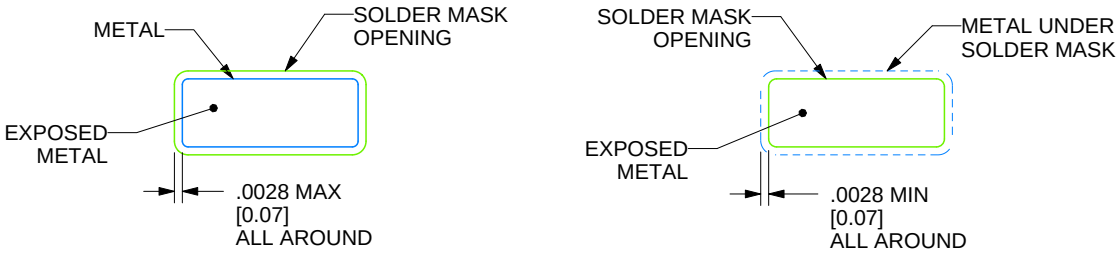



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

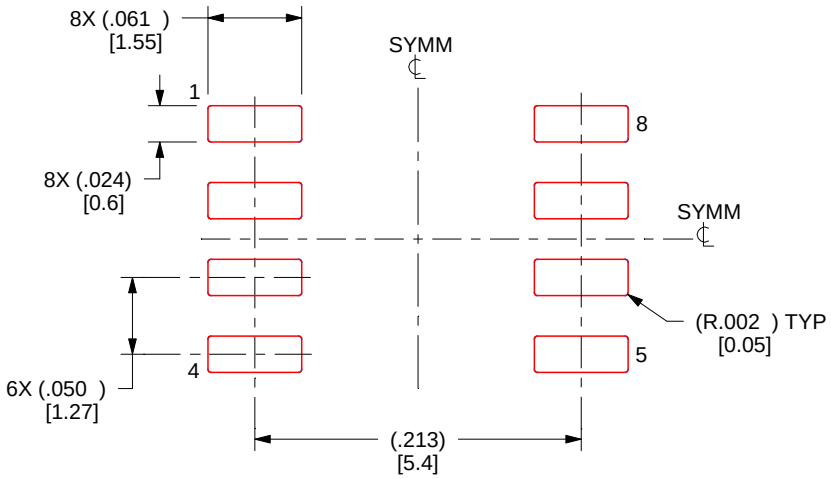
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



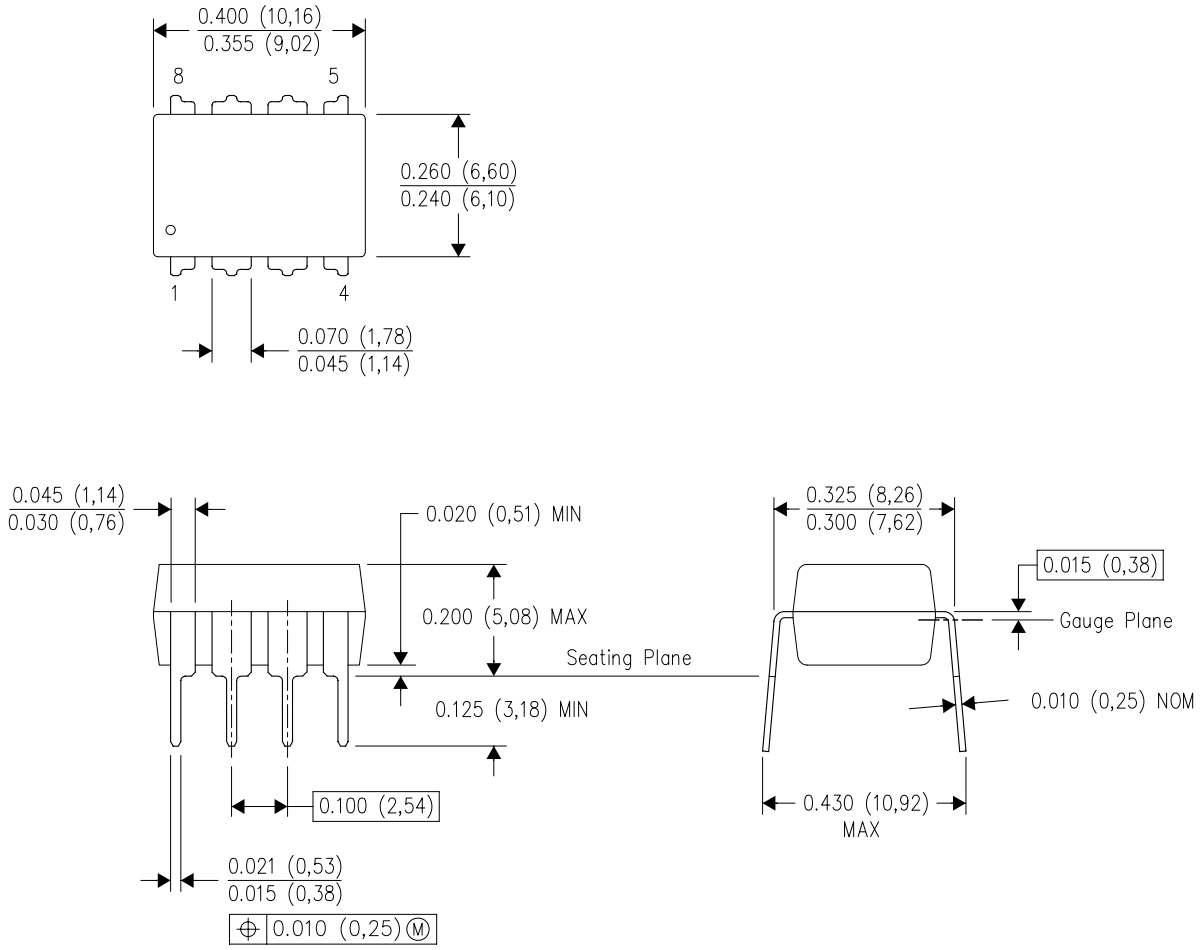

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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