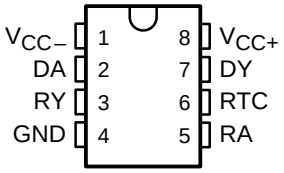
- **Meets or Exceeds the Requirements of ANSI TIA/EIA-232-C**
- **Wide Range of Supply Voltage V_{CC} = ±4.5 V to ±15 V**
- **Low Power . . . 117 mW (V_{CC} = ±9 V)**
- **Receiver Output TTL Compatible**
- **Response Control Provides:**
  - **Input Threshold Shifting**
  - **Input Noise Filtering**

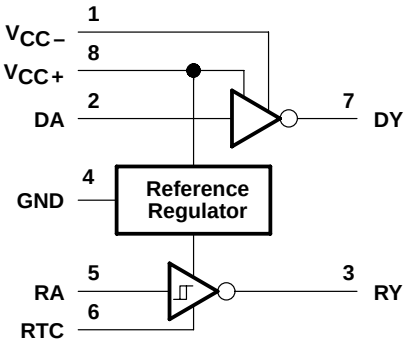
P OR PS PACKAGE
TOP VIEW



description

The SN751701 line driver and receiver is designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI TIA/EIA-232-E. The driver used is similar to the SN75188. The receiver used is similar to the SN75189A. The device operates over a wide range of supply voltages (V_{CC} = ±4.5 V to ±15 V) from the included reference regulator.

logic diagram

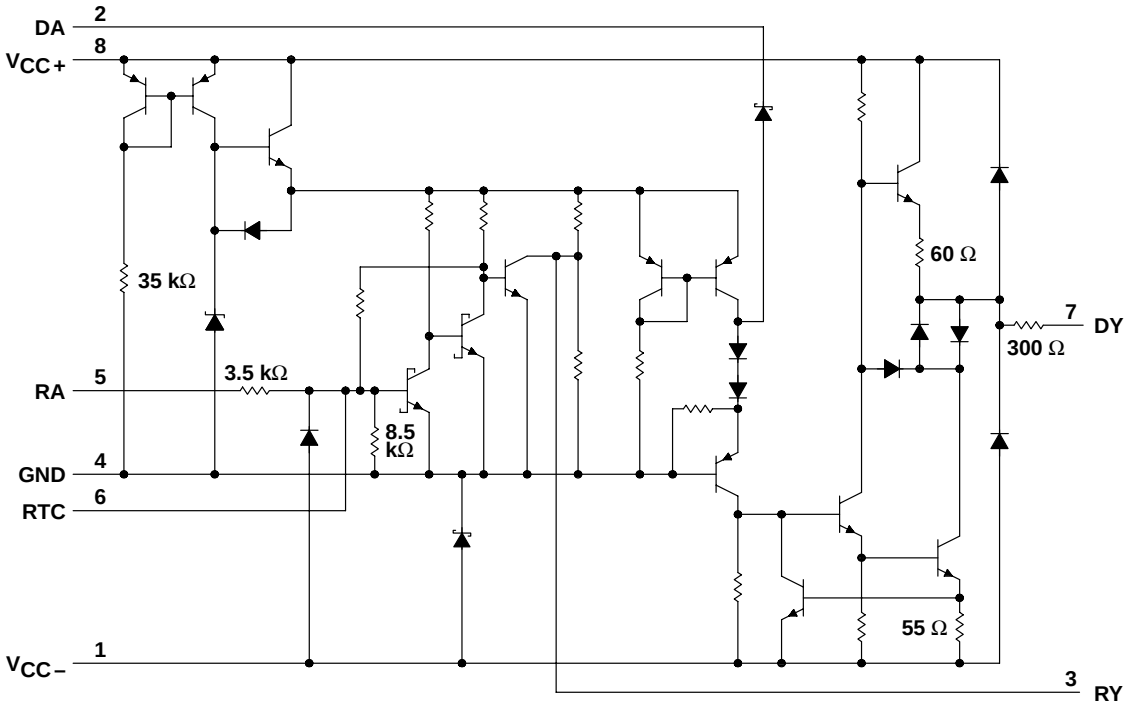


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2002, Texas Instruments Incorporated

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC+} (see Note 1) . . . . . –0.4 V to 18 V
Supply voltage range, V_{CC-} (see Note 1) . . . . . 0.4 V to –18 V
Input voltage range, V_I: Driver . . . . . –5 V to 18 V
Receiver . . . . . –30 V to 30 V
Output voltage range, V_O: Driver . . . . . –25 V to 25 V
Receiver . . . . . –0.4 V to 7 V
Output current, I_O (D) Driver . . . . . 50 mA
Response control current range, I_{RES} . . . . . –10 mA to 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 2): P package . . . . . 85°C/W
PS package . . . . . 95°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		4.5	15	V
V_{CC-}	Supply voltage		–4.5	–15	V
$V_{I(D)}$	Input voltage, driver			15	V
$V_{I(R)}$	Input voltage, receiver		–25	25	V
I_{RESP}	Response control current		–5.5	5.5	mA
$I_{O(R)}$	Output current, receiver			24	mA
T_A	Operating free-air temperature	P package	–20	85	°C
		PS package	–20	70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

total device

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{CCH+}	High-level supply current	V_{CC} = ±5 V	$V_{I(D)}$ = 2 V, $V_{I(R)}$ = $V_{T+(max)}$, Output open		6.3	8.1	mA
		V_{CC} = ±9 V			9.1	11.9	
		V_{CC} = ±12 V			10.4	14	
I_{CCL+}	Low-level supply current	V_{CC} = ±5 V	$V_{I(D)}$ = 0.8 V, $V_{I(R)}$ = $V_{T-(min)}$, Output open		2.5	3.4	mA
		V_{CC} = ±9 V			3.7	5.1	
		V_{CC} = ±12 V			4.1	5.6	
I_{CCH-}	High-level supply current	V_{CC} = ±5 V	$V_{I(D)}$ = 2 V, $V_{I(R)}$ = $V_{T+(max)}$, Output open		–2.4	–3.1	mA
		V_{CC} = ±9 V			–3.9	–4.9	
		V_{CC} = ±12 V			–4.8	–6.1	
I_{CCL-}	Low-level supply current	V_{CC} = ±5 V	$V_{I(D)}$ = 0.8 V, $V_{I(R)}$ = $V_{T-(min)}$, Output open		–0.2	–0.35	mA
		V_{CC} = ±9 V			–0.25	–0.4	
		V_{CC} = ±12 V			–0.27	–0.45	
I_{CC+}	Positive supply current	V_{CC} = ±5 V	$V_{I(R)}$ = $V_{T+(max)}$, $V_{I(D)}$ = 0 V, V_{CC-} = 0 V, Output open		4.8	6.4	mA
		V_{CC} = ±12 V			6.7	9.1	

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = –12 V (unless otherwise noted)

driver section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	$V_{I(D)}$ = 0.8 V, R_L = 3 kΩ	V_{CC} = ±5 V	3.2	3.7		V
			V_{CC} = ±9 V	6.5	7.2		
			V_{CC} = ±12 V	8.9	9.8		
V_{OL}	Low-level output voltage	$V_{I D)}$ = 2 V, R_L = 3 kΩ	V_{CC} = ±5 V		–3.6	–3.2	V
			V_{CC} = ±9 V		–7.1	–6.4	
			V_{CC} = ±12 V		–9.7	–8.8	
I_{IH}	High-level input current	$V_{I(D)}$ = 7 V				5	µA
I_{IL}	Low-level input current	$V_{I(D)}$ = 0 V			–0.73	–1.2	mA
$I_{OS(H)}$	High-level short-circuit output current	$V_{I(D)}$ = 0.8 V, $V_{O(D)}$= 0 V		–7	–12	–14.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	$V_{I(D)}$ = 2 V, $V_{O(D)}$= 0 V		6.5	11.5	14	mA
r_O	Output resistance	V_{CC+} = 0 V, $V_{O(D)}$ = –2 V to 2 V		300			Ω

† All typical values are at T_A = 25°C.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = –12 V, T_A = 25°C (unless otherwise noted)

driver section (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ, C_L = 50 pF		340	480	ns
t_{PHL}	Propagation delay time, high- to low-level output			100	150	
t_{TLH}	Transition time, low- to high-level output	R_L = 3 kΩ, C_L = 50 pF		120	180	ns
t_{THL}	Transition time, high- to low-level output			105	160	
t_{TLH}	Transition time, low- to high-level output	R_L = 3 kΩ to 7 kΩ (see Note 3), C_L = 2500 pF		2.1	3	µs
t_{THL}	Transition time, high- to low-level output			2.1	3	

NOTE 3: The time is measured between 3 V and –3 V on output waveform.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = –12 V (unless otherwise noted)

receiver section (see Figure 1) (see Note 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage			1.2	1.9	2.3	V
V_{IT-}	Negative-going input threshhold voltage			0.6	0.95	1.2	V
V_{hys}	Hystresis voltage ($V_{IT+} – V_{IT-}$)			0.6			V
$V_{O(H)}$	High-level output voltage	$V_{I(R)} = V_{T-(min)}$, I_{OL} = –10 µA	V_{CC+} = 5 V	3.7	4.1	4.5	V
			V_{CC+} = 12 V	4.4	4.7	5.2	
		$V_{I(R)} = V_{T-(min)}$, I_{OH} = –0.4 mA	V_{CC+} = 5 V	3.1	3.4	3.8	
			V_{CC+} = 12 V	3.6	4	4.5	
$V_{O(L)}$	Low-level output voltage	$V_{I(R)} = V_{T+(max)}$,	I_{OL} = 24 mA		0.2	0.3	V
I_{IH}	High-level input current	$V_{I(R)}$ = 25 V		3.6	6.7	8.3	mA
		$V_{I(R)}$ = 3 V		0.43	0.67	1	mA
I_{IL}	Low-level input current	$V_{I(R)}$ = –25 V		–3.6	–6.7	–8.3	mA
		$V_{I(R)}$ = –3 V		–0.43	–0.74	–1	mA
I_{OS}	Short-circuit output current	$V_{I(R)} = V_{T-(min)}$			–2.8	–3.7	mA

† All typical values are at T_A = 25°C.

NOTE 4: Response Control pin is open.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = –12 V, T_A = 25°C (unless otherwise noted)

receiver section (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 400 kΩ, C_L = 50 pF		150	240	ns
t_{PHL}	Propagation delay time, high- to low-level output			50	100	
t_{TLH}	Transition time, low- to high-level output	R_L = 400 kΩ, C_L = 50 pF		250	360	ns
t_{THL}	Transition time, high- to low-level output			18	35	

PARAMETER MEASUREMENT INFORMATION

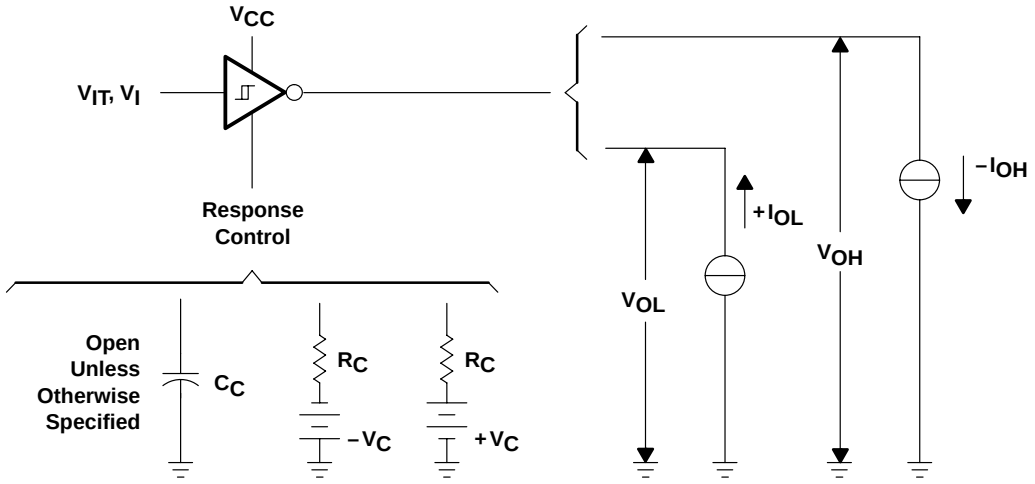
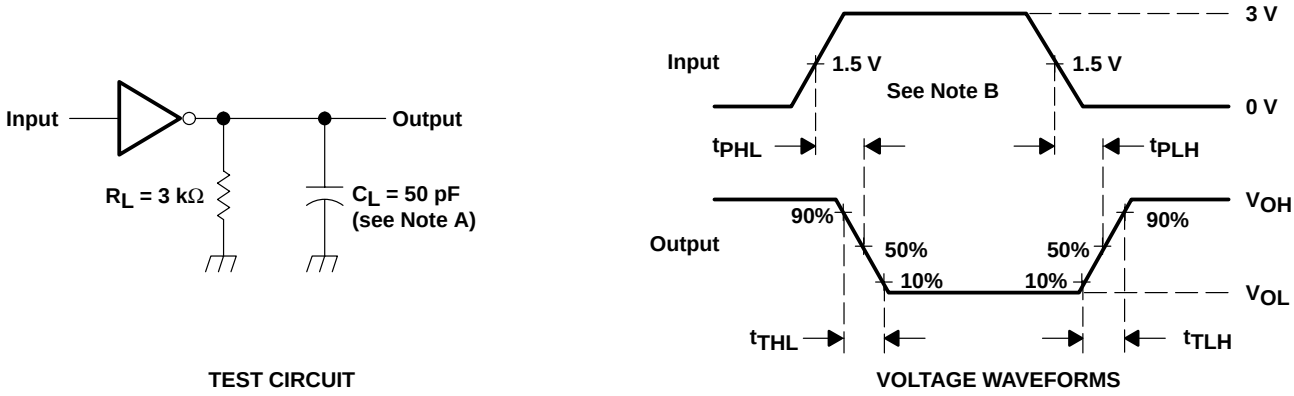


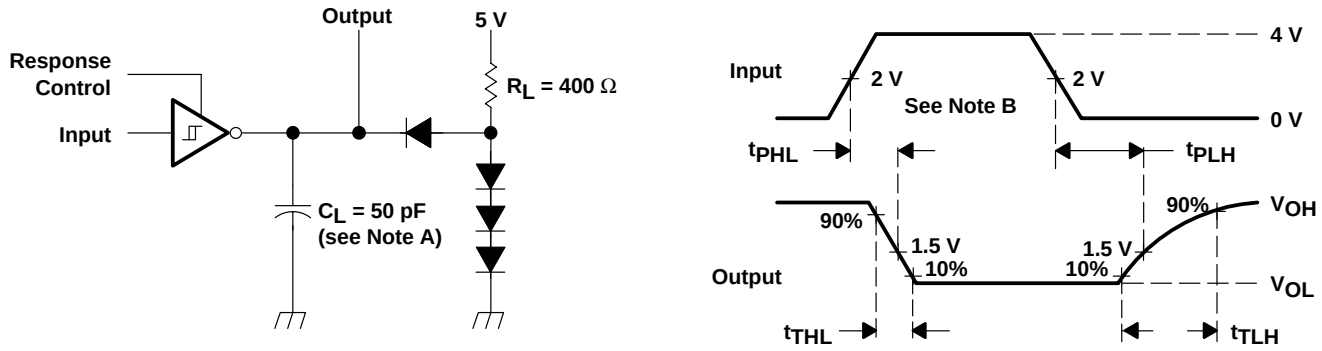
Figure 1. Receiver Section Test Circuit (V_{IT+}, V_{IT-}, V_{OH}, V_{OL})



NOTES: A. C_L includes probe and jig capacitance.
B. The input waveform is supplied by a generator having the following characteristics: Z_O = 50 Ω, t_W = 500 ns, $t_{TLH} \le 5$ ns, $t_{THL} \le 5$ ns.

Figure 2. Driver Section Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. C_L includes probe and jig capacitance.
B. The input waveform is supplied by a generator having the following characteristics: Z_O = 50 Ω, t_W = 500 ns, $t_{THL} \le 5$ ns, $t_{TLH} \le 5$ ns.

Figure 3. Receiver Section Switching Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER
VOLTAGE TRANSFER CHARACTERISTICS

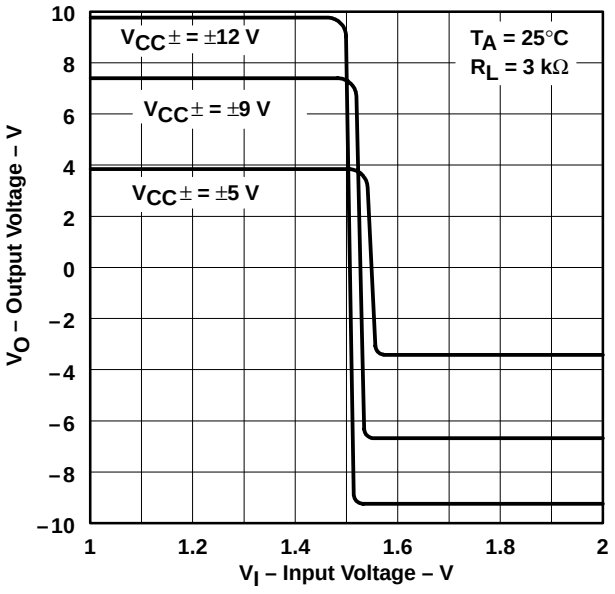


Figure 4

DRIVER
OUTPUT CURRENT
vs
OUTPUT VOLTAGE

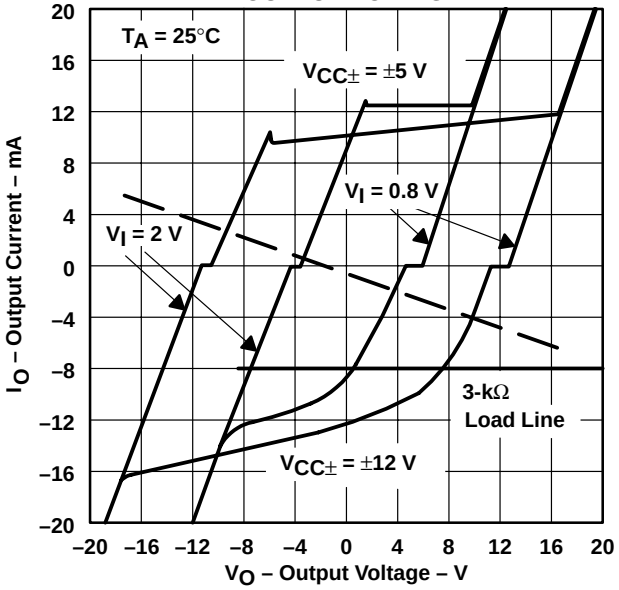


Figure 5

DRIVER
SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

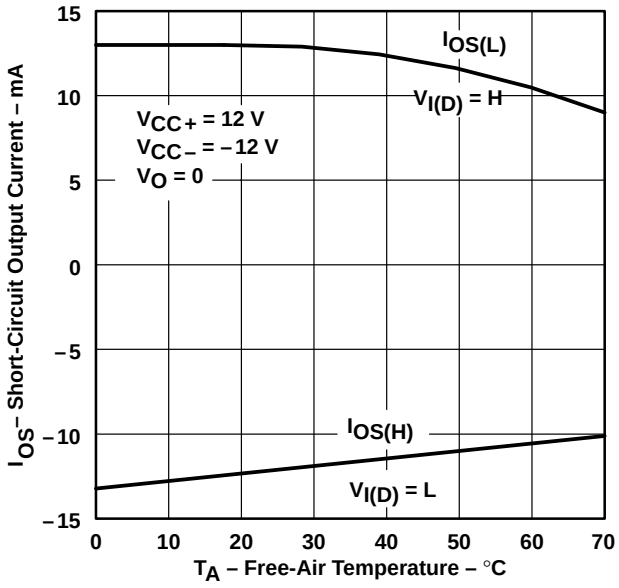


Figure 6

DRIVER
SLEW RATE
vs
LOAD CAPACITANCE

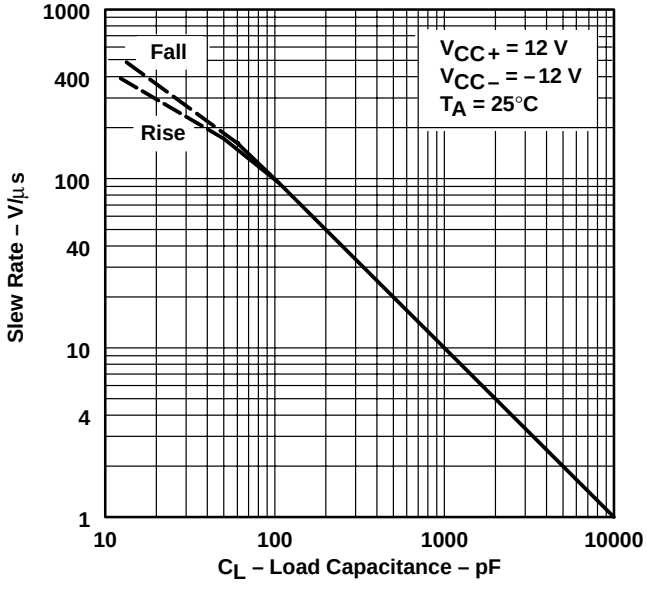


Figure 7

TYPICAL CHARACTERISTICS

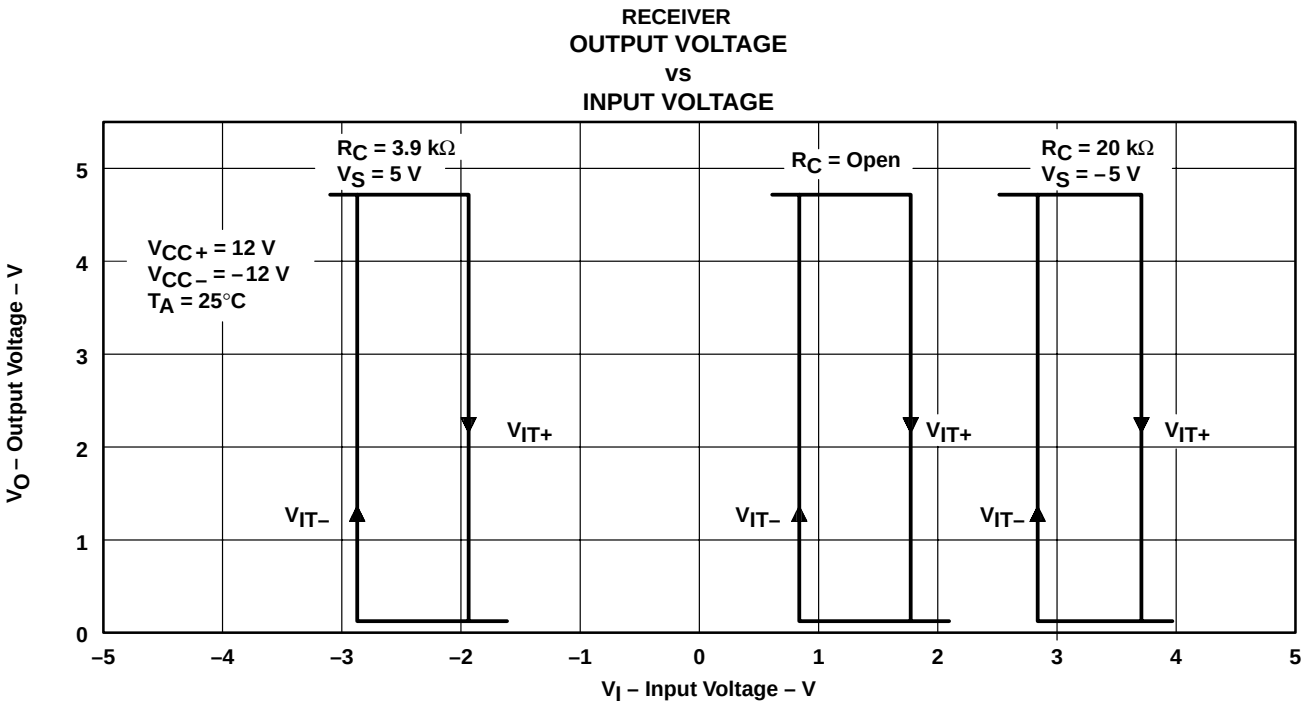


Figure 8

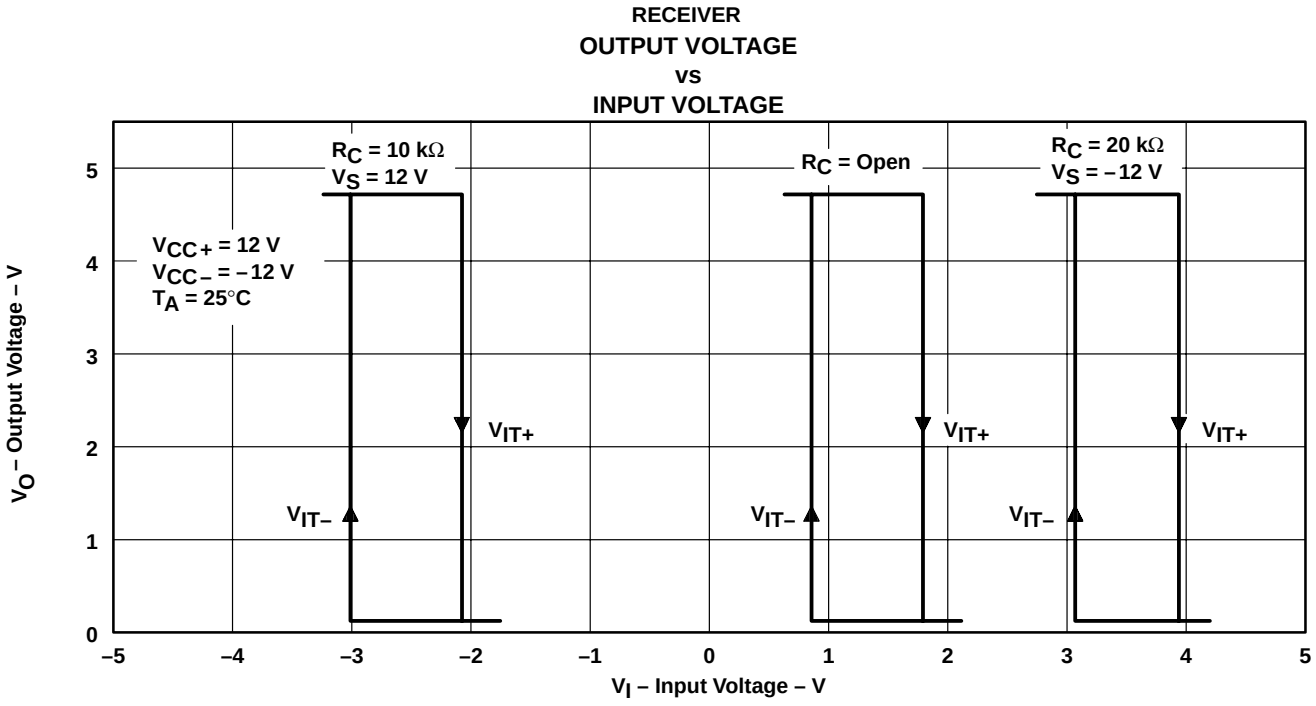


Figure 9

TYPICAL CHARACTERISTICS

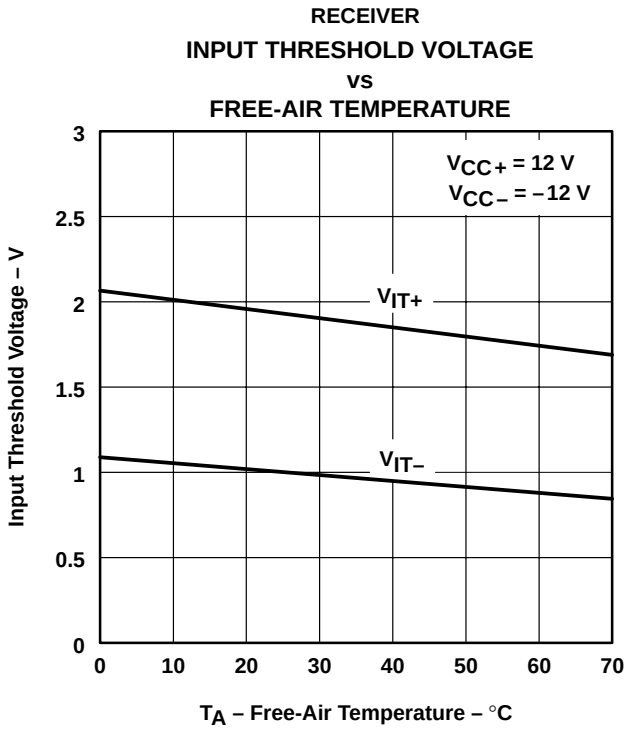


Figure 10

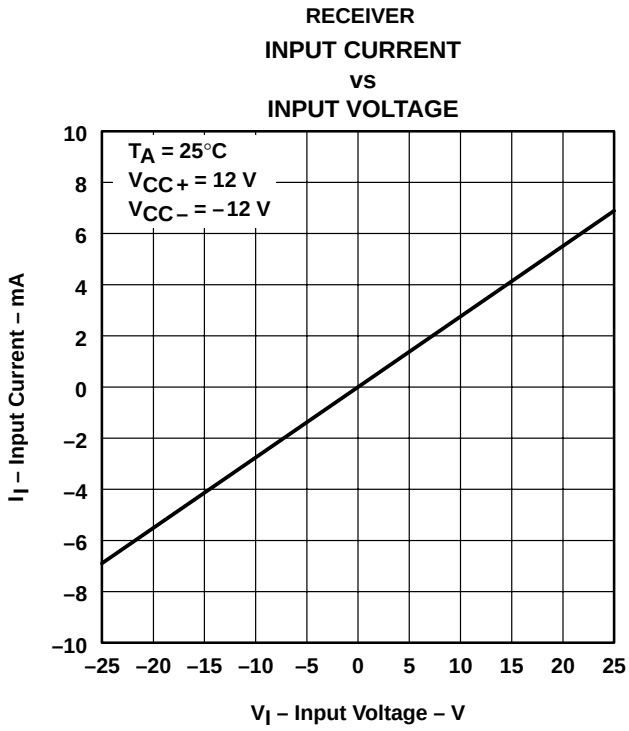


Figure 11

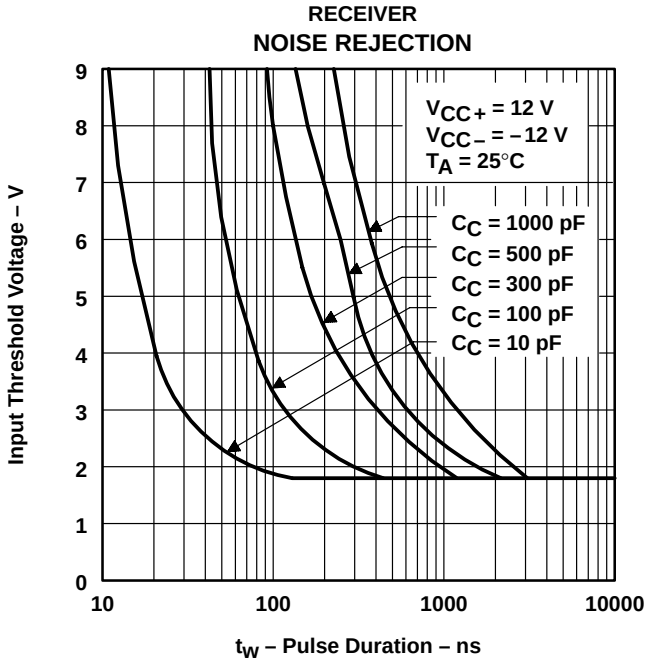


Figure 12

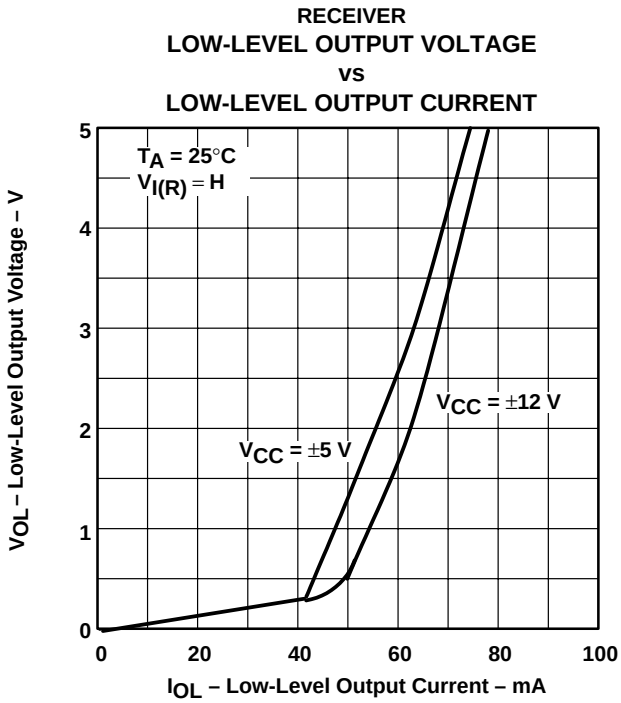


Figure 13

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

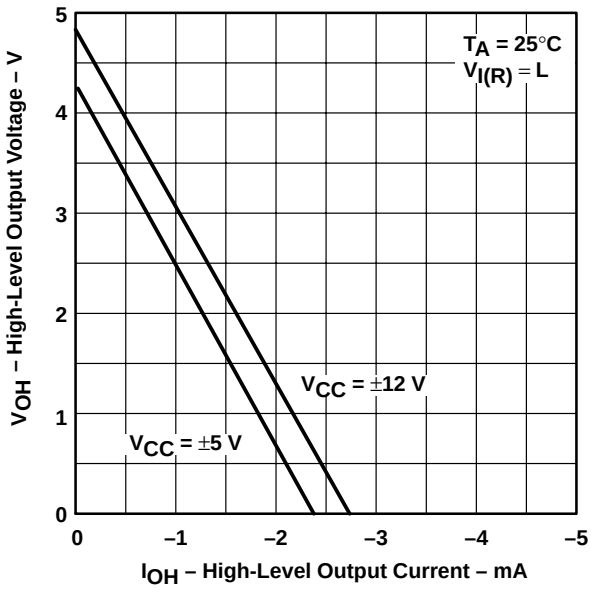


Figure 14

RECEIVER
OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

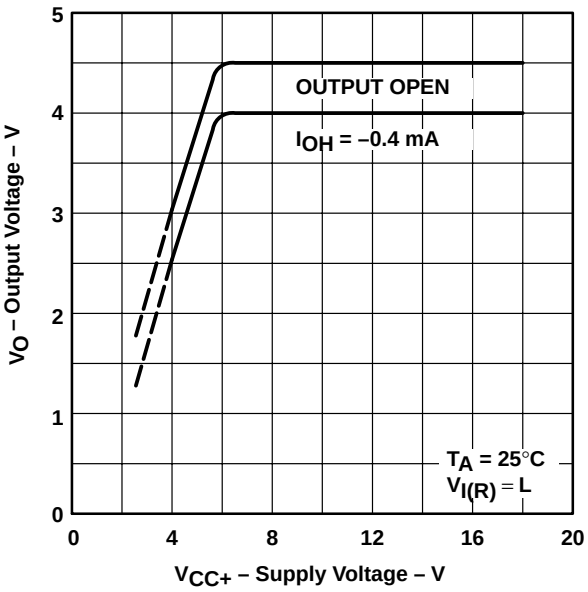


Figure 15

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN751701P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN751701P
SN751701P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN751701P
SN751701PSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	A1701
SN751701PSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	A1701

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

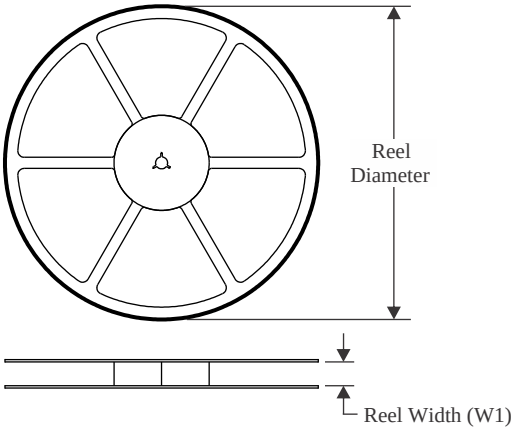
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

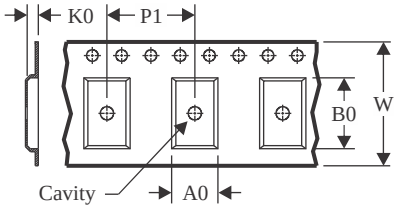
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

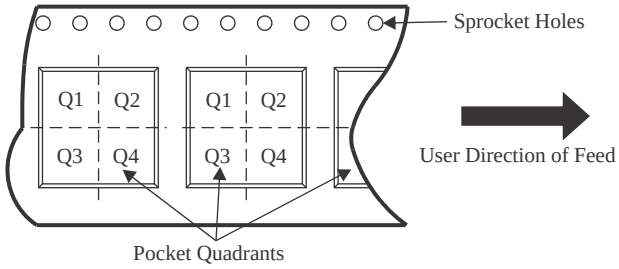


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

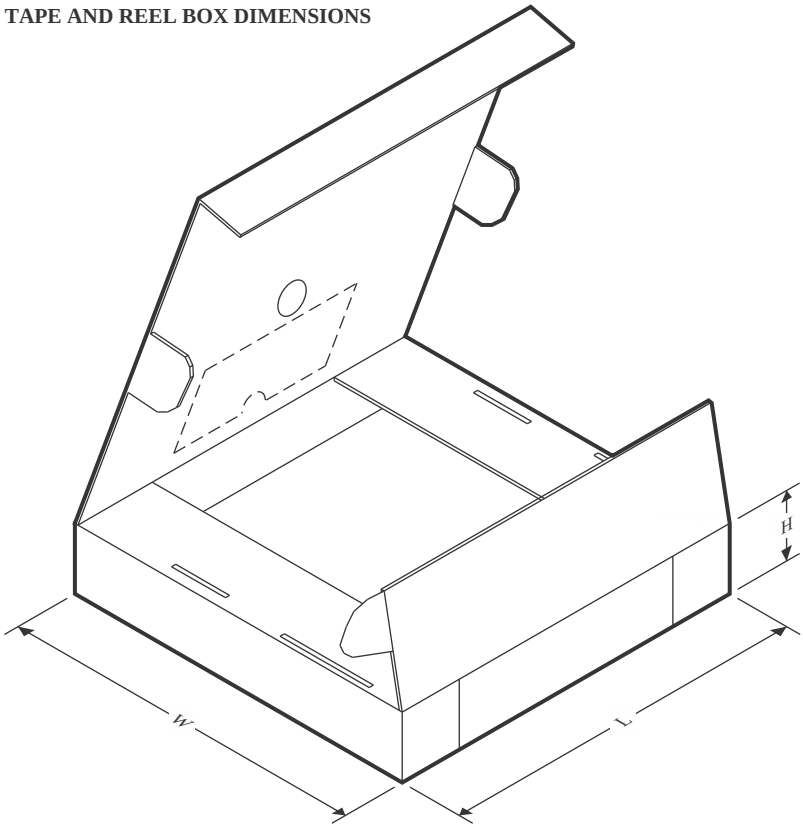
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN751701PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

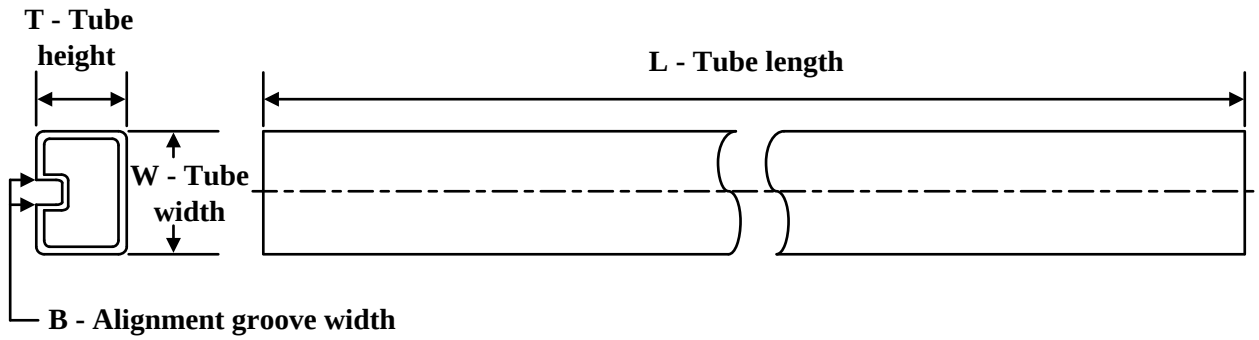
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN751701PSR	SO	PS	8	2000	353.0	353.0	32.0

TUBE

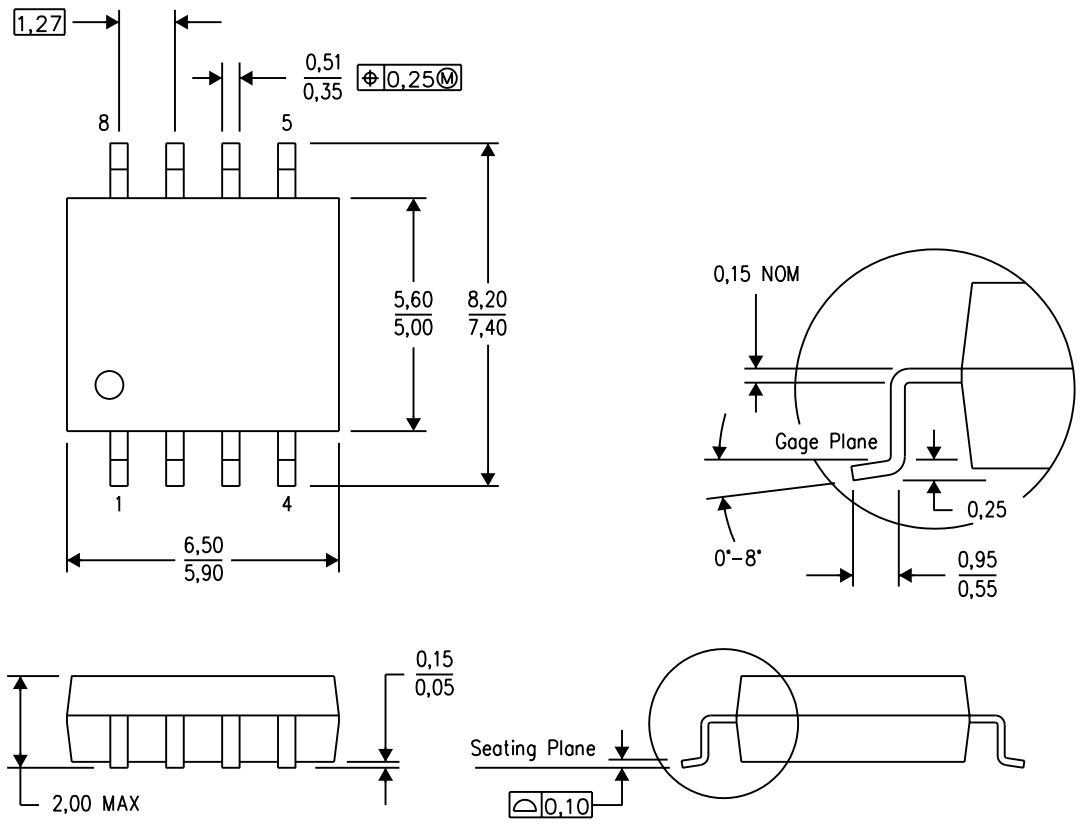


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN751701P	P	PDIP	8	50	506	13.97	11230	4.32
SN751701P.A	P	PDIP	8	50	506	13.97	11230	4.32

MECHANICAL DATA

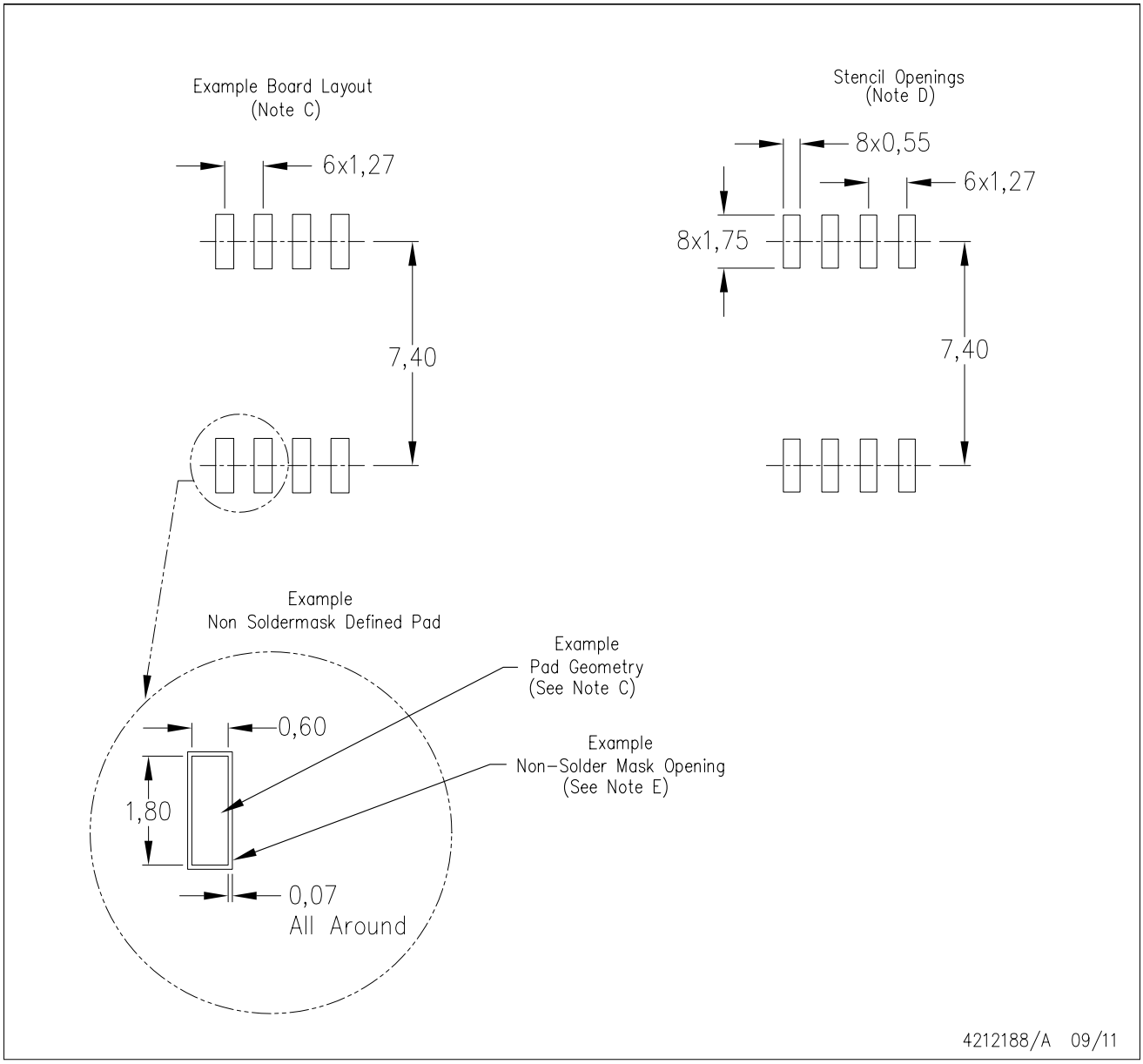
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

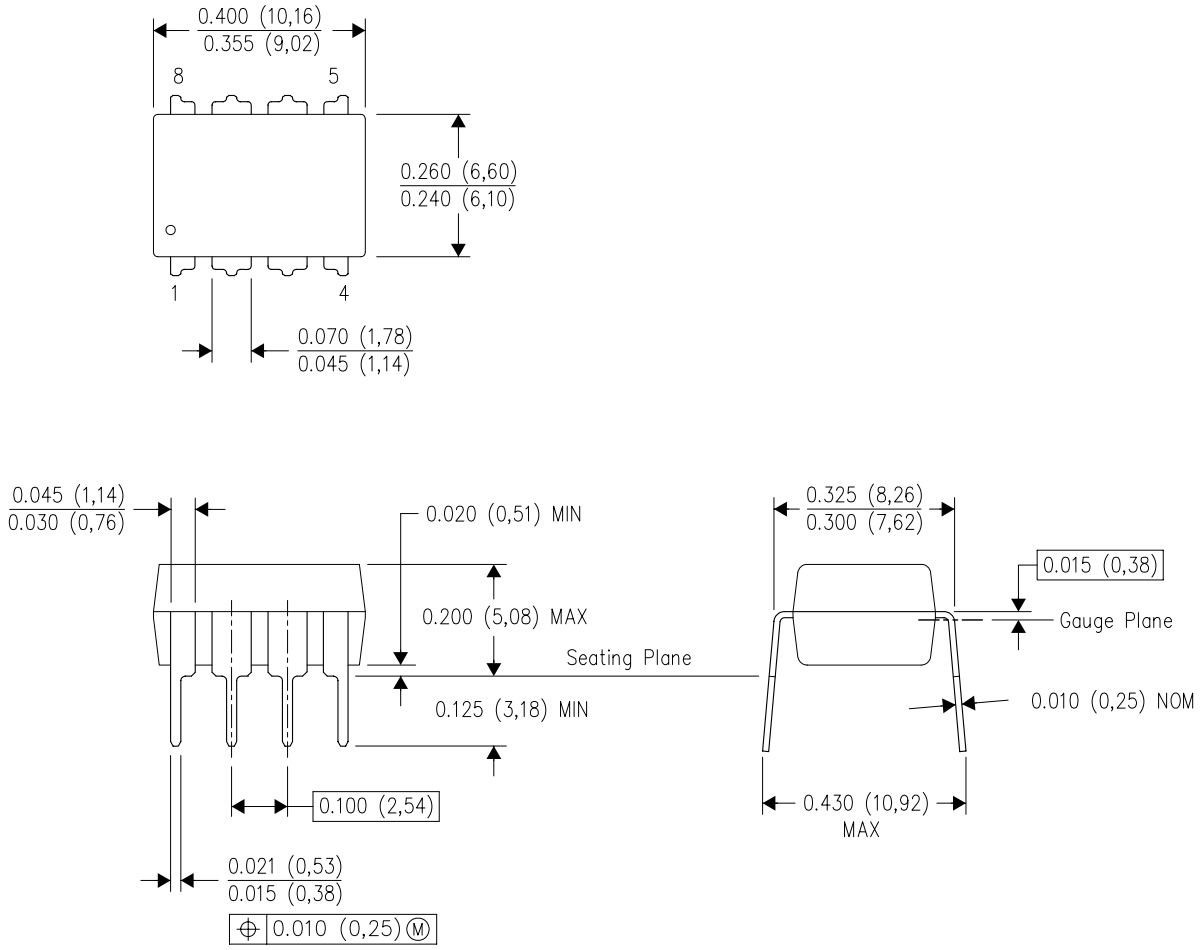
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated