

- Designed to be Used in Voltage-Limiting Applications
- 6.5-Ω On-State Connection Between Ports A and B
- Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing
- Direct Interface With GTL+ Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

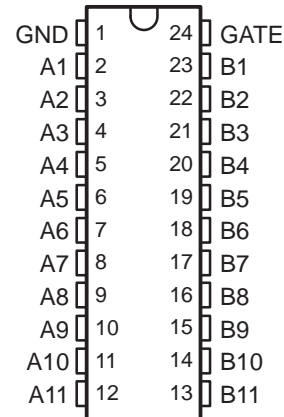
### description/ordering information

The SN74TVC3010 provides 11 parallel NMOS pass transistors with a common gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can be used as a 10-bit switch with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots. (See Application Information in this data sheet.)

All of the transistors in the TVC array have the same electrical characteristics; therefore, any one of them can be used as the reference transistor. Since, within the device, the characteristics from transistor to transistor are equal, the maximum output high-state voltage ( $V_{OH}$ ) is approximately the reference voltage ( $V_{REF}$ ), with minimal deviation from one output to another. This is a large benefit of the TVC solution over discrete devices. Because the fabrication of the transistors is symmetrical, either port connection of each bit can be used as the low-voltage side, and the I/O signals are bidirectional through each FET.

### DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)



### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74TVC3010DW	TVC3010
		Tape and reel	SN74TVC3010DWR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74TVC3010DBQR	TVC3010
	TSSOP – PW	Tape and reel	SN74TVC3010PWR	TT010
	TVSOP – DGV	Tape and reel	SN74TVC3010DGVR	TT010

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

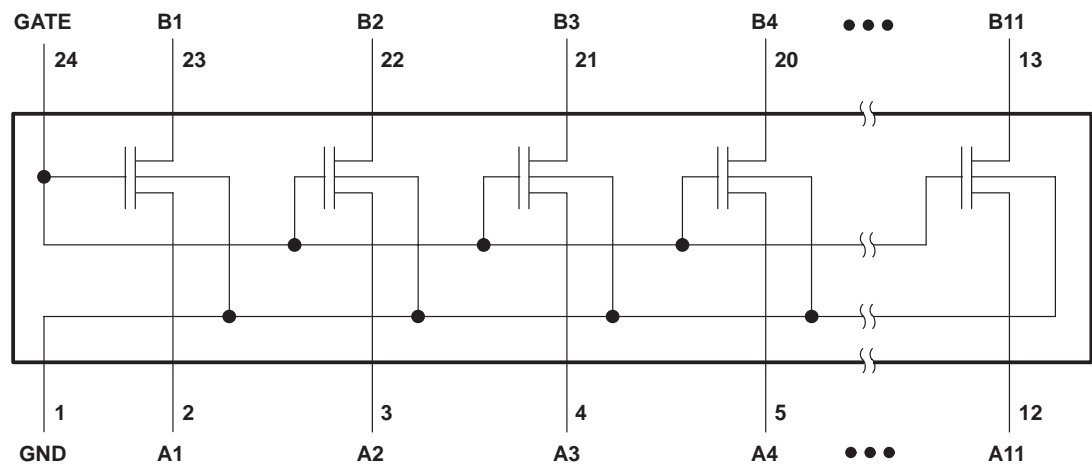
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SN74TVC3010  
10-BIT VOLTAGE CLAMP

SCDS088G – APRIL 1999 – REVISED AUGUST 2003

simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Input/output voltage range, $V_{I/O}$ (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	TYP	MAX	UNIT
$V_{I/O}$	Input/output voltage	0		5	V
$V_{GATE}$	GATE voltage	0		5	V
$I_{PASS}$	Pass-transistor current		20	64	mA
$T_A$	Operating free-air temperature	–40		85	°C

**application operating conditions (see Figure 3)**

		MIN	TYP	MAX	UNIT
V <sub>BIAS</sub>	BIAS voltage	V <sub>REF</sub> + 0.6	2.1	5	V
V <sub>GATE</sub>	GATE voltage	V <sub>REF</sub> + 0.6	2.1	5	V
V <sub>REF</sub>	Reference voltage	0	1.5	4.4	V
V <sub>DPU</sub>	Drain pullup voltage	2.36	2.5	2.64	V
I <sub>PASS</sub>	Pass-transistor current		14		mA
I <sub>REF</sub>	Reference-transistor current		5		μA
T <sub>A</sub>	Operating free-air temperature	–40		85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	V <sub>BIAS</sub> = 0,	I <sub>I</sub> = –18 mA				–1.2	V
V <sub>OL</sub>	I <sub>REF</sub> = 5 μA, V <sub>DPU</sub> = 2.625 V,	V <sub>REF</sub> = 1.365 V, R <sub>DPU</sub> = 150 Ω	V <sub>S</sub> = 0.175 V, See Figure 1			350	mV
C <sub>i</sub> (GATE)	V <sub>I</sub> = 3 V or 0				24		pF
C <sub>io</sub> (off)	V <sub>O</sub> = 3 V or 0				4	12	pF
C <sub>io</sub> (on)	V <sub>O</sub> = 3 V or 0				12	30	pF
r <sub>on</sub> ‡	I <sub>REF</sub> = 5 μA, V <sub>DPU</sub> = 2.625 V,	V <sub>REF</sub> = 1.365 V, R <sub>DPU</sub> = 150 Ω	V <sub>S</sub> = 0.175 V, See Figure 1			12.5	Ω

† All typical values are at T<sub>A</sub> = 25°C.

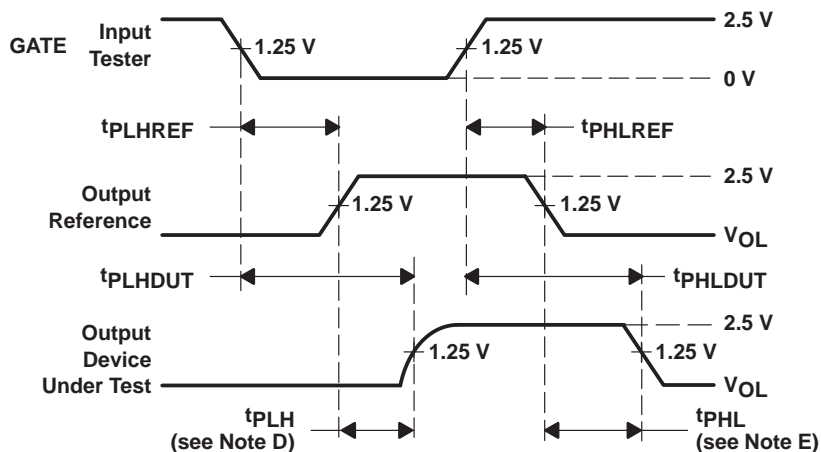
‡ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range, V<sub>DPU</sub> = 2.36 V to 2.64 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>PLH</sub>	A or B	B or A	0	4	ns
t <sub>PHL</sub>			0	4	

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DEFINITION	SYMBOL
Output tested	†
Output reference	‡
Input tested	§



## VOLTAGE WAVEFORMS

### PROPAGATION DELAY TIMES

- NOTES:
- A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - B. The outputs are measured one at a time with one transition per measurement.
  - C. Test procedure:  $t_{PLHREF}$  and  $t_{PLHREF}$  are obtained by measuring the propagation delay of a reference measuring point.  $t_{PLHDUT}$  and  $t_{PLHDUT}$  are obtained by measuring the propagation delay of the device under test.
  - D.  $t_{PLH} = t_{PLHDUT} - t_{PLHREF}$
  - E.  $t_{PHL} = t_{PHLDUT} - t_{PHLREF}$

### Figure 1. Tester Calibration Setup and Voltage Waveforms

## APPLICATION INFORMATION

### TVC background information

In personal computer (PC) architecture, there are industry-accepted bus standards. These standards define, among other things, the I/O voltage levels at which the bus communicates. Examples include the GTL+ host bus, the AGP graphics port, and the PCI local bus. In new designs, the system components must communicate with existing bus infrastructure. Providing an evolutionary upgrade path is important in the design of PC architecture, but the existing bus standards must be preserved.

To achieve the ever-present need for smaller, faster, lighter devices that draw less power, yet have faster performance, most new high-performance digital integrated circuits are being designed and produced with advanced submicron semiconductor process technologies. These devices have thin gate-oxide or short channel lengths and very low absolute-maximum voltages that can be tolerated at the inputs/outputs (I/Os) without causing damage. In many cases, the I/Os of these devices are not tolerant of the high-state voltage levels on the preexisting buses with which they must communicate. Therefore, it became necessary to protect the I/Os of devices by limiting the I/O voltages.

The Texas Instruments (TI) translation voltage-clamp (TVC) family was designed specifically for protecting sensitive I/Os (see Figure 2). The information in this data sheet describes the I/O-protection application of the TVC family and should enable the design engineer to successfully implement an I/O-protection circuit utilizing the TI TVC solution.

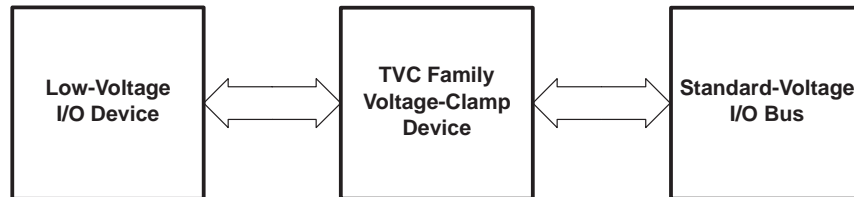
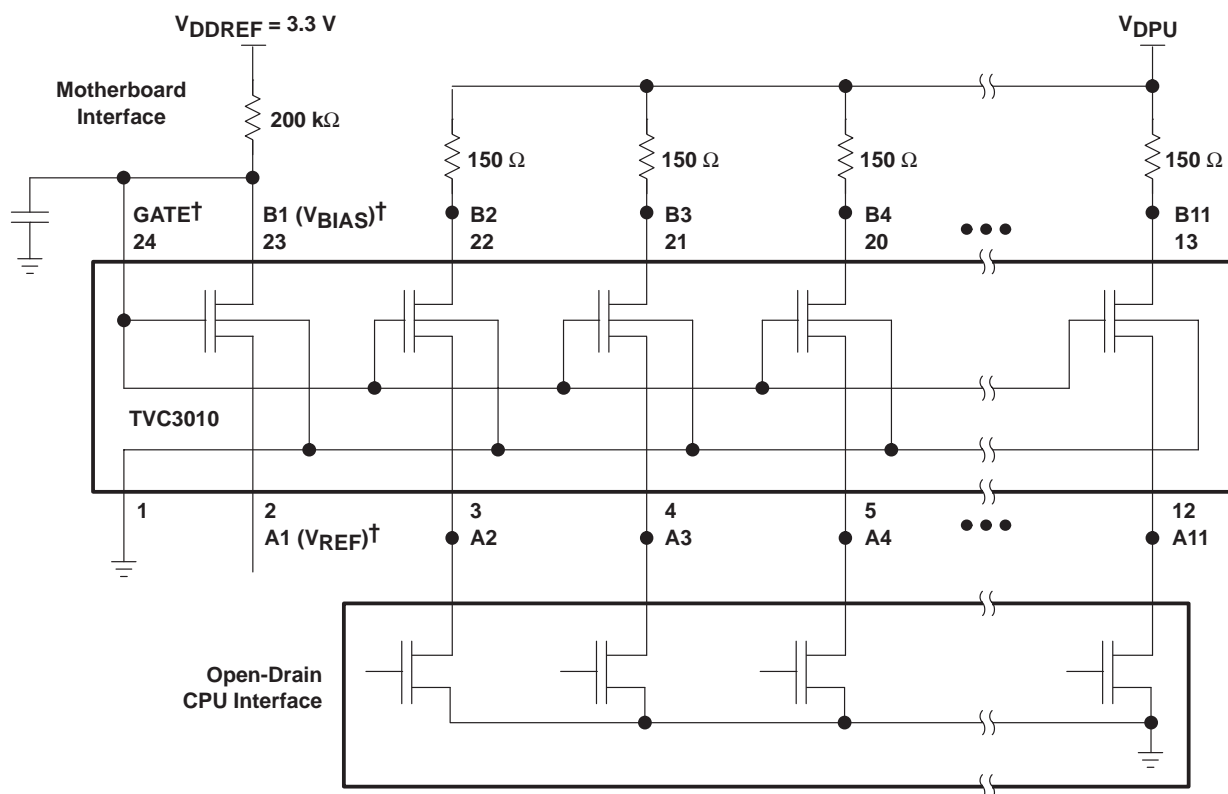


Figure 2. Thin Gate-Oxide Protection Application

### APPLICATION INFORMATION

#### TVC voltage-limiting application

For the voltage-limiting configuration, the common GATE input must be connected to one side (A or B) of any one of the transistors (see Figure 3). This connection determines the  $V_{BIAS}$  input of the reference transistor. The  $V_{BIAS}$  input is connected through a pullup resistor (typically, 200 k $\Omega$ ) to the  $V_{DD}$  supply. A filter capacitor on  $V_{BIAS}$  is recommended. The opposite side of the reference transistor is used as the reference voltage ( $V_{REF}$ ) connection. The  $V_{REF}$  input must be less than  $V_{DDREF} - 1$  V to bias the reference transistor into conduction. The reference transistor regulates the gate voltage ( $V_{GATE}$ ) of all the pass transistors.  $V_{GATE}$  is determined by the characteristic gate-to-source voltage difference ( $V_{GS}$ ) because  $V_{GATE} = V_{REF} + V_{GS}$ . The low-voltage side of the pass transistors has a high-level voltage limited to a maximum of  $V_{GATE} - V_{GS}$ , or  $V_{REF}$ .



†  $V_{REF}$  and  $V_{BIAS}$  can be applied to any one of the pass transistors. GATE must be connected externally to  $V_{BIAS}$ .

Figure 3. Typical Application Circuit

## APPLICATION INFORMATION

### electrical characteristics

The electrical characteristics of the NMOS transistors used in the TVC devices are illustrated by TI SPICE simulations. Figure 4 shows the test configuration for the TI SPICE simulations. The results, shown in Figures 5 and 6, show the current through a pass transistor versus the voltage at the source for different reference voltages. The plots of the dc characteristics clearly reveal that the device clamps at the desired reference voltage for the varying device environments.

Figure 5 shows the V-I characteristics, with low reference voltages and a reference-transistor drain-supply voltage of 3.3 V. To further investigate the spread of the V-I characteristic curves,  $V_{REF}$  was held at 2.5 V and  $I_{REF}$  was increased by raising  $V_{DDREF}$  (see Figure 6). The result was a tighter grouping of the V-I curves.

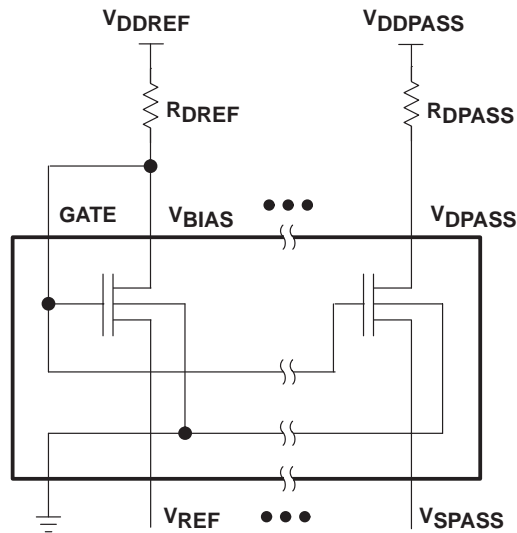


Figure 4. TI SPICE Simulation Schematic and Voltage-Node Names

APPLICATION INFORMATION

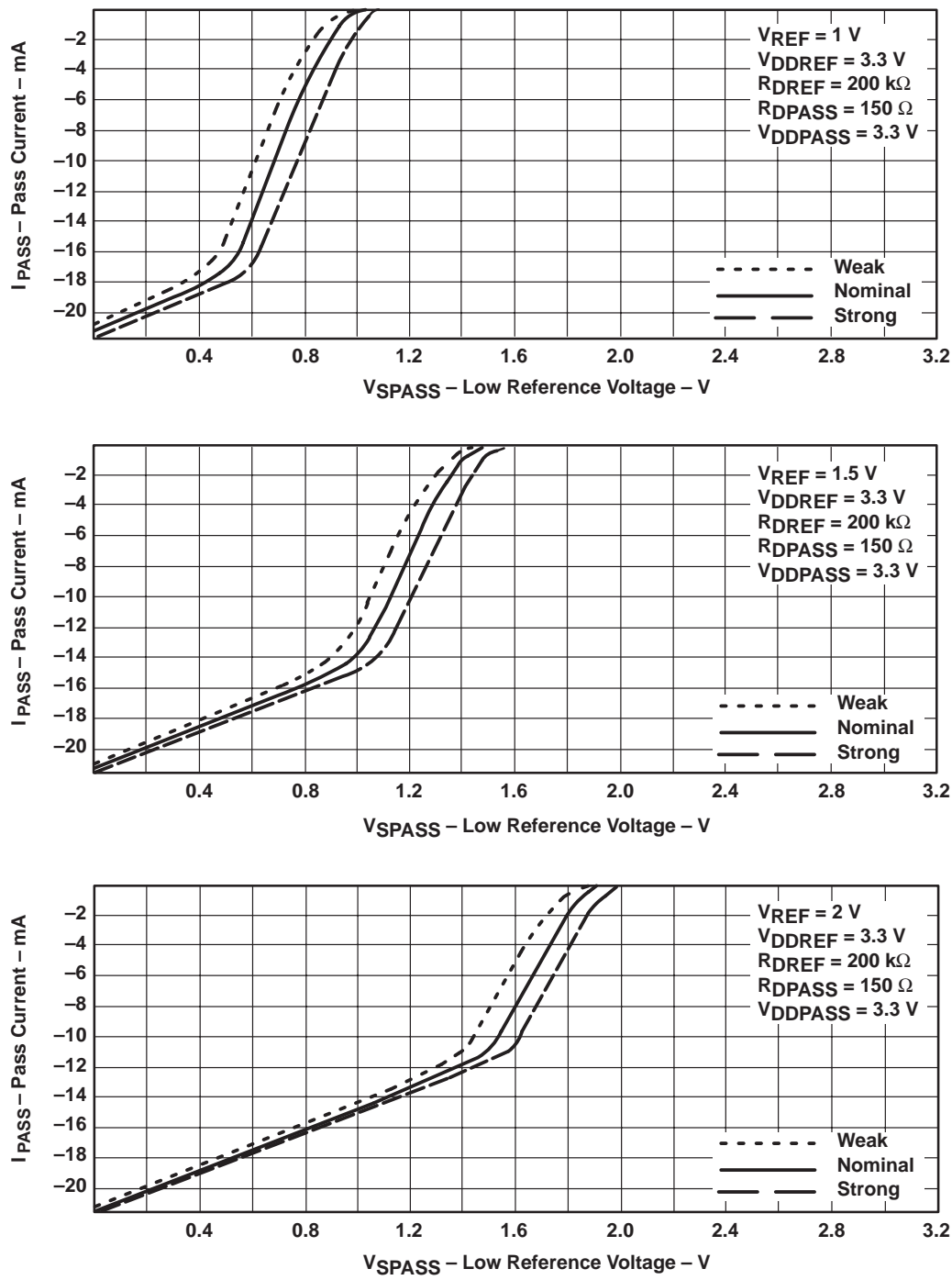


Figure 5. Electrical Characteristics at Low  $V_{REF}$  Voltages



## APPLICATION INFORMATION

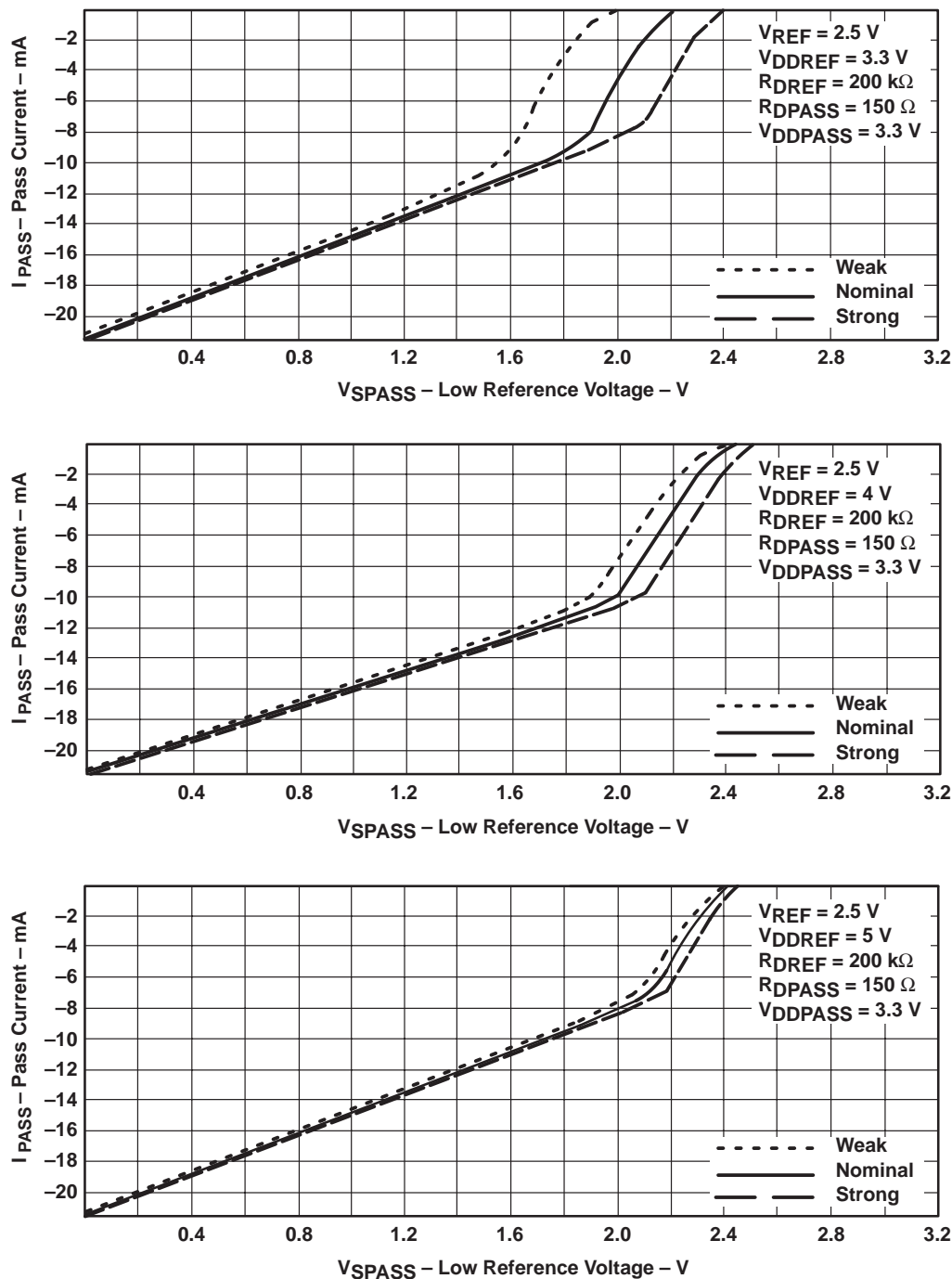


Figure 6. Electrical Characteristics at  $V_{REF} = 2.5\text{ V}$

### APPLICATION INFORMATION

#### features and benefits

The TVC family has several features that benefit a system designer when implementing a sensitive-I/O-protection solution. Table 1 lists these features and their associated benefits.

**Table 1. Features and Benefits**

FEATURES	BENEFITS
Any FET can be used as the reference transistor.	Ease of layout
All FETs on one die, tight process control	Very low spread of $V_O$ relative to $V_{REF}$
No active control logic (passive device)	No logic power supply ( $V_{CC}$ ) required
Flow-through pinout	Ease of trace routing
Devices offered in different bit-widths and packages	Optimizes design and cost effectiveness
Designer flexibility with $V_{REF}$ input	Allows migration to lower-voltage I/Os without board redesign

#### conclusion

The TI TVC family provides the designer with a solution for protection of circuits with I/Os that are sensitive to high-state voltage-level overshoots. The flexibility of TVC enables a low-voltage migration path for advanced designs to align with industry standards.

#### frequently asked questions (FAQ)

- Q: Can any of the transistors in the array be used as the reference transistor?  
A: Yes, any transistor can be used as long as its  $V_{BIAS}$  pin is connected to the GATE pin.
- Q: In the recommended operating conditions table of the data sheet, the typical  $V_{BIAS}$  is 3.3 V. Should  $V_{BIAS}$  be equal to or greater than  $V_{REF}$  on the reference transistor?  
A:  $V_{BIAS}$  is a variable that is determined by  $V_{REF}$ .  $V_{BIAS}$  is connected to  $V_{DD}$  through a resistor to allow the bias voltage to be controlled by  $V_{REF}$ .  $V_{DD}$  can be as high as 5.5 V.  $V_{REF}$  needs to be at least 1 V less than  $V_{DDREF}$  on the reference transistor.
- Q: Do both A and B ports have 5-V I/O tolerance or is 5-V I/O tolerance provided only on the low-voltage side?  
A: Both ports are 5-V tolerant.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74TVC3010DBQR</a>	NRND	Production	SSOP (DBQ)   24	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TVC3010
SN74TVC3010DBQR.A	NRND	Production	SSOP (DBQ)   24	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TVC3010
<a href="#">SN74TVC3010DGVR</a>	NRND	Production	TVSOP (DGV)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TT010
SN74TVC3010DGVR.A	NRND	Production	TVSOP (DGV)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TT010
<a href="#">SN74TVC3010DW</a>	NRND	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC3010
SN74TVC3010DW.A	NRND	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC3010
<a href="#">SN74TVC3010DWR</a>	NRND	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC3010
SN74TVC3010DWR.A	NRND	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC3010
<a href="#">SN74TVC3010PW</a>	NRND	Production	TSSOP (PW)   24	60   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TT010
SN74TVC3010PW.A	NRND	Production	TSSOP (PW)   24	60   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TT010
<a href="#">SN74TVC3010PWR</a>	NRND	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TT010
SN74TVC3010PWR.A	NRND	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TT010

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74TVC3010DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74TVC3010DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74TVC3010DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74TVC3010DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74TVC3010DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
SN74TVC3010DWR	SOIC	DW	24	2000	350.0	350.0	43.0

## TUBE

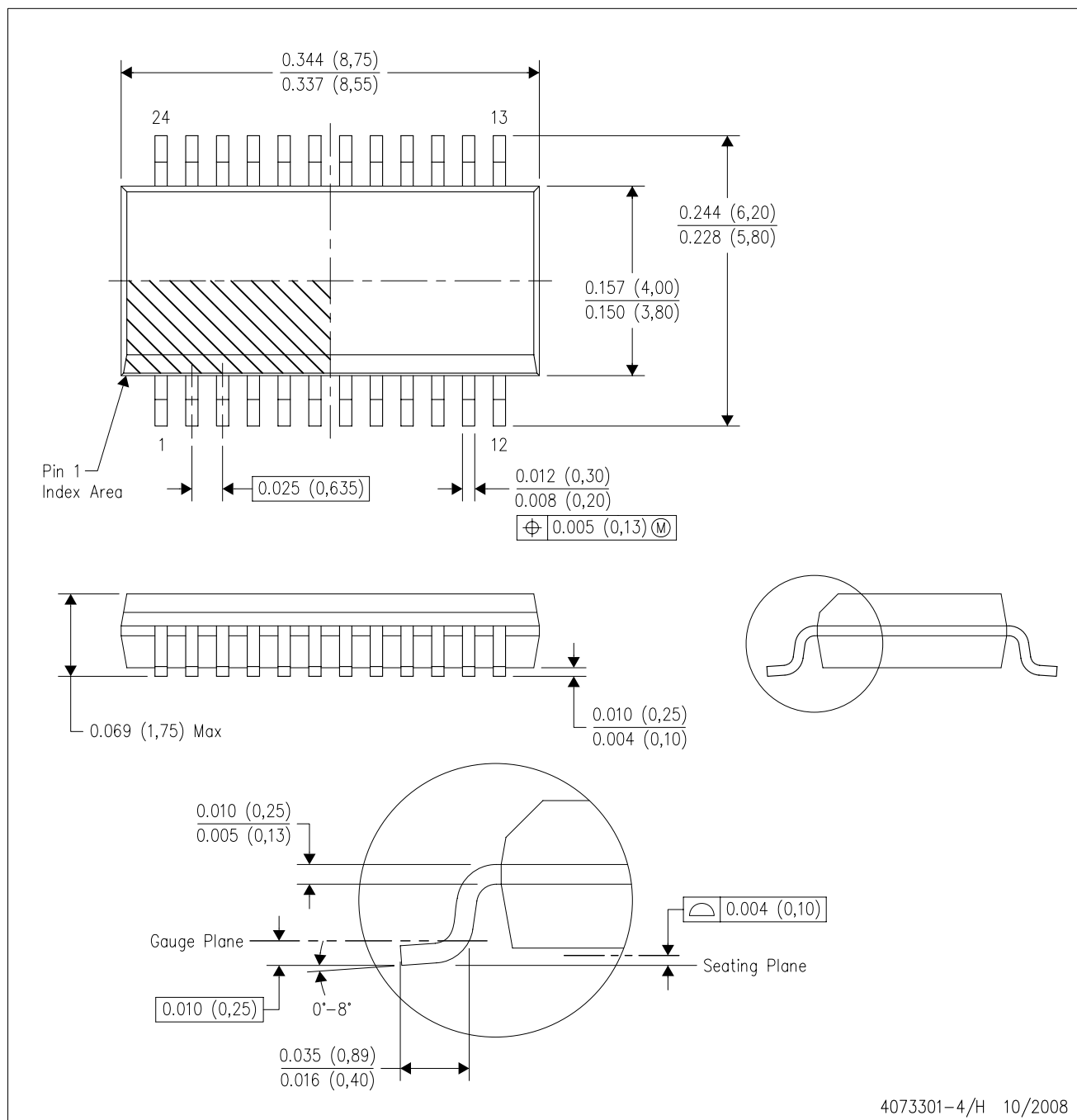


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74TVC3010DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74TVC3010DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74TVC3010PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74TVC3010PW.A	PW	TSSOP	24	60	530	10.2	3600	3.5

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.





## PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

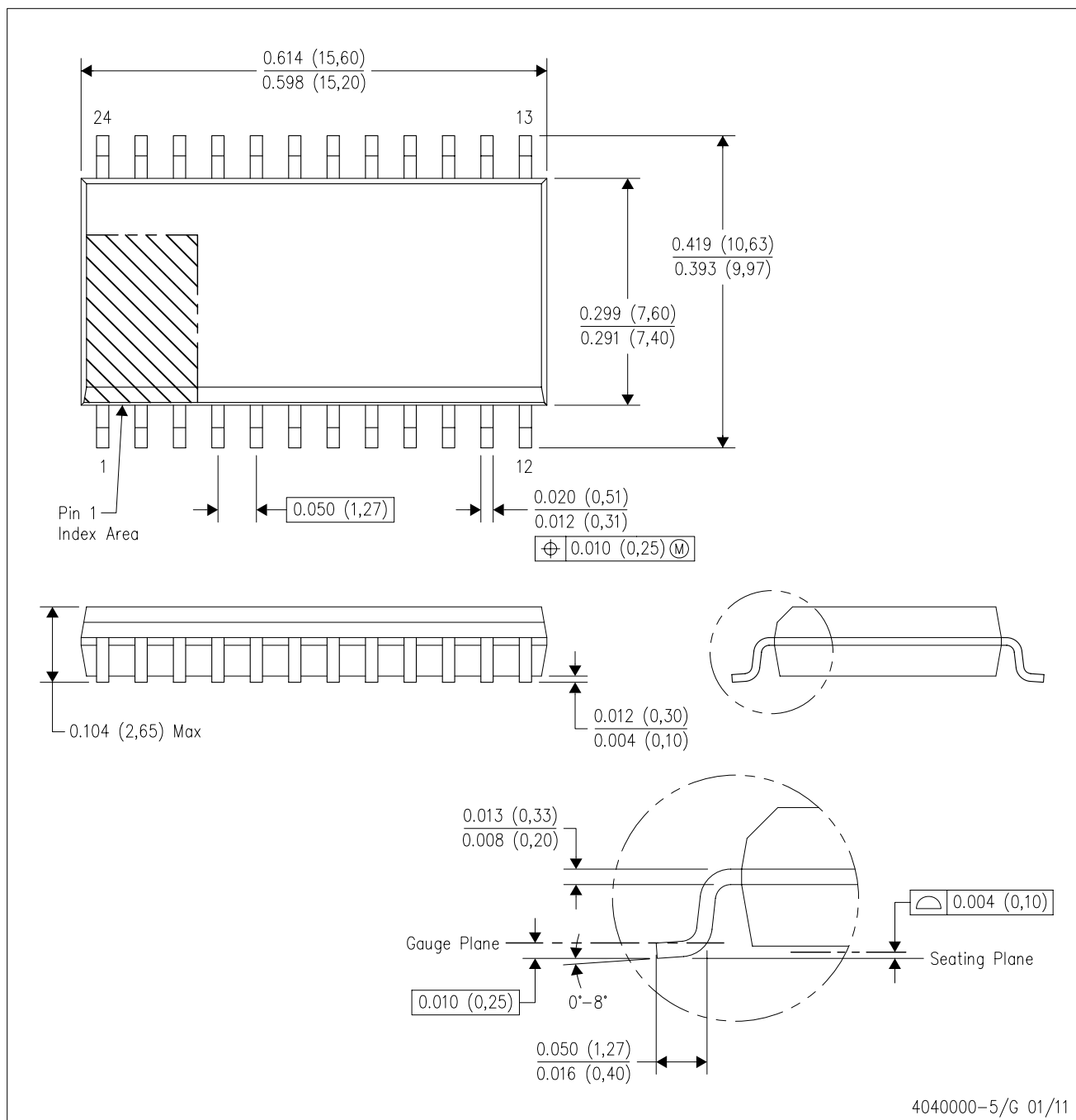
4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.



**TVSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



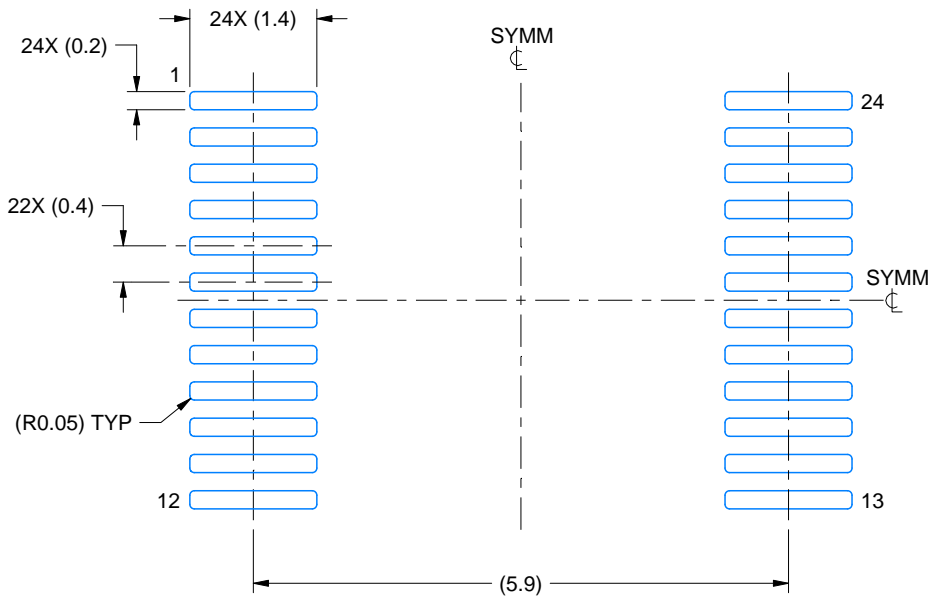
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

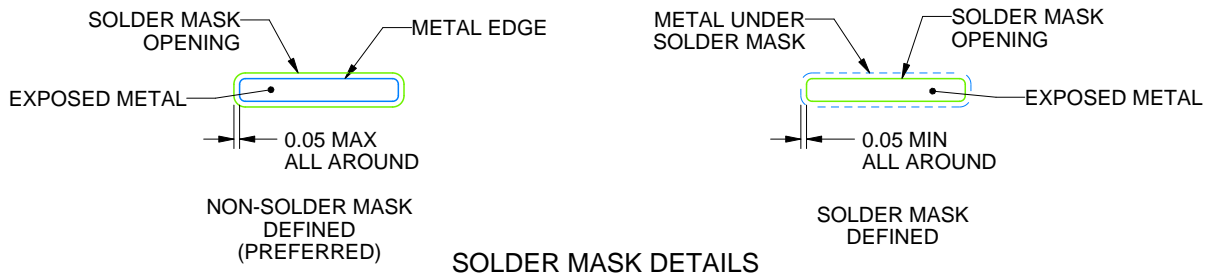
DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 12X



SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

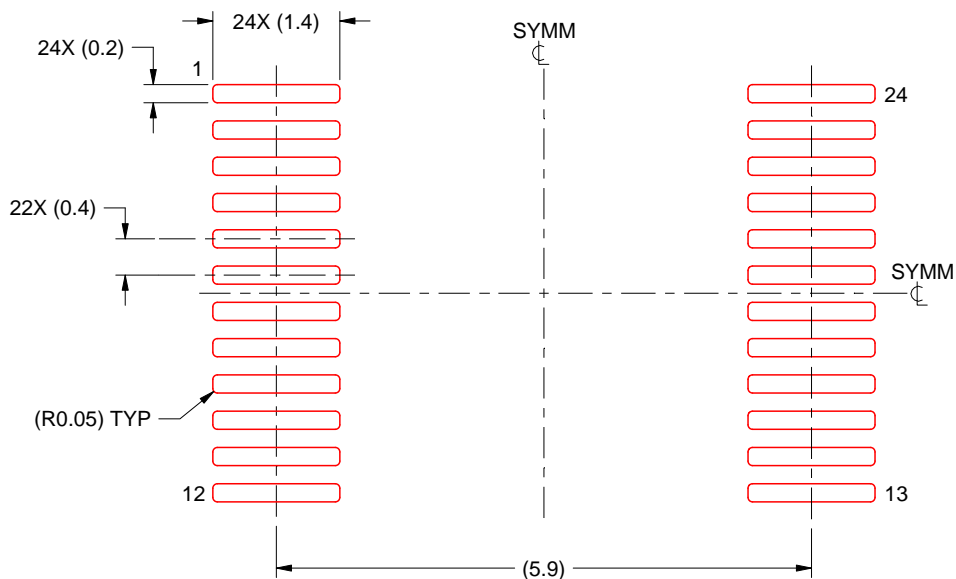
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 12X

4229221/A 12/2022

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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