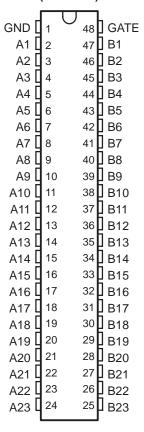
- **Member of the Texas Instruments** Widebus™ Family
- Designed to Be Used in Voltage-Limiting **Applications**
- **6.5-**Ω On-State Connection Between Ports A and B
- Flow-Through Pinout for Ease of Printed **Circuit Board Trace Routing**
- **Direct Interface With GTL+ Levels**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

The SN74TVC16222A provides 23 parallel NMOS pass transistors with a common gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delav.

The device can be used as a 22-bit switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots. (See Application Information in this data sheet.)

DGG, DGV, OR DL PACKAGE (TOP VIEW)



All of the transistors in the TVC array have the same electrical characteristics; therefore, any one of them can be used as the reference transistor. Because, within the device, the characteristics from transistor to transistor are equal, the maximum output high-state voltage (V_{OH}) is approximately the reference voltage (V_{REF}), with minimal deviation from one output to another. This is a benefit of the TVC solution over discrete devices. Because the fabrication of the transistors is symmetrical, either port connection of each bit can be used as the low-voltage side, and the I/O signals are bidirectional through each FET.

ORDERING INFORMATION

TA	PACK	∖GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	CCOD DI	Tube	SN74TVC16222DL	TVC4C000A		
4000 to 0500	SSOP – DL	Tape and reel	SN74TVC16222DLR	TVC16222A		
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74TVC16222DGGR	TVC16222A		
	TVSOP - DGV	Tape and reel	SN74TVC16222DGVR	TW222A		

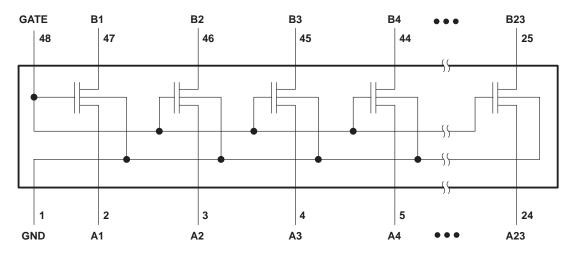
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Input/output voltage range, V _{I/O} (see Note 1)		0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
***	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	TYP	MAX	UNIT
V _{I/O}	Input/output voltage	0		5.5	V
VGATE	GATE voltage	0		5.5	V
IPASS	Pass-transistor current		20	64	mA
TA	Operating free-air temperature	-40		85	°C

application operating conditions (see Figure 3)

		MIN	TYP	MAX	UNIT
V _{BIAS}	BIAS voltage	V _{REF} + 0.6	2.1	5	V
VGATE	GATE voltage	V _{REF} + 0.6	2.1	5	V
VREF	Reference voltage	0	1.5	4.4	V
V _{DPU}	Drain pullup voltage	2.36	2.5	2.64	V
IPASS	Pass-transistor current		14	20	mA
I _{REF}	Reference-transistor current		5		μΑ
TA	Operating free-air temperature	-40		85	°C



NOTES: 1. The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	3	MIN	TYP	MAX	UNIT
VIK	$V_{BIAS} = 0$,	$I_{I} = -18 \text{ mA}$				-1.2	V
V _{OL}	$I_{REF} = 5 \mu A,$ $V_{DPU} = 2.625 V,$	V_{REF} = 1.365 V, R_{DPU} = 150 Ω	$V_S = 0.175 V$, See Figure 2			350	mV
C _i (GATE)	V _I = 3 V or 0				73		pF
C _{io(off)}	V _O = 3 V or 0				4	12	pF
C _{io(on)}	V _O = 3 V or 0				12	25	pF
r _{on} ‡	I _{REF} = 5 μA, V _{DPU} = 2.625 V,	$V_{REF} = 1.365 V,$ $R_{DPU} = 150 \Omega$	$V_S = 0.175 \text{ V}$, See Figure 2			12.5	Ω

[†] All typical values are at $T_A = 25$ °C.

electrical characteristics from -40°C to 75°C

PARAMETER		M	N MAX	UNIT		
r _{on} ‡	I _{REF} = 5 μA, V _{DPU} = 2.625 V,	V_{REF} = 1.552 V, R_{DPU} = 150 Ω	$V_S = 0.175 V$, See Figure 2		10	Ω

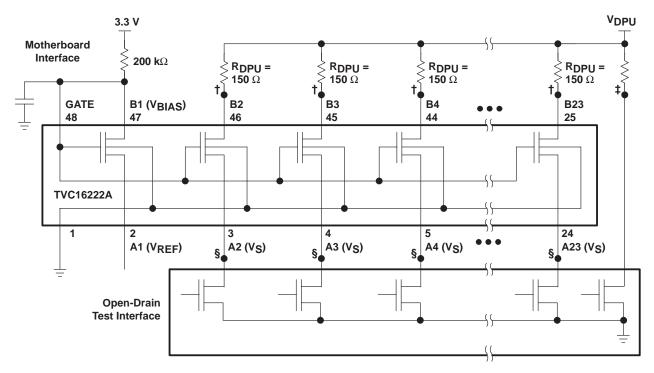
[‡] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $V_{DPU} = 2.36 \text{ V}$ to 2.64 V (unless otherwise noted) (see Figure 1)

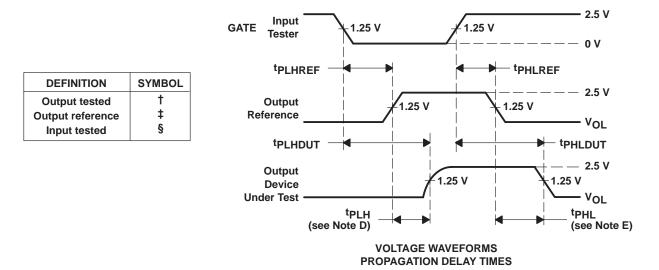
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{PLH}	A B	D A	0	4	
^t PHL	A or B	B or A	0	4	ns

[‡] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

PARAMETER MEASUREMENT INFORMATION



TESTER CALIBRATION SETUP (see Note C)



NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns. $t_f \leq$ 2 ns.

- B. The outputs are measured one at a time, with one transition per measurement.
- C. Test procedure: tpLHREF and tpHLREF are obtained by measuring the propagation delay of a reference measuring point. tPLHDUT and tPHLDUT are obtained by measuring the propagation delay of the device under test.
- D. tplH = tplHDUT tplHREF E. tpHL = tpHLDUT tpHLREF

Figure 1. Tester Calibration Setup and Voltage Waveforms



TVC background information

In personal computer (PC) architecture, there are industry-accepted bus standards. These standards define, among other things, the I/O voltage levels at which the bus communicates. Examples include the GTL+ host bus, the AGP graphics port, and the PCI local bus. In new designs, the system components must communicate with existing bus infrastructure. Providing an evolutionary upgrade path is important in the design of PC architecture, but the existing bus standards must be preserved.

To achieve the ever-present need for smaller, faster, lighter devices that draw less power, yet have faster performance, most new high-performance digital integrated circuits are designed and produced with advanced submicron semiconductor process technologies. These devices have thin gate-oxide or short channel lengths and very low absolute-maximum voltages that can be tolerated at the inputs/outputs (I/Os) without causing damage. In many cases, the I/Os of these devices are not tolerant of the high-state voltage levels on the preexisting buses with which they must communicate. Therefore, it became necessary to protect the I/Os of devices by limiting the I/O voltages.

The Texas Instruments (TITM) translation voltage-clamp (TVC) family is designed specifically for protecting sensitive I/Os (see Figure 2). The information in this data sheet describes the I/O-protection application of the TVC family and should enable the design engineer to successfully implement an I/O-protection circuit utilizing the TI TVC solution.

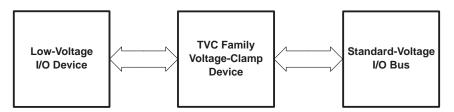
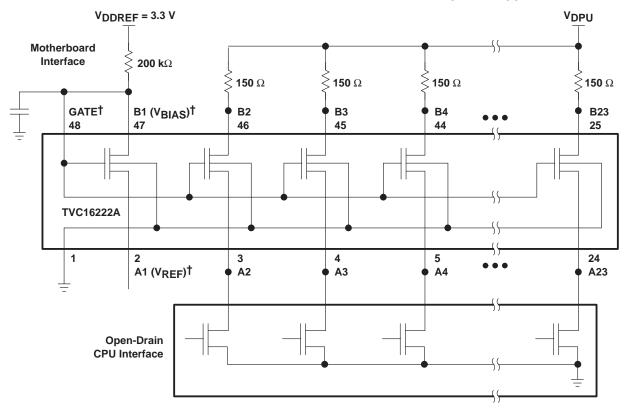


Figure 2. Thin Gate-Oxide Protection Application

TVC voltage-limiting application

For the voltage-limiting configuration, the common GATE input must be connected to one side (A or B) of any one of the transistors (see Figure 3). This connection determines the V_{BIAS} input of the reference transistor. The V_{BIAS} input is connected through a pullup resistor (typically 200 k Ω) to the V_{DD} supply. A filter capacitor on V_{BIAS} is recommended. The opposite side of the reference transistor is used as the reference voltage (V_{REF}) connection. The V_{REF} input must be less than $V_{DDREF}-1$ V to bias the reference transistor into conduction. The reference transistor regulates the gate voltage (V_{GATE}) of all the pass transistors. V_{GATE} is determined by the characteristic gate-to-source voltage difference (V_{GS}) because $V_{GATE}=V_{REF}+V_{GS}$. The low-voltage side of the pass transistors has a high-level voltage limited to a maximum of $V_{GATE}-V_{GS}$, or V_{REF} .



[†]VREF and VBIAS can be applied to any one of the pass transistors. GATE must be connected externally to VBIAS.

Figure 3. Typical Application Circuit



electrical characteristics

The electrical characteristics of the NMOS transistors used in the TVC devices are illustrated by TI SPICE simulations. Figure 4 shows the test configuration for the TI SPICE simulations. The results, shown in Figures 5 and 6, show the current through a pass transistor versus the voltage at the source for different reference voltages. The plots of the dc characteristics clearly reveal that the device clamps at the desired reference voltage for the varying device environments.

Figure 5 shows the V-I characteristics with low reference voltages and a reference-transistor drain-supply voltage of 3.3 V. To further investigate the spread of the V-I characteristic curves, V_{REF} was held at 2.5 V and I_{REF} was increased by raising V_{DDRFF} (see Figure 6). The result was a tighter grouping of the V-I curves.

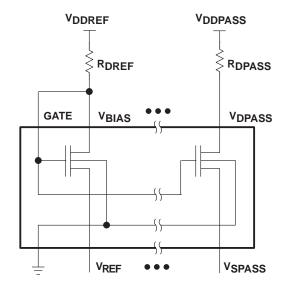


Figure 4. TI SPICE-Simulation Schematic and Voltage-Node Names

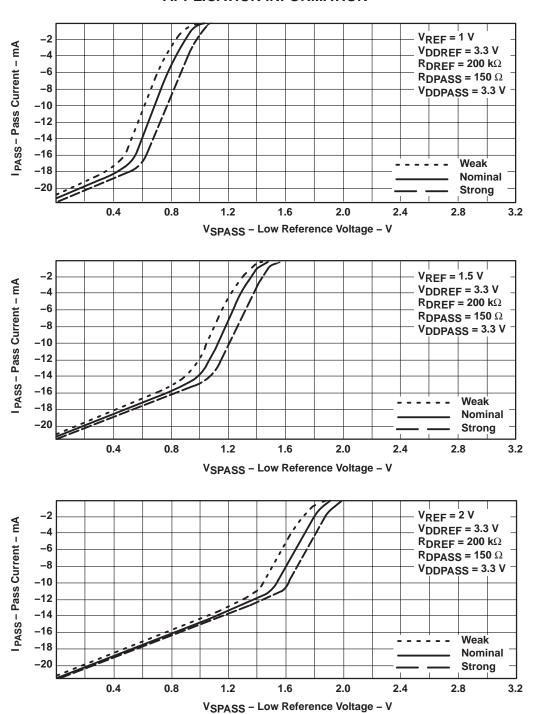


Figure 5. V-I Electrical Characteristics at Low V_{REF} Voltages



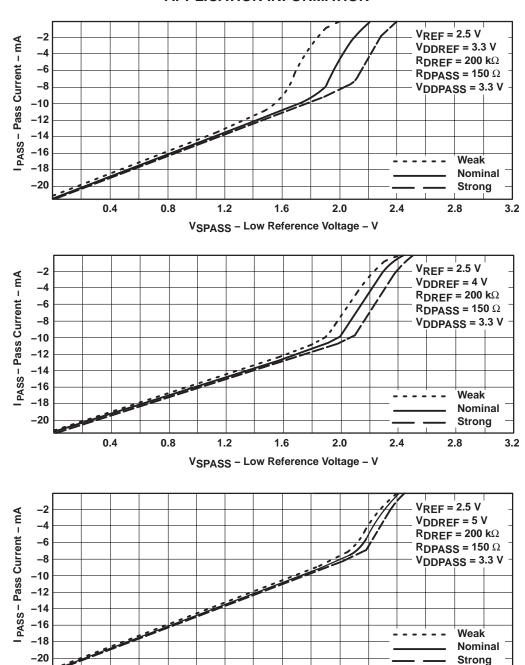


Figure 6. V-I Electrical Characteristics at $V_{REF} = 2.5 \text{ V}$

1.6

VSPASS - Low Reference Voltage - V

2.0

2.4

3.2

2.8

1.2

0.4

8.0



features and benefits

The TVC family has several features that benefit a system designer when implementing a sensitive-I/O-protection solution. Table 1 lists these features and their associated benefits.

Table 1. Features and Benefits

FEATURES	BENEFITS
Any FET can be used as the reference transistor.	Ease of layout
All FETs on one die, tight process control	Very low spread of VO relative to VREF
No active control logic (passive device)	No logic power supply (V _{CC}) required
Flow-through pinout	Ease of trace routing
Devices offered in different bit widths and packages	Optimizes design and cost effectiveness
Designer flexibility with V _{REF} input	Allows migration to lower-voltage I/Os without board redesign

conclusion

The TI TVC family provides the designer with a solution for protection of circuits with I/Os that are sensitive to high-state voltage-level overshoots. The flexibility of TVC enables a low-voltage migration path for advanced designs to align with industry standards.

frequently asked questions (FAQs)

- 1. Q: Can any of the transistors in the array be used as the reference transistor?
 - A: Yes, any transistor can be used as long as its V_{BIAS} pin is connected to the GATE pin.
- 2. Q: In the *recommended operating conditions* table of the data sheet, the typical V_{BIAS} is 3.3 V. Should V_{BIAS} be equal to or greater than V_{REF} on the reference transistor?
 - A: V_{BIAS} is a variable that is determined by V_{REF}. V_{BIAS} is connected to V_{DD} through a resistor to allow the bias voltage to be controlled by V_{REF}. V_{DD} can be as high as 5.5 V. V_{REF} needs to be at least 1 V less than V_{DDRFF} on the reference transistor.
- 3. Q: Do both A and B ports have 5-V I/O tolerance or is 5-V I/O tolerance provided only on the low-voltage side?
 - A: Both ports are 5-V tolerant.



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74TVC16222ADGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC16222A
SN74TVC16222ADGGR.A	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC16222A
SN74TVC16222ADGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TW222A
SN74TVC16222ADGVR.A	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TW222A
SN74TVC16222ADL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC16222A
SN74TVC16222ADL.A	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC16222A
SN74TVC16222ADLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC16222A
SN74TVC16222ADLR.A	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TVC16222A

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74TVC16222ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74TVC16222ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74TVC16222ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74TVC16222ADGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74TVC16222ADGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74TVC16222ADLR	SSOP	DL	48	1000	356.0	356.0	53.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74TVC16222ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74TVC16222ADL.A	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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