28-Bit to 56-Bit Registered Buffer With Address Parity Test One Pair to Four Pair Differential Clock PLL Driver

Check for Samples: SN74SSQEA32882

FEATURES

- **JEDEC SSTE32882 Compliant**
- **1-to-2 Register Outputs and 1-to-4 Clock Pair Outputs Support Stacked DDR3 RDIMMs**
- **CKE Powerdown Mode for Optimized System Power Consumption**
- **1.5V/1.35V Phase Lock Loop Clock Driver for Buffering One Differential Clock Pair (CK and $\overline{CK}$) and Distributing to Four Differential Outputs**
- **1.5V/1.35V CMOS Inputs**
- **Checks Parity on Command and Address (CS-Gated) Data Inputs**
- **Configurable Driver Strength**
- **Uses Internal Feedback Loop**

APPLICATIONS

- **DDR3 Registered DIMMs up to DDR3-1600**
- **DDR3L Registered DIMMs up to DDR3L-1333**
- **Single-, Dual- and Quad-Rank RDIMM**

DESCRIPTION

This JEDEC SSTE32882-compliant, 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for operation on DDR3 registered DIMMs with V_{DD} of 1.5 V and on DDR3L registered DIMMs with V_{DD} of 1.35 V.

All inputs are 1.5 V and 1.35 V CMOS compatible. All outputs are CMOS drivers optimized to drive DRAM signals on terminated traces in DDR3 RDIMM applications. The clock outputs Yn and $\overline{Yn}$ and control net outputs DxCKEn, $\overline{DxCSn}$ and DxODTn can be driven with a different strength and skew to optimize signal integrity, compensate for different loading and equalize signal travel speed.

The SN74SSQEA32882 has two basic modes of operation associated with the Quad Chip Select Enable ($\overline{QCSEN}$) input. When the $\overline{QCSEN}$ input pin is open (or pulled high), the component has two chip select inputs, $\overline{DCS0}$ and $\overline{DCS1}$, and two copies of each chip select output, $\overline{QACS0}$, $\overline{QACS1}$, $\overline{QBCS0}$ and $\overline{QBCS1}$. This is the "QuadCS disabled" mode. When the $\overline{QCSEN}$ input pin is pulled low, the component has four chip select inputs $\overline{DCS[3:0]}$, and four chip select outputs, $\overline{QCS[3:0]}$. This is the "QuadCS enabled" mode. Through the remainder of this specification, $\overline{DCS[n:0]}$ will indicate all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. $\overline{QxCS[n:0]}$ will indicate all of the chip select outputs.

The device also supports a mode where a single device can be mounted on the back side of a DIMM. If MIRROR=HIGH, Input Bus Termination (IBT) has to stay enabled for all input signals in this case.

The SN74SSQEA32882 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going HIGH, and $\overline{CK}$ going LOW. This data could be either re-driven to the outputs or it could be used to access device internal control registers.

The input bus data integrity is protected by a parity function. All address and command input signals are added up and the last bit of the sum is compared to the parity signal delivered by the system at the input PAR_IN one clock cycle later. If they do not match the device pulls the open drain output $\overline{ERROUT}$ LOW. The control signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{DCS[n:0]}$) are not part of this computation.

The SN74SSQEA32882 implements different power saving mechanisms to reduce thermal power dissipation and to support system power down states. By disabling unused outputs the power consumption is further reduced.

The package is optimized to support high density DIMMs. By aligning input and output positions towards DIMM finger signal ordering and SDRAM ballout the device de-scrambles the DIMM traces allowing low cross talk design with low interconnect latency.

Edge controlled outputs reduce ringing and improve signal eye opening at the SDRAM inputs.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION

$T_{CASE(max)}$	PACKAGE(1)		ORDERABLE (2) PART NUMBER	TOP-SIDE MARKING
See Table 4	176ZAL	Tape and Reel	SN74SSQEA32882ZALR	EA32882B

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

APPLICATION INFORMATION

Vendor Specific SPD Content

SPD EEPROM on DDR3 RDIMMs has 3 vendor specific bytes for vendor and revision ID. This information can be sued by the system BIOS. The following table showsthe correct values for SN74SSQEA32882.

Table 2. Vendor specific SPD content for SN74SSQEA32882

Byte	Value	Description
65	0x80	Vendor ID, part 1
66	0x97	Vendor ID, part 2
67	0x28	Revision ID

Application Reports

For additional Information on SN74SSQEA32882 DDR3 Register please review the following application reports:

- DDR3 Register CMR programming
- DDR3 RDIMM SPD settings
- Yn phase shift on SN74SSQEA32882
- DDR3 Register IBT Measurement

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings Over Operating Free-Air Temperature Range(1)

PARAMETER			VALUE	UNIT
V_{DD}	Supply voltage		–0.4 to +1.975	V
V_I	Receiver input voltage	See (2) and (3)	–0.4 to V_{DD} + 0.5	V
V_{REF}	Reference voltage		–0.4 to V_{DD} + 0.5	V
V_O	Driver output voltage	See (2) and (3)	–0.4 to V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		±100	mA
T_{stg}	Storage temperature		–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 1.975 V maximum.

Table 4. Case Temperature vs Speed Node

PARAMETER		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	UNIT
$T_{case(max)}$	Maximum case temperature (1)	+109	+108	+106	+103	°C

(1) The temperature values fit to JEDEC RAW cards A, B, and C. The user must keep T_{case} below the specified values in order to keep the junction temperature below +125°C. Other combinations of features and termination resistors can require lower case temperature and extra cooling. These combinations depend on the specific application.

PACKAGE INFORMATION

Pinout Configuration

The package is a 8mm × 13.5mm 176-pin BGA with 0.65mm ball pitch in a 11 × 20 grid. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.

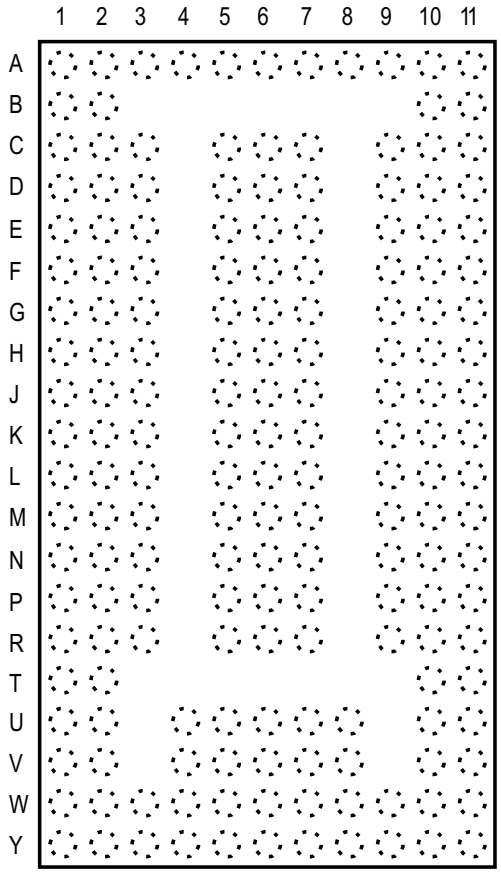


Figure 1. Pinout Configuration

Top View for 176-ball TFBGA (front configuration)

Table 5. Ball Assignment; MIRROR=LOW, QCSEN=HIGH or Floating

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QACS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	$\overline{\text{QBRAS}}$
R	DCKE1	DA14	DA15		DA5	RSVD	DA2		DA1	DA10	DODT1
T	DCKE0	$\overline{\text{DCS0}}$								$\overline{\text{DCS1}}$	DODT0
U	DA12	DBA2		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DA13	$\overline{\text{DCAS}}$
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		$\overline{\text{DRAS}}$	$\overline{\text{DWE}}$
W	DA8	DA6	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA0	DBA0
Y	DA7	RSVD	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9, R6, W7 and Y2 are reserved for future functions must not be connected on system, the system must provide a solder pad for these pins. The device design tolerates floating on these pins. A3 may be left floating since it has an internal pull-up resistor.
Blank space indicate no ball is populated at that gridpoint – vias on the module may be located in these areas

Top View for 176-ball TFBGA (back configuration)

MIRROR=HIGH and QCSEN=HIGH or floating specifies the pinout for SN74SSQEA32882 in back configuration. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

Table 6. Ball Assignment; MIRROR=HIGH, QCSEN=HIGH or Floating

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QACS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	$\overline{\text{QBRAS}}$
R	DODT1	DA10	DA1		DA2	RSVD	DA5		DA15	DA14	DCKE1
T	DODT0	$\overline{\text{DCS1}}$								$\overline{\text{DCS0}}$	DCKE0
U	$\overline{\text{DCAS}}$	DA13		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DBA2	DA12
V	$\overline{\text{DWE}}$	$\overline{\text{DRAS}}$		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	RSVD	DA7

Pins A9, R6, W7 and Y10 are reserved for future functions must not be connected on system, the system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.
Blank space indicate no ball is populated at that gridpoint – vias on the module may be located in these areas

Top View for 176-ball TFBGA (front configuration) in Quad Rank Mode

Table 7. Ball Assignment; MIRROR=LOW, QCSEN=LOW

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QCS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	$\overline{\text{QBRAS}}$
R	DCKE1	DA14	DA15		DA5	$\overline{\text{DCS3}}$	DA2		DA1	DA10	DODT1
T	DCKE0	$\overline{\text{DCS0}}$								$\overline{\text{DCS1}}$	DODT0
U	DA12	DBA2		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DA13	$\overline{\text{DCAS}}$
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		$\overline{\text{DRAS}}$	$\overline{\text{DWE}}$
W	DA8	DA6	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA0	DBA0
Y	DA7	$\overline{\text{DCS2}}$	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9 and W7 are reserved for future functions must not be connected on system, the system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Blank space indicate no ball is populated at that gridpoint – vias on the module may be located in these areas

Top view for 176-ball TFBGA (back configuration) in Quad Rank Mode

Table 8. Ball Assignment; MIRROR=HIGH, QCSEN=LOW

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	QCS0#	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	$\overline{\text{QBRAS}}$
R	DODT1	DA10	DA1		DA2	$\overline{\text{DCS3}}$	DA5		DA15	DA14	DCKE1
T	DODT0	$\overline{\text{DCS1}}$								$\overline{\text{DCS0}}$	DCKE0
U	$\overline{\text{DCAS}}$	DA13		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DBA2	DA12
V	$\overline{\text{DWE}}$	$\overline{\text{DRAS}}$		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	$\overline{\text{DCS2}}$	DA7

Pins A9 and W7 are reserved for future functions must not be connected on system, the system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Blank space indicate no ball is populated at that gridpoint – vias on the module may be located in these areas

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74SSQEA32882ZALR	Active	Production	NFBGA (ZAL) | 176	2000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	EA32882B
SN74SSQEA32882ZALR.A	Active	Production	NFBGA (ZAL) | 176	2000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	EA32882B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

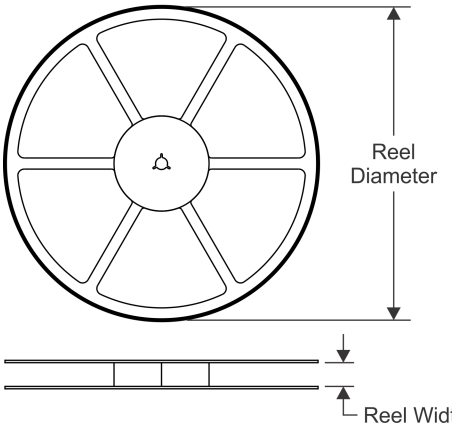
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

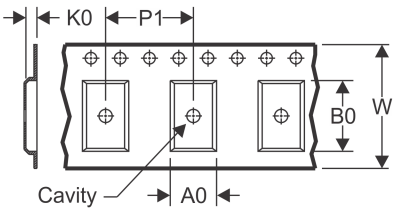
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

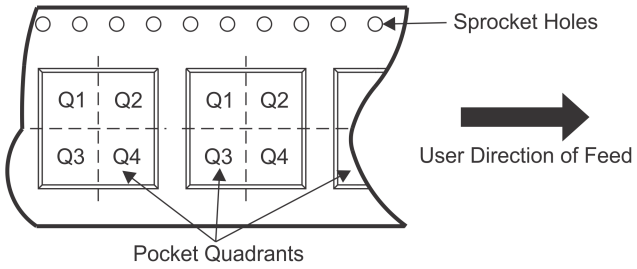


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

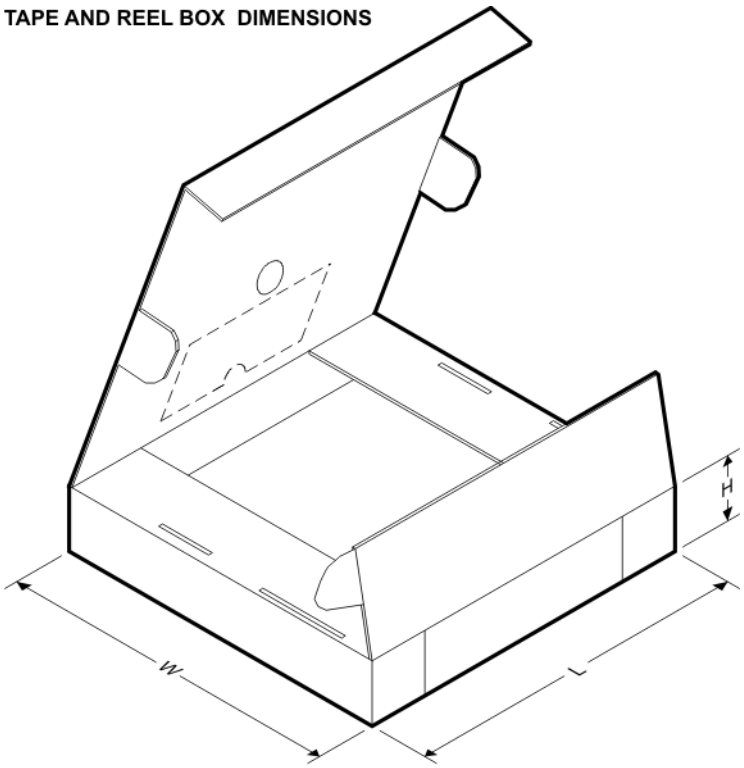
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSQEA32882ZALR	NFBGA	ZAL	176	2000	330.0	24.4	8.3	13.8	1.8	12.0	24.0	Q1

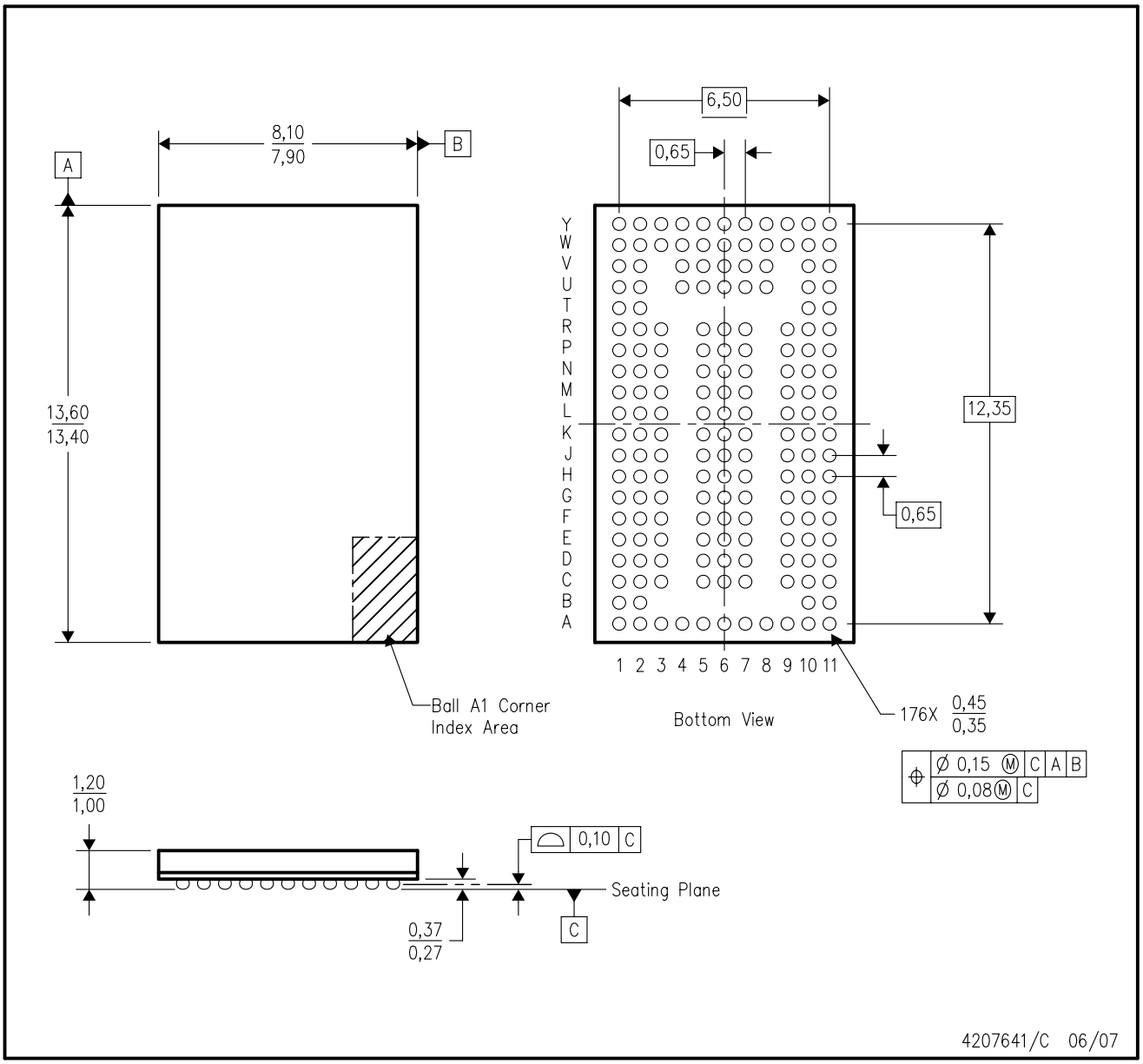
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSQEA32882ZALR	NFBGA	ZAL	176	2000	367.0	367.0	38.0

ZAL (R–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is lead–free.

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