SN74LXCH8T245 8-bit Translating Transceiver with Configurable Level Shifting

1 Features

- Fully Configurable Dual-Rail Design Allows Each Port to Operate from 1.1 V to 5.5 V
- Robust, Glitch-Free Power Supply Sequencing
- Up to 420-Mbps Support for 3.3 V to 5.0 V
- Bus Hold on Data Inputs Eliminates the Need for External Pull-Up and Pull-Down Resistors
- Schmitt-Trigger Control Inputs Allow for Slow or Noisy Inputs
- Control Inputs with Integrated Static Pull-Down Resistors Allow for Floating Control Inputs
- High Drive Strength (up to 32 mA at 5 V)
- Low Power Consumption
  - 4-µA Maximum (25°C)
  - 12-µA Maximum (–40°C to 125°C)
- V_{CC} Isolation and V_{CC} Disconnect feature
  - If Either V_{CC} Supply is < 100 mV All I/O's Become High-Impedance
  - $I_{off-float}$ Supports V_{CC} Disconnect Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Compatible with LVC Family Level Shifters
- Control Logic (DIR and $\overline{OE}$) are Referenced to V_{CCA}
- Operating Temperature from –40°C to +125°C
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 4000-V Human-Body Model
  - 1000-V Charged-Device Model

2 Applications

- Eliminate Slow or Noisy Input Signals
- Driving Indicator LEDs or Buzzers
- Debouncing a Mechanical Switch
- General Purpose I/O Level Shifting
- Push-Pull Level Shifting (UART, SPI, JTAG, and so forth.)

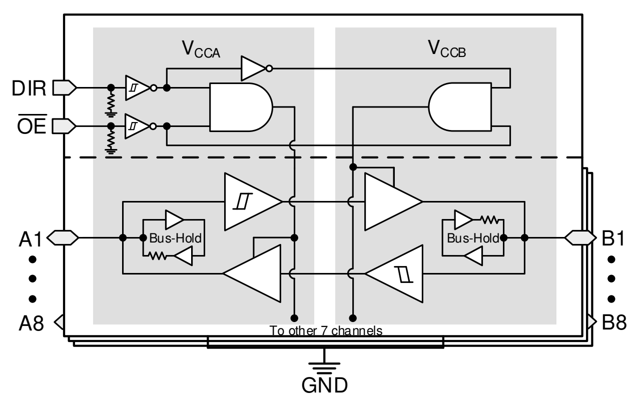
3 Description

The SN74LXCH8T245 is an 8-bit, dual-supply noninverting bidirectional voltage level translation device with bus-hold circuitry. Ax pins and control pins (DIR and $\overline{OE}$) are referenced to V_{CCA} logic levels, and Bx pins are referenced to V_{CCB} logic levels. The A port is able to accept I/O voltages ranging from 1.1 V to 5.5 V, while the B port can accept I/O voltages from 1.1 V to 5.5 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state. See *Device Functional Modes* for a summary of the operation of the control logic.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LXCH8T245PWR	TSSOP (24)	7.80 mm × 6.40 mm
SN74LXCH8T245RHLR	VQFN (24)	5.50 mm × 3.50 mm

(1) See the orderable addendum at the end of the data sheet for all available packages.



Functional Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

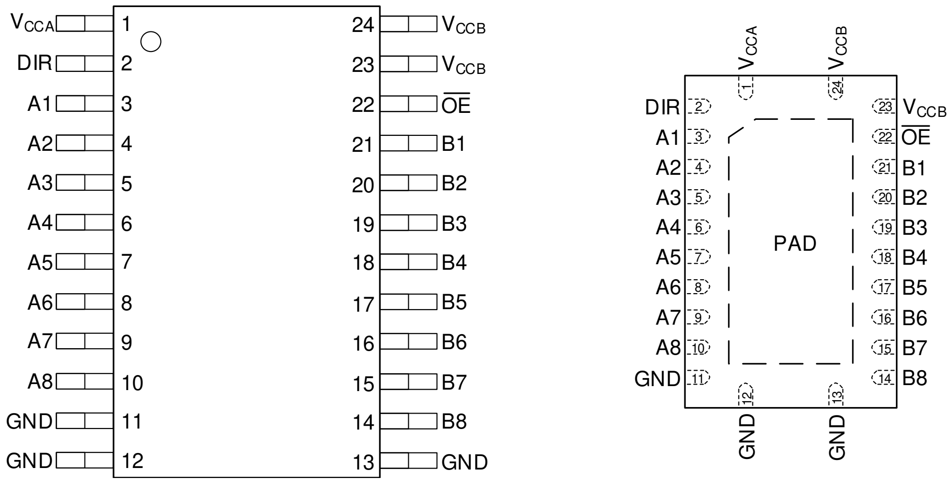
Changes from Revision A (January 2021) to Revision B (March 2021) — **Page**

- Updated t_{pd} values in *Switching Characteristics, V_{CCA} = 1.2 ± 0.1 V* section....9
- Updated t_{pd} values in *Switching Characteristics, V_{CCA} = 1.5 ± 0.1 V* section....10
- Updated t_{pd} values in *Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V* section....11
- Updated t_{pd} values in *Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V* section....12
- Updated t_{pd} values in *Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V* section....13
- Updated t_{pd} values in *Switching Characteristics, V_{CCA} = 5.0 ± 0.5 V* section....14
- Changed the t_{sk} – output skew's maximum operating free-air temperature (T_A) range for V_{CCI} and V_{CCO} in the *Switching Characteristics: T_{sk}, T_{MAX}* section....15

Changes from Revision * (January 2021) to Revision A (January 2021) — **Page**

- Changed I_{OZ} spec at 25C....6

5 Pin Configuration and Functions



All packages are on the same relative scale.

Figure 5-1. PW, and RHL Package 24-Pin TSSOP, and VQFN Transparent Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	PW, RHL		
A1	3	I/O	Input or output A1. Referenced to V_{CCA}.
A2	4	I/O	Input or output A2. Referenced to V_{CCA}.
A3	5	I/O	Input or output A3. Referenced to V_{CCA}.
A4	6	I/O	Input or output A4. Referenced to V_{CCA}.
A5	7	I/O	Input or output A5. Referenced to V_{CCA}.
A6	8	I/O	Input or output A6. Referenced to V_{CCA}.
A7	9	I/O	Input or output A7. Referenced to V_{CCA}.
A8	10	I/O	Input or output A8. Referenced to V_{CCA}.
B1	21	I/O	Input or output B1. Referenced to V_{CCB}.
B2	20	I/O	Input or output B2. Referenced to V_{CCB}.
B3	19	I/O	Input or output B3. Referenced to V_{CCB}.
B4	18	I/O	Input or output B4. Referenced to V_{CCB}.
B5	17	I/O	Input or output B5. Referenced to V_{CCB}.
B6	16	I/O	Input or output B6. Referenced to V_{CCB}.
B7	15	I/O	Input or output B7. Referenced to V_{CCB}.
B8	14	I/O	Input or output B8. Referenced to V_{CCB}.
DIR	2	I	Direction-control signal for all ports. Referenced to V_{CCA}.
GND	11	—	Ground.
	12	—	Ground.
	13	—	Ground.
$\overline{OE}$	22	I	Output Enable. Pull to GND to enable all outputs. Pull to V_{CCA} to place all outputs in high-impedance mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. 1.1 V ≤ V_{CCA} ≤ 5.5 V.
V_{CCB}	23	—	B-port supply voltage. 1.1 V ≤ V_{CCB} ≤ 5.5 V.
	24	—	B-port supply voltage. 1.1 V ≤ V_{CCB} ≤ 5.5 V.
PAD	—	—	Thermal pad. May be grounded (recommended) or left floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	6.5	V
V_{CCB}	Supply voltage B		–0.5	6.5	V
V_I	Input Voltage[(2)]	I/O Ports (A Port)	–0.5	6.5	V
		I/O Ports (B Port)	–0.5	6.5	
		Control Inputs	–0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state[(2)]	A Port	–0.5	6.5	V
		B Port	–0.5	6.5	
V_O	Voltage applied to any output in the high or low state[(2) (3)]	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$	–50		mA
I_{OK}	Output clamp current	$V_O < 0$	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–200	200	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure beyond the limits listed in *Recommended Operating Conditions.* may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			1.1	5.5	V
V_{CCB}	Supply voltage B			1.1	5.5	V
V_{IH}	High-level input voltage	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	V_{CCI} = 1.1 V - 1.3 V	V_{CCI} x 0.8		V
			V_{CCI} = 1.4 V - 1.95 V	V_{CCI} x 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.7		
			V_{CCI} = 3.0 V - 3.6 V	2		
			V_{CCI} = 4.5 V - 5.5 V	V_{CCI} x 0.7		
V_{IL}	Low-level input voltage	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	V_{CCI} = 1.1 V - 1.3 V		V_{CCI} x 0.2	V
			V_{CCI} = 1.4 V - 1.95 V		V_{CCI} x 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3.0 V - 3.6 V		0.8	
			V_{CCI} = 4.5 V - 5.5 V		V_{CCI} x 0.3	
I_{OH}	High-level output current		V_{CCO} = 1.1 V		–0.1	mA
			V_{CCO} = 1.4 V		–2	
			V_{CCO} = 1.65 V		–4	
			V_{CCO} = 2.3 V		–12	
			V_{CCO} = 3 V		–24	
			V_{CCO} = 4.5 V		–32	
I_{OL}	Low-level output current		V_{CCO} = 1.1 V		0.1	mA
			V_{CCO} = 1.4 V		2	
			V_{CCO} = 1.65 V		4	
			V_{CCO} = 2.3 V		12	
			V_{CCO} = 3 V		24	
			V_{CCO} = 4.5 V		32	
V_I	Input voltage			0	5.5	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	5.5	
Δt/Δv	Input transition rise and fall time				20	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port. V_{CCO} is the V_{CC} associated with the output port.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LXC8T245		UNIT
		PW (TSSOP)	RHL (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.2	45.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	41.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.3	23.3	°C/W
Y_{JT}	Junction-to-top characterization parameter	5.8	2.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	52.9	23.3	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	13.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics app report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) 25°C			–40°C to 85°C			–40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going input-threshold voltage	Control Inputs ($\overline{OE}$, DIR) (Referenced to V_{CCA})	1.1 V	1.1 V				0.44		0.88	0.44		0.88	V
			1.4 V	1.4 V				0.60		0.98	0.60		0.98	
			1.65 V	1.65 V				0.76		1.13	0.76		1.13	
			2.3 V	2.3 V				1.08		1.56	1.08		1.56	
			3 V	3 V				1.48		1.92	1.48		1.92	
			4.5 V	4.5 V				2.19		2.74	2.19		2.74	
			5.5 V	5.5 V				2.65		3.33	2.65		3.33	
V_{T-}	Negative-going input-threshold voltage	Control Inputs ($\overline{OE}$, DIR) (Referenced to V_{CCA})	1.1 V	1.1 V				0.17		0.48	0.17		0.48	V
			1.4 V	1.4 V				0.28		0.6	0.28		0.6	
			1.65 V	1.65 V				0.35		0.71	0.35		0.71	
			2.3 V	2.3 V				0.56		1	0.56		1	
			3 V	3 V				0.89		1.5	0.89		1.5	
			4.5 V	4.5 V				1.51		2	1.51		2	
			5.5 V	5.5 V				1.88		2.46	1.88		2.46	
ΔV_T	Input-threshold hysteresis ($V_{T+} – V_{T-}$)	Control Inputs ($\overline{OE}$, DIR) (Referenced to V_{CCA})	1.1 V	1.1 V				0.2		0.4	0.2		0.4	V
			1.4 V	1.4 V				0.25		0.5	0.25		0.5	
			1.65 V	1.65 V				0.3		0.55	0.3		0.55	
			2.3 V	2.3 V				0.38		0.65	0.38		0.65	
			3 V	3 V				0.46		0.72	0.46		0.72	
			4.5 V	4.5 V				0.58		0.93	0.58		0.93	
			5.5 V	5.5 V				0.69		1.06	0.69		1.06	
V_{OH}	High-level output voltage [(3)]	I_{OH} = –100 µA	1.1V – 5.5V	1.1V – 5.5V				V_{CCO} – 0.1			V_{CCO} – 0.1			V
		I_{OH} = –4 mA	1.4 V	1.4 V				1			1			
		I_{OH} = –8 mA	1.65 V	1.65 V				1.2			1.2			
		I_{OH} = –12 mA	2.3 V	2.3 V				1.9			1.9			
		I_{OH} = –24 mA	3 V	3 V				2.4			2.4			
		I_{OH} = –32 mA	4.5 V	4.5 V				3.8			3.8			
V_{OL}	Low-level output voltage [(4)]	I_{OL} = 100 µA	1.1V – 5.5V	1.1V – 5.5V						0.1			0.1	V
		I_{OL} = 4 mA	1.4 V	1.4 V						0.3			0.3	
		I_{OL} = 8 mA	1.65 V	1.65 V						0.45			0.45	
		I_{OL} = 12 mA	2.3 V	2.3 V						0.3			0.3	
		I_{OL} = 24 mA	3 V	3 V						0.55			0.55	
		I_{OL} = 32 mA	4.5 V	4.5 V						0.55			0.55	
I_{BHL}	Bus-hold low sustaining current Port A or Port B [(6)]	V_I = 0.39	1.1 V	1.1 V				4			4			µA
		V_I = 0.49	1.4 V	1.4 V				15			10			
		V_I = 0.58	1.65 V	1.65 V				25			20			
		V_I = 0.70	2.3 V	2.3 V				45			45			
		V_I = 0.80	3 V	3 V				75			75			
		V_I = 1.35	4.5 V	4.5 V				100			100			

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)[1] [2]

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{BHH}	Bus-hold high sustaining current Port A or Port B [7]	V_I = 0.71 V	1.1 V	1.1 V				–4			–4			µA
		V_I = 0.91 V	1.4 V	1.4 V				–15			–10			
		V_I = 1.07 V	1.65 V	1.65 V				–25			–20			
		V_I = 1.70 V	2.3 V	2.3 V				–45			–45			
		V_I = 2.00 V	3 V	3 V				–75			–75			
		V_I = 3.15 V	4.5 V	4.5 V				–100			–100			
I_{BHLO}	Bus-hold low overdrive current [8]	Ramp input up V_I = 0 to V_{CCI}	1.3 V	1.3 V				75			75			µA
			1.6 V	1.6 V				125			125			
			1.95 V	1.95 V				200			200			
			2.7 V	2.7 V				300			300			
			3.6 V	3.6 V				500			500			
			5.5 V	5.5 V				900			900			
I_{BHHO}	Bus-hold high overdrive current [9]	Ramp input down V_I = V_{CCI} to 0	1.3 V	1.3 V				–75			–75			µA
			1.6 V	1.6 V				–125			–125			
			1.95 V	1.95 V				–200			–200			
			2.7 V	2.7 V				–300			–300			
			3.6 V	3.6 V				–500			–500			
			5.5 V	5.5 V				–900			–900			
I_I	Input leakage current	Control inputs (DIR, $\overline{OE}$) V_I = V_{CCA} or GND	1.1V – 5.5V	1.1V – 5.5V	–0.1		1.5	–0.1		2	–0.1		2	µA
		Data Inputs (Ax, Bx) V_I = V_{CCI} or GND	1.1V – 5.5V	1.1V – 5.5V	–0.3		0.3	–1		1	–2		2	µA
I_{off}	Partial power down current	A Port V_I or V_O = 0 V - 5.5 V	0 V	0 V – 5.5 V	–1.5		1.5	–2		2	–2.5		2.5	µA
		B Port V_I or V_O = 0 V - 5.5 V	0 V – 5.5 V	0 V	–1.5		1.5	–2		2	–2.5		2.5	
$I_{off-float}$	Floating supply Partial power down current	A Port V_I or V_O = GND	Floating	0 V – 5.5 V	–1.5		1.5	–2		2	–2.5		2.5	µA
		B Port V_I or V_O = GND	0 V - 5.5 V	Floating	–1.5		1.5	–2		2	–2.5		2.5	
I_{OZ}	Tri-state output current [5]	A or B Port: (Rev) V_I = V_{CCI} or GND V_O = V_{CCO} or GND $\overline{OE}$ = $V_{T+(MAX)}$	1.1V – 5.5V	1.1V – 5.5V	–1		1	–1		1	–2		2	µA
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND I_O = 0	1.1V – 5.5V	1.1V – 5.5V			2			4			8	µA
			0 V	5.5 V	–0.2			–0.5			–1			
			5.5 V	0 V			2			4			8	
			5.5 V	Floating			2			4			8	
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND I_O = 0	1.1V – 5.5V	1.1V – 5.5V			2			4			8	µA
			0 V	5.5 V			2			4			8	
			5.5 V	0 V	–0.2			–0.5			–1			
			Floating	5.5 V			2			4			8	

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) 25°C MIN	25°C TYP	25°C MAX	–40°C to 85°C MIN	–40°C to 85°C TYP	–40°C to 85°C MAX	–40°C to 125°C MIN	–40°C to 125°C TYP	–40°C to 125°C MAX	UNIT
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND I_O = 0	1.1V – 5.5V	1.1V – 5.5V			4			8			12	µA
ΔI_{CCA}	V_{CCA} additional supply current per input	Control inputs (DIR, $\overline{OE}$): V_I = V_{CCA} – 0.6 V A port = VCCA or GND B Port = open	3.0 V – 5.5V	3.0 V – 5.5V						50			75	µA
C_i	Control Input Capacitance	V_I = 3.3 V or GND	3.3 V	3.3 V		2.9				5			5	pF
C_{io}	Data I/O Capacitance	$\overline{OE}$ = V_{CCA}, V_O = 1.65V DC +1 MHz -16 dBm sine wave	3.3 V	3.3 V		5.9				10			10	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) Tested at V_I = $V_{T+(MAX)}$.
(4) Tested at V_I = $V_{T-(MIN)}$.
(5) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(6) I_{BHL} should be measured after lowering V_I to GND and then raising it to the defined input voltage.
(7) I_{BHH} should be measured after raising V_I to V_{CCI} and then lowering it to the defined input voltage.
(8) An external driver must source at least I_{BHLO} to switch this node from low-to-high.
(9) An external driver must sink at least I_{BHHO} to switch this node from high to low.

6.6 Switching Characteristics, V_{CCA} = 1.2 ± 0.1 V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1 V			1.5 ± 0.1 V			1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	10		65	10		31	7		25	7		24	5		22	5		21	ns
				-40°C to 125°C	10		70	10		33	7		27	7		26	5		24	5		23	
		B	A	-40°C to 85°C	10		62	10		55	10		49	8		42	8		40	8		39	
				-40°C to 125°C	10		68	10		60	10		54	8		47	8		45	8		44	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	20		64	20		64	20		64	20		64	20		64	20		64	ns
				-40°C to 125°C	20		69	20		69	20		69	20		69	20		69	20		69	
		$\overline{OE}$	B	-40°C to 85°C	20		80	20		62	20		54	20		48	20		47	20		45	
				-40°C to 125°C	20		85	20		67	20		59	20		52	20		50	20		48	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	20		90	20		91	20		91	20		91	20		90	20		90	ns
				-40°C to 125°C	20		97	20		98	20		97	20		96	20		96	20		96	
		$\overline{OE}$	B	-40°C to 85°C	20		95	20		57	15		48	10		38	10		36	10		36	
				-40°C to 125°C	20		100	20		61	15		53	10		42	10		39	10		39	

6.7 Switching Characteristics, V_{CCA} = 1.5 ± 0.1 V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1 V			1.5 ± 0.1 V			1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	10		52	5		25	5		23	5		17	5		14	3		13	ns
				-40°C to 125°C	10		57	5		26	5		23	5		18	5		16	3		14	
		B	A	-40°C to 85°C	8		36	7		28	7		26	5		20	5		18	5		17	
				-40°C to 125°C	8		40	7		29	7		26	5		22	5		20	5		18	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	15		40	15		40	15		40	15		40	15		40	15		40	ns
				-40°C to 125°C	15		44	15		44	15		44	15		44	15		44	15		44	
		$\overline{OE}$	B	-40°C to 85°C	20		69	20		50	15		45	15		35	15		34	14		31	
				-40°C to 125°C	20		74	20		54	15		48	15		39	15		37	14		33	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	15		48	15		48	15		48	15		48	15		48	15		48	ns
				-40°C to 125°C	15		52	15		52	15		52	15		52	15		52	15		52	
		$\overline{OE}$	B	-40°C to 85°C	20		85	15		50	15		40	10		31	10		26	10		24	
				-40°C to 125°C	20		91	15		54	15		44	10		33	10		29	10		26	

6.8 Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB}) 1.2 ± 0.1 V MIN	1.2 ± 0.1 V TYP	1.2 ± 0.1 V MAX	1.5 ± 0.1 V MIN	1.5 ± 0.1 V TYP	1.5 ± 0.1 V MAX	1.8 ± 0.15 V MIN	1.8 ± 0.15 V TYP	1.8 ± 0.15 V MAX	2.5 ± 0.2 V MIN	2.5 ± 0.2 V TYP	2.5 ± 0.2 V MAX	3.3 ± 0.3 V MIN	3.3 ± 0.3 V TYP	3.3 ± 0.3 V MAX	5.0 ± 0.5 V MIN	5.0 ± 0.5 V TYP	5.0 ± 0.5 V MAX	UNIT
t_{pd}	Propagation delay	A	B	-40°C to 85°C	8		50	6		21	6		18	4		14	4		11	2		10	ns
				-40°C to 125°C	8		53	6		23	6		20	4		15	4		12	2		11	
		B	A	-40°C to 85°C	5		32	5		21	5		19	4		17	4		15	4		15	
				-40°C to 125°C	5		33	5		23	5		21	4		18	4		16	4		16	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	10		34	10		33	10		33	10		33	10		33	10		33	ns
				-40°C to 125°C	10		36	10		35	10		35	10		35	10		35	10		35	
		$\overline{OE}$	B	-40°C to 85°C	20		64	15		45	15		40	12		31	12		31	10		26	
				-40°C to 125°C	20		69	15		49	15		44	12		33	12		38	10		28	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	10		38	10		38	10		38	10		38	10		38	10		38	ns
				-40°C to 125°C	10		40	10		40	10		40	10		40	10		40	10		40	
		$\overline{OE}$	B	-40°C to 85°C	20		84	15		47	10		38	10		29	10		25	8		23	
				-40°C to 125°C	20		89	15		51	10		42	10		30	10		26	8		25	

6.9 Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1 V			1.5 ± 0.1 V			1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	7		40	5		21	4		16	3		12	3		10	3		8	ns
				-40°C to 125°C	7		45	5		22	4		17	3		13	3		11	3		9	
		B	A	-40°C to 85°C	5		26	5		16	5		15	4		12	3		11	3		10	
				-40°C to 125°C	5		28	5		17	5		15	4		13	3		12	3		11	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	10		24	10		24	10		24	10		24	10		22	10		24	ns
				-40°C to 125°C	10		26	10		26	10		24	10		24	10		24	10		24	
		$\overline{OE}$	B	-40°C to 85°C	15		56	15		41	12		34	12		25	10		24	10		21	
				-40°C to 125°C	15		62	15		44	12		37	12		29	10		26	10		22	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	8		25	8		25	8		25	8		25	8		25	8		25	ns
				-40°C to 125°C	8		27	8		27	8		27	8		27	8		27	8		27	
		$\overline{OE}$	B	-40°C to 85°C	20		80	15		46	10		34	10		25	5		23	5		18	
				-40°C to 125°C	20		86	15		48	10		37	10		27	5		25	5		20	

6.10 Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1 V			1.5 ± 0.1 V			1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	8		41	6		19	4		15	3		10	3		9	2		6.5	ns
				-40°C to 125°C	8		43	6		21	4		16	3		11	3		10	2		7.5	
		B	A	-40°C to 85°C	5		22	5		15	4		12	3		10	3		9	3		8.5	
				-40°C to 125°C	5		24	5		16	4		13	3		11	3		10	3		9	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	9		19	9		19	9		19	8		19	8		19	8		19	ns
				-40°C to 125°C	9		20	9		20	9		20	8		20	8		20	8		20	
		$\overline{OE}$	B	-40°C to 85°C	15		52	15		38	12		32	10		23	10		22	9		18	
				-40°C to 125°C	15		59	15		41	12		35	10		26	10		23	9		20	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	5		20	5		20	5		20	5		20	5		20	5		20	ns
				-40°C to 125°C	5		22	5		22	5		22	5		22	5		22	5		22	
		$\overline{OE}$	B	-40°C to 85°C	20		80	15		43	10		34	5		24	5		19	5		16	
				-40°C to 125°C	20		85	15		46	10		36	5		27	5		21	5		18	

6.11 Switching Characteristics, V_{CCA} = 5.0 ± 0.5 V

See Figure 7-1 and Table 7-1 for test circuit and loading. See Figure 7-2, Figure 7-3, and Figure 7-4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																		UNIT
					1.2 ± 0.1 V			1.5 ± 0.1 V			1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	8		38	6		15	3		14	3		9.5	2		8	2		6	ns
				-40°C to 125°C	8		42	6		17	3		15	3		10.5	2		8.5	2		7	
		B	A	-40°C to 85°C	5		22	4		13	3		10.5	3		8	2		7.5	2		7	
				-40°C to 125°C	5		24	4		15	3		11.5	3		8.5	2		8	2		7.5	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	7		15	5		15	5		15	5		15	5		14	5		14	ns
				-40°C to 125°C	7		16	5		16	5		16	5		16	5		15	5		15	
		$\overline{OE}$	B	-40°C to 85°C	15		52	12		33	10		31	10		22	10		21	5		16	
				-40°C to 125°C	15		56	12		37	10		35	10		24	10		23	5		18	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	5		15	5		15	5		15	5		15	5		15	5		15	ns
				-40°C to 125°C	5		16	5		16	5		16	5		16	5		16	5		16	
		$\overline{OE}$	B	-40°C to 85°C	20		80	15		44	10		33	5		24	5		18	5		15	
				-40°C to 125°C	20		85	15		48	10		35	5		26	5		20	5		17	

6.12 Switching Characteristics: T_{sk}, T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCI}	V_{CCO}	Operating free-air temperature (T_A) -40°C to 125°C MIN	TYP	MAX	UNIT
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	Up Translation	3.0 V – 3.6 V	4.5 V – 5.5 V	200	420		Mbps
			1.65 V – 1.95 V	4.5 V – 5.5 V	100	200		Mbps
			1.1 V – 1.3 V	4.5 V – 5.5 V	20	40		Mbps
			1.65 V – 1.95 V	3.0 V – 3.6 V	100	210		Mbps
			1.1 V – 1.3 V	3.0 V – 3.6 V	10	20		Mbps
			1.1 V – 1.3 V	1.65 V – 1.95 V	5	10		Mbps
		Down Translation	4.5 V – 5.5 V	3.0 V – 3.6 V	100	210		Mbps
			4.5 V – 5.5 V	1.65 V – 1.95 V	50	75		Mbps
			4.5 V – 5.5 V	1.1 V – 1.3 V	15	30		Mbps
			3.0 V – 3.6 V	1.65 V – 1.95 V	40	75		Mbps
			3.0 V – 3.6 V	1.1 V – 1.3 V	10	20		Mbps
			1.65 V – 1.95 V	1.1 V – 1.3 V	5	10		Mbps
t_{sk} – Output skew	Timing skew between any two switching outputs within the same device	Up Translation	3.0 V – 3.6 V	4.5 V – 5.5 V			0.5	ns
			1.65 V – 1.95 V	4.5 V – 5.5 V			1	
			1.1 V – 1.3 V	4.5 V – 5.5 V			1.5	
			1.65 V – 1.95 V	3.0 V – 3.6 V			1	
			1.1 V – 1.3 V	3.0 V – 3.6 V			1.5	
			1.1 V – 1.3 V	1.65 V – 1.95 V			2	
		Down Translation	4.5 V – 5.5 V	3.0 V – 3.6 V			0.5	
			4.5 V – 5.5 V	1.65 V – 1.95 V			1	
			4.5 V – 5.5 V	1.1 V – 1.3 V			1.5	
			3.0 V – 3.6 V	1.65 V – 1.95 V			1	
			3.0 V – 3.6 V	1.1 V – 1.3 V			1.5	
			1.65 V – 1.95 V	1.1 V – 1.3 V			2	

6.13 Operating Characteristics

T_A = 25°C (1)

PARAMETER		Test Conditions	Supply Voltage (V_{CCB} = V_{CCA}) 1.2 ± 0.1V TYP	1.5 ± 0.1V TYP	1.8 ± 0.15V TYP	2.5 ± 0.2V TYP	3.3 ± 0.3V TYP	5.0 ± 0.5V TYP	UNIT
C_{pdA} (2)	A to B: outputs enabled	A Port CL = 0, RL = Open f = 10 MHz t_{rise} = t_{fall} = 1 ns	1	4	4	4	5	5	pF
	A to B: outputs disabled		3	3	3	4	4	4	
	B to A: outputs enabled		22	22	22	23	24	25	
	B to A: outputs disabled		1	1	1	1	1	2	
C_{pdB} (2)	A to B: outputs enabled	B Port CL = 0, RL = Open f = 10 MHz t_{rise} = t_{fall} = 1 ns	22	22	22	23	24	25	pF
	A to B: outputs disabled		1	1	1	1	1	2	
	B to A: outputs enabled		1	1	1	1	1	5	
	B to A: outputs disabled		3	3	3	1	1	1	

(1) See the CMOS Power Consumption and C_{pd} Calculation application report for more information about power dissipation capacitance.
(2) C_{pdA} and C_{pdB} are respectively A-Port and B-Port power dissipation capacitances per transceiver.

6.14 Typical Characteristics

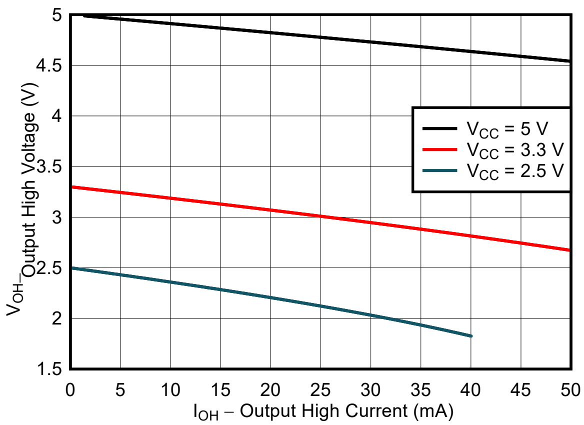


Figure 6-1. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

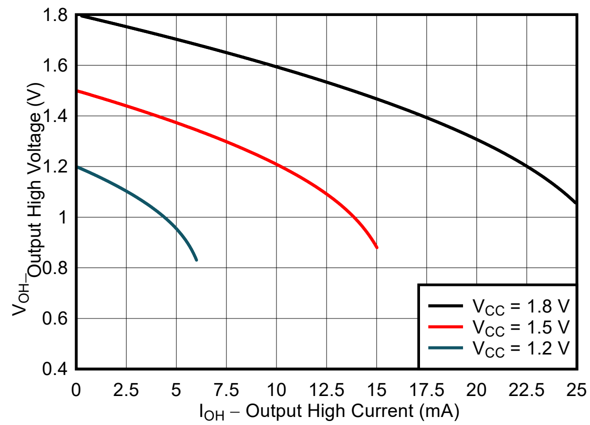


Figure 6-2. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

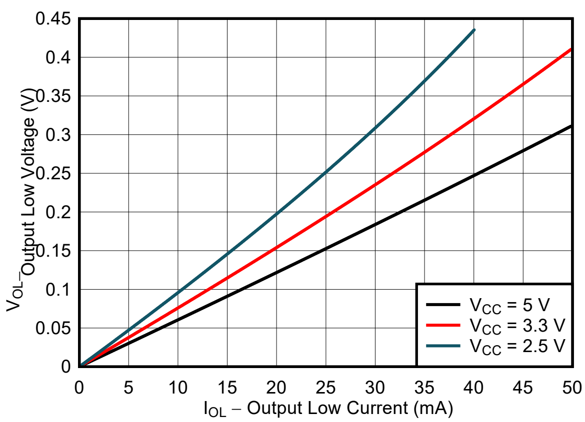


Figure 6-3. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

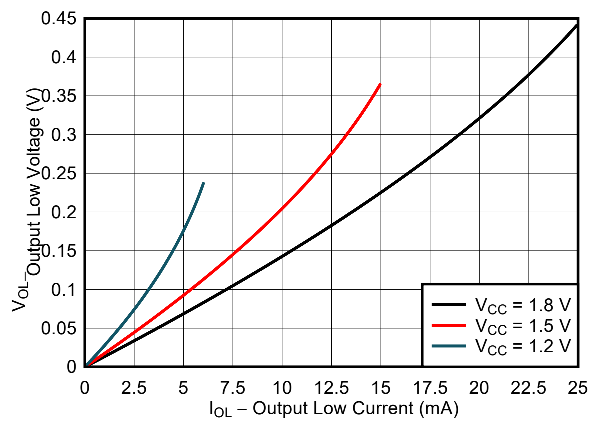


Figure 6-4. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

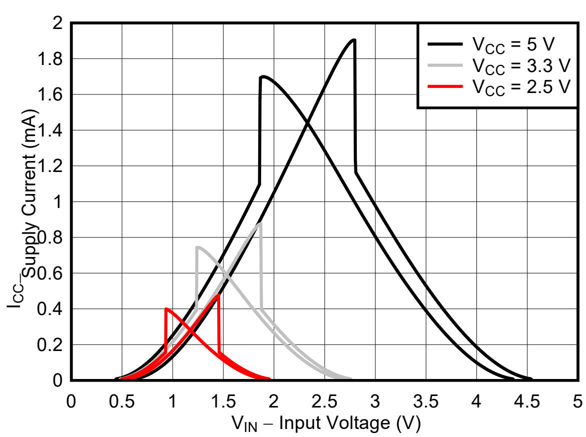


Figure 6-5. Typical (T_A=25°C) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

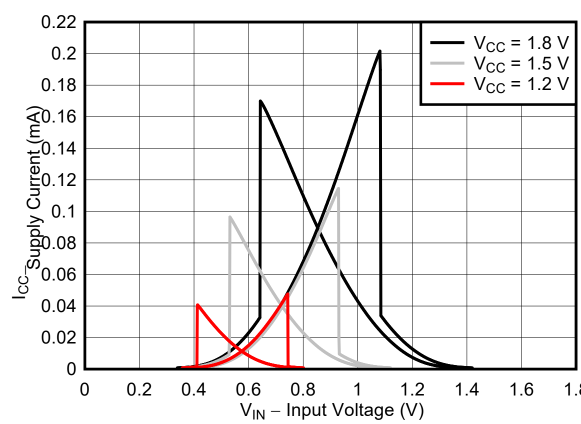


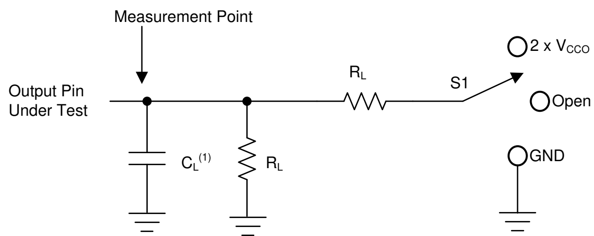
Figure 6-6. Typical (T_A=25°C) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- Δt/ΔV ≤ 1 ns/V

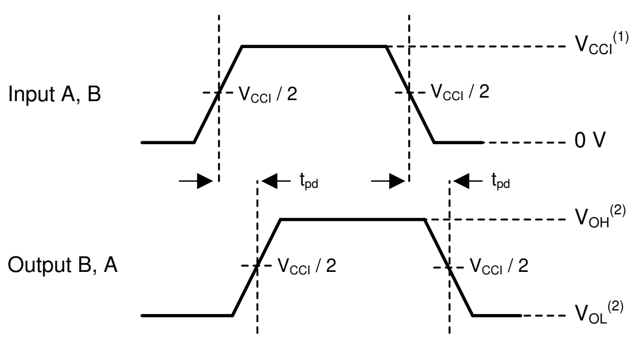


A. C_L includes probe and jig capacitance.

Figure 7-1. Load Circuit

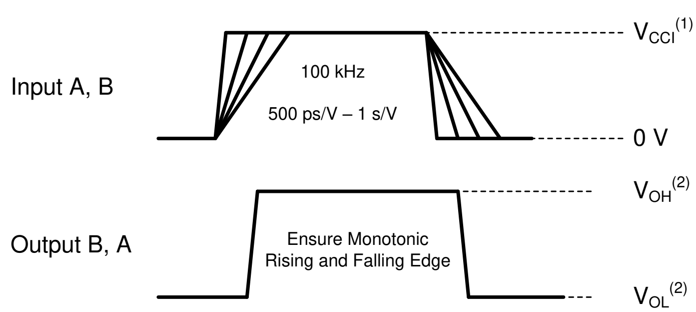
Table 7-1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
t_{pd}	Propagation (delay) time	1.1 V – 5.5 V	2 kΩ	15 pF	Open	N/A
t_{en}, t_{dis}	Enable time or disable time	1.1 V – 1.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.1 V
		1.65 V – 2.7 V	2 kΩ	15 pF	2 × V_{CCO}	0.15 V
		3.0 V – 5.5 V	2 kΩ	15 pF	2 × V_{CCO}	0.3 V
t_{en}, t_{dis}	Enable time or disable time	1.1 V – 1.6 V	2 kΩ	15 pF	GND	0.1 V
		1.65 V – 2.7 V	2 kΩ	15 pF	GND	0.15 V
		3.0 V – 5.5 V	2 kΩ	15 pF	GND	0.3 V



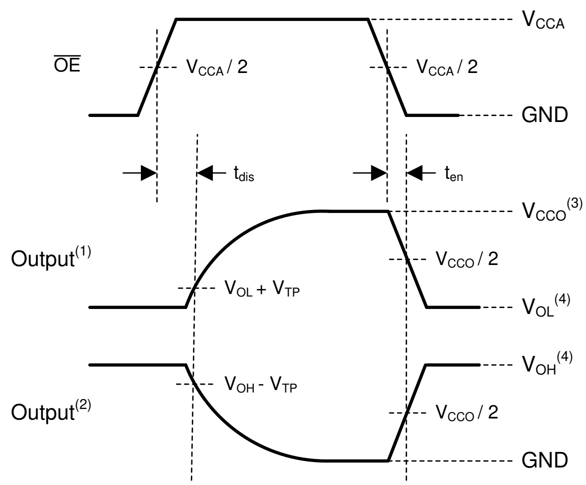
1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1.

Figure 7-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1.

Figure 7-3. Input Transition Rise and Fall Rate



1. Output waveform on the condition that input is driven to a valid Logic Low.
2. Output waveform on the condition that input is driven to a valid Logic High.
3. V_{CCO} is the supply pin associated with the output port.
4. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

Figure 7-4. Enable Time And Disable Time

8 Detailed Description

8.1 Overview

The SN74LXCH8T245 is an 8-bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with V_{CCA} and V_{CCB} supplies as low as 1.1 V and as high as 5.5 V. Additionally, the device operates with V_{CCA} = V_{CCB}. The A port is designed to track V_{CCA}, and the B port is designed to track V_{CCB}.

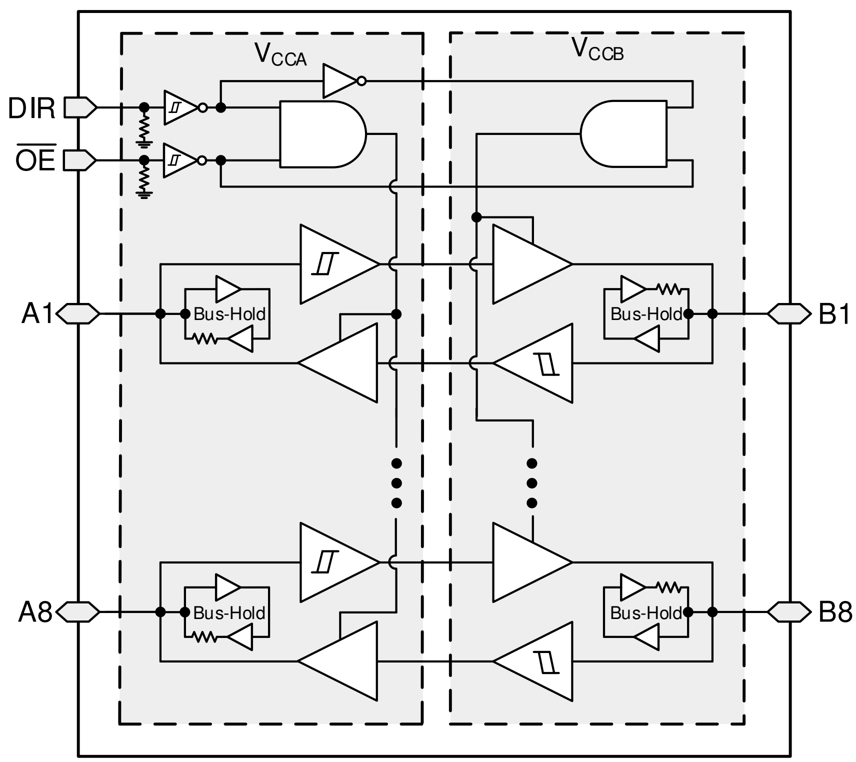
The SN74LXCH8T245 device is designed for asynchronous communication between data buses and transmits data from the A bus to the B bus or from the B bus to the A bus based on the logic level of the direction-control input (DIR). The output-enable input ($\overline{OE}$) is used to disable the outputs so the buses are effectively isolated. The control pins of the SN74LXCH8T245 (DIR and $\overline{OE}$) are referenced to V_{CCA}. The $\overline{OE}$ pin should be tied to V_{CCA} through a pullup resistor to ensure the high-impedance state of the level shifter I/Os during power up or power down.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or sourced into an input, output, or I/O while the device is powered down.

The V_{CC} isolation and V_{CC} disconnect feature ensures that if either V_{CC} is less than 100 mV or floating with the complementary supply within the recommended operating conditions, both I/O ports are set to the high-impedance state by disabling their outputs and the supply current is maintained.

Glitch-free power supply sequencing allows either supply rail to power on or off in any order while providing robust power sequencing performance.

8.2 Functional Block Diagram



Note: Bus-hold circuits are only present for data inputs, not control inputs

Figure 8-1. SN74LXCH8T245 Functional Block Diagram

8.3 Feature Description

8.3.1 CMOS Schmitt-Trigger Inputs with Integrated Pulldowns

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the Electrical Characteristics. The worst case resistance is calculated with the maximum input voltage, given in the Absolute Maximum Ratings, and the maximum input leakage current, given in the Electrical Characteristics, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the Electrical Characteristics, which makes this device extremely tolerant to slow or noisy inputs. Driving the inputs slowly will increase dynamic current consumption of the device. See Understanding Schmitt Triggers for additional information regarding Schmitt-trigger inputs.

8.3.1.1 Control Inputs with Integrated Static Pull-Down Resistors

Similar to the data I/O's, floating control inputs can cause high current consumption. This device has integrated weak static pull-downs of 5-MΩ typical on the control inputs (DIR and $\overline{OE}$) to help avoid this concern. These pull-downs are always present. For example, if the DIR pin is left floating, then the B port will be configured as an input and the A port will be configured as an output.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the Absolute Maximum Ratings must be followed at all times.

8.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. I_{off} in the Electrical Characteristics specifies the maximum leakage into or out of any input or output pin on the device.

8.3.4 V_{CC} Isolation and V_{CC} Disconnect

The inputs and outputs for this device enter a high-impedance state when either supply is <100 mV, requiring one supply to connect to the device. Note: the bus-hold circuitry always remains active even when the device is disabled and all outputs are in the high-impedance state.

Either supply can be disconnected (floated), while the other supply is still connected and the device will maitain the maximum supply current specified by $I_{CCx(floating)}$, in the Electrical Characteristics. The I/O's will not enter a high-impedance state unless the supply is disconnected after it is driven to <100 mV. $I_{off(float)}$ in the Electrical Characteristics specifies the maximum leakage into or out of any input or output pin on the device.

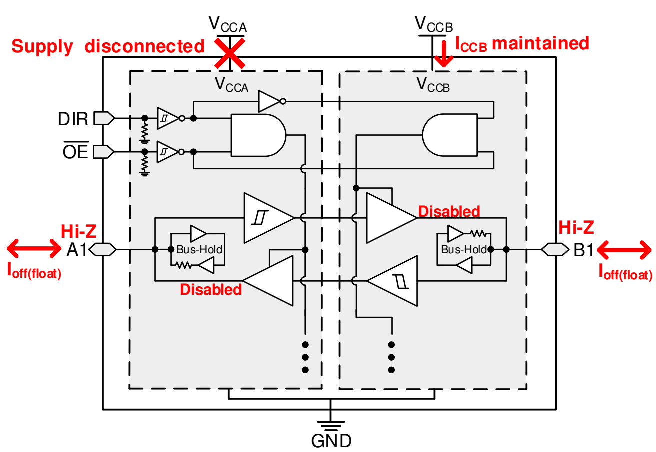


Figure 8-2. V_{CC} Disconnect Feature

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage as long as they remain below the maximum input voltage value specified in the Recommended Operating Conditions.

8.3.6 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

8.3.7 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 8-3.

> **CAUTION**
>
> Voltages beyond the values specified in Section 6.1 table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

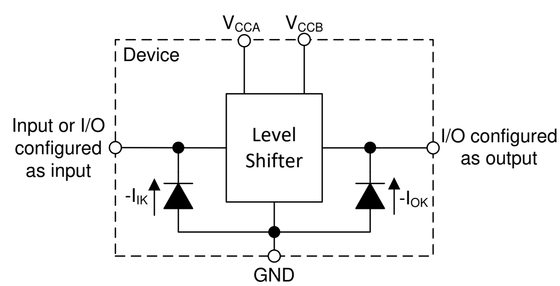


Figure 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.8 Fully Configurable Dual-Rail Design

The V_{CCA} and V_{CCB} pins can be supplied at any voltage from 1.1 V to 5.5 V, making the device suitable for translating between any of the voltage nodes (1.2 V, 1.5 V, 1.8 V, 3.3 V, and 5.0 V).

8.3.9 Supports High-Speed Translation

The SN74LXCH8T245 device can support high data-rate applications. The translated signal data rate can be up to 420 Mbps when the signal is translated from 3.3 V to 5.0 V.

8.3.10 Bus-Hold Data Inputs

Each data input on this device includes a weak latch that maintains a valid logic level on the input. The state of these latches is unknown at startup and remains unknown until the input has been forced to a valid high or low state. After data is sent through a channel, the latch maintains the previous state on the input (if the line is left floating). It is not recommended to use pull-up or pull-down resistors together with a bus-hold input, as it may cause undefined inputs to occur which leads to excessive current consumption.

Bus-hold data inputs prevent floating inputs on this device. The Implications of Slow or Floating CMOS Inputs application report explains the problems associated with leaving the CMOS inputs floating. These latches remain active at all times, independent of all control signals such as direction control or output enable. The latches also remain active when the device is in the partial power down state, corresponding supply is still present, or when the I/O's are floated. The Bus-Hold Circuit application report has additional details regarding bus-hold inputs.

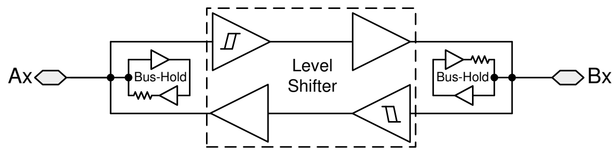


Figure 8-4. Schematic Description of Location of Bus-Hold Circuits

8.4 Device Functional Modes

Table 8-1. Function Table(1)

CONTROL INPUTS		Port Status		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LXCH8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74LXCH8T245 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 420 Mbps when the device translates a signal from 3.3 V to 5.0 V.

9.2 Typical Application

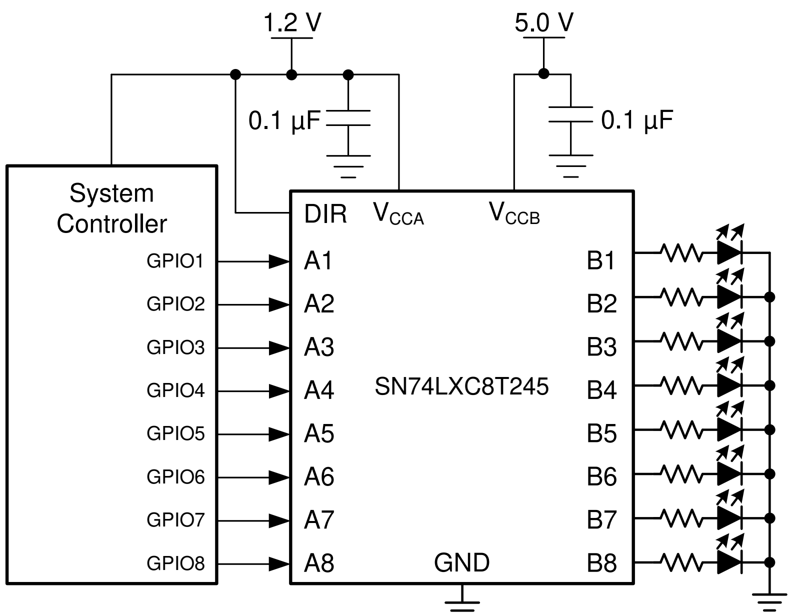


Figure 9-1. LED Driver Application

9.2.1 Design Requirements

Use the parameters listed in Table 9-1 for this design example.

Table 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.1 V to 5.5 V
Output voltage range	1.1 V to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range:
  - Use the supply voltage of the device that is driving the SN74LXCH8T245 device to determine the input voltage range. The value must exceed the high-level input voltage (V_{IH}) of the input port for a valid logic-high. The value must be less than the low-level input voltage (V_{IL}) of the input port for a valid logic low.
- Output voltage range:
  - Use the device's supply voltage that the SN74LXCH8T245 device is driving to determine the output voltage range.

9.2.3 Application Curve

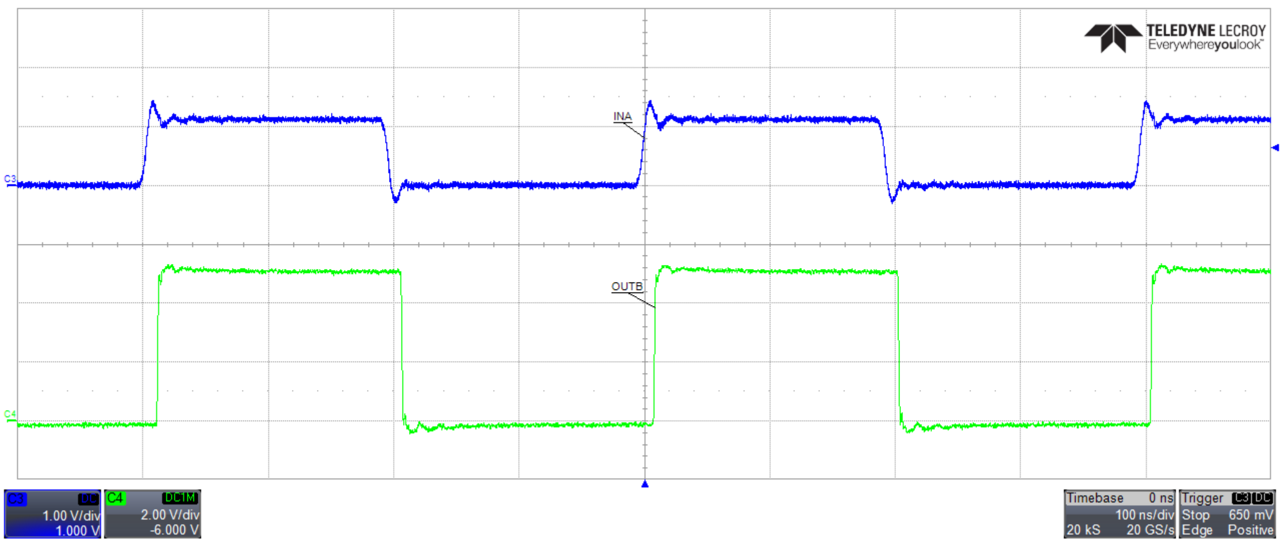


Figure 9-2. Up Translation at 2.5 MHz (1.2 V to 5 V)

10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

Section 8.3.6 describes how this device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices.

11 Layout

11.1 Layout Guidelines

Following common printed-circuit board layout guidelines are recommended to ensure reliability of the device, which follows:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 µF capacitor is recommended, but transient performance can be improved by having both 1 µF and 0.1 µF capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads; so routing and load conditions should be considered to prevent ringing.

11.2 Layout Example

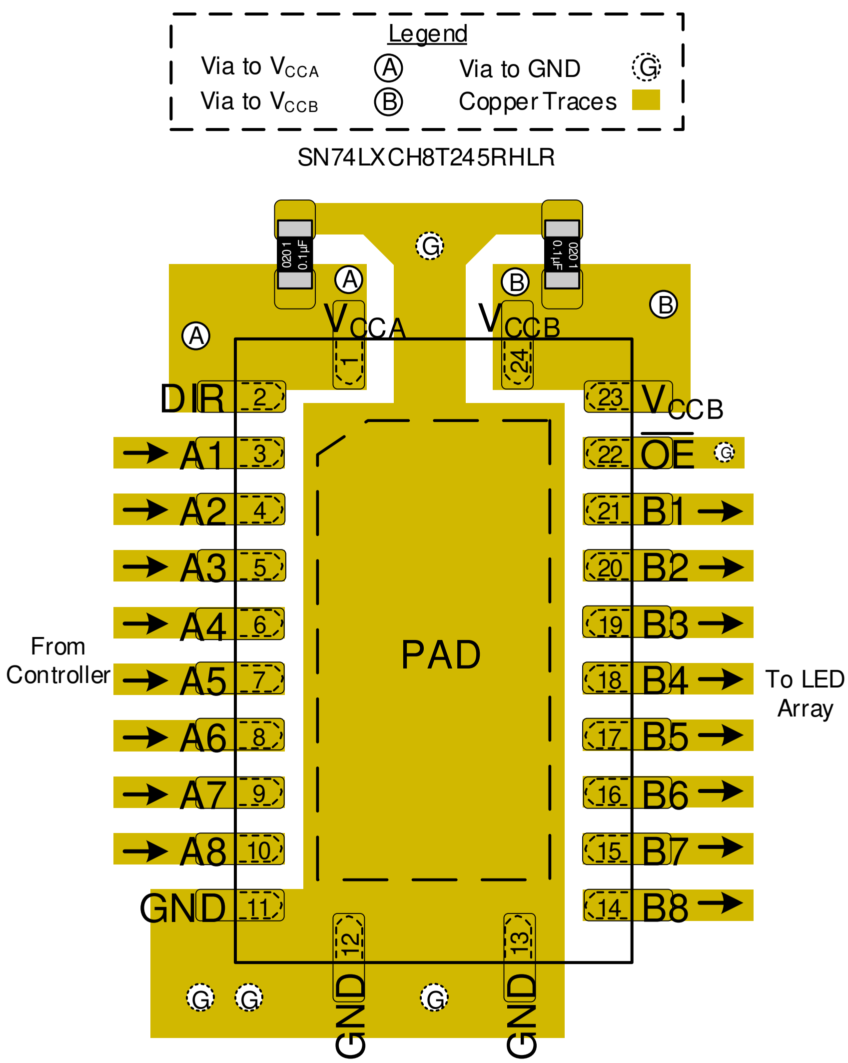


Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and C_{pd} Calculation application report
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application report
- Texas Instruments, Semiconductor and IC Package Thermal Metrics appliction report
- Texas Instruments, System Considerations for Using Bus-Hold Curcuits to Avoid Floating Inputs application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LXCH8T245RHLRG4	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LX8T245H
74LXCH8T245RHLRG4.A	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LX8T245H
SN74LXCH8T245PWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LXH8T245
SN74LXCH8T245PWR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LXH8T245
SN74LXCH8T245PWRG4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LXH8T245
SN74LXCH8T245PWRG4.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LXH8T245
SN74LXCH8T245RHLR	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LX8T245H
SN74LXCH8T245RHLR.A	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LX8T245H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

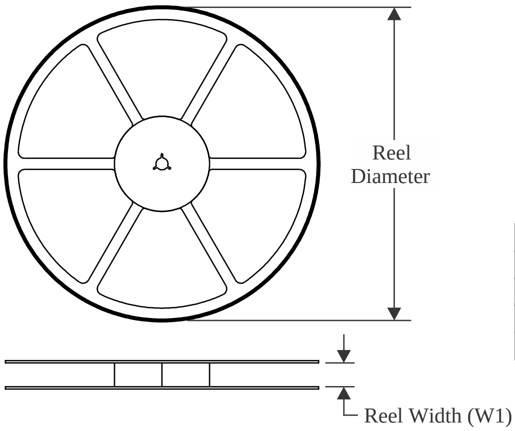
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

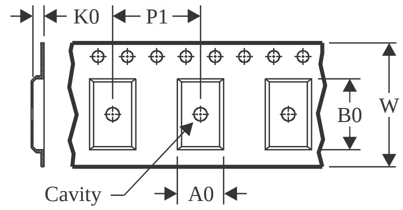
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

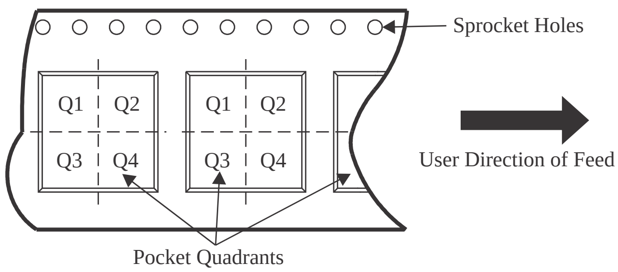


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

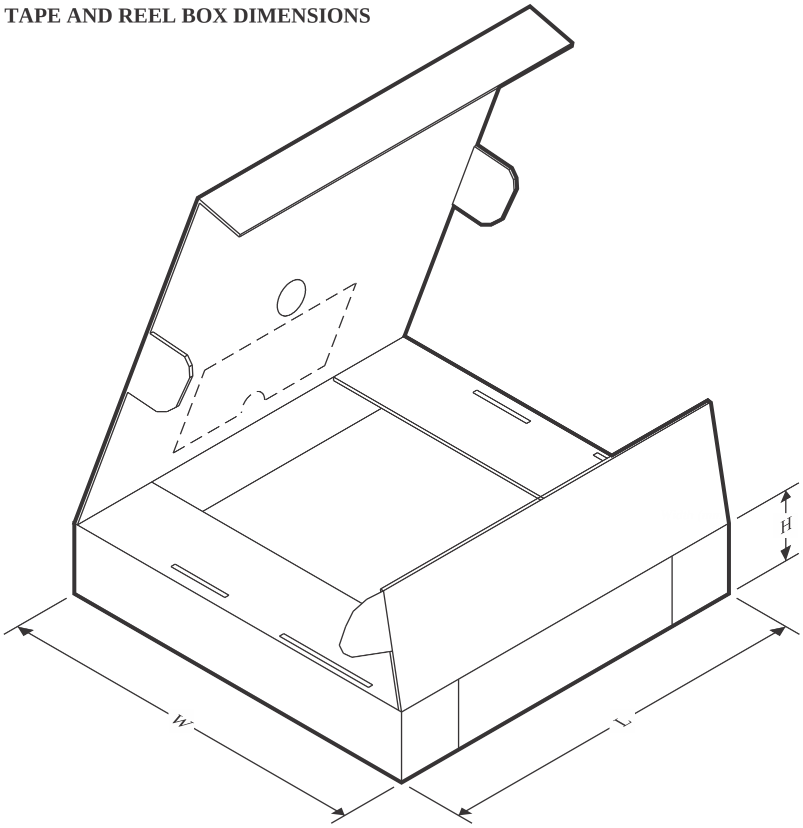
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

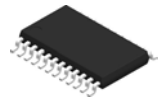
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LXCH8T245RHLRG4	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74LXCH8T245RHLR	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LXCH8T245RHLRG4	VQFN	RHL	24	3000	367.0	367.0	35.0
SN74LXCH8T245RHLR	VQFN	RHL	24	3000	367.0	367.0	35.0

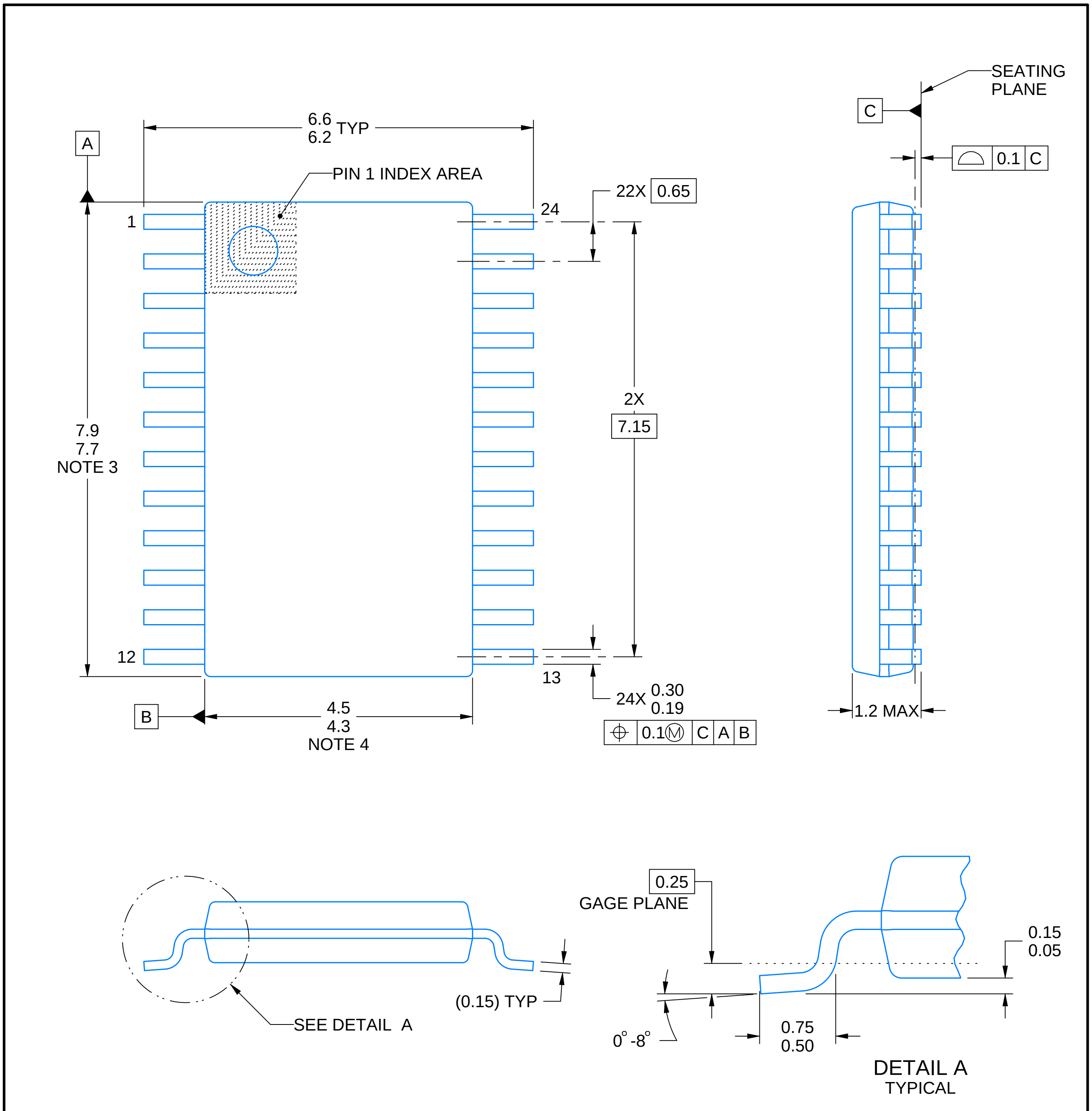


PACKAGE OUTLINE

PW0024A

TSSOP - 1.2 mm max height

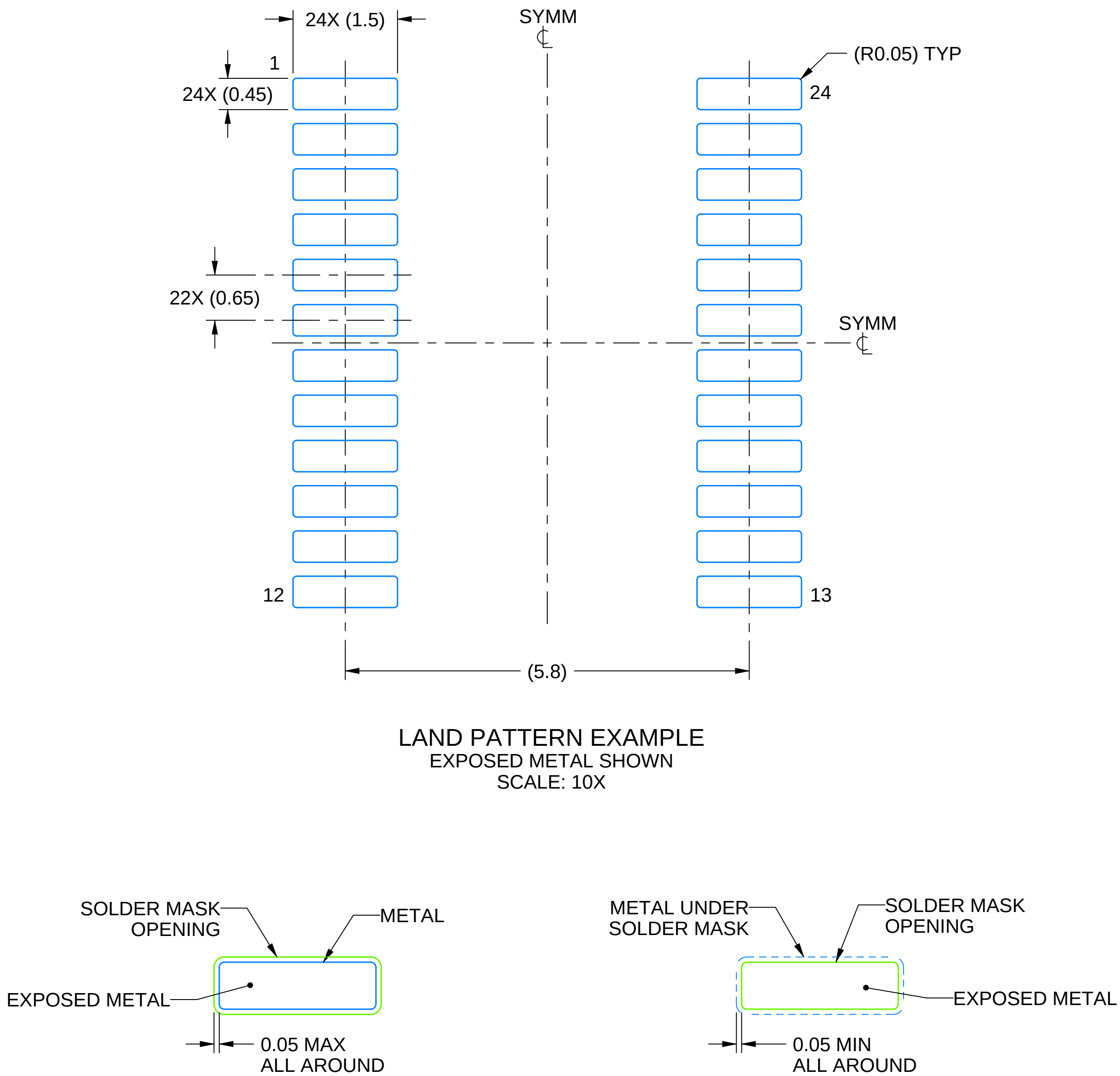
SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

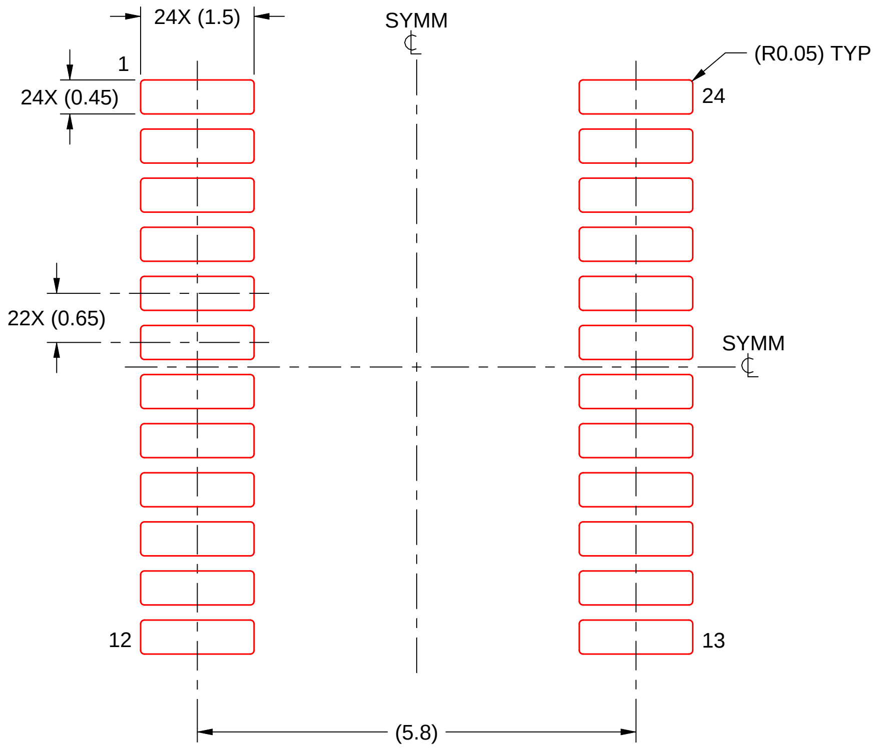
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

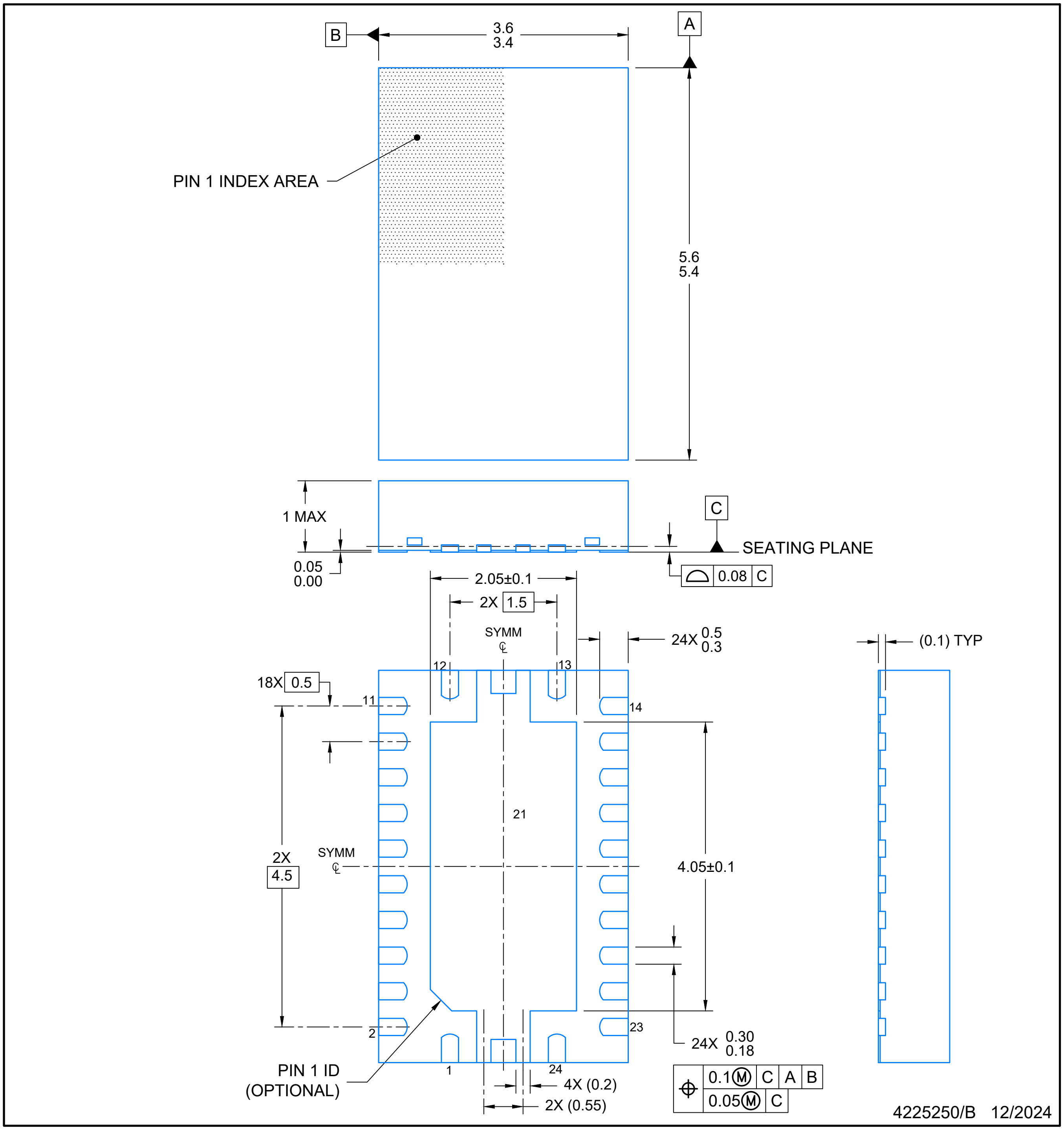


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

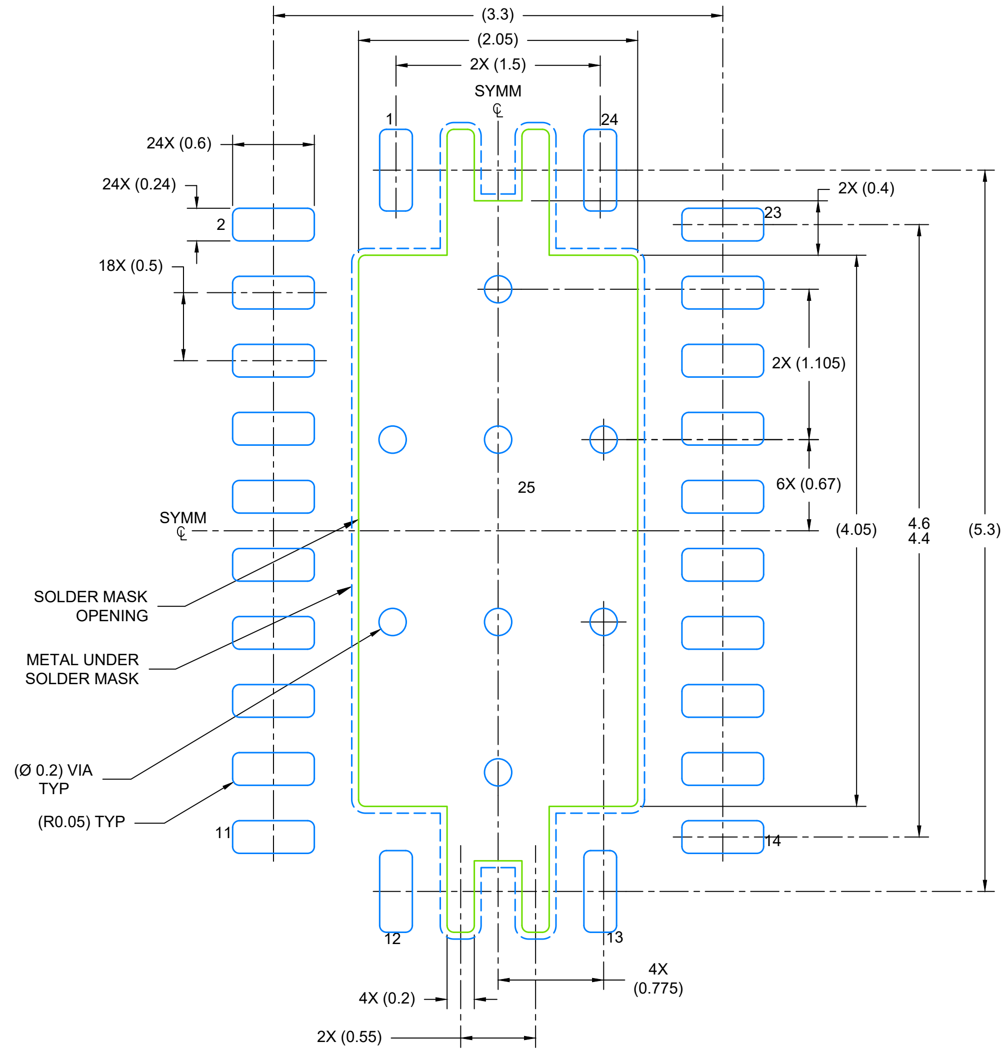
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

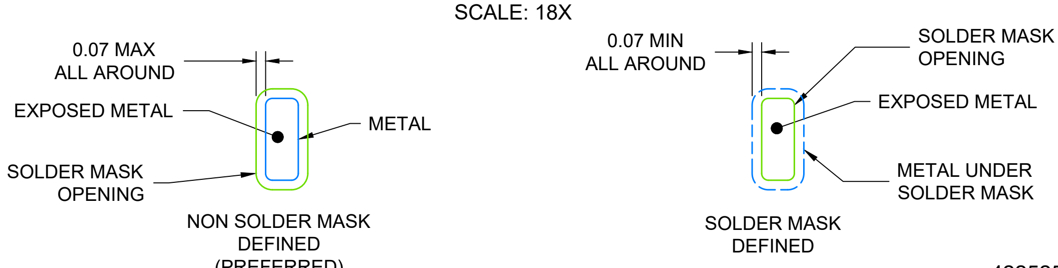


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

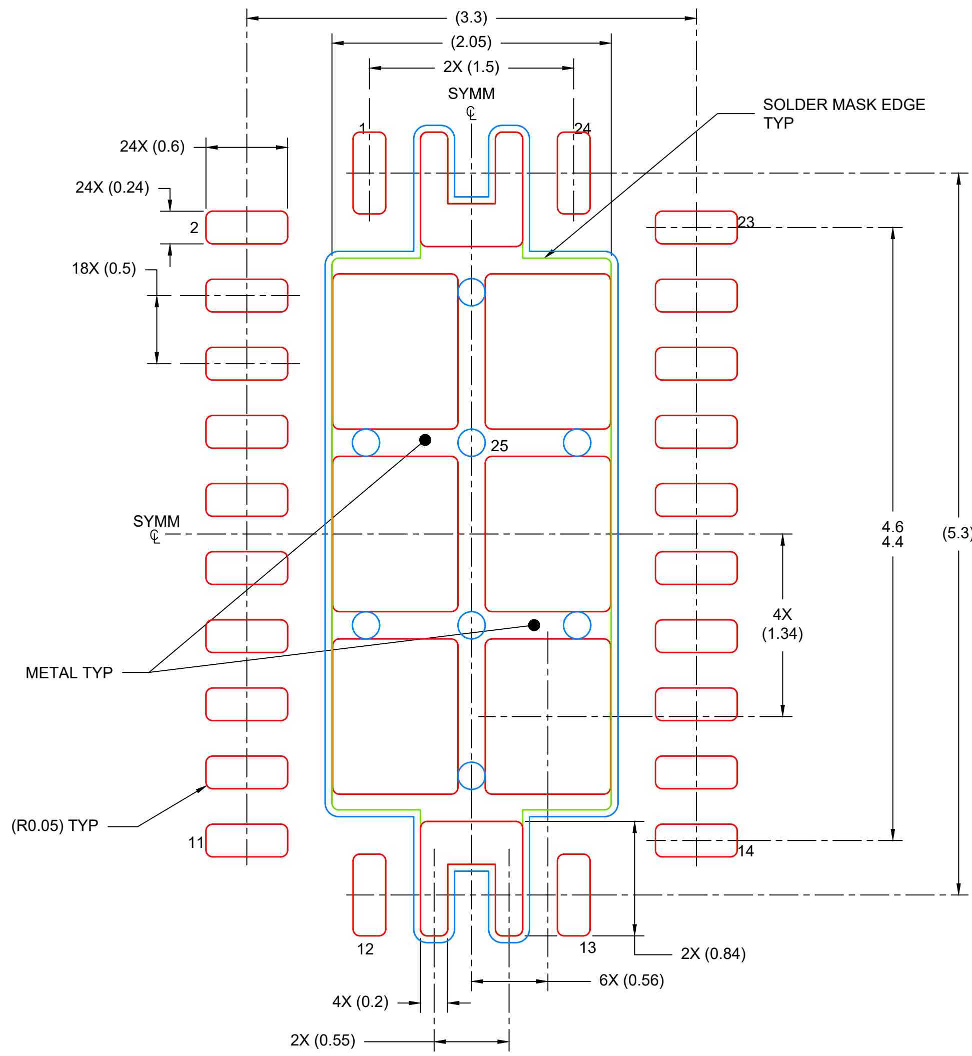


SOLDER MASK DETAILS

4225250/B 12/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/B 12/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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