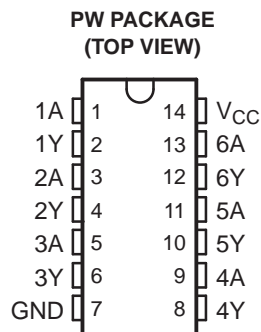


HEX INVERTER

FEATURES

- Qualified for Automotive Applications
- 2-V to 5.5-V V_{CC} Operation
- Unbuffered Outputs
- Typical V_{OLP} (Output Ground Bounce)
 $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
 $>2.3\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports



DESCRIPTION/ORDERING INFORMATION

This hex inverter is designed for 2-V to 5.5-V V_{CC} operation.

The SN74LVU04A-Q1 contains six independent inverters with unbuffered outputs. This device performs the Boolean function $Y = \overline{A}$.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	TSSOP – PW	Reel of 2000	SN74LVU04AQPWRQ1	LU04AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE (EACH INVERTER)

INPUT A	OUTPUT Y
H	L
L	H

LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	−0.5	7	V
V_I	Input voltage range ⁽²⁾	−0.5	7	V
V_O	Output voltage range ^{(2) (3)}	−0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		−20 mA
I_{OK}	Output clamp current	$V_O < 0$		−50 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25 mA
	Continuous current through V_{CC} or GND			±50 mA
θ_{JA}	Package thermal impedance ⁽⁴⁾			113 °C/W
ESD rating ⁽⁵⁾	Human-Body Model		1.5 (H1C)	kV
	Charged-Device Model		1 (C5)	
	Machine Model		200 (M3)	V
T_{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) ESD protection level per AEC Q100 classification

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.7	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.8$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.8$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.8$	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.3	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.2$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.2$	
		$V_{CC} = 4.5$ V to 5.5 V	0.8	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V	−50	μA
		$V_{CC} = 2.3$ V to 2.7 V	−2	mA
		$V_{CC} = 3$ V to 3.6 V	−6	
		$V_{CC} = 4.5$ V to 5.5 V	−12	
I_{OL}	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 2.3$ V to 2.7 V	2	mA
		$V_{CC} = 3$ V to 3.6 V	6	
		$V_{CC} = 4.5$ V to 5.5 V	12	
T_A	Operating free-air temperature	−40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	–40°C to 125°C			–40°C to 85°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	V _{IL} = 0 V	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
	I _{OH} = –2 mA		2			2				
	I _{OH} = –6 mA		2.48			2.48				
	I _{OH} = –12 mA		3.7			3.8				
V _{OL}	I _{OL} = 50 μA	V _{IH} = V _{CC}	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA		0.4			0.4				
	I _{OL} = 6 mA		0.44			0.44				
	I _{OL} = 12 mA		0.55			0.55				
I _I	V _I = 5.5 V or GND		0 V to 5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0		5.5 V	20			20			μA
C _i	V _I = V _{CC} or GND		3.3 V	4			4			pF

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 125°C		–40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 50 pF		4.7	11.4	1	16	1	13	ns

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 125°C		–40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 50 pF		3.9	7	1	11	1	8	ns

Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C⁽¹⁾

PARAMETER		MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.5	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		–0.1	–0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		3		V
V _{IH(D)}	High-level dynamic input voltage		2.31		V
V _{IL(D)}	Low-level dynamic input voltage			0.99	V

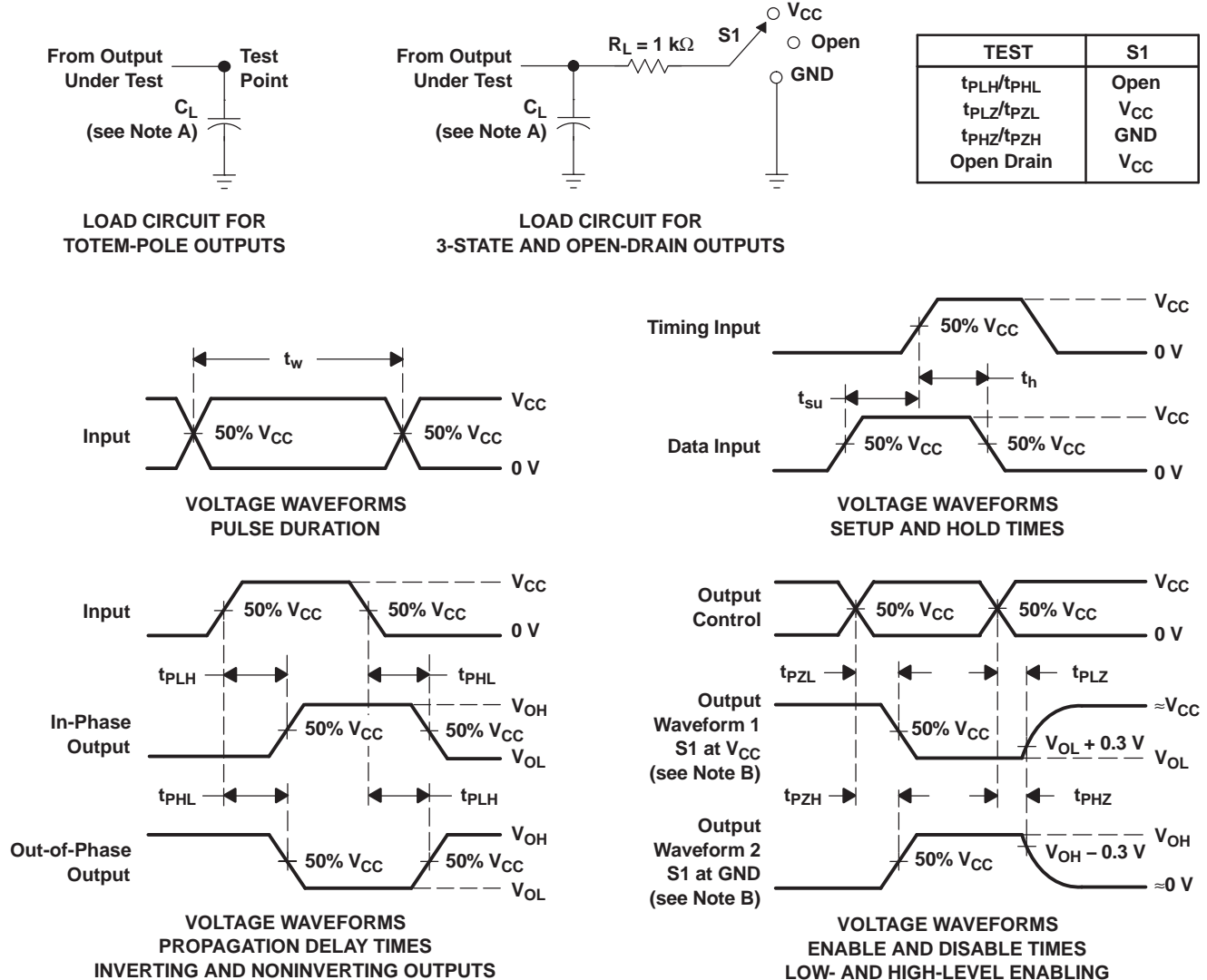
(1) Characteristics are for surface-mount packages only.

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz		3.3 V	5.6	pF
				5 V	6.7	

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVU04AQPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LU04AQ
SN74LVU04AQPWRG4Q1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LU04AQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVU04A-Q1 :

- Catalog : [SN74LVU04A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVU04AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVU04AQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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