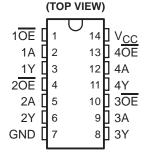
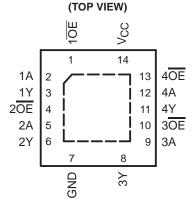
SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS703I - AUGUST 1997 - REVISED OCTOBER 2003

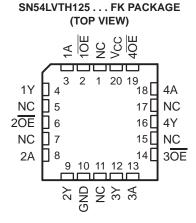
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH125 . . . J OR W PACKAGE SN74LVTH125 . . . D, DB, DGV, NS, OR PACKAGE





SN74LVTH125 . . . RGY PACKAGE



NC - No internal connection

description/ordering information

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH125 devices feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (OE) input is high.

ORDERING INFORMATION

TA	PACK	AGET	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	QFN – RGY	Tape and reel	SN74LVTH125RGYR	LXH125	
-40°C to 85°C	0010 D	Tube	SN74LVTH125D	IVELIA OF	
	SOIC - D	Tape and reel	SN74LVTH125DR	LVTH125	
	SOP - NS	Tape and reel	SN74LVTH125NSR	LVTH125	
	SSOP – DB	Tape and reel	SN74LVTH125DBR	LXH125	
	TOCOD DW	Tube	SN74LVTH125PW	LVIIIOS	
	TSSOP – PW	Tape and reel	SN74LVTH125PWR	LXH125	
	TVSOP - DGV	Tape and reel	SN74LVTH125DGVR	LXH125	
	CDIP – J	Tube	SNJ54LVTH125J	SNJ54LVTH125J	
-55°C to 125°C	CFP – W	Tube	SNJ54LVTH125W	SNJ54LVTH125W	
	LCCC - FK	Tube	SNJ54LVTH125FK	SNJ54LVTH125FK	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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description/ordering information (continued)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

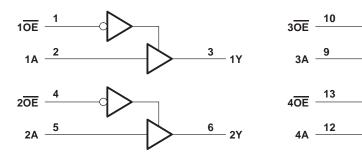
When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	
Voltage range applied to any output in the high-impedance or power-off state, V _O (see Note 1)	V to 7 V
Voltage range applied to any output in the high state, V _O (see Note 1)	+ 0.5 V
Current into any output in the low state, IO: SN54LVTH125	. 96 mA
SN74LVTH125	
Current into any output in the high state, IO (see Note 2): SN54LVTH125	. 48 mA
SN74LVTH125	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$)	
Package thermal impedance, θ _{JA} (see Note 3): D package	
(see Note 3): DB package	
(see Note 3): DGV package	
(see Note 3): NS package	
(see Note 3): PW package	
(see Note 4): RGY package	
Storage temperature range, T _{sta} –65°C t	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.
- 4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LV	TH125	SN74LV	TH125	LINUT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	N	2		V
V _{IL}	Low-level input voltage			0.8		8.0	V
VI	Input voltage	Q	5.5		5.5	V	
loн	High-level output current		6	-24		-32	mA
loL	Low-level output current		770	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	190	10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEOT 001	UDITIONS	SN54	LVTH12	5	SN74LVTH125			
PAR	AMETER	TEST COI	NUTTIONS	MIN	TYP†	MAX	MIN	TYPT MAX		UNIT
٧ıK		$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA			-1.2			-1.2	٧
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V},$	$I_{OH} = -100 \mu A$ $V_{CC} - 0.2$ $V_{CC} - 0.2$							
		$V_{CC} = 2.7 \text{ V},$	IOH = -8 mA	2.4			2.4			V
VOH		V 2.V	$I_{OH} = -24 \text{ mA}$	2						V
		ACC = 3 A	$I_{OH} = -32 \text{ mA}$				2			
		V 27V	$I_{OL} = 100 \mu A$			0.2			0.2	
		vCC = 2.7 v	$I_{OL} = 24 \text{ mA}$			0.5			0.5	
\/ - ·			$I_{OL} = 16 \text{ mA}$			0.4			0.4	V
		$I_{OL} = 32 \text{ mA}$			0.5			0.5	V	
	VOL Control inputs Data inputs IGH IOZH IOZPU IOZPU ICC ΔICC Ci	vCC = 3 v	I _{OL} = 48 mA			0.55				
			I _{OL} = 64 mA						0.55	
		$V_{CC} = 0 \text{ or } 3.6 \text{ V},$	V _I = 5.5 V			10			10	
lį		V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND	CC or GND ±1					±1	μА
•		TEST CONDITIONS	1							
	Data inputs	VCC = 3.6 V	V _I = 0		7	-5			0.2 0.5 0.4 0.5 0.55 10	
l _{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V	ċ	5				±100	μΑ
			V _I = 0.8 V	75,0	/		75			
I _{I(hold)}	Data inputs	ACC = 3 A	V _I = 2 V	-75			-75			μΑ
, ,	Data inputs \\ f \\ hold) Data inputs \\ \text{X}	$V_{CC} = 3.6 V^{\ddagger}$,	$V_{I} = 0 \text{ to } 3.6 \text{ V}$						±500	
lozh		$V_{CC} = 3.6 \text{ V},$	V _O = 3 V			5			5	μΑ
lozL		$V_{CC} = 3.6 \text{ V},$	$V_0 = 0.5 V$			-5			-5	μΑ
lozpu		$\frac{V_{CC}}{OE} = 0$ to 1.5 V, $V_{O} = 0$	0.5 V to 3 V,			±50*			±50	μΑ
lozpd		$\frac{V_{CC}}{OE}$ = 1.5 V to 0, V _O = $\frac{V_{CC}}{OE}$ = don't care	0.5 V to 3 V,			±50*			±50	μΑ
		Vcc = 3.6 V.	Outputs high		0.12	0.19		0.12	0.19	
ICC		$I_{O} = 0$,	Outputs low		4.5	7		4.5	7	mA
	$V_I = V_{CC}$ or GND		Outputs disabled		0.12	0.19		0.12	0.19	
Δl _{CC} §		$V_{CC} = 3 \text{ V to } 3.6 \text{ V, On}$ Other inputs at V_{CC} or	e input at V _{CC} – 0.6 V, GND		_	0.3		_	0.2	mA
Ci		V _I = 3 V or 0			4			4		pF
Со		V _O = 3 V or 0			6.5			6.5		pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.



[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡]This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

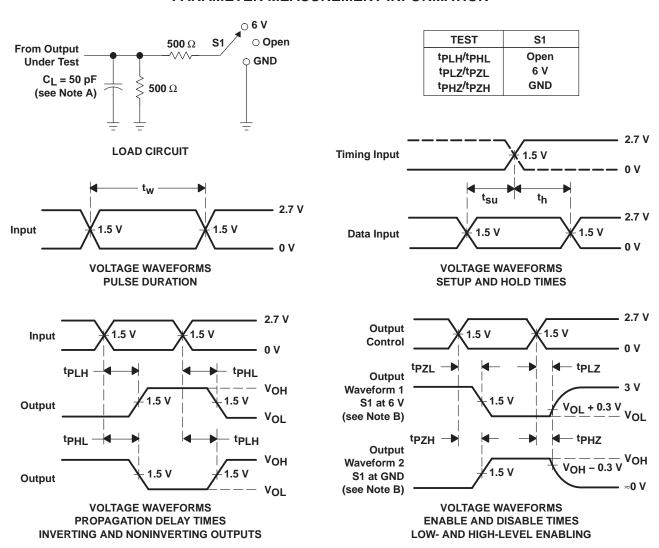
[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than VCC or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54L\	/TH125			SN7	74LVTH1	125			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
t _{PLH}	А	V	1	4.2	3/	4.7	1	2	3.5		4.5	20	
^t PHL		Y	1	4.1	36	5.1	1	2.1	3.9		4.9	ns	
^t PZH	7	V	1	4.9	Z	5.6	1	2	4		5.5	20	
t _{PZL}	ŌĒ	Y	1.1	4.9		5.6	1.1	2.1	4		5.4	ns	
^t PHZ	ŌĒ			1.5	5.3		5.9	1.5	2.3	4.5		5.7	
t _{PLZ}	OE	Y	1.3	4.7		4.2	1.3	2.8	4.5		4	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVTH125D	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH125
SN74LVTH125D.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH125
SN74LVTH125DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125DBR.B	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125DBRE4	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125DGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125DGVR.B	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125DGVRG4	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125DGVRG4.B	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH125
SN74LVTH125DR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH125
SN74LVTH125DRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH125
SN74LVTH125NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH125
SN74LVTH125NSR.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH125
SN74LVTH125NSRE4	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH125
SN74LVTH125PW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125PW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125PWE4	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125PWG4	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125PWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH125
SN74LVTH125RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LXH125
SN74LVTH125RGYR.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LXH125
SN74LVTH125RGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LXH125
SN74LVTH125RGYRG4.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LXH125

⁽¹⁾ Status: For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVTH125:

Enhanced Product: SN74LVTH125-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH125DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVTH125DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVTH125DGVRG4	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVTH125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVTH125NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVTH125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVTH125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74LVTH125RGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH125DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVTH125DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LVTH125DGVRG4	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LVTH125DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74LVTH125NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVTH125PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVTH125RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0
SN74LVTH125RGYRG4	VQFN	RGY	14	3000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVTH125D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVTH125D.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVTH125PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVTH125PW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVTH125PWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVTH125PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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