

SN74LVC86A-Q1 Automotive Quadruple 2-Input Exclusive-OR Gate

1 Features

- Qualified for automotive applications
- ESD protection exceeds 2000V per MIL-STD-883, Method 3015
- Operates from 2V to 3.6V
- Inputs accept voltages to 5.5V
- Max t_{pd} of 4.6ns at 3.3V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, $T_A = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} $= 3.3V, T_A = 25^{\circ}C$

2 Description

The SN74LVC86A-Q1 quadruple 2-input exclusive-OR gate is designed for 2.7V to 3.6V V_{CC} operation.

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
SN74LVC86A-Q1	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

- (1) For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Exclusive-OR Logic



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3 Pin Configuration and Functions

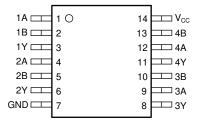


Figure 3-1. SN74LVC86A-Q1 D or PW Package, 14-Pin SOIC or TSSOP (Top View)

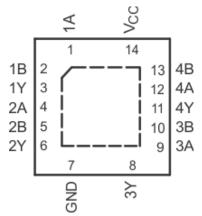


Figure 3-2. SN74LVC86A-Q1 BQA Package, 14-Pin WQFN (Top View)

Table 3-1. Pin Functions

	PIN		Thir unctions		
NO.	D, PW, BQA	TYPE ⁽¹⁾	DESCRIPTION		
NO.	14 PINS				
1A	1	I	Gate 1 input		
1B	2	I	Gate 1 input		
1Y	3	0	Gate 1 output		
2A	4	I	Gate 2 input		
2B	5	I	Gate 2 input		
2Y	6	0	Gate 2 output		
3Y	8	0	Gate 3 output		
3A	9	I	Gate 3 input		
3B	10	I	Gate 3 input		
4Y	11	0	Gate 4 output		
4A	12	I	Gate 4 input		
4B	13	I	Gate 4 input		
GND	7	_	Ground Pin		
NC	_	_	Do not connect		
V _{CC}	14	_	Power Pin		
Thermal pad ⁽²⁾		_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.		



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V _{CC}	Supply voltage range			-0.5	6.5	V
VI	Input voltage range ⁽²⁾			-0.5	6.5	V
Vo	Output voltage range ^{(2) (3)}		-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0			-50	mA
I _{OK}	Output clamp current	V _O < 0	0		-50	mA
Io	Continuous output current				±50	mA
	Continuous current through V _{CC} or GND			±100	mA	
T _{stg}	Storage temperature range			-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

			VALUE	UNIT
V _{(ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V	Supply voltage	Operating	2	3.6	V
V _{CC}	Supply voltage	Data retention only	1.5		V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage	·	0	5.5	V
Vo	Output voltage		0	V _{CC}	V
	High-level output current	V _{CC} = 2.7 V		-12	mΛ
Іон	nigh-level output current	V _{CC} = 3 V		-24	mA
	Low-level output current	V _{CC} = 2.7 V		12	mA
I _{OL}	Low-level output current	V _{CC} = 3 V		24	ША
Δt/Δν	Input transition rise or fall rate			9	ns/V
T _A	Operating free-air temperature		-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC(1)			SN74LVC86A-Q1			
		BQA	D	PW	UNIT	
			14 PINS	14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.3	127.8	150.8	°C/W	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

Product Folder Links: SN74LVC86A-Q1

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.



4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP(1) MAX	UNIT
	I _{OH} = -100μA	2.7V to 3.6V	V _{CC} - 0.2	
V _{OH}	I _{OH} = -12mA	2.7V	2.2	V
VOH	10H12111A	3V	2.4	V
	I _{OH} = -24mA	3V	2.2	
	I _{OL} = 100μA	2.7V to 3.6V	0.2	
V _{OL}	I _{OL} = 12mA	2.7V	0.4	V
	I _{OL} = 24mA	3V	0.55	
I _I	V _I = 5.5V or GND	3.6V	±5	μΑ
I _{CC}	$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6V	10	μΑ
ΔI _{CC}	One input at V _{CC} -0.6 V, Other inputs at V _{CC} or GND	2.7V to 3.6V	500	μΑ
C _i	V _I = V _{CC} or GND	3.3V	5	pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

4.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.7 V	V _{CC} = ± 0.3	V _{CC} = 3.3 V ± 0.3 V	
	(INFOT)		MIN MAX	MIN	MAX	
t _{pd}	A	Υ	5.6	1	4.6	ns

4.7 Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER		TEST	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
		CONDITIONS	TYP	TYP	ONII
С	Power dissipation capacitance per gate	f = 10 MHz	7.5	8.5	pF

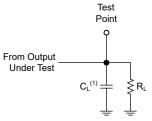


5 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_O = 50\Omega$, $t_t \leq$ 2.5ns.

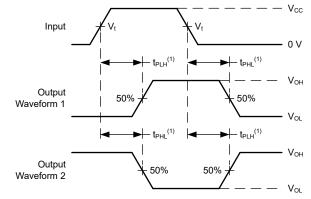
The outputs are measured individually with one input transition per measurement.

V _{cc}	V _t	R _L	CL	ΔV
1.8V ± 0.15V	V _{CC} /2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V _{CC} /2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



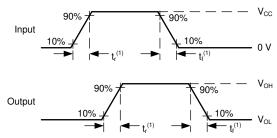
(1) C_L includes probe and test-fixture capacitance.

Figure 5-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 5-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 5-3. Voltage Waveforms, Input and Output Transition Times

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6 Detailed Description

6.1 Overview

The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A \overline{B}$ in positive logic.

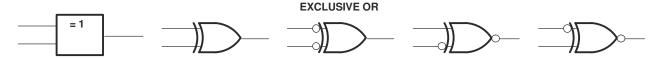
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

6.2 Functional Block Diagram

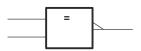
Exclusive-OR Logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



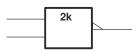
These five equivalent exclusive-OR symbols are valid for an SN74LVC86A gate in positive logic; negation may be shown at any two ports.





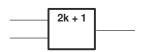
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active

6.3 Device Functional Modes

Function Table (Each Gate)

INP	UTS	OUTPUT
Α	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

7 Application and Implementation

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 4.3 table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Section 7.2.2 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

7.2.2 Layout Example

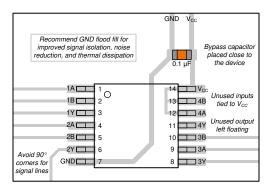


Figure 7-1. Example Layout for the SN74LVC86A-Q1

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8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS		PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
	SN74LVC86A-Q1	Click here	Click here	Click here	Click here	Click here	

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

(Changes from Revision D (August 2024) to Revision E (December 2024)	Page
•	• Updated RθJA values: D = 86 to 127.8, all values in °C/W	4
-		

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking	
	(1)	(2)			(3)	Ball material	Peak reflow		(6)	
						(4)	(5)			
SN74LVC86AQDRG4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86AQ	
SN74LVC86AQDRG4Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86AQ	
SN74LVC86AQDRG4Q1.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86AQ	
SN74LVC86AQPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86AQ	
SN74LVC86AQPWRG4Q1.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86AQ	
SN74LVC86AQPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86AQ	
SN74LVC86AQPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86AQ	
SN74LVC86AQPWRQ1.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86AQ	
SN74LVC86AWBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86Q	
SN74LVC86AWBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86Q	

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC86A-Q1:

Catalog: SN74LVC86A

● Enhanced Product: SN74LVC86A-EP

Military: SN54LVC86A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC86AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC86AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC86AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC86AWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

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*All dimensions are nominal

7 th difference and fronting									
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)		
SN74LVC86AQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0		
SN74LVC86AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0		
SN74LVC86AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0		
SN74LVC86AWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0		



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

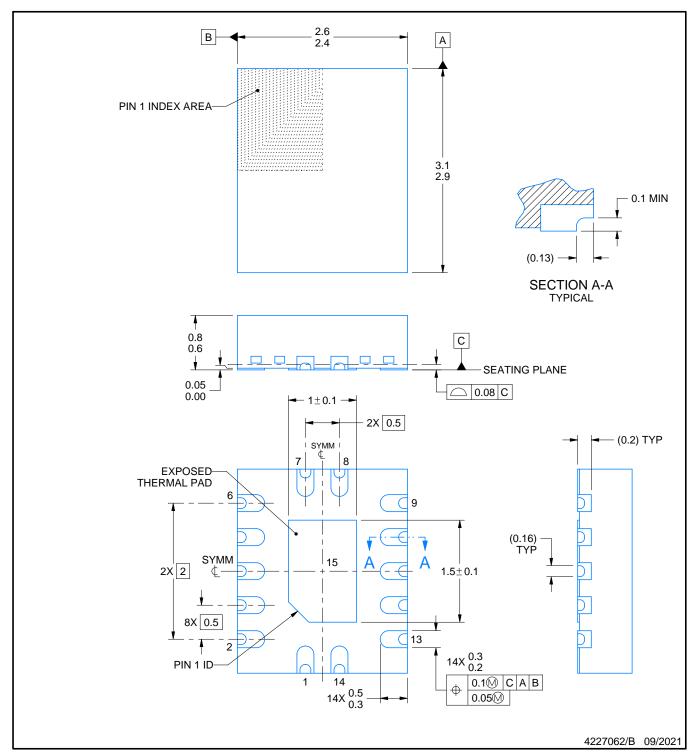
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD

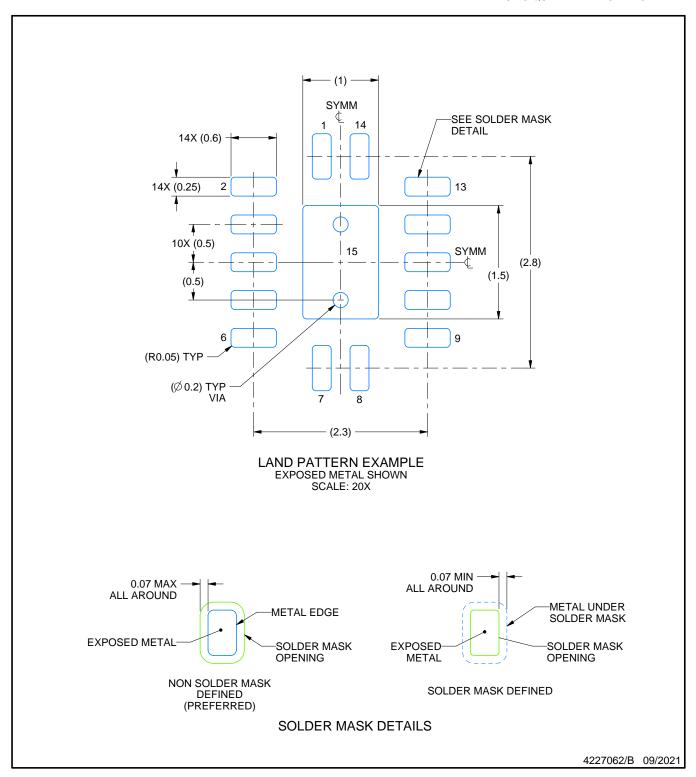


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

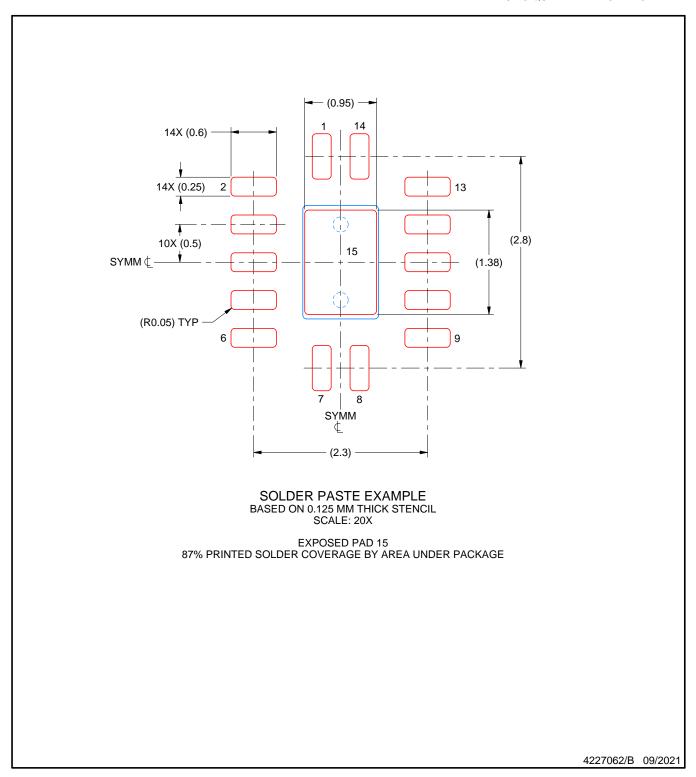


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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