







SN74LVC74A-Q1

SCES481E - AUGUST 2003 - REVISED AUGUST 2024

SN74LVC74A-Q1 Automotive Dual Positive-Edge-Triggered D-Type Flip-Flop With **Clear and Preset**

1 Features

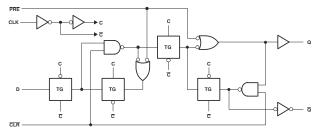
- Qualified for automotive applications
- ESD protection exceeds 2000V per MIL-STD-883, Method 3015
- Operates from 2V to 3.6V
- Inputs accept voltages to 5.5V
- Max t_{pd} of 5.2ns at 3.3V
- Typical V_{OLP} (output ground bounce) <0.8V at V_{CC} $= 3.3V, T_A = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) >2V at V_{CC} $= 3.3V, T_A = 25$ °C

2 Description

The SN74LVC74A-Q1 dual positive-edge-triggered D-type flip-flop is designed for 2.7V to 3.6V $V_{\rm CC}$ operation.

PART NUMBER	PACKAGE (1)	PACKAGE SIZE ⁽²⁾	BODY SIZE(3)
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
SN74LVC74A-Q1	D (SOIC, 14)	8.65mm x 6mm	8.65mm × 3.91mm
	PW (TSSOP, 14)	5mm x 6.4mm	5.00mm × 4.40mm

- For more information, see Mechanical, Packaging, and Orderable Information.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Flip-Flop (Positive Logic)



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3 Pin Configuration and Functions

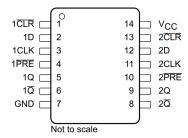


Figure 3-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

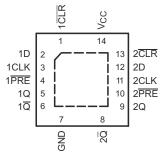


Figure 3-2. BQA Package 14-Pin WQFN With Exposed Thermal Pad (Top View)

Table 3-1. Pin Functions

	PIN	I/O ⁽¹⁾	DESCRIPTION
NAME	SOIC, TSSOP, VQFN	1/0(1)	DESCRIPTION
1CLK	3	1	Channel 1 clock input
1 CLR	1	I	Channel 1 clear input. Pull low to set Q output low.
1D	2	I	Channel 1 data input
1 PRE	4	I	Channel 1 preset input. Pull low to set Q output high.
1Q	5	0	Channel 1 output
1 Q	6	0	Channel 1 inverted output
2CLK	11	I	Channel 2 clock input
2 CLR	13	I	Channel 2 clear input. Pull low to set Q output low.
2D	12	I	Channel 2 data input
2 PRE	10	- 1	Channel 2 preset input. Pull low to set Q output high.
2Q	9	0	Channel 2 output
2 Q	8	0	Channel 2 Inverted output
GND	7	_	Ground
NC	_	_	No connect
V _{CC}	14	_	Supply
Thermal pad		_	Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V	
VI	Input voltage range ⁽¹⁾			-0.5	6.5	V
Vo	Output voltage range ⁽¹⁾ (2)		-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0			-50	mA
I _{OK}	Output clamp current	V _O < 0			-50	mA
Io	Continuous output current				±50	mA
	Continuous current through V _{CC} or GND			±100	mA	
T _{stg}	Storage temperature range			-65	150	°C

⁽¹⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V	Cumply voltage	Operating	2	3.6	V
V _{CC}	Supply voltage	Data retention only	1.5		v
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage	·	0	5.5	V
Vo	Output voltage		0	V _{CC}	V
	Heat Level and a second	V _{CC} = 2.7 V		-12	mA
I _{OH}	High-level output current	V _{CC} = 3 V		-24	IIIA
	Low-level output current	V _{CC} = 2.7 V		12	mA
I _{OL}	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature	Q suffix	-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4.4 Thermal Information

			SN74LVC74A-Q1				
	THERMAL METRIC(1)	BQA (WQFN)	D (SOIC)	PW (TSSOP)	UNIT		
		14 PINS	14 PINS	14 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.3	127.8	150.8	°C/W		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	96.8	81.9	78.3	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	84.4	93.8	°C/W		
ΨЈТ	Junction-to-top characterization parameter	16.6	39.6	24.7	°C/W		

⁽²⁾ The value of V_{CC} is provided in the recommended operating conditions table.



THERMAL METRIC(1)			SN74LVC74A-Q1			
		BQA (WQFN)	D (SOIC)	PW (TSSOP)	UNIT	
		14 PINS	14 PINS	14 PINS		
ΨЈВ	Junction-to-board characterization parameter	70.9	83.9	93.2	°C/W	
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	50.1	N/A	N/A	°C/W	

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT
	I _{OH} = -100 μA	2.7 V to 3.6 V	V _{CC} - 0.2		
V	L = 12 mA	2.7 V	2.2		V
V _{OH}	I _{OH} = -12 mA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	2.7 V to 3.6 V		0.2	
V _{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
I _I	V _I = 5.5 V or GND	3.6 V		±5	μA
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μA
ΔI _{CC}	One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND	2.7 V to 3.6 V		500	μA
Ci	$V_I = V_{CC}$ or GND	3.3 V		5	pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

4.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

	, ğ ,	3 (/ \	V _{CC} =	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
				MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency				83		100	MHz
t Dula	Pulse duration	Nulsa duration		3.3		3.3		ne
L _W	ruise duration	CLK high or low	3.3		3.3		ns	
	Saturatima hafara CLK+		Data	3.4		3		no
t _{su}	Setup time before CLK↑	PRE or CLR inactive	2.2		2		ns	
t _h	Hold time, data after CLK↑			1		1		ns

4.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2	2.7 V	V _{CC} = 3 ± 0.3	3.3 V 3 V	UNIT
	(IIAF O1)	(OUTFOT)	MIN	MAX	MIN	MAX	
f _{max}			83		100		MHz
t _{pd}	CLK	Q or $\overline{\mathbb{Q}}$		6	1	5.2	ns
	PRE or CLR			6.4	1	5.4	115



4.8 Operating Characteristics

T_A = 25°C

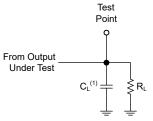
PARAMETER		TEST	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
	FAIAMETER	CONDITIONS	TYP	TYP	ONIT
C _{pd}	Power dissipation capacitance per flip-flop	f = 10 MHz	47	51	pF

5 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_O = 50\Omega$, $t_t \leq$ 2.5ns.

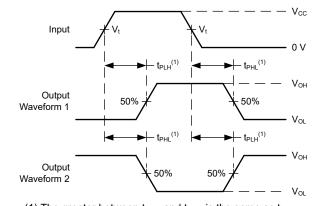
The outputs are measured individually with one input transition per measurement.

V _{cc}	V _t	R _L	CL	ΔV
1.8V ± 0.15V	V _{CC} /2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V _{CC} /2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



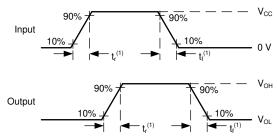
(1) C_L includes probe and test-fixture capacitance.

Figure 5-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 5-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 5-3. Voltage Waveforms, Input and Output Transition Times

6 Detailed Description

6.1 Overview

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

6.2 Functional Block Diagram

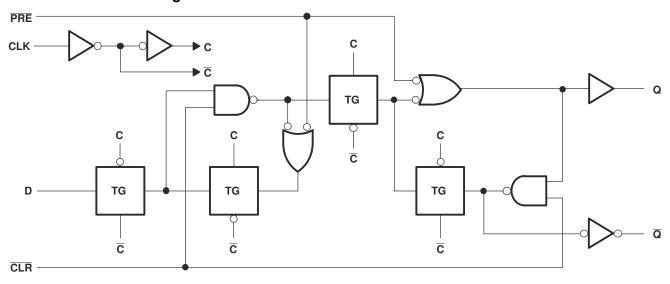


Figure 6-1. Logic Diagram, Each Flip-Flop (Positive Logic)

6.3 Device Functional Modes

Function Table

	INP	OUTI	PUTS		
PRE	CLR	CLK	D	Q	Q
L	Н	Χ	Χ	Н	L
Н	L	Χ	X	L	Н
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
Н	Н	↑	Н	Н	L
Н	Н	↑	L	L	Н
Н	Н	L	Χ	Q_0	\overline{Q}_0

This configuration is nonstable; that is, it does not persist when (1) PRE or CLR returns to its inactive (high) level.



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply may be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01- μ F or 0.022- μ F capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

7.2 Layout

7.2.1 Layout Guidelines

Inputs must not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Layout Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC} , whichever makes more sense or is more convenient.

7.2.2 Layout Example

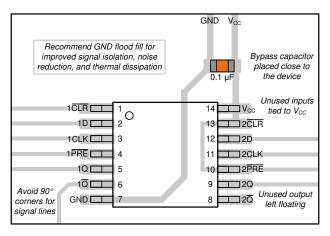


Figure 7-1. Layout Diagram



8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN74LVC74A-Q1	Click here	Click here	Click here	Click here	Click here	

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2024) to Revision E (August 2024)

Page

Changes from Revision C (August 2003) to Revision D (May 2024)

Page

- Added BQA package to Package Information table, Pin Configuration and Functions section, and Thermal
 Information table



•	Deleted references to machine model in <i>Features</i> section
•	Updated RθJA values: D = 86 to 127.8, all values in °C/W

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74LVC74ADRQ1	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74ADRQ1.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74AQDRG4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74AQDRG4Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74AQDRG4Q1.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74AQPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74AQPWRG4Q1.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74AQPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74AQPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74AQPWRQ1.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74AQ
SN74LVC74AWBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74Q
SN74LVC74AWBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF SN74LVC74A-Q1:

Catalog: SN74LVC74A

Enhanced Product: SN74LVC74A-EP

Military: SN54LVC74A

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC74ADRQ1	SOIC	D	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74LVC74AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74AWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1



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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC74ADRQ1	SOIC	D	14	3000	340.5	336.1	32.0
SN74LVC74AQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC74AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC74AWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

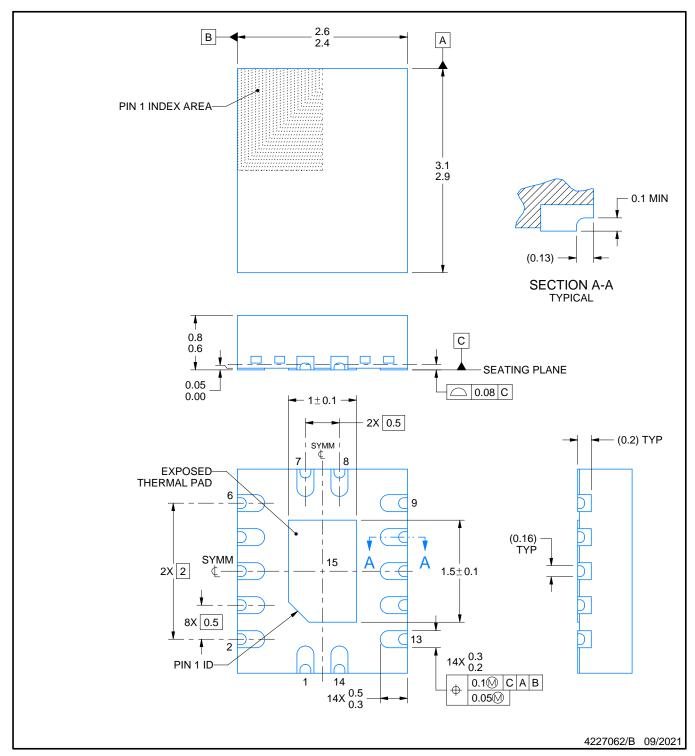
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD

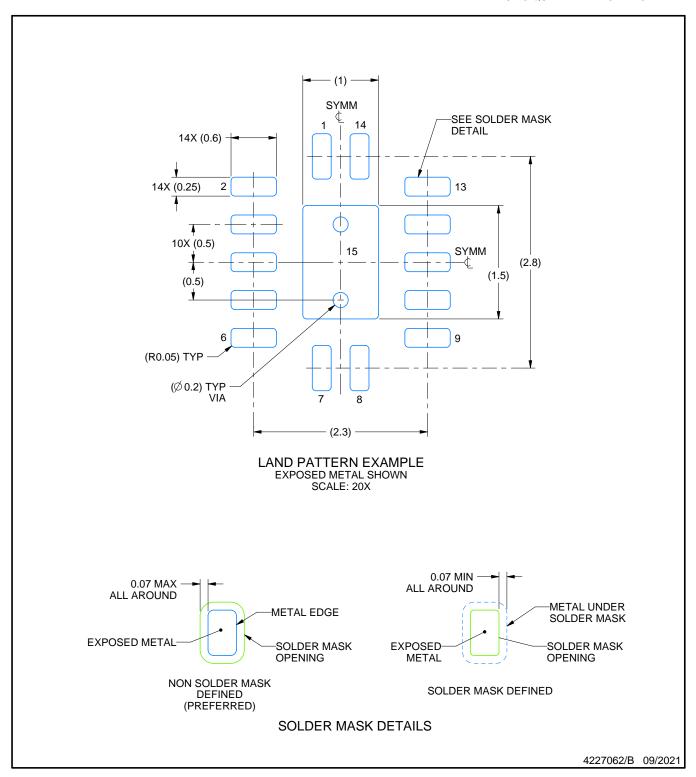


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

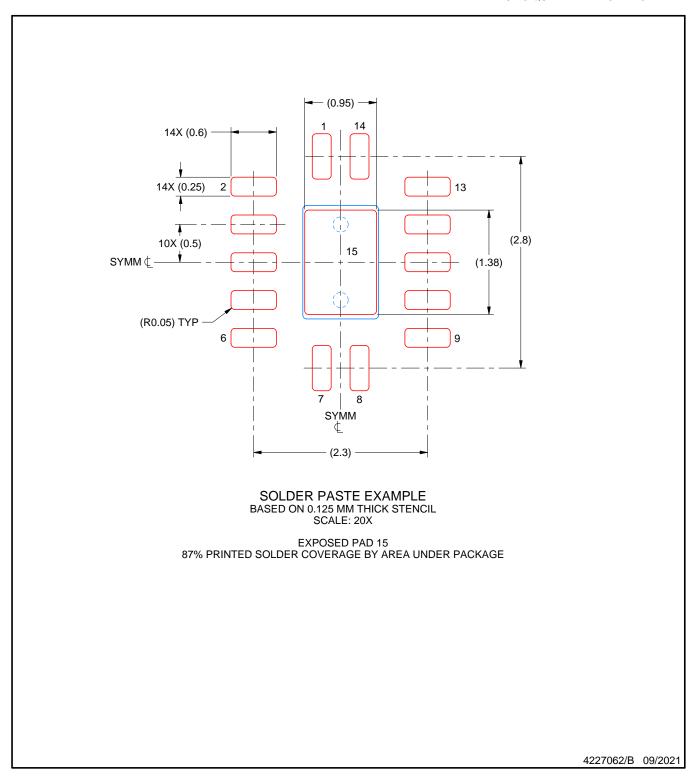


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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