SN74LVC7266A-Q1 Automotive Quad 2-Input XNOR Gates

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in wettable flank QFN (WBQA) package
- Operating range from 1.1V to 3.6V
- 5.5V tolerant input pins
- Supports standard pinouts
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Combining power good signals
- Enable digital signals

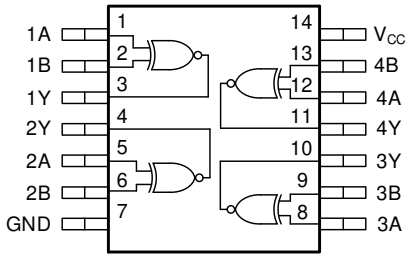
3 Description

The SN74LVC7266A-Q1 contains four independent 2-input XNOR gates. Each gate performs the Boolean function $Y = \overline{A \oplus B}$ in positive logic.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
SN74LVC7266A-Q1	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram

Table of Contents

4 Pin Configuration and Functions

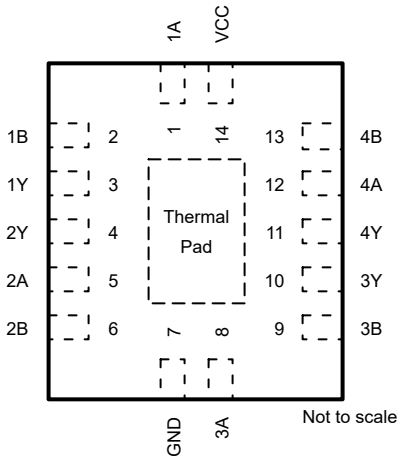


Figure 4-1. SN74LVC7266A-Q1 BQA Package, 14-Pin WQFN (Top View)

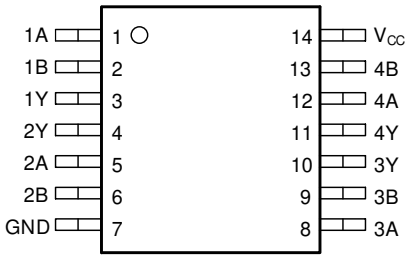


Figure 4-2. SN74LVC7266A-Q1 PW Package, 14-Pin TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
1Y	3	O	Channel 1, Output Y
2Y	4	O	Channel 2, Output Y
2A	5	I	Channel 2, Input A
2B	6	I	Channel 2, Input B
GND	7	—	Ground
3A	8	I	Channel 3, Input A
3B	9	I	Channel 3, Input B
3Y	10	O	Channel 3, Output Y
4Y	11	O	Channel 4, Output Y
4A	12	I	Channel 4, Input A
4B	13	I	Channel 4, Input B
V_{CC}	14	—	Positive Supply
Thermal Information[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = input, O = output
(2) For BQA package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	3.6	V
V_I	Input voltage			5.5	V
V_O	Output voltage	(High or low state)		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8V		-4	mA
		V_{CC} = 2.3V		-8	
		V_{CC} = 2.7V		-12	
		V_{CC} = 3V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.8V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 2.7V		12	
		V_{CC} = 3V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	125	°C
V_{IH}	High-level input voltage	V_{CC} = 1.1V	0.75		V
V_{IH}	High-level input voltage	V_{CC} = 1.5V	0.975		V
V_{IH}	High-level input voltage	V_{CC} = 1.65V	1.075		V
V_{IH}	High-level input voltage	V_{CC} = 1.95V	1.2675		V
V_{IH}	High-level input voltage	V_{CC} = 2.3V	1.7		V

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{IH}	High-level input voltage	V_{CC} = 2.7V	1.7		V
V_{IH}	High-level input voltage	V_{CC} = 3.6V	2		V
V_{IL}	Low-Level input voltage	V_{CC} = 1.1V		0.40	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.5V		0.525	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.65V		0.5775	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.95V		0.6825	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.3V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.7V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 3.6V		0.8	V

5.4 Thermal Information

THERMAL METRIC[1]		Package Options		UNIT
		PW (TSSOP)	BQA (WQFN)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150.8	102.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.3	96.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.8	70.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	24.7	16.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	93.2	70.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	50.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH}= –100µA	1.1V to 3.6V	V_{CC} - 0.2			V
V_{OH}	I_{OH}= –4mA	1.65V	1.2			V
V_{OH}	I_{OH}= –8mA	2.3V	1.75			V
V_{OH}	I_{OH}= –12mA	2.7V	2.2			V
V_{OH}		3V	2.4			V
V_{OH}	I_{OH}= –24mA	3V	2.2			V
V_{OL}	I_{OH}= 100µA	1.1V to 3.6V			0.15	V
V_{OL}	I_{OH}= 4mA	1.65V			0.45	V
V_{OL}	I_{OH}= 8mA	2.3V			0.7	V
V_{OL}	I_{OH}= 12mA	2.7V			0.4	V
V_{OL}	I_{OH}= 24mA	3V			0.55	V
I_I	V_I = V_{CC} or GND	3.6V			±5	µA
I_{off}	V_I or V_O = V_{CC}	0V			±10	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6V			40	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	2.7V to 3.6V			500	µA
C_I	V_I = V_{CC} or GND	3.3V				pF

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
C_O	V_O = V_{CC} or GND	3.3V				pF
C_{PD}	f = 10MHz	1.8V		31		pF
C_{PD}	f = 10MHz	2.5V		31		pF
C_{PD}	f = 10MHz	3.3V		32		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	A or B	Y	C_L = 15 pF	1.2V ± 0.1V		12	44	ns
t_{pd}	A or B	Y	C_L = 15 pF	1.5V ± 0.12V		9	15	ns
t_{pd}	A or B	Y	C_L = 30 pF	1.8V ± 0.15V			10.2	ns
t_{pd}	A or B	Y	C_L = 30 pF	2.5V ± 0.2V			6.9	ns
t_{pd}	A or B	Y	C_L = 50 pF	2.7V			6.4	ns
t_{pd}	A or B	Y	C_L = 50 pF	3.3V ± 0.3V			5.6	ns
$t_{sk(o)}$				3.3V ± 0.3V			1.5	ns

5.7 Noise Characteristics

VCC = 3.3V, CL = 50 pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	2.2	3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.0			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

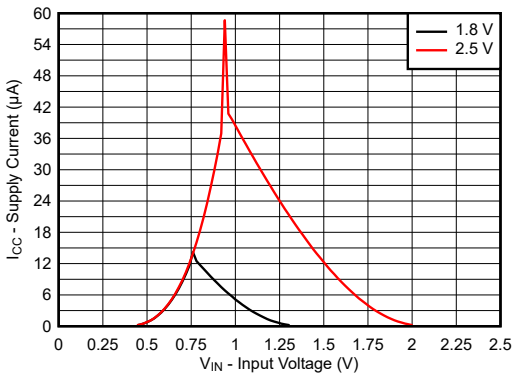


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

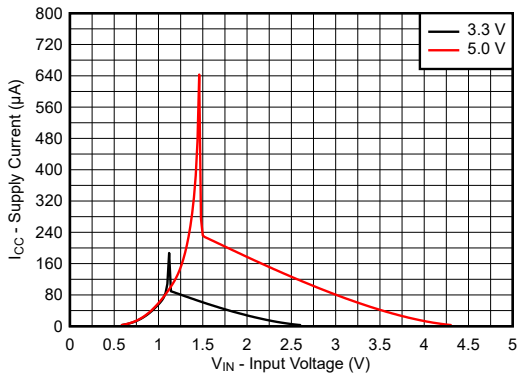


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

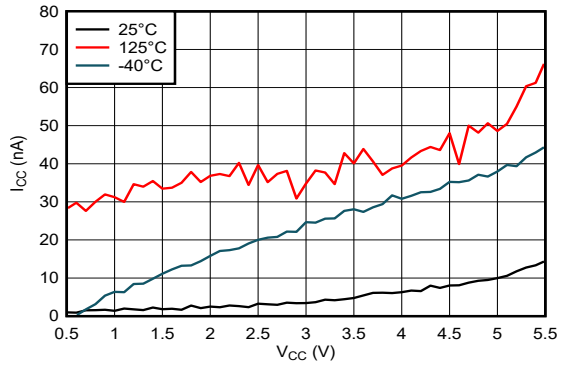


Figure 5-3. Supply Current Across Supply Voltage

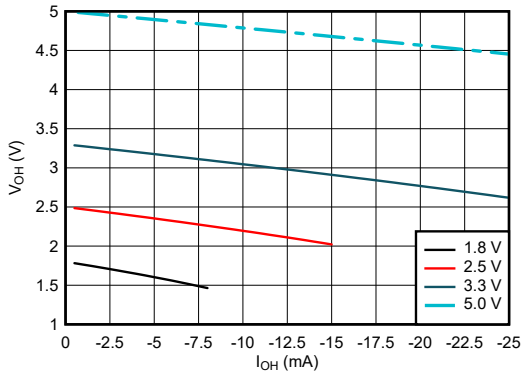


Figure 5-4. Output Voltage vs Current in HIGH State

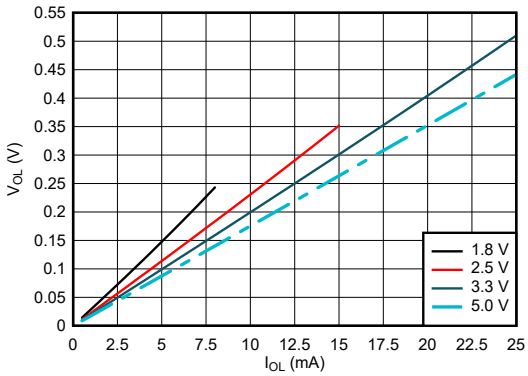


Figure 5-5. Output Voltage vs Current in LOW State

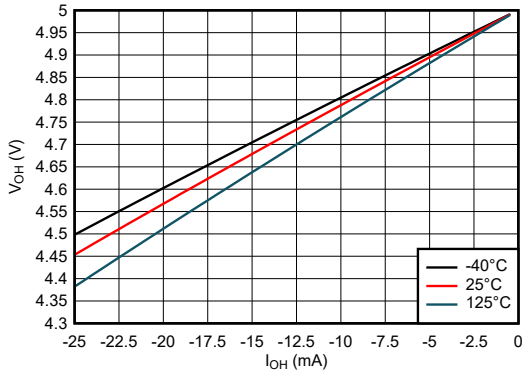


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

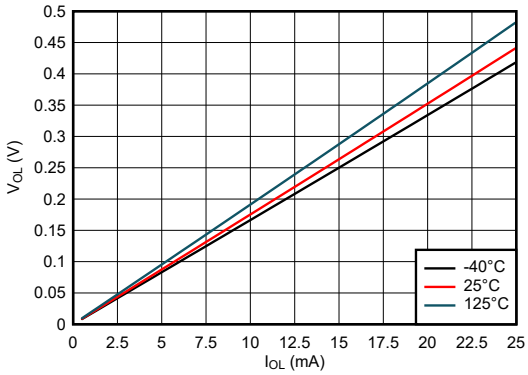


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

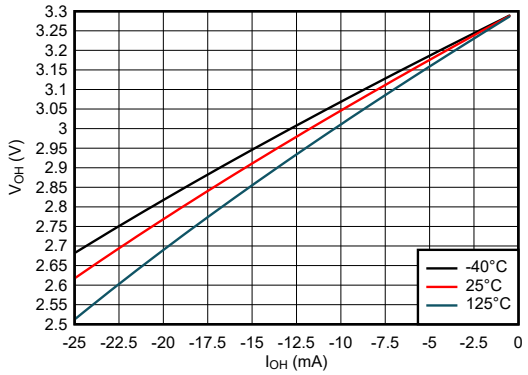


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

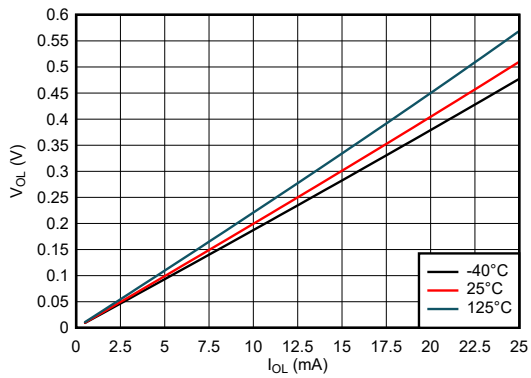


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

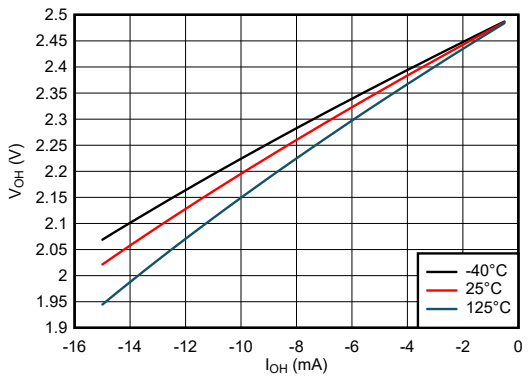


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

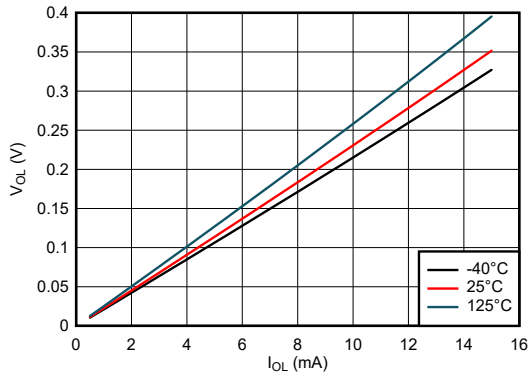


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

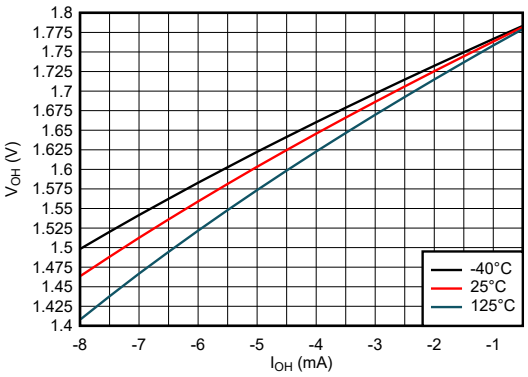


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

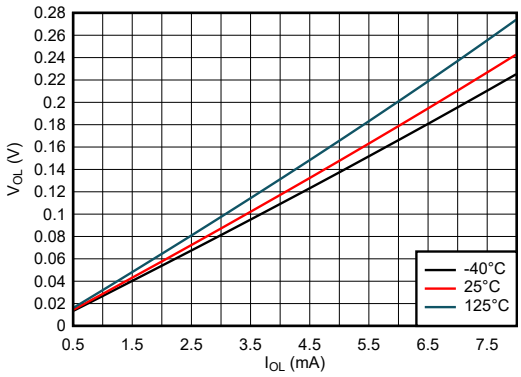


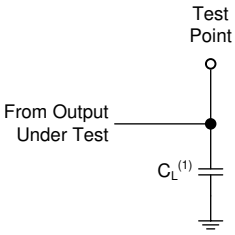
Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω.

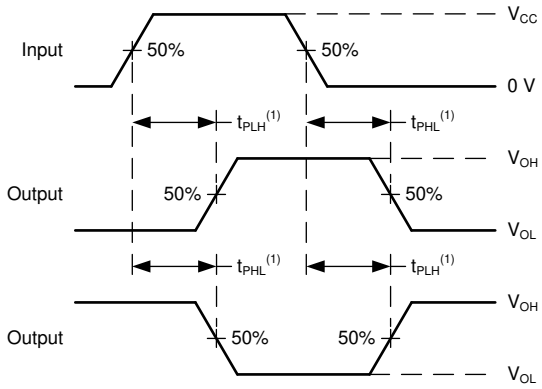
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



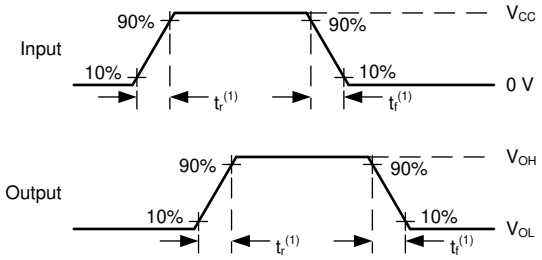
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

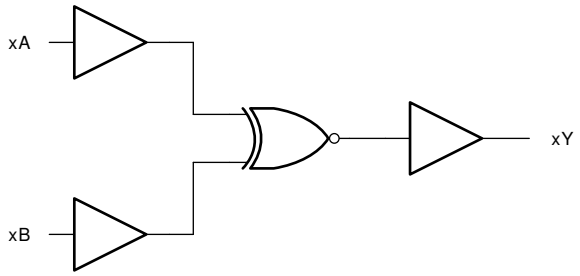
Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

This device contains four independent 2-input XNOR gates. Each gate performs the Boolean function $Y = \overline{A \oplus B}$ in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74LVC7266A-Q1 can drive a load with a total capacitance less than or equal to the maximum load listed in the *Switching Characteristics* connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *Absolute Maximum Ratings*.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.3 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

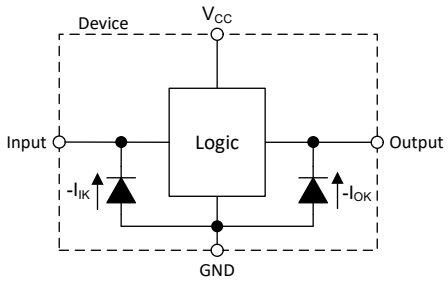


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

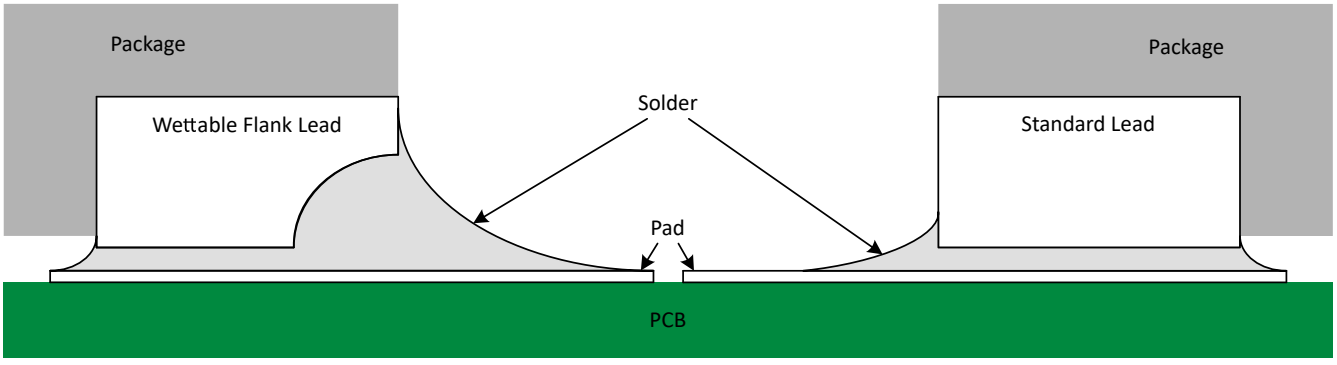


Figure 7-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, a 2-input XNOR gate is used as a phase difference detector as shown in *Figure 8-1*. The remaining three gates can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

The device is used to identify phase difference between a reference clock and another input clock. Whenever the clock states are different, the XNOR output will pulse HIGH until the clocks return to the same state. The output is fed into a low-pass filter to obtain a DC representation of the phase difference.

8.2 Typical Application

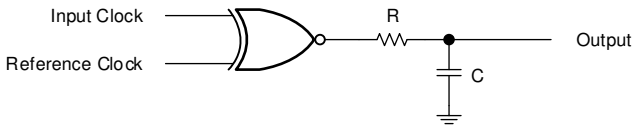


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC7266A-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *Absolute Maximum Ratings*.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{pd} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, T_J(max) listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross V_{t-}(min) to be considered a logic LOW, and V_{t+}(max) to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings* .

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the

SN74LVC7266A-Q1, as specified in the *Electrical Characteristics* , and the desired input transition rate. A 10kΩ resistor value is often used due to these factors.

The SN74LVC7266A-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the ΔV_T(min) in the *Electrical Characteristics* . This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to *Section 7.3* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Section 7.3* for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Section 8.4*.
2. Ensure the capacitive load at the output is ≤ 70pF. This is not a hard limit; however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC7266A-Q1 to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / I_O(max)) Ω. This will not violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

8.2.3 Application Curves

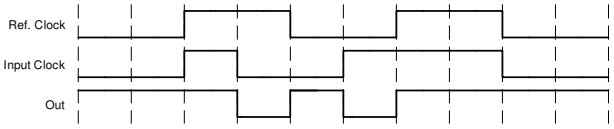


Figure 8-2. Typical Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Figure 8-3*.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

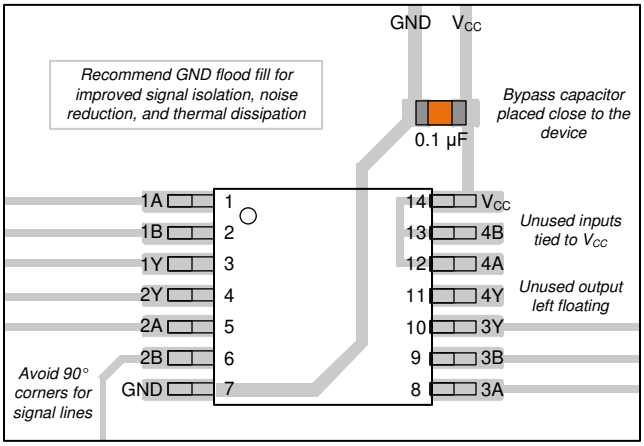


Figure 8-3. Example Layout for the SN74LVC7266A-Q1

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Introduction to Logic* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
March 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CLVC7266AWBQARQ1	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC726Q
CLVC7266AWBQARQ1.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC726Q
SN74LVC7266APWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC7266Q
SN74LVC7266APWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC7266Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC7266A-Q1 :

- Catalog : SN74LVC7266A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

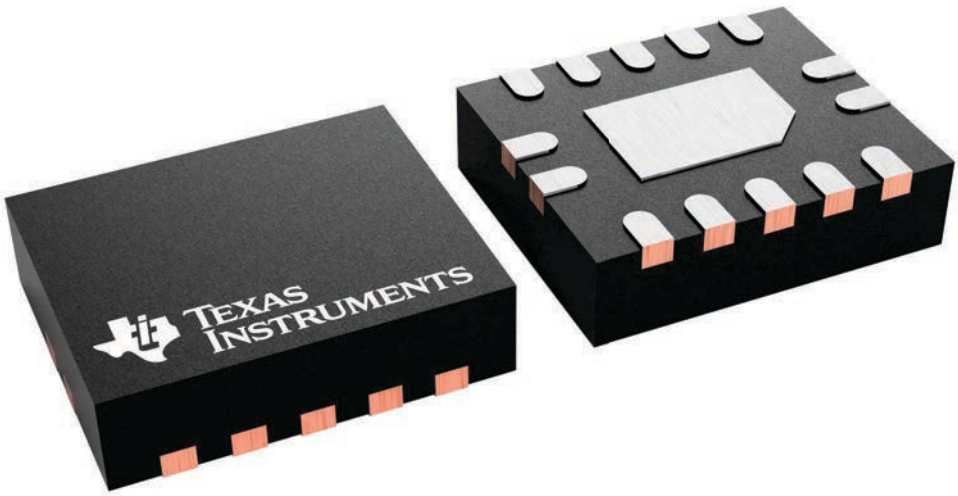
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

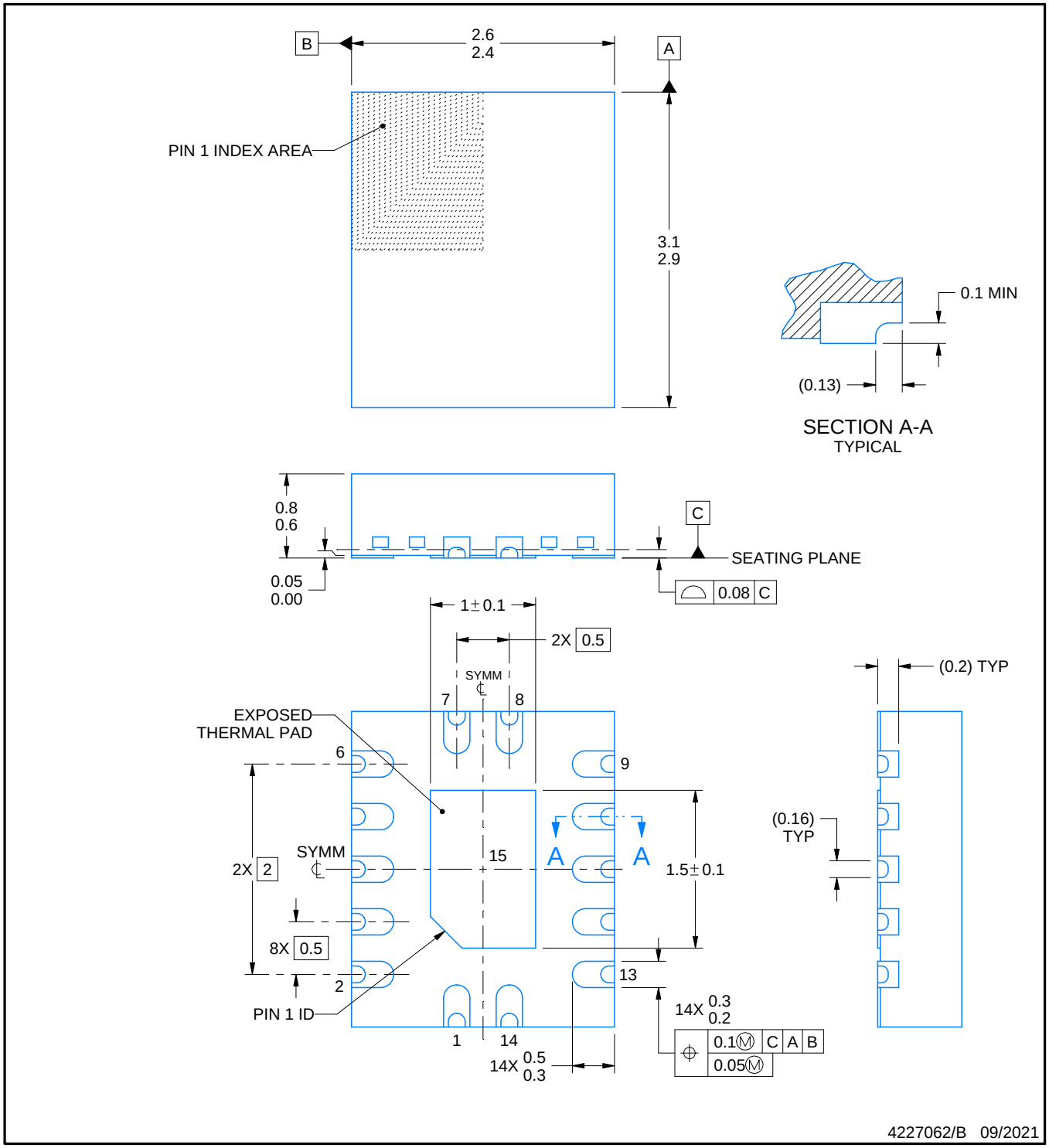


BQA0014B

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

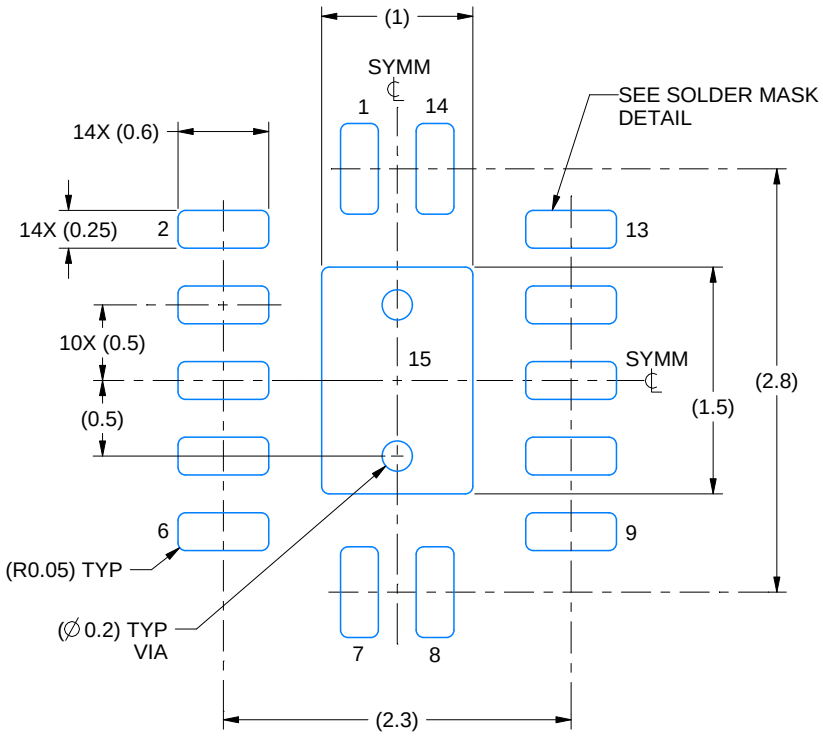
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

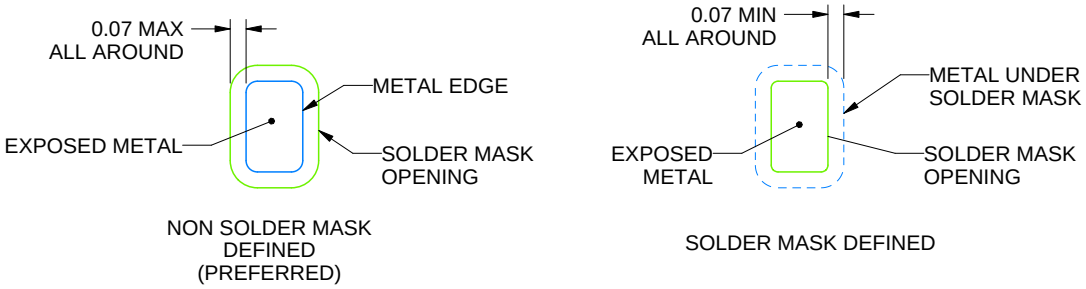
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

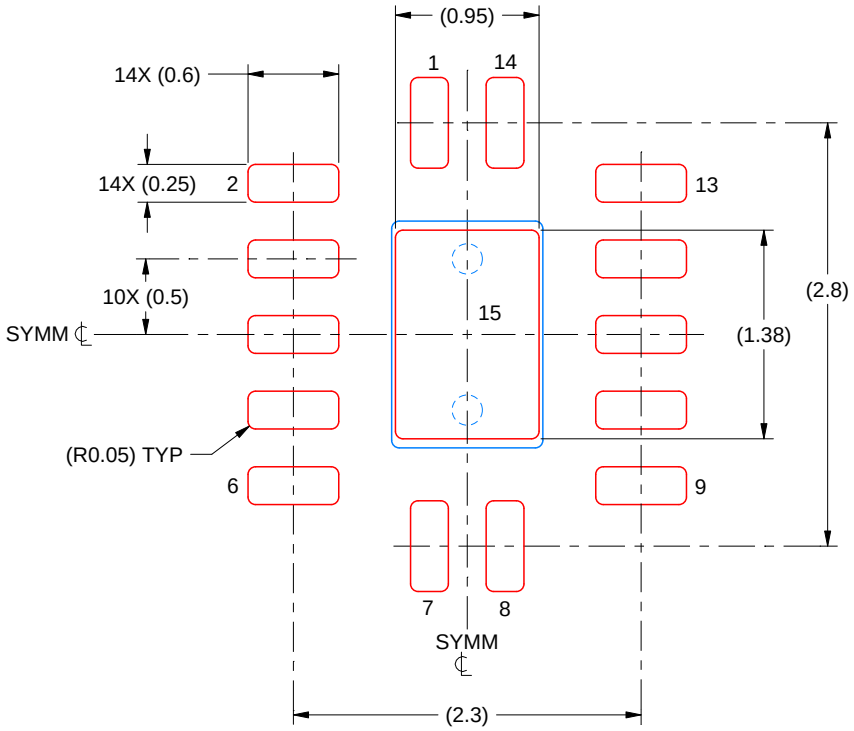


SOLDER MASK DETAILS

4227062/B 09/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

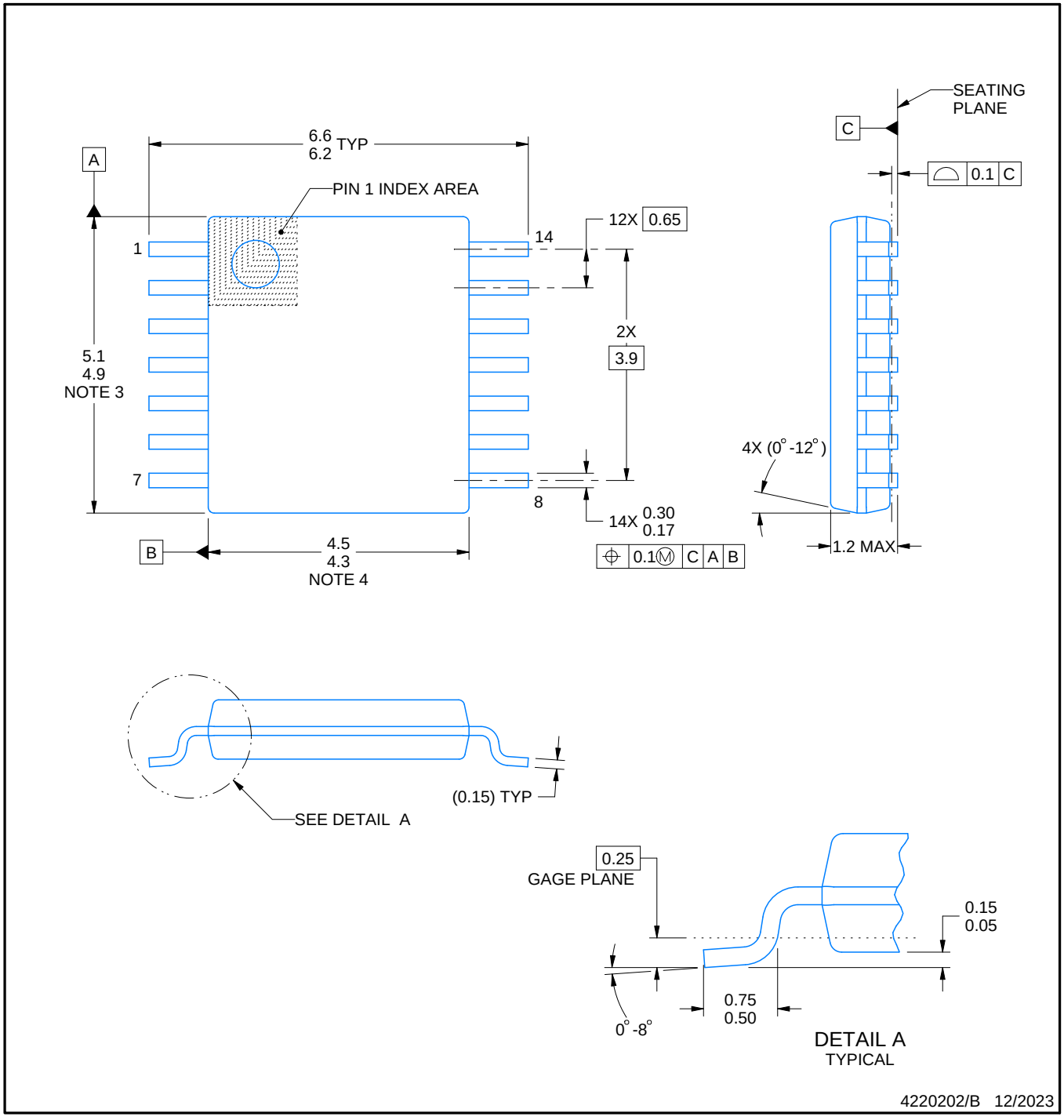
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

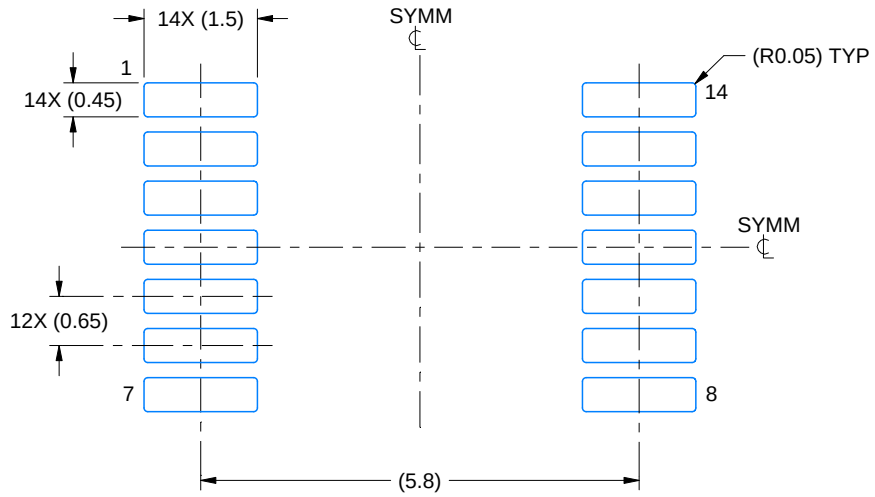
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

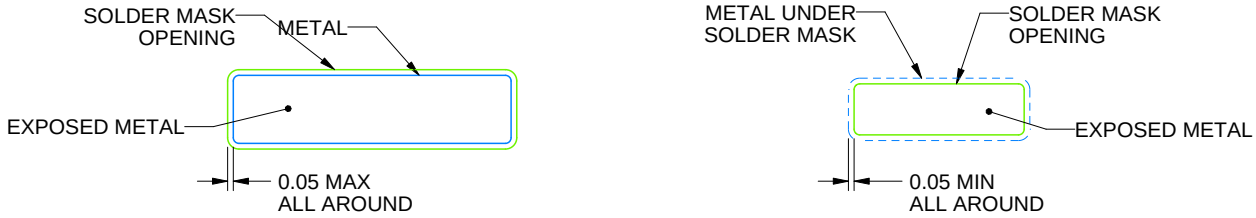


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

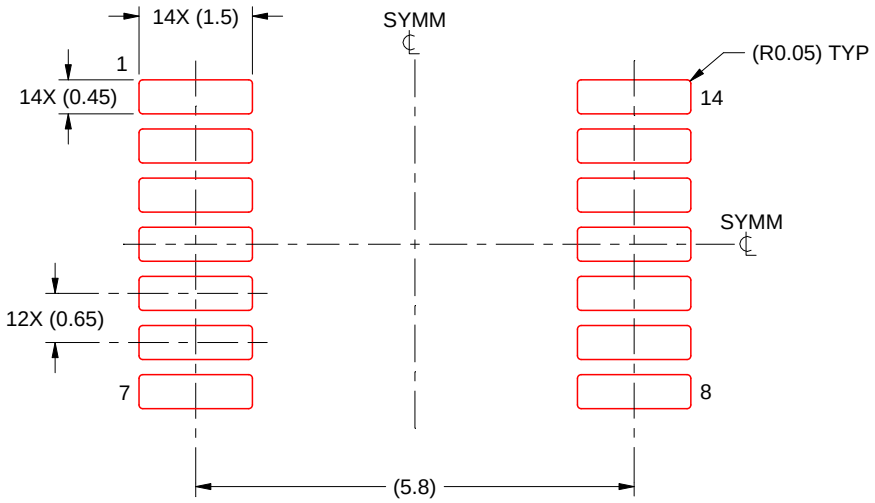


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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