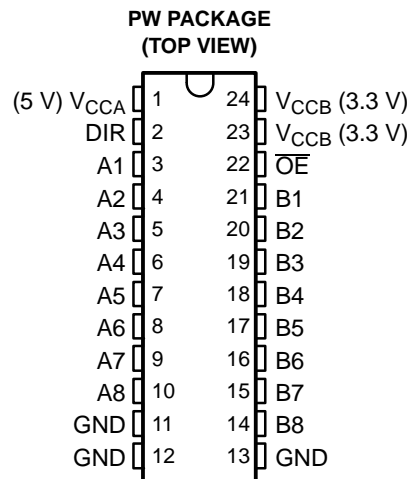


FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
 - **Enhanced Diminishing Manufacturing Sources (DMS) Support**
 - **Enhanced Product-Change Notification**
 - **Qualification Pedigree ⁽¹⁾**
 - **Bidirectional Voltage Translator**
 - **5.5 V on A Port and 2.7 V to 3.6 V on B Port**
 - **Latch-Up Performance Exceeds 250 mA Per JESD 17**
 - **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



DESCRIPTION/ORDERING INFORMATION

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 3.3 V, and A port has V_{CCA}, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The SN74LVC4245A pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional '245 pinout.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW Reel of 2000	SN74LVC4245AIPWREP	C4245AEP

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

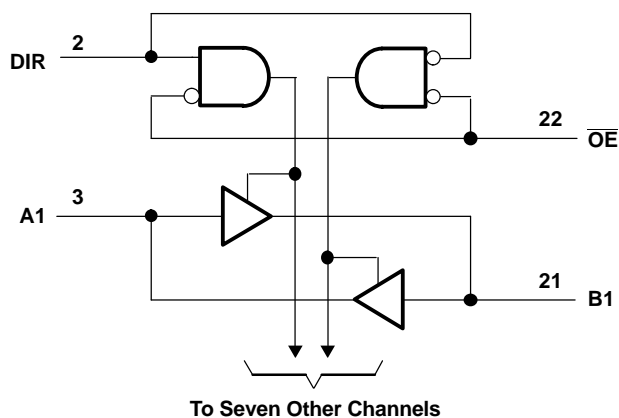
SN74LVC4245A-EP
OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER
WITH 3-STATE OUTPUTS

SCAS742–DECEMBER 2003–REVISED AUGUST 2005

FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

 over operating free-air temperature range for $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$ (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range	A port ⁽²⁾	-0.5	$V_{CCA} + 0.5$	V
		Control inputs	-0.5	6	
V_O	Output voltage range	A port ⁽²⁾	-0.5	$V_{CCA} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA} or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽³⁾			88	°C/W
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 6 V maximum.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Absolute Maximum Ratings⁽¹⁾

 over operating free-air temperature range for $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$ (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range	B port ⁽²⁾	-0.5	$V_{CCB} + 0.5$	V
V_O	Output voltage range	B port ⁽²⁾	-0.5	$V_{CCB} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCB} or GND			±100	mA
θ_{JA}	Package thermal impedance ⁽³⁾			88	°C/W
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 4.6 V maximum.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC4245A-EP

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS742–DECEMBER 2003–REVISED AUGUST 2005

Recommended Operating Conditions⁽¹⁾

for $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CCA}	V
V_O	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions⁽¹⁾

for $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CCB} = 2.7\text{ V to }3.6\text{ V}$	2		V
V_{IL}	Low-level input voltage	$V_{CCB} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
V_I	Input voltage		0	V_{CCB}	V
V_O	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	$V_{CCB} = 2.7\text{ V}$		-12	mA
		$V_{CCB} = 3\text{ V}$		-24	
I_{OL}	Low-level output current	$V_{CCB} = 2.7\text{ V}$		12	mA
		$V_{CCB} = 3\text{ V}$		24	
T_A	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics⁽¹⁾

 over recommended operating free-air temperature range for $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu\text{A}$	4.5 V	4.3			V
			5.5 V	5.3			
		$I_{OH} = -24\ \text{mA}$	4.5 V	3.7			
			5.5 V	4.7			
V_{OL}		$I_{OL} = 100\ \mu\text{A}$	4.5 V			0.2	V
			5.5 V			0.2	
		$I_{OL} = 24\ \text{mA}$	4.5 V			0.55	
			5.5 V			0.55	
I_i	Control inputs	$V_i = V_{CCA}$ or GND	5.5 V			± 1	μA
$I_{OZ}^{(3)}$	A port	$V_O = V_{CCA}$ or GND	5.5 V			± 5	μA
I_{CCA}		$V_i = V_{CCA}$ or GND, $I_O = 0$	5.5 V			80	μA
$\Delta I_{CCA}^{(4)}$		One input at 3.4 V, Other inputs at V_{CCA} or GND	5.5 V			1.5	mA
C_i	Control inputs	$V_i = V_{CCA}$ or GND	Open		5		pF
C_{iO}	A port	$V_O = V_{CCA}$ or GND	5 V		11		pF

 (1) $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$

 (2) All typical values are measured at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

 (3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

 (4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC} .

Electrical Characteristics⁽¹⁾

 over recommended operating free-air temperature range for $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCB}	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu\text{A}$	2.7 V to 3.6 V	$V_{CC} - 0.2$			V
			2.7 V	2.2			
		$I_{OH} = -12\ \text{mA}$	3 V	2.4			
			3 V	2			
V_{OL}		$I_{OL} = 100\ \mu\text{A}$	2.7 V to 3.6 V			0.2	V
		$I_{OL} = 12\ \text{mA}$	2.7 V			0.4	
		$I_{OL} = 24\ \text{mA}$	3 V			0.55	
$I_{OZ}^{(3)}$	B port	$V_O = V_{CCB}$ or GND	3.6 V			± 5	μA
I_{CCB}		$V_i = V_{CCB}$ or GND, $I_O = 0$	3.6 V			50	μA
$\Delta I_{CCB}^{(4)}$		One input at $V_{CCB} - 0.6\text{ V}$, Other inputs at V_{CCB} or GND	2.7 V to 3.6 V			0.5	mA
C_{iO}	B port	$V_O = V_{CCB}$ or GND	3.3 V		11		pF

 (1) $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$

 (2) All typical values are measured at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

 (3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

 (4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC} .

SN74LVC4245A-EP

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS742–DECEMBER 2003–REVISED AUGUST 2005

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$, $V_{CCB} = 2.7\text{ V to } 3.6\text{ V}$		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	\overline{OE}	A	1	9	ns
t_{PZH}			1	8.1	
t_{PZL}	\overline{OE}	B	1	8.8	ns
t_{PZH}			1	9.8	
t_{PLZ}	\overline{OE}	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	\overline{OE}	B	1	7.7	ns
t_{PHZ}			1	7.8	

Operating Characteristics

$V_{CCA} = 4.5\text{ V to } 5.5\text{ V}$, $V_{CCB} = 2.7\text{ V to } 3.6\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	$C_L = 0$, $f = 10\text{ MHz}$	39.5	pF
			5	

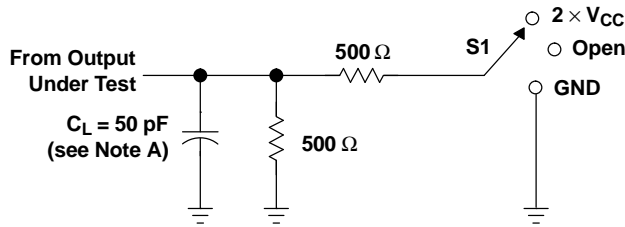
Power-up Considerations⁽¹⁾

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.

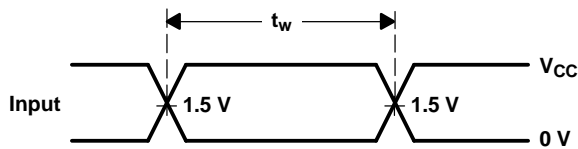
(1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

PARAMETER MEASUREMENT INFORMATION
A PORT

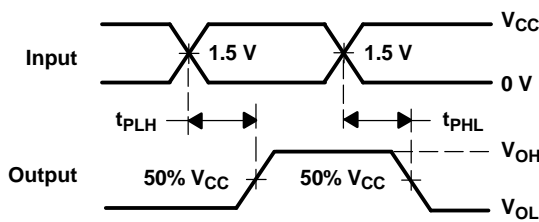


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

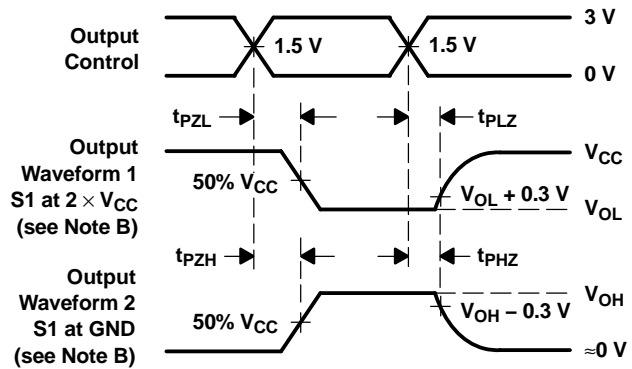
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

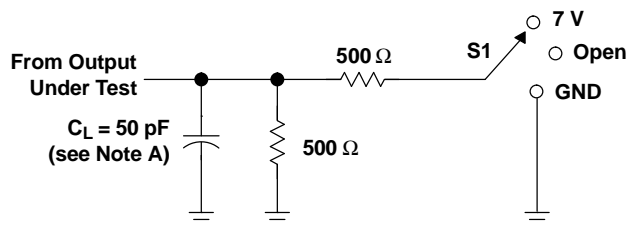


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

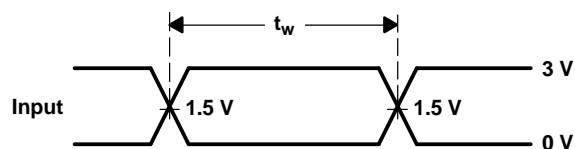
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 B PORT

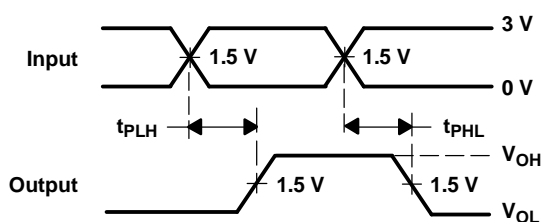


LOAD CIRCUIT

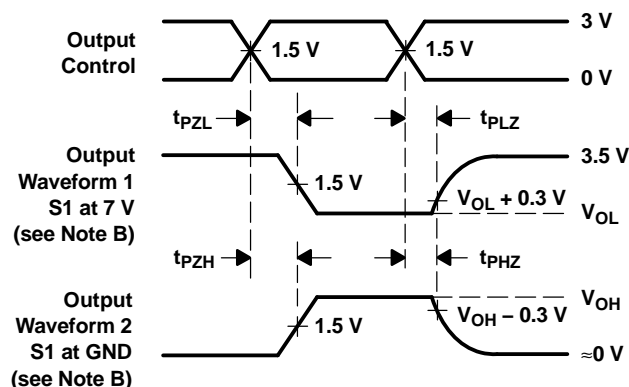
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC4245AIPWREP	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C4245AEP
V62/04664-01XE	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C4245AEP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC4245A-EP :

- Catalog : [SN74LVC4245A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC4245AIPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC4245AIPWREP	TSSOP	PW	24	2000	353.0	353.0	32.0

PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

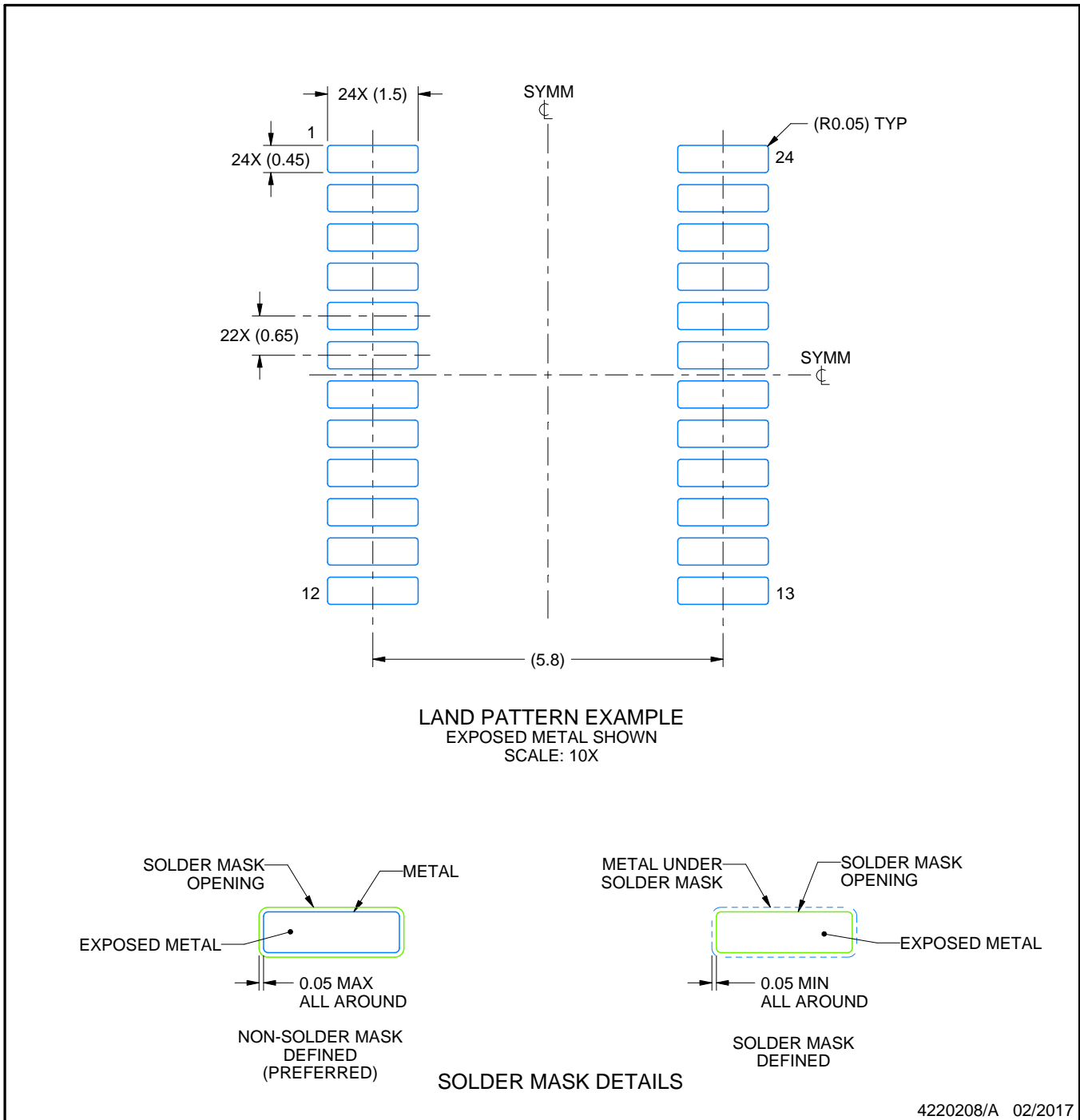
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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