











SN74LVC3G34

SCES366L - AUGUST 2001-REVISED OCTOBER 2015

SN74LVC3G34 Triple Buffer Gate

Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.1 ns at 3.3 V
- Low Power Consumption, 10-µA Maximum I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Maximum of 5.5 V Down to the V_{CC}
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- **AV Receivers**
- Audio Docks: Portable
- Blu-ray Players and Home Theaters
- **DVD Recorders and Players**
- **Embedded PCs**
- MP3 Players and Recorders (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid-State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Servers
- Wireless Headsets, Keyboards, and Mice

3 Description

The SN74LVC3G34 device is a triple buffer gate designed for 1.65-V to 5.5-V V_{CC} operation. The SN74LVC3G34 device performs the Boolean function Y = A in positive logic.

NanoFree package technology is breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC3G34DCT	SM8 (8)	2.95 mm × 2.80 mm
SN74LVC3G34DCU	VSSOP (8)	2.30 mm × 2.00 mm
SN74LVC3G34YZP	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

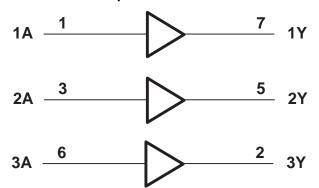






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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	hanges from Revision J (Feburary 2007) to Revision K	Page
•	Updated document to new TI data sheet format	1
•	Removed Ordering Information table.	1
•	Updated Features section	1
•	Updated operating temperature range.	4

Changes from Revision K (November 2013) to Revision L

Page

- Added Applications, Device Information table, Pin Configuration and Functions section, ESD Ratings table, Thermal
 Information table, Typical Characteristics section, Feature Description section, Device Functional Modes,
 Application and Implementation section, Power Supply Recommendations section, Layout section, Device and
 Documentation Support section, and Mechanical, Packaging, and Orderable Information section
- Deleted part number from Switching Characteristics table headers.

 5



Pin Configuration and Functions



YZP Package 8-Pin DSBGA **Bottom View**

GND	0450	2Y
2A	O3 6O	ЗА
3Y	0270	1Y
1A	0180	Vcc

Pin Functions⁽¹⁾

PIN		1/0	DECORPTION	
NAME	NO.	- I/O	DESCRIPTION	
1A	1	1	Buffer Input 1	
1Y	7	0	Buffer Output 1	
2A	3	1	Buffer Input 2	
2Y	5	0	Buffer Output 2	
3A	6	1	Buffer Input 3	
3Y	2	0	Buffer Output 3	
GND	4	_	Ground pin	
V _{CC}	8	_	Power pin	

⁽¹⁾ See mechanical drawings for dimensions

Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	6.5	V
VI	Input voltage ⁽²⁾		-0.5	6.5	V
Vo	Voltage applied to any output in the high-impedance or power-off state (2)		-0.5	6.5	V
Vo	Voltage applied to any output in the	e high or low state (2)(3)	-0.5	$V_{CC} + 0.5$	V
I _{IK}	Input clamp current	V _I < 0		- 50	mA
I _{OK}	Output clamp current	V _O < 0		- 50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or	GND		±100	mA
TJ	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Product Folder Links: SN74LVC3G34

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The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

The value of V_{CC} is provided in the *Recommended Operating Conditions* table.



6.2 ESD Ratings

				VALUE	UNIT	
Floatroatatio	Electrostatio	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2500			
	V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	1500	V	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
V	Cupaly voltage	Operating	1.65	5.5	V	
v _{CC}	Supply voltage	Data retention only	1.5		V	
Vo		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
.,	High lavel input valtage	V _{CC} = 2.3 V to 2.7 V	1.7		V	
VIH	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		·	
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
.,	Lavo laval Sanatorika na	V _{CC} = 2.3 V to 2.7 V		0.7	.,	
VIL	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}		
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
	High-level output current	V _{CC} = 1.65 V		-4		
		V _{CC} = 2.3 V		-8		
I _{OH}		V _{CC} = 3 V		-16	mA	
		VCC = 3 V		-24	·	
		V _{CC} = 4.5 V		-32		
		V _{CC} = 1.65 V		4		
		V _{CC} = 2.3 V		8		
I _{OL}	Low-level output current	V 0V		16	mA	
		V _{CC} = 3 V		24		
		V _{CC} = 4.5 V		32		
		V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20		
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V	
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5	•	
_	On another free printers and	DCT, DCU Package	-40	125	00	
T _A	Operating free-air temperature	YZP Package	-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.

6.4 Thermal Information

			SN74LVC3G34		
THERMAL METRIC ⁽¹⁾		DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)	UNIT
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	227	140	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.



6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	NDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	AX	UNIT
	I _{OH} = -100 μA	$I_{OH} = -100 \mu A$		V _{CC} - 0.1			
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
	$I_{OH} = -8 \text{ mA}$		2.3 V	1.9			
V_{OH}	I _{OH} = -16 mA		3 V	2.4			V
	I _{OH} = -24 mA		3 V	2.3			
	$I_{OH} = -32 \text{ mA}$		4.5 V	3.8			
	I _{OL} = 100 μA		1.65 V to 5.5 V			0.1	
	I _{OL} = 4 mA		1.65 V		(.45	
	I _{OL} = 8 mA		2.3 V			0.3	
	I _{OL} = 16 mA	O _L = 16 mA				0.4	
V_{OL}	1 24 mA	T _A = -40°C to 85°C	3 V		(.55	V
	I _{OL} = 24 mA	T _A = -40°C to 125°C	3 V		(.75	
		T _A = -40°C to 85°C	4574		(.55	
	I _{OL} = 32 mA	$T_A = -40^{\circ}\text{C} \text{ to}$ 125°C	4.5 V		(.75	
I _I A inputs	V _I = 5.5 V or GND	·	0 to 5.5 V			±5	μA
I _{off}	V_I or $V_O = 5.5 \text{ V}$		0			±10	μA
I _{cc}	$V_I = 5.5 \text{ V or GND},$	I _O = 0	1.65 V to 5.5 V			10	μA
ΔI _{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 5.5 V			500	μΑ
C _I	V _I = V _{CC} or GND	T _A = -40°C to 85°C	3.3 V		3.5		pF

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OPERATING FREE-AIR TEMPERATURE (T _A)	V _{cc}	MIN	MAX	UNIT	
				$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	3.2	7.9		
	A Y	V	Y —40°C to 85°C	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.5	4.4	no	
t _{pd}		r		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.4	4.1	ns	
				$V_{CC} = 5 V \pm 0.5 V$	1.1	3.2		
	A Y				$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	3.2	8.9	
		A Y	-40°C to 125°C	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.5	5.4	ns	
t _{pd}				$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.4	5.1		
				$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	1.1	3.8		

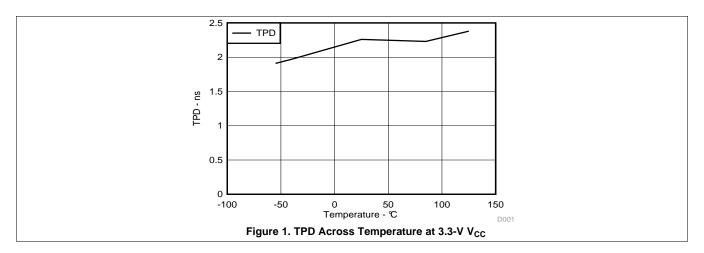
6.7 Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{cc}	TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	V _{CC} = 1.8 V	19	_
			V _{CC} = 2.5 V	19	
			V _{CC} = 3.3 V	19	pF
			V _{CC} = 5 V	21	

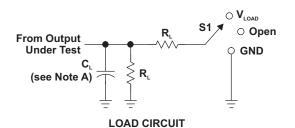


6.8 Typical Characteristics



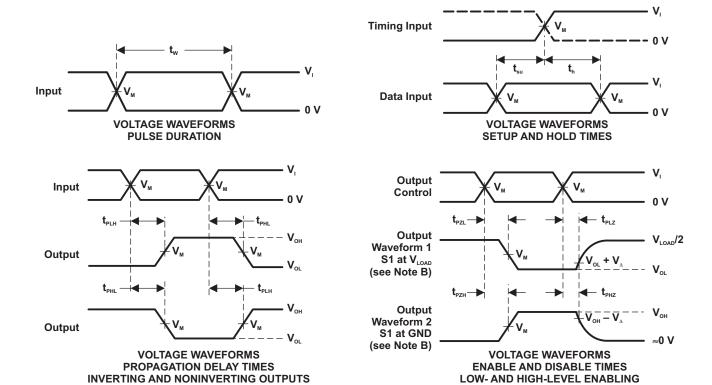


7 Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

INPUTS			V		-	.,		
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	$R_{\scriptscriptstyle L}$	V _A	
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V	
2.5 V ± 0.2 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V	
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V	



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{\circ} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\mbox{\tiny PLZ}}$ and $t_{\mbox{\tiny PHZ}}$ are the same as $t_{\mbox{\tiny dis}}.$
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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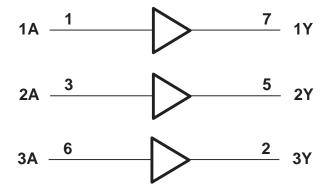


8 Detailed Description

8.1 Overview

The SN74LVC3G34 device contains three buffer gates that each perform the Boolean function Y = A. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

The SN74LVC3G34 device has a wider operating voltage range, operating from 1.65 V to 5.5 V, and allows down voltage translation. The SN74LVC3G34 I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC3G34.

Table 1. Function Table

INPUT A	OUTPUT Y
Н	Н
L	L

Product Folder Links: SN74LVC3G34

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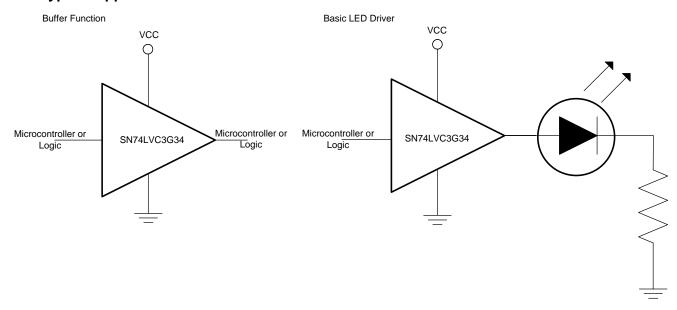


9 Application and Implementation

9.1 Application Information

The SN74LVC3G34 is a high-drive CMOS device that can be used as a buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V, making it ideal for driving multiple outputs and good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant, allowing it to translate down to $V_{\rm CC}$.

9.2 Typical Application



9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - Rise time and fall time specs. See $(\Delta t/\Delta V)$ in the *Recommended Operating Conditions* table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.
 - Inputs are overvoltage tolerant allowing them to go as high as (VI max) in the Recommended Operating
 Conditions table at any valid V_{CC}.

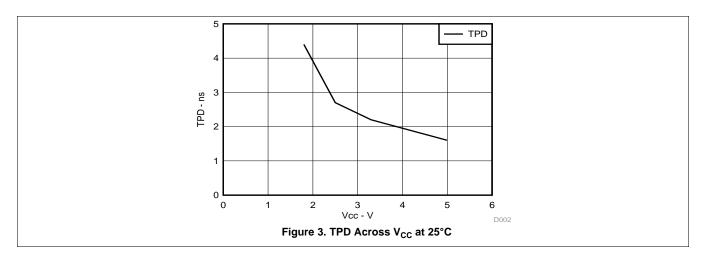
2. Recommended Output Conditions

- Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Recommended Operating Conditions* table.
- Outputs must not be pulled above V_{CC} under normal operating conditions.



Typical Application (continued)

9.2.3 Application Curve



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended and if there are multiple V_{CC} pins then a 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

11.2 Layout Example





12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Documentation Support

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC3G34DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(2X35, C34) (R, Z)
SN74LVC3G34DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2X35, C34) (R, Z)
SN74LVC3G34DCTRG4	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C34 (R, Z)
SN74LVC3G34DCTRG4.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C34 (R, Z)
SN74LVC3G34DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(34, C34J, C34Q, C 34R) (CR, CZ)
SN74LVC3G34DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(34, C34J, C34Q, C 34R) (CR, CZ)
SN74LVC3G34DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C34R
SN74LVC3G34DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C34R
SN74LVC3G34DCUT	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C34J, C34Q, C34R)
									CR
SN74LVC3G34DCUT.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C34J, C34Q, C34R)
									CR
SN74LVC3G34DCUTG4	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C34R
SN74LVC3G34DCUTG4.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C34R
SN74LVC3G34YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9N
SN74LVC3G34YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9N

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

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- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC3G34DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC3G34DCTRG4	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74LVC3G34DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC3G34DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC3G34DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC3G34DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC3G34YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC3G34DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC3G34DCTRG4	SSOP	DCT	8	3000	183.0	183.0	20.0
SN74LVC3G34DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC3G34DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC3G34DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC3G34DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC3G34YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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