

Triple Inverter Gate

Check for Samples: SN74LVC3G04

FEATURES

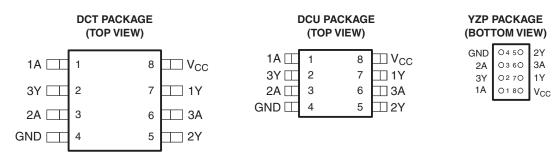
- Available in the Texas Instruments NanoFree[™] Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.1 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Max of 5.5 V Down to the V_{CC} Level
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION

This triple inverter is designed for 1.65-V to 5.5-V V_{CC} operation. The SN74LVC3G04 device performs the Boolean function $Y = \overline{A}$.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



See mechanical drawings for dimensions.

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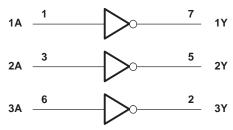


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Function Table (Each Inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

Logic Diagram (Positive Logic)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_{I}	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output whe	-0.5	6.5	V	
Vo	Voltage range applied to any output whe	-0.5	V _{CC} + 0.5	V	
I_{IK}	Input clamp current	V ₁ < 0		-50	mA
lok	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
		DCT package		220	
θ_{JA}	Package thermal impedance (4)	DCU package	227		°C/W
		YZP package		102	
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
\ /	Cumply valtage	Operating	1.65	5.5	V
V_{CC}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
.,	I Park Javan Parant and to me	V _{CC} = 2.3 V to 2.7 V	1.7		
V_{IH}	High-level input voltage	gn-ievei input voitage $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$			V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
.,	Lave lavel inner treatment	V _{CC} = 2.3 V to 2.7 V		\ /	
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
I_{OH}	High-level output current	v 2V		-16	mA
		$V_{CC} = 3 V$	-24		
		V _{CC} = 4.5 V		-32	
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
I_{OL}	Low-level output current	V 0V		16	mA
		$V_{CC} = 3 V$		24	
		V _{CC} = 4.5 V		32	<u> </u>
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5	
T _A	Operating free-air temperature		-40	125	°C
IA	Operating free-air temperature		-40	125	-(

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Product Folder Links: SN74LVC3G04



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	.,	-40°0	C to 85°C		-40°C	to 125°C	:	UNIT
PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP ⁽¹⁾ MAX		MAX	MIN	TYP ⁽¹⁾	MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.1			V _{CC} - 0.1			
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			1.2			
V _{OH}	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			1.9			V
	$I_{OH} = -16 \text{ mA}$	3 V	2.4			2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2.3			2.3			
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			3.8			
	I _{OL} = 100 μA	1.65 V to 5.5 V			0.1			0.1	
	I _{OL} = 4 mA	1.65 V			0.45			0.45	
V_{OL}	I _{OL} = 8 mA	2.3 V			0.3			0.3	V
	I _{OL} = 16 mA	3 V			0.4			0.4	
	I _{OL} = 24 mA	3 V			0.55			0.55	
	I _{OL} = 32 mA	4.5 V			0.55			0.75	
I _I A inputs	V _i = 5.5 V or GND	0 to 5.5 V			±5			±5	μΑ
I _{off}	V_I or $V_O = 5.5 \text{ V}$	0			±10			±10	μΑ
I _{cc}	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10			10	μA
ΔI _{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	μΑ
Ci	$V_1 = V_{CC}$ or GND	3.3 V		3.5					pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

						SN74LV -40°C t					
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		3.3 V V	V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Y	3.2	7.9	1.5	4.4	1.4	4.1	1.1	3.2	ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN74LVC3G04 -40°C to 125°C								
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		3.3 V V	V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	3.2	8.9	1.5	5.4	1.4	5.1	1.1	3.8	ns

Operating Characteristics

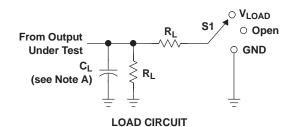
 $T_{\Delta} = 25^{\circ}C$

· A -	<u> </u>			•	•		
	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	$V_{CC} = 2.5 V$	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 V$	UNIT
	PARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNII
C_{pd}	Power dissipation capacitance	f = 10 MHz	16	16	16	18	pF

Product Folder Links: SN74LVC3G04

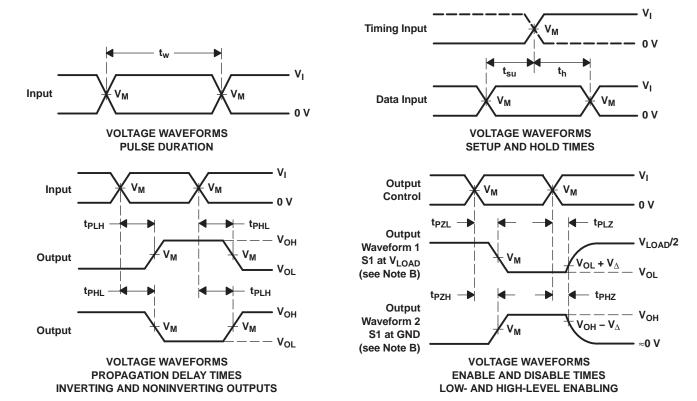


Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	INF	PUTS	.,	.,		_	v
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_{Δ}
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V_{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	V_{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Product Folder Links: SN74LVC3G04

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SCES363L - AUGUST 2001 - REVISED NOVEMBER 2013



REVISION HISTORY

CI	hanges from Revision K (May 2007) to Revision L	Page
•	Updated document to new TI data sheet format.	1
•	Removed ordering information.	1
•	Updated Features.	1
•	Added ESD warning.	2
•	Updated operating temperature range.	3

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11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC3G04DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(2WW5, C04) Z
SN74LVC3G04DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2WW5, C04) Z
SN74LVC3G04DCTRG4	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 Z
SN74LVC3G04DCTRG4.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04 Z
SN74LVC3G04DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C04J, C04Q, C04R)
SN74LVC3G04DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C04J, C04Q, C04R)
SN74LVC3G04DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04R
SN74LVC3G04DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04R
SN74LVC3G04DCUT	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C04J, C04Q, C04R)
SN74LVC3G04DCUT.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C04J, C04Q, C04R)
SN74LVC3G04YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	CCN
SN74LVC3G04YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	CCN

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION





_	<u> </u>
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC3G04DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC3G04DCTRG4	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74LVC3G04DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC3G04DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC3G04DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC3G04DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC3G04YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC3G04DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC3G04DCTRG4	SSOP	DCT	8	3000	183.0	183.0	20.0
SN74LVC3G04DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC3G04DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC3G04DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC3G04DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC3G04YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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