

# **Dual Inverter Gate**

Check for Samples: SN74LVC2GU04

## **FEATURES**

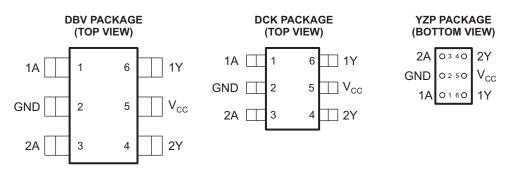
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 3.7 ns at 3.3 V
- Low Power Consumption, 10-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Max of 5.5 V Down to the V<sub>CC</sub> Level
- Unbuffered Outputs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### DESCRIPTION

This dual inverter is designed for 1.65-V to 5.5-V  $V_{\text{CC}}$  operation.

The SN74LVC2GU04 device contains two inverters with unbuffered outputs and performs the Boolean function  $Y = \overline{A}$ .

NanoFree<sup>™</sup> package technology is a major breakthrough in IC packaging concepts, using the die as the package.



See mechanical drawings for dimensions.

M

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



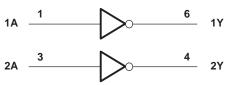


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# Function Table (Each Inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

## **Logic Diagram (Positive Logic)**



# Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	6.5	V
VI	Input voltage range <sup>(2)</sup>	-0.5	6.5	V	
Vo	Voltage range applied to any output in the hig	h or low state <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current		±50	mA	
	Continuous current through V <sub>CC</sub> or GND			±100	mA
		DBV package		165	
$\theta_{JA}$	Package thermal impedance (4)	DCK package		259	°C/W
		YZP package		123	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

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# Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT	
$V_{CC}$	Supply voltage		1.65	5.5	V	
$V_{IH}$	High-level input voltage	$I_{O} = -100 \ \mu A$	0.75 × V <sub>CC</sub>		V	
$V_{IL}$	Low-level input voltage	I <sub>O</sub> = 100 μA		0.25 × V <sub>CC</sub>	V	
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V <sub>CC</sub>	V	
		V <sub>CC</sub> = 1.65 V		-4		
		V <sub>CC</sub> = 2.3 V		-8		
$I_{OH}$	High-level output current	V 2.V		-16	mA	
		V <sub>CC</sub> = 3 V		-24		
		V <sub>CC</sub> = 4.5 V		-32		
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V	8			
$I_{OL}$	Low-level output current	V 2.V		16	mA	
		V <sub>CC</sub> = 3 V		24		
		V <sub>CC</sub> = 4.5 V		32		
T <sub>A</sub>	Operating free-air temperature		-40	125	°C	

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS		.,	-40	0°C to 85°C		-40	-40°C to 125°C		
PARAMETER	IES	I CONDITIONS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	UNIT
		Ι <sub>ΟΗ</sub> = -100 μΑ	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1			
		I <sub>OH</sub> = -4 mA	1.65 V	1.2			1.2			
$V_{OH}$	V <sub>IL</sub> = 0 V	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			1.9			V
		$I_{OH} = -16 \text{ mA}$	3 V	2.4			2.4			
		$I_{OH} = -24 \text{ mA}$	3 V	2.3			2.3			
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			3.8			
		$I_{OL} = 100 \mu A$	1.65 V to 5.5 V			0.1			0.1	
		$I_{OL} = 4 \text{ mA}$	1.65 V			0.45			0.45	V
V	V - V	$I_{OL} = 8 \text{ mA}$	2.3 V			0.3			0.3	
$V_{OL}$	$V_{IH} = V_{CC}$	$I_{OL} = 16 \text{ mA}$	3 V			0.4			0.4	V
		$I_{OL} = 24 \text{ mA}$	3 V			0.55			0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55			0.55	
I <sub>I</sub> A inputs	V <sub>I</sub> = 5.5 V or GND		0 to 5.5 V			±5			±5	μΑ
I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0		1.65 V to 5.5 V			10			10	μΑ
Cı	$V_1 = V_{CC}$ or GND		3.3 V		7					pF

<sup>(1)</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

						SN74LV -40°C t	C2GU04 to 85°C				
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		3.3 V V	V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Υ	1.2	5.5	1	4	1.1	3.7	1	3	ns

Product Folder Links: SN74LVC2GU04



# **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			`			, ,		•			
DADAMETED			SN74LVC2GU04 −40°C to 125°C								
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Υ	1.2	6.3	1	4.5	1.1	4.2	1	3.5	ns

# **Operating Characteristics**

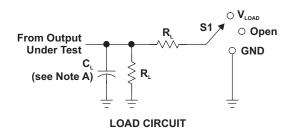
 $T_A = 25$ °C

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 V$	UNIT	
	FARAMETER	TEST CONDITIONS	TYP	TYP TYP TYP		TYP	UNII	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	7	7	8	23	pF	

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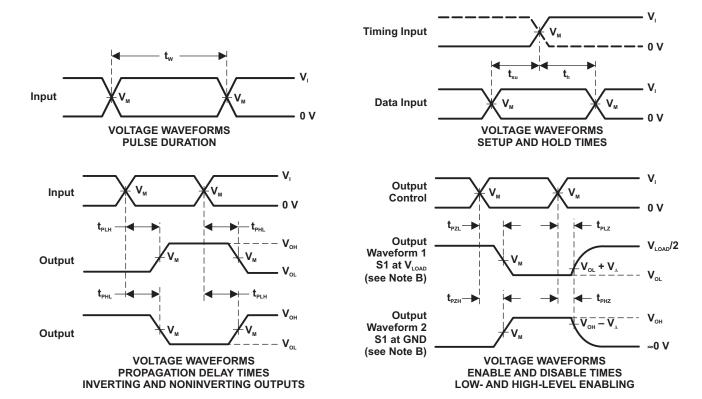


#### **Parameter Measurement Information**



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
$t_{_{\mathrm{PLZ}}}/t_{_{\mathrm{PZL}}}$	<b>V</b> <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

.,	INPUTS		.,,	v		-	.,
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>∟</sub>	$R_{\scriptscriptstyle L}$	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V ± 0.2 V	$V_{cc}$	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	500 $\Omega$	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V ± 0.5 V	$V_{cc}$	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	<b>500</b> Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o$  = 50  $\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{\mbox{\tiny PLZ}}$  and  $\dot{t}_{\mbox{\tiny PHZ}}$  are the same as  $t_{\mbox{\tiny dis}}.$
- F.  $t_{\mbox{\tiny PZL}}$  and  $t_{\mbox{\tiny PZH}}$  are the same as  $t_{\mbox{\tiny en}}.$
- G.  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  are the same as  $t_{\text{pd}}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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# SCES197N - APRIL 1999 - REVISED DECEMBER 2013



# **REVISION HISTORY**

CI	hanges from Revision M (February 2007) to Revision N	Page
•	Updated document to new TI data sheet format.	1
•	Removed ordering information.	1
•	Updated Features.	1
•	Added ESD warning.	2
•	Updated operating temperature range	3

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
74LVC2GU04DBVRG4	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CU45, CU4R)
74LVC2GU04DCKRG4	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD5
74LVC2GU04DCKRG4.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD5
74LVC2GU04DCKTG4	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD5
74LVC2GU04DCKTG4.B	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD5
SN74LVC2GU04DBVR	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CU45, CU4R)
SN74LVC2GU04DBVR.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CU45, CU4R)
SN74LVC2GU04DBVT	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CU45, CU4R)
SN74LVC2GU04DBVT.B	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CU45, CU4R)
SN74LVC2GU04DCKR	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CD5, CDF, CDJ, CD K, CDR)
SN74LVC2GU04DCKR.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CD5, CDF, CDJ, CD K, CDR)
SN74LVC2GU04DCKT	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CD5, CDF, CDJ, CD K, CDR)
SN74LVC2GU04DCKT.B	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CD5, CDF, CDJ, CD K, CDR)
SN74LVC2GU04YZPR	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CDN
SN74LVC2GU04YZPR.B	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CDN

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# **PACKAGE OPTION ADDENDUM**

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN74LVC2GU04:

Automotive: SN74LVC2GU04-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC2GU04DCKRG4	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
74LVC2GU04DCKTG4	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC2GU04DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC2GU04DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC2GU04DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC2GU04DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC2GU04DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC2GU04DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC2GU04YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



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\*All dimensions are nominal

All difficultions are norminal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC2GU04DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
74LVC2GU04DCKTG4	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC2GU04DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC2GU04DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74LVC2GU04DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC2GU04DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74LVC2GU04DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74LVC2GU04DCKT	SC70	DCK	6	250	210.0	185.0	35.0
SN74LVC2GU04YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

  4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



#### NOTES:

NanoFree Is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- 3. NanoFree<sup>™</sup> package configuration.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
 For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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