

# Single D-Type Flip-Flop With 3-State Output

Check for Samples: SN74LVC1G374

#### **FEATURES**

- Available in the Texas Instruments NanoStar<sup>™</sup> and NanoFree<sup>™</sup> Packages
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V<sub>CC</sub>
- Max t<sub>pd</sub> of 4 ns at 3.3 V
- Low Power Consumption, 10-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- I<sub>off</sub> Supports Live Insertion, Partial-Power-Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### DESCRIPTION

This single D-type latch is designed for 1.65-V to 5.5-V  $V_{\text{CC}}$  operation.

The SN74LVC1G374 features a 3-state output designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

NanoStar $^{\text{TM}}$  and NanoFree $^{\text{TM}}$  package technology is a major breakthrough in IC packaging concepts, using the die as the package.

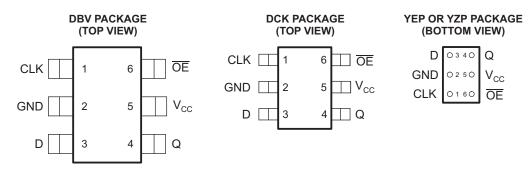
On the positive transition of the clock (CLK) input, the Q output is set to the logic level set up at the data (D) input.

A buffered output-enable  $(\overline{OE})$  input can be used to place the output in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operations of the flipflop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



See mechanical drawings for dimensions.

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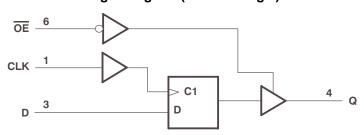


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### **Function Table**

	INPUTS		OUTPUT
ŌĒ	CLK	Q	
L	1	L	L
L	<b>↑</b>	Н	Н
L	H or L	Χ	Q
Н	X	Χ	Z

#### Logic Diagram (Positive Logic)



# Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range <sup>(2)</sup>		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impe	edance or power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in the high or lo	w state <sup>(2) (3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		<b>-</b> 50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
		DBV package		165	
$\theta_{JA}$	Package thermal impedance (4)	DCK package		259	°C/W
		YEP/YZP package		123	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

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<sup>(3)</sup> The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



# **Recommended Operating Conditions**(1)

			MIN	MAX	UNIT
.,	O mark a calle and	Operating	1.65	5.5	
$V_{CC}$	Supply voltage	Data retention only	1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
,		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
√ <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
,	Lavo Israel Sanata valta va	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	.,
/ <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>	
/ <sub>I</sub>	Input voltage		0	5.5	V
/ <sub>0</sub>	Output voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
ОН	High-level output current	V 0.V		-16	mΑ
		$V_{CC} = 3 V$		-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
OL	Low-level output current	V 0.V		16	mΑ
		$V_{CC} = 3 V$		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
∆t/Δv	t/Δv Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/\
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5	
ГА	Operating free-air temperature		-40	125	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Product Folder Links: SN74LVC1G374



#### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLIANC	V V	-40°	C to 85°C		-40°C	to 125°C		UNIT
PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	UNII
	I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1			
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			1.2			
$V_{OH}$	I <sub>OH</sub> = -8 mA	2.3 V	1.9			1.9			V
0.1	I <sub>OH</sub> = -16 mA	3 V	2.4			2.4			
	I <sub>OH</sub> = -24 mA	3 V	2.3			2.3			
	I <sub>OH</sub> = -32 mA	4.5 V	3.8			3.8			
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1			0.1	
	I <sub>OL</sub> = 4 mA	1.65 V			0.45			0.45	
$V_{OL}$	I <sub>OL</sub> = 8 mA	2.3 V			0.3			0.3	V
	I <sub>OL</sub> = 16 mA	2.1/			0.4			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55			0.65	
	I <sub>OL</sub> = 32 mA	4.5 V			0.55			0.65	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1			±2	μA
l <sub>oz</sub>	V <sub>O</sub> = 0 to 5.5 V				±5			±5	μA
I <sub>off</sub>	$V_1$ or $V_0 = 5.5 \text{ V}$	0			±10			±10	μA
I <sub>cc</sub>	V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V			10			10	μA
$\Delta I_{CC}$	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500			500	μA
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3			3		pF
Co	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		6			6		pF

<sup>(1)</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

## **Timing Requirements**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN74LVC1G374 -40°C to 85°C							
		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		$V_{CC} = 3.3 \text{ V} \\ \pm 0.3 \text{ V}$		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		100		125		150		175	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3.3		3		2.8		2.5		ns
t <sub>su</sub>	Setup time, data before CLK ↑	3.5		2.5		2		1.5		ns
t <sub>h</sub>	Hold time, data after CLK ↑	3.4		1.6		1.5		1.5		ns

## **Timing Requirements**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN74LVC1G374 -40°C to 125°C							
		V <sub>CC</sub> = 1. ± 0.15		V <sub>CC</sub> = 2 ± 0.2		V <sub>CC</sub> = 3 ± 0.3		V <sub>CC</sub> = 5 ± 0.5	5 V V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		100		125		150		175	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3.3		3		2.8		2.5		ns
t <sub>su</sub>	Setup time, data before CLK ↑	3.5		2.5		2		1.5		ns
t <sub>h</sub>	Hold time, data after CLK ↑	3.4		1.6		1.5		1.5		ns

Product Folder Links: SN74LVC1G374



## **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see Figure 1)

						SN74LV0 -40°C to					
PARAMETER	FROM INPUT	TO (OUTPUT)	V <sub>CC</sub> = 1 ± 0.15		V <sub>CC</sub> = : ± 0.2		V <sub>CC</sub> = 3 ± 0.3		V <sub>CC</sub> = ± 0.5		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100		125		150		175		MHz
t <sub>pd</sub>	CLK	Q	2.5	15	2	6	1.4	4	1	3	ns
t <sub>en</sub>	ŌĒ	Q	2.2	12	2	4.8	1.3	3.8	1.1	2.5	ns
t <sub>dis</sub>	ŌĒ	Q	2.2	11	2	4.8	1.6	4.5	1.2	3.1	ns

## **Switching Characteristics**

over recommended operating free-air temperature range, C<sub>L</sub> = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

			SN74LVC1G374 −40°C to 85°C								
PARAMETER	FROM INPUT	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100		125		150		175		MHz
t <sub>pd</sub>	CLK	Q	2.7	18.3	1.8	8.2	1.6	6	1	4	ns
t <sub>en</sub>	ŌĒ	Q	2	13	1.5	6.3	0.9	5	0.7	3.5	ns
t <sub>dis</sub>	ŌĒ	Q	2	14	1.1	5.3	1.4	4.5	0.8	3.1	ns

## **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  or 50 pF (unless otherwise noted) (see Figure 2)

						SN74LV -40°C to					
PARAMETER	FROM INPUT	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100		125		150		175		MHz
t <sub>pd</sub>	CLK	Q	2.7	18.3	1.8	10.2	1.6	7	1	5	ns
t <sub>en</sub>	ŌĒ	Q	2	14	1.5	8.3	0.9	6.5	0.7	5.5	ns
t <sub>dis</sub>	ŌĒ	Q	2	16	1.1	7.3	1.4	6	0.8	5.1	ns

## **Operating Characteristics**

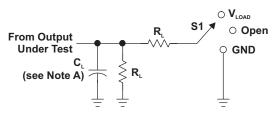
 $T_A = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	V <sub>CC</sub> = 3.3 V TYP	V <sub>CC</sub> = 5 V TYP	UNIT		
_	Power dissipation	Outputs enabled	f = 10 MHz	24	24	25	27	۲	
$C_{pd}$			I = IU WINZ	8	8	9	11	pF	

Product Folder Links: SN74LVC1G374



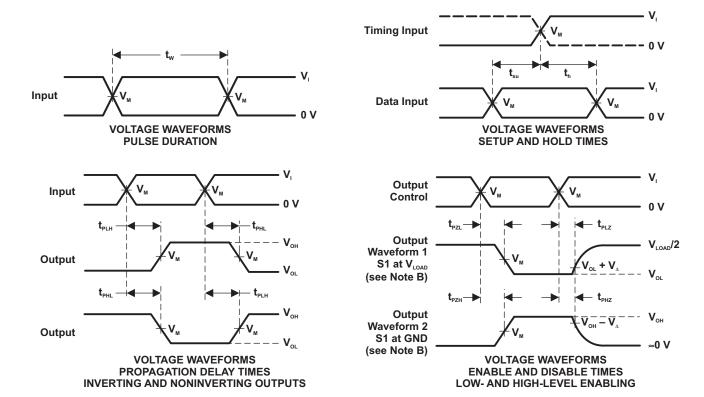
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	<b>V</b> <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

**LOAD CIRCUIT** 

.,	INI	PUTS	.,	.,			.,
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>⊾</sub>	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 M</b> Ω	0.15 V
2.5 V ± 0.2 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 M</b> Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	<b>1 M</b> Ω	0.3 V
5 V ± 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 M</b> Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o$  = 50  $\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{\mbox{\tiny PLZ}}$  and  $\dot{t}_{\mbox{\tiny PHZ}}$  are the same as  $t_{\mbox{\tiny dis}}.$
- F.  $t_{\mbox{\tiny PZL}}$  and  $t_{\mbox{\tiny PZH}}$  are the same as  $t_{\mbox{\tiny en}}.$
- G.  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  are the same as  $t_{\text{pd}}$ .
- H. All parameters and waveforms are not applicable to all devices.

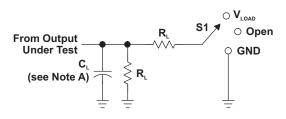
Figure 1. Load Circuit and Voltage Waveforms

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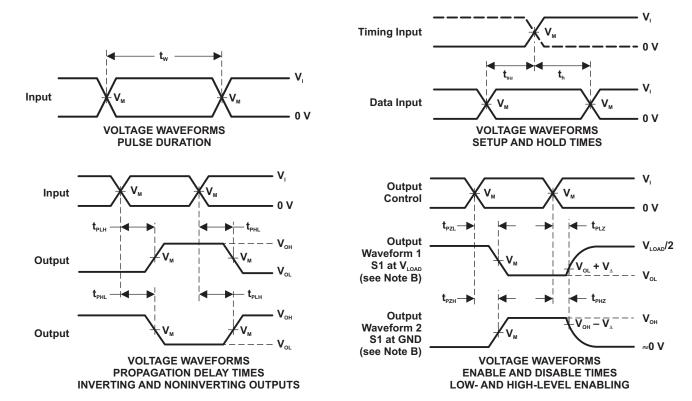
#### PARAMETER MEASUREMENT INFORMATION (continued)



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	<b>V</b> <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

LOAD CIRCUIT

.,	V <sub>i</sub> t <sub>r</sub> /t <sub>r</sub>			V		_	.,
V <sub>cc</sub>			V <sub>M</sub>	<b>V</b> <sub>LOAD</sub>	C <sub>∟</sub>	R <sub>⊾</sub>	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	<b>1 k</b> Ω	0.15 V
$2.5~V~\pm~0.2~V$	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \,\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $\dot{t}_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}^{r2L}$  and  $t_{PHL}^{r2H}$  are the same as  $t_{pd}^{eff}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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## SCES520C - DECEMBER 2003 - REVISED DECEMBER 2013



## **REVISION HISTORY**

CI	hanges from Revision B (September 2006) to Revision C	Page
•	Updated document to new TI data sheet format.	1
•	Removed Ordering Information table.	2
•	Added ESD warning.	2
•	Updated operating temperature range.	3

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
74LVC1G374DCKRG4	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D45
74LVC1G374DCKRG4.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D45
SN74LVC1G374DBVR	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CA45, CA4R)
SN74LVC1G374DBVR.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CA45, CA4R)
SN74LVC1G374DCKR	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(D45, D4J, D4R)
SN74LVC1G374DCKR.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(D45, D4J, D4R)
SN74LVC1G374DCKRG4.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
SN74LVC1G374YZPR	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D4N
SN74LVC1G374YZPR.B	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D4N

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# PACKAGE OPTION ADDENDUM

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#### OTHER QUALIFIED VERSIONS OF SN74LVC1G374:

Automotive: SN74LVC1G374-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G374DCKRG4	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G374DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G374DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G374DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G374DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G374YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



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## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G374DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G374DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G374DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G374DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74LVC1G374DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74LVC1G374YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



#### NOTES:

NanoFree Is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- 3. NanoFree<sup>™</sup> package configuration.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
 For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

  4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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