# SN74LVC1G373 Single D-Type Latch With 3-State Output

## 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V $V_{CC}$ Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to $V_{CC}$
- Max $t_{pd}$ of 4 ns at 3.3 V
- Low Power Consumption: 10-μA Maximum $I_{CC}$
- ±24-mA Output Drive at 3.3 V
- $I_{off}$ Supports Partial-Power-Down Mode and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## 2 Applications

- Servers
- Printers
- Telecom and Grid Infrastructure
- Memory Addressing
- Buffer Registers
- Electronic Point of Sale

## 3 Description

The SN74LVC1G373 device is a single D-type latch designed for 1.65-V to 5.5-V $V_{CC}$ operation.

This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

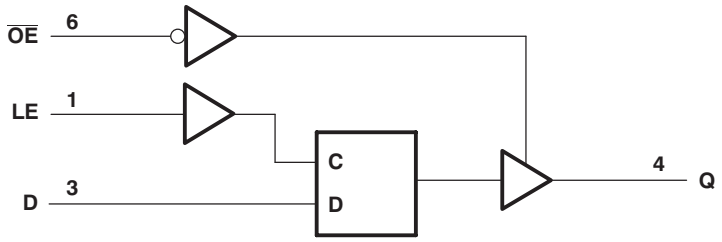
$\overline{OE}$ does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

**Device Information(1)**

| PACKAGE NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC1G373DBV | SOT-23 (6) | 2.90 mm × 1.60 mm |
| SN74LVC1G373DCK | SC70 (6) | 2.00 mm × 1.25 mm |
| SN74LVC1G373YZP | DSBGA (6) | 1.41 mm × 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision E (September 2016) to Revision F** — **Page**

- Changed YZP Package pinout diagram and added YZP pin numbers in *Pin Functions* table ... 3
- Added *Balanced High-Drive CMOS Push-Pull Outputs*, *Standard CMOS Inputs*, *Clamp Diodes*, *Partial Power Down ($I_{off}$)*, *Over-voltage Tolerant Inputs* ... 12
- Added *Trace Example* in *Layout Example* section ... 16
- Added *Documentation Support* section ... 17

**Changes from Revision D (December 2013) to Revision E** — **Page**

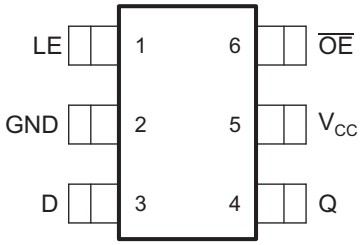
- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision C (May 2007) to Revision D** — **Page**

- Updated document to new TI data sheet format. ... 1
- Deleted Ordering Information table; see POA at the end of the data sheet. ... 1
- Updated operating temperature range. ... 5

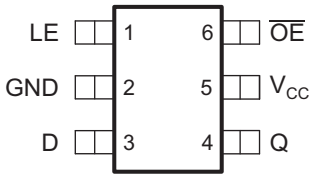
# 5 Pin Configuration and Functions

**DBV Package**
**6-Pin SOT-23**
**Top View**

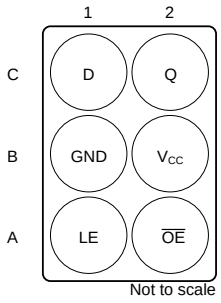



See mechanical drawings for dimensions.

**DCK Package**
**6-Pin SC70**
**Top View**




**YZP Package**
**6-Pin DSBGA**
**Bottom View**




Not to scale

**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DCK, DBV | YZP | | |
| LE | 1 | A1 | I | Latch Enable; output follows D input when high |
| GND | 2 | B1 | — | Ground |
| D | 3 | C1 | I | D latch input |
| Q | 4 | C2 | O | Q latch output |
| $V_{CC}$ | 5 | B2 | — | Positive supply |
| $\overline{OE}$ | 6 | A2 | I | Active low output enable; Hi-Z output when high |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2)(3) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_J$ | Absolute maximum Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions*.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. CDM tested on DBV package

## 6.3 Recommended Operating Conditions

See (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | 5.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | 5.5 | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | 5.5 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.7 × $V_{CC}$ | 5.5 | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0 | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | 0 | 0.8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0 | 0.3 × $V_{CC}$ | |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 3 V | | –16 | |
| | | | | –24 | |
| | | $V_{CC}$ = 4.5 V | | –32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 10 | |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 5 | |
| $T_A$ | Operating free-air temperature | DSBGA package | –40 | 85 | °C |
| | | All other packages | –40 | 125 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LVC1G373 | | | UNIT |
|---|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | YZP (DSBGA) | |
| | | 6 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 219.8 | 255.2 | 131 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 189 | 121.9 | 1.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 65.8 | 58 | 22.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 67.3 | 7.2 | 5.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 65.2 | 57.3 | 22.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $I_{OH}$ = –100 µA | | 1.65 V to 5.5 V | $V_{CC}$ – 0.1 | | | V |
| | $I_{OH}$ = –4 mA | | 1.65 V | 1.2 | | | |
| | $I_{OH}$ = –8 mA | | 2.3 V | 1.9 | | | |
| | $I_{OH}$ = –16 mA | | 3 V | 2.4 | | | |
| | $I_{OH}$ = –24 mA | | | 2.3 | | | |
| | $I_{OH}$ = –32 mA | | 4.5 V | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | | 1.65 V to 5.5 V | | | 0.1 | V |
| | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | |
| | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.3 | |
| | $I_{OL}$ = 16 mA | | 3 V | | | 0.4 | |
| | $I_{OL}$= 24 mA | $T_A$ = –40°C to 85°C | | | | 0.55 | |
| | | $T_A$ = –40°C to 125°C | | | | 0.65 | |
| | $I_{OL}$= 32 mA | $T_A$ = –40°C to 85°C | 4.5 V | | | 0.55 | |
| | | $T_A$ = –40°C to 125°C | | | | 0.65 | |
| $I_I$ | $V_I$ = 5.5 V or GND | | 0 V to 5.5 V | | | ±1 | µA |
| $I_{OZ}$ | $V_O$ = 0 to 5.5 V | | 3.6 V | | | ±5 | |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±10 | |
| $I_{CC}$ | $V_I$ = 5.5 V or GND, $I_O$ = 0 | | 1.65 V to 5.5 V | | | 10 | |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | 3 V to 5.5 V | | | 500 | |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | $T_A$ = –40°C to 85°C | 3.3 V | | 3.5 | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | $T_A$ = –40°C to 85°C | 3.3 V | | 6 | | |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## 6.6 Timing Requirements: $T_A$ = –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_w$ | Pulse duration, LE high | | 3 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | $V_{CC}$ = 1.8 V ± 0.15 V | 2.4 | | |
| | | $V_{CC}$ = 2.5 V ± 0.2 V | 2 | | |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.5 | | |
| | | $V_{CC}$ = 5 V ± 0.5 V | 1.5 | | |
| $t_h$ | Hold time, data after LE↓ | $V_{CC}$ = 1.8 V ± 0.15 V | 2.5 | | |
| | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | | |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.5 | | |
| | | $V_{CC}$ = 5 V ± 0.5 V | 1.5 | | |

## 6.7 Timing Requirements: $T_A$ = –40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_w$ | Pulse duration, LE high | | 3 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | $V_{CC}$ = 1.8 V ± 0.15 V | 2.9 | | |
| | | $V_{CC}$ = 2.5 V ± 0.2 V | 2.1 | | |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.5 | | |
| | | $V_{CC}$ = 5 V ± 0.5 V | 1.5 | | |
| $t_h$ | Hold time, data after LE↓ | $V_{CC}$ = 1.8 V ± 0.15 V | 3 | | |
| | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | | |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.5 | | |
| | | $V_{CC}$ = 5 V ± 0.5 V | 1.5 | | |

## 6.8 Switching Characteristics: $T_A$ = –40°C to +85°C

over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | D | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 15 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 15 | 5 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 4 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3.5 | |
| | LE | | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 15 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 5 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 4 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3.5 | |
| $t_{en}$ | $\overline{OE}$ | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 12.5 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 4.5 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 4 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 2.5 | |
| $t_{dis}$ | $\overline{OE}$ | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 14 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 7 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 7.9 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 5.3 | |

## 6.9 Switching Characteristics: $T_A$ = –40°C to +85°C

over recommended operating free-air temperature range, $C_L$ = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | D | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 16 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 7.3 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 5.4 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 4 | |
| | LE | | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 16.3 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 7.4 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 5.5 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 4 | |
| $t_{en}$ | $\overline{OE}$ | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 13 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 6.3 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 5.1 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3.7 | |
| $t_{dis}$ | $\overline{OE}$ | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 17.4 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 5.9 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 6.5 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 4.6 | |

## 6.10 Switching Characteristics: $T_A$ = –40°C to +125°C

over recommended operating free-air temperature range, $C_L$ = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | D | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 17 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 8 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 6 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 4.5 | |
| | LE | | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 17 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 8 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 6 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 4.5 | |
| $t_{en}$ | $\overline{OE}$ | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 13.5 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 7 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 5.5 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 4 | |
| $t_{dis}$ | $\overline{OE}$ | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 18.4 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 6.2 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 6.8 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 5 | |
| $t_{en}$ | $\overline{OE}$ | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 14 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.5 | 8.3 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 0.9 | 6.5 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 0.7 | 5.5 | |
| $t_{dis}$ | $\overline{OE}$ | Q | $V_{CC}$ = 1.8 V ± 0.15 V | 2 | 16 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1.1 | 7.3 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.4 | 6 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 0.8 | 5.1 | |

## 6.11 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | f = 10 MHz | $V_{CC}$ = 1.8 V | 19 | pF |
| | | | | $V_{CC}$ = 2.5 V | 19 | |
| | | | | $V_{CC}$ = 3.3 V | 19 | |
| | | | | $V_{CC}$ = 5 V | 20 | |
| | | Outputs disabled | | $V_{CC}$ = 1.8 V | 3 | |
| | | | | $V_{CC}$ = 2.5 V | 3 | |
| | | | | $V_{CC}$ = 3.3 V | 3 | |
| | | | | $V_{CC}$ = 5 V | 4 | |

## 6.12 Typical Characteristics

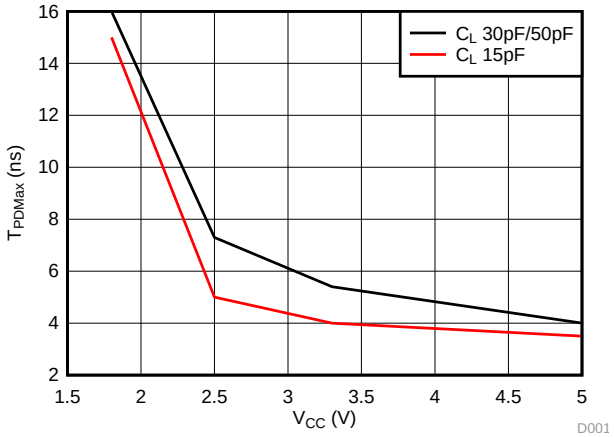
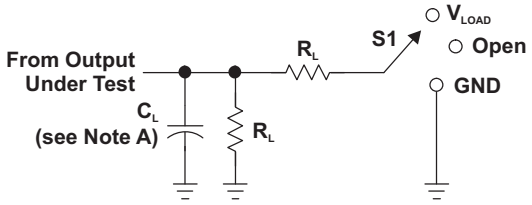



**Figure 1. Propagation delay vs $V_{CC}$**

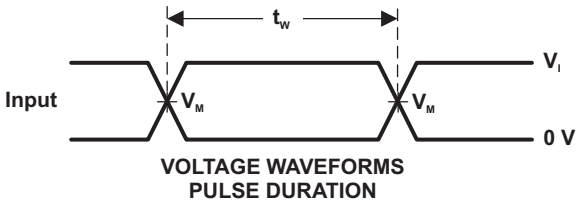
# 7 Parameter Measurement Information



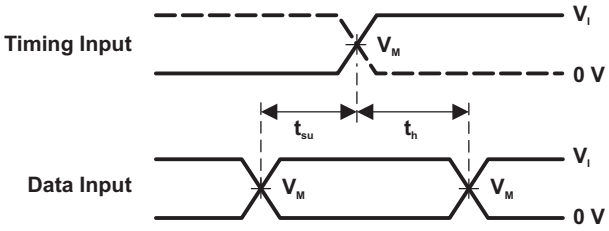

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

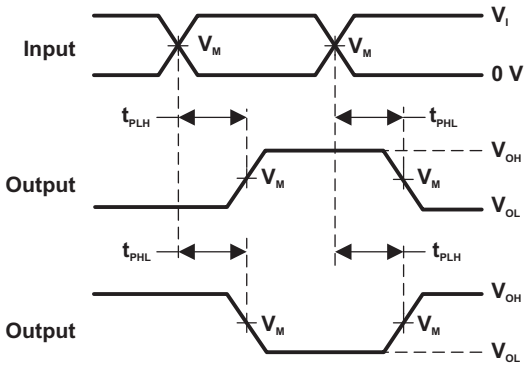
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 15 pF | 1 MΩ | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.3 V |



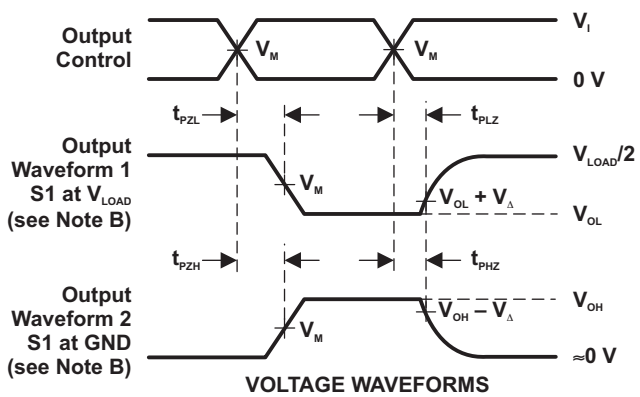

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

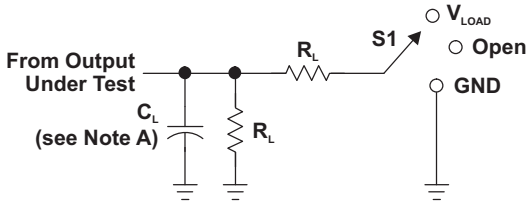



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

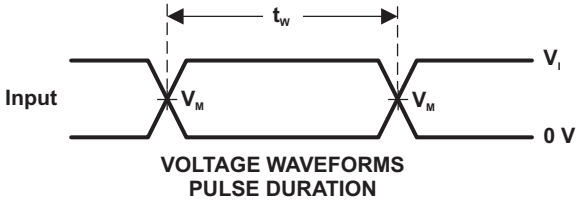
## Parameter Measurement Information (continued)



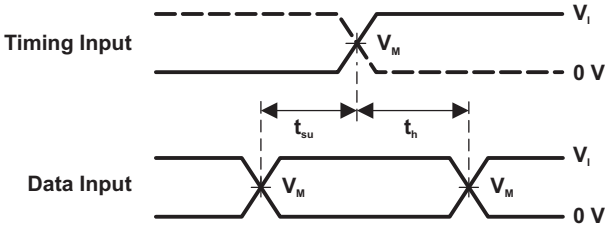

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

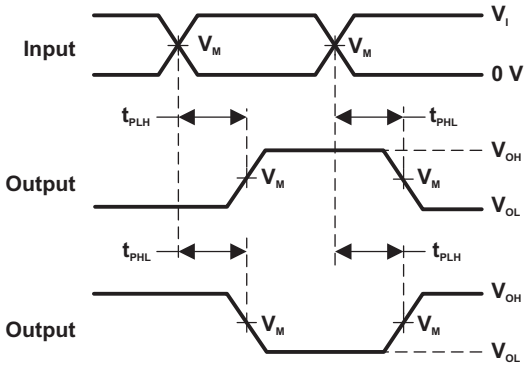
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



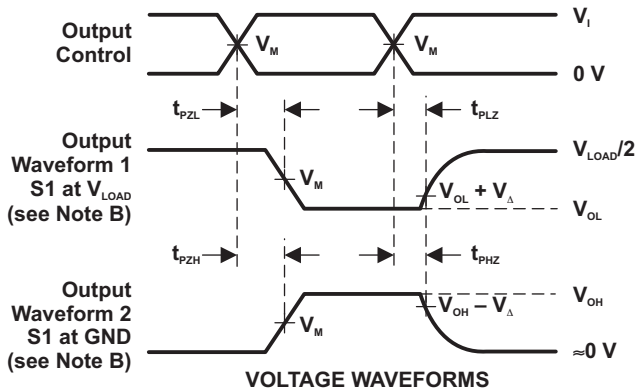

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

A buffered output-enable ($\overline{OE}$) input can be used to place the output in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 8.2 Functional Block Diagram

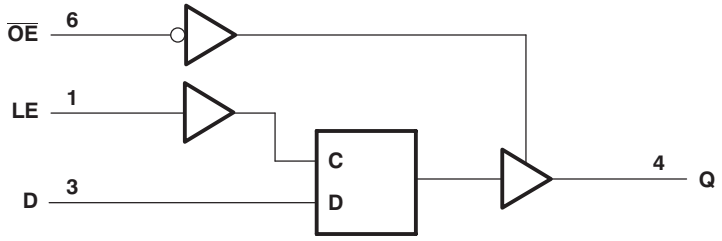



**Figure 4. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

### 8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

## Feature Description (continued)

### 8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

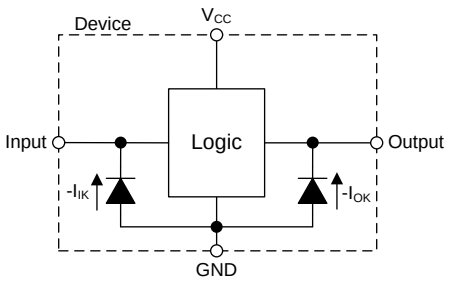



**Figure 5. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.3.4 Partial Power Down ($I_{off}$)

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by $I_{off}$ in the *Electrical Characteristics*.

### 8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings*.

## 8.4 Device Functional Modes

Table 1 lists the functions of this device.

**Table 1. Function Table**

| INPUTS | | | OUTPUT Q |
|---|---|---|---|
| $\overline{OE}$ | LE | D | |
| L | H | L | L |
| L | H | H | H |
| L | L | X | $Q_0$ |
| H | X | X | Hi-Z |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LVC1G373 latches can be used to store one bit of data. Figure 6 shows a typical application. The multiplexer is used to convert parallel data coming in from the latch into serial data using the A, B, and C select pins moving up in a sequence. With latch input low by a trigger event, the output Q holds the previous $Q_0$ data entered until the LE pin is cleared.

## 9.2 Typical Application

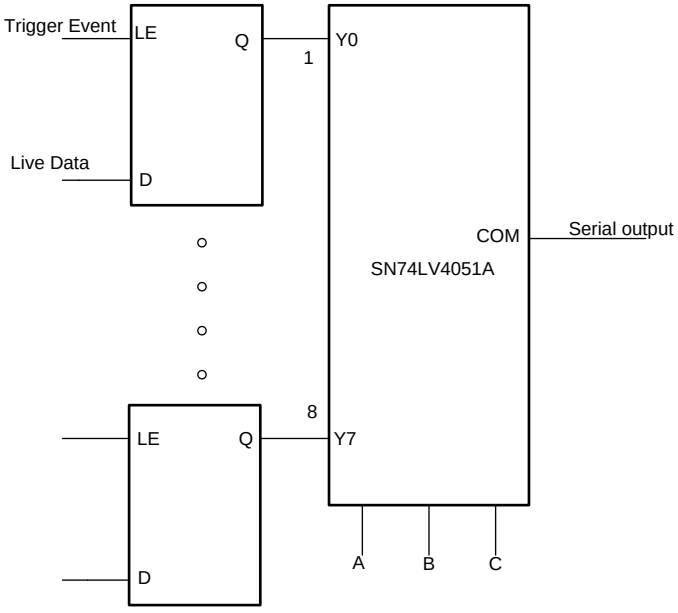





**Figure 6. Latch Used With Multiplexer for Parallel to Serial Conversion**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see $\Delta t/\Delta V$ in *Recommended Operating Conditions*.
   - For specified High and low levels, see $V_{IH}$ and $V_{IL}$ in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommended Output Conditions
   - Load currents should not exceed 32 mA per output and 100 mA total through the part.
   - Outputs must not be pulled above $V_{CC}$.

### 9.2.3 Application Curve

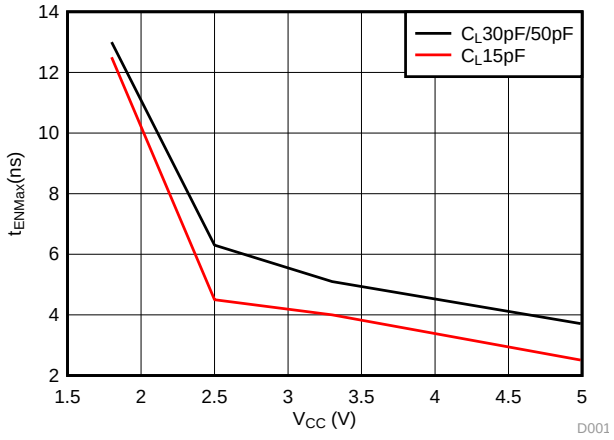



**Figure 7. Enable Time vs $V_{CC}$**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF bypass capacitor. If there are multiple $V_{CC}$ pins, TI recommends 0.01-µF or 0.022-µF bypass capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient.

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 9 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

### 11.2 Layout Example

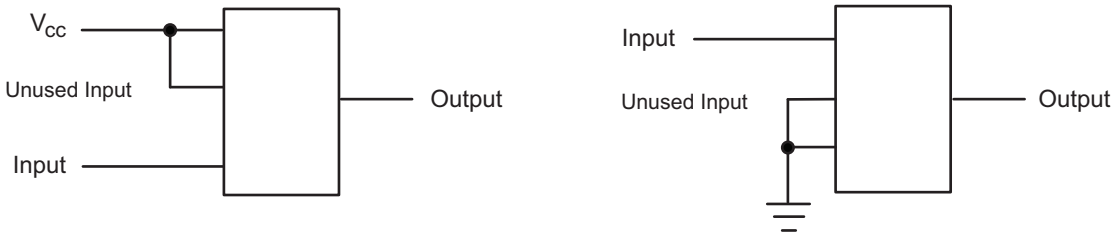



**Figure 8. Proper Multiple Input Termination Diagram**

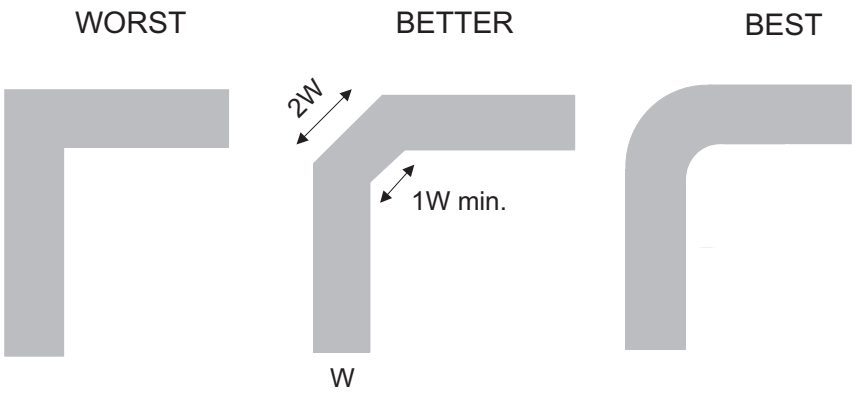



**Figure 9. Trace Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs* (SCBA004)

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 74LVC1G373DBVR1G4 | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CA35, CA3R) |
| 74LVC1G373DBVR1G4.B | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CA35, CA3R) |
| 74LVC1G373DBVRE4 | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CA35, CA3R) |
| 74LVC1G373DCKRE4 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | D35 |
| 74LVC1G373DCKRG4 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | D35 |
| 74LVC1G373DCKRG4.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | D35 |
| SN74LVC1G373DBVR | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (CA35, CA3R) |
| SN74LVC1G373DBVR.B | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (CA35, CA3R) |
| SN74LVC1G373DCKR | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (D35, D3J, D3R) |
| SN74LVC1G373DCKR.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (D35, D3J, D3R) |
| SN74LVC1G373YZPR | Active | Production | DSBGA (YZP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | D3N |
| SN74LVC1G373YZPR.B | Active | Production | DSBGA (YZP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | D3N |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

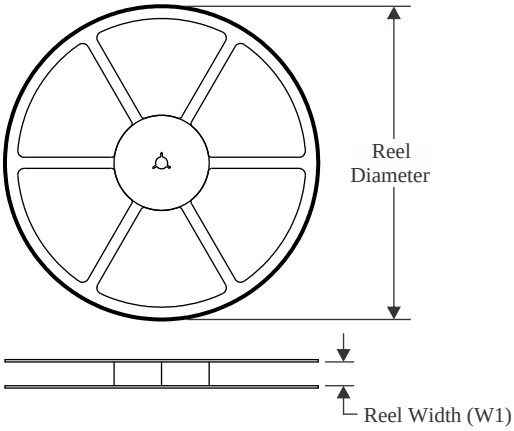
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

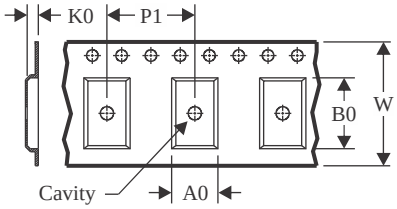
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

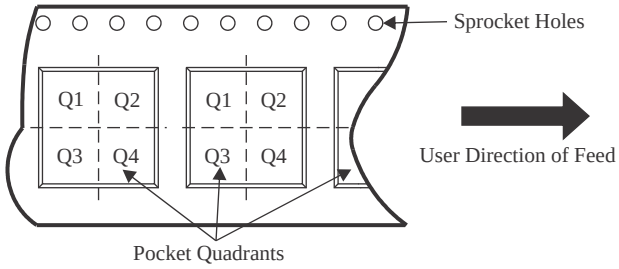



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

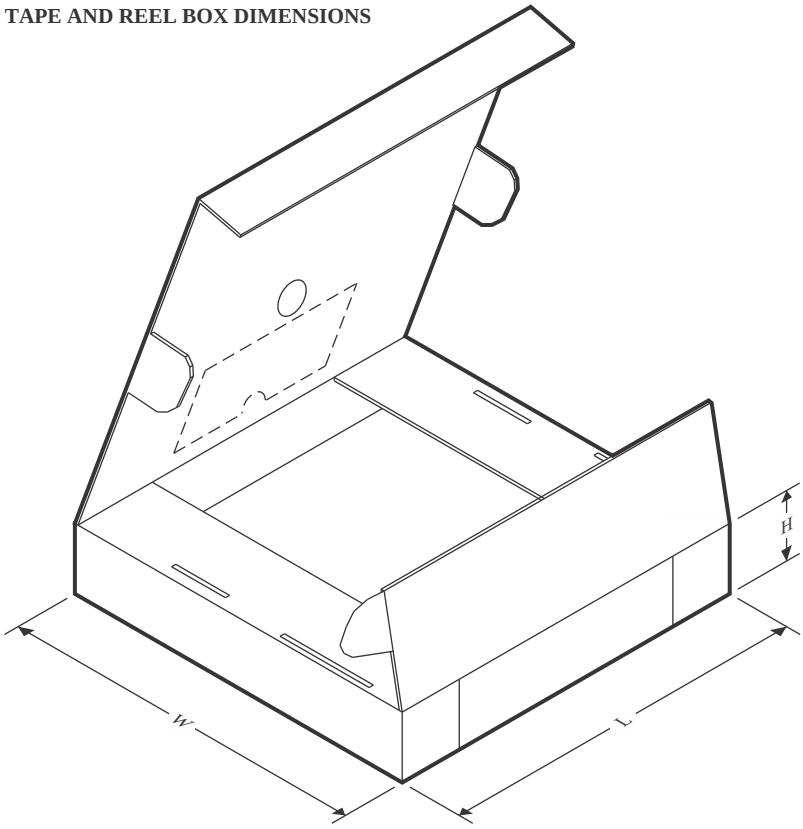
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74LVC1G373DBVR1G4 | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| 74LVC1G373DBVR1G4 | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| 74LVC1G373DCKRG4 | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G373DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G373DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G373DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G373YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

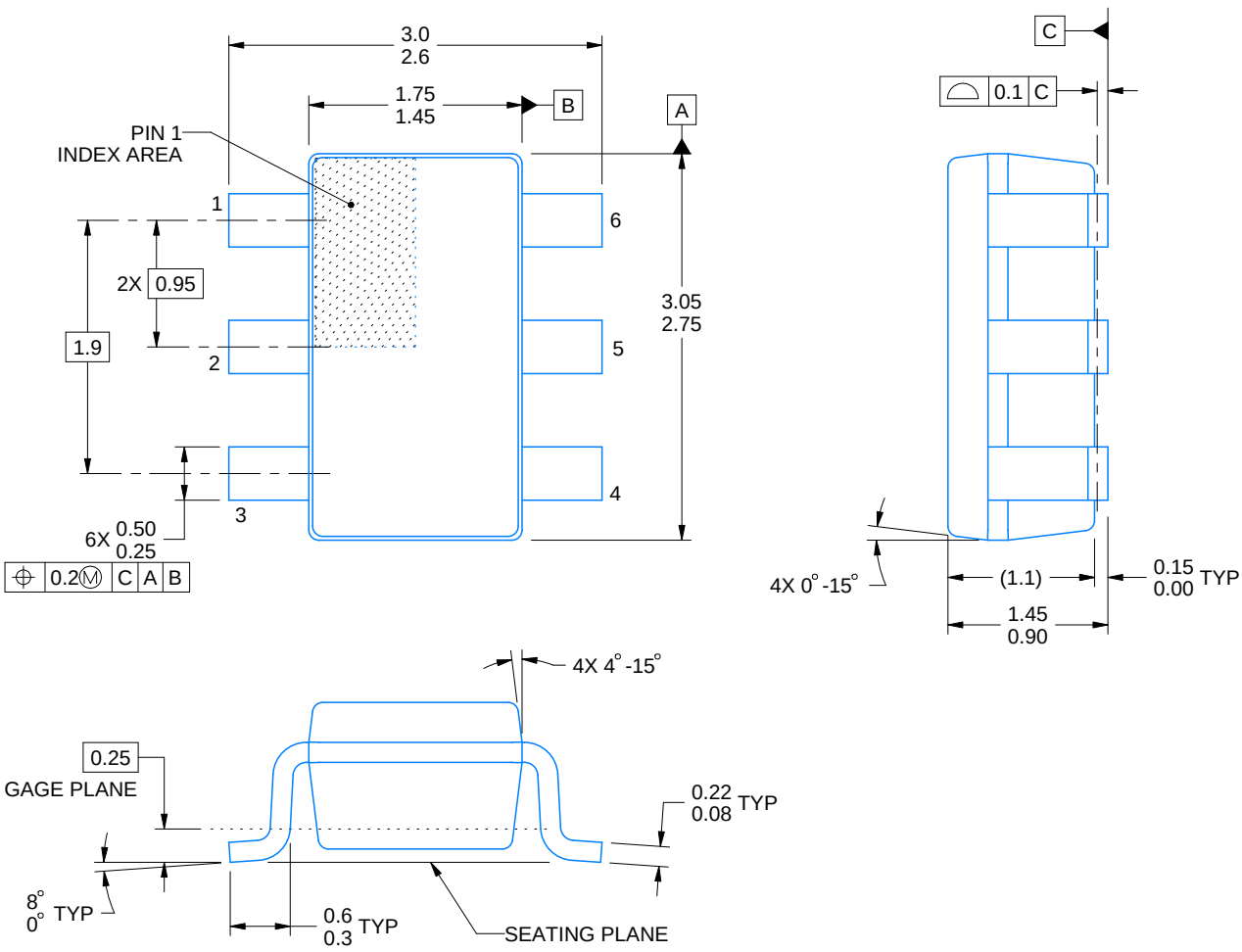
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74LVC1G373DBVR1G4 | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| 74LVC1G373DBVR1G4 | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| 74LVC1G373DCKRG4 | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G373DBVR | SOT-23 | DBV | 6 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74LVC1G373DCKR | SC70 | DCK | 6 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74LVC1G373DCKR | SC70 | DCK | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G373YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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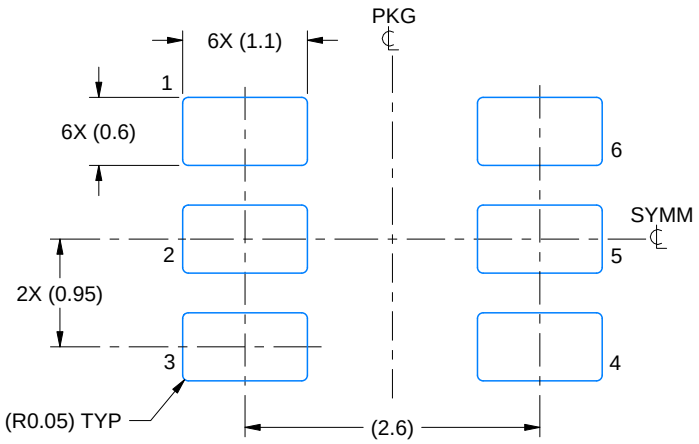
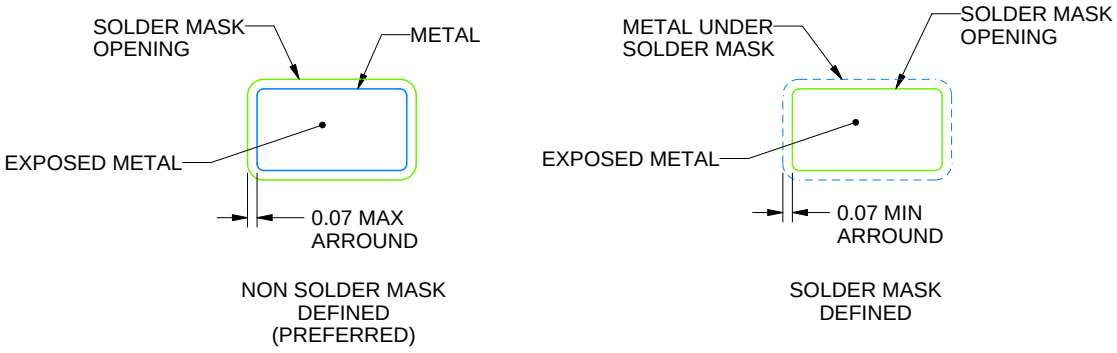
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

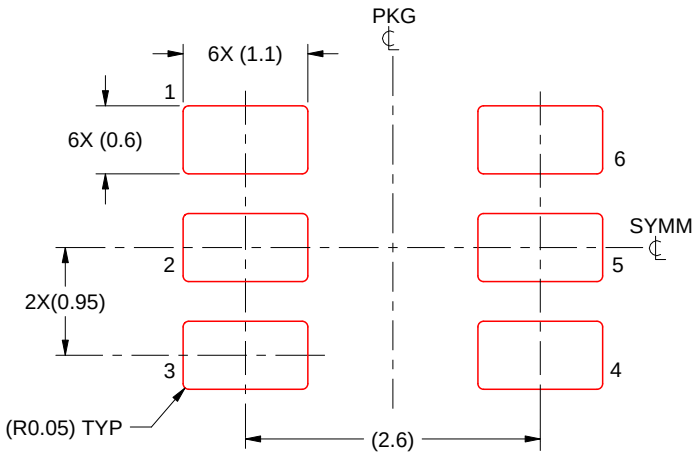



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

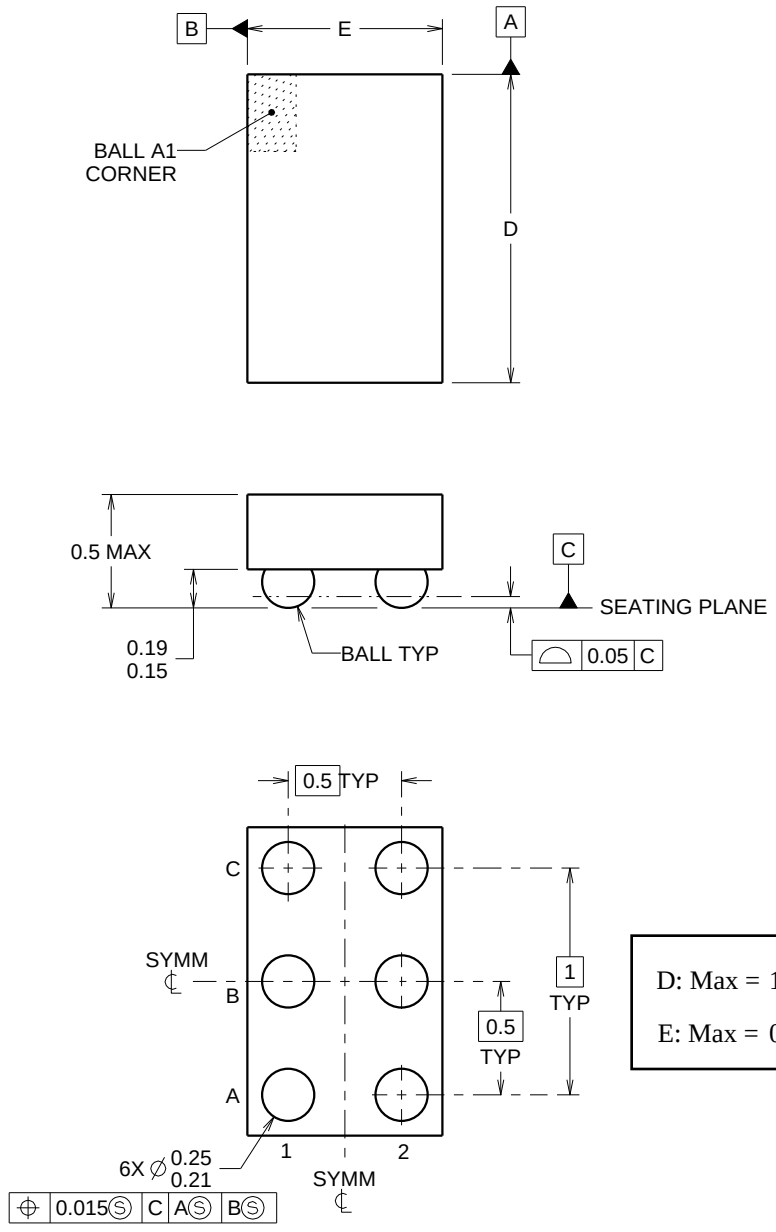
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## YZP0006

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




D: Max = 1.418 mm, Min =1.358 mm

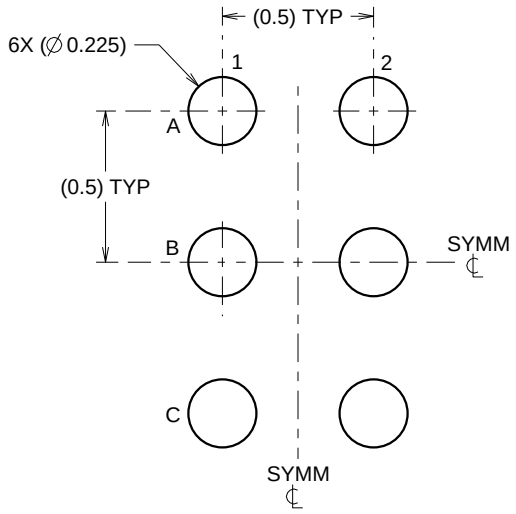
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

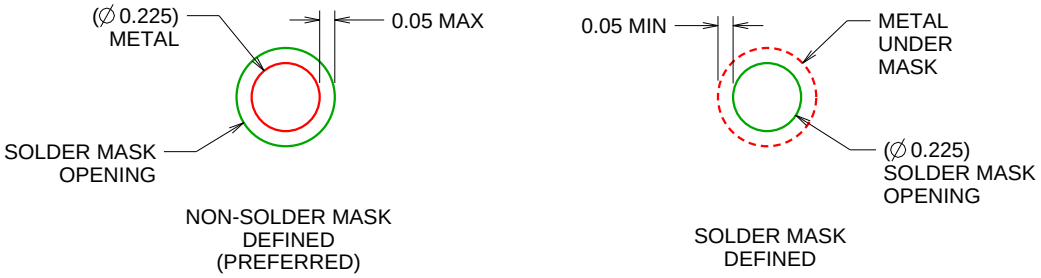
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.




LAND PATTERN EXAMPLE
SCALE:40X

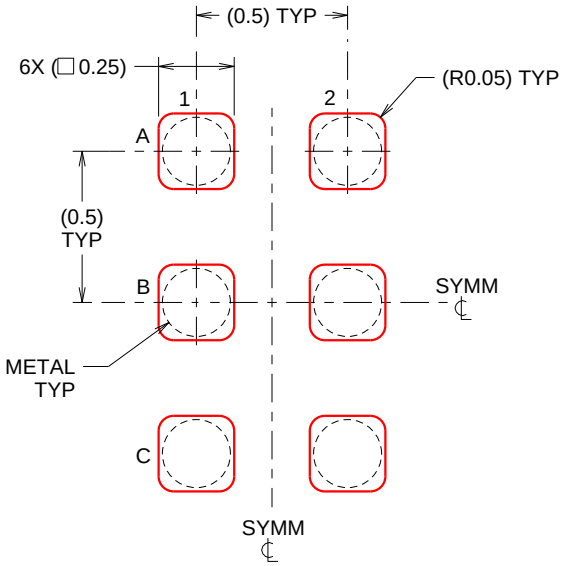



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

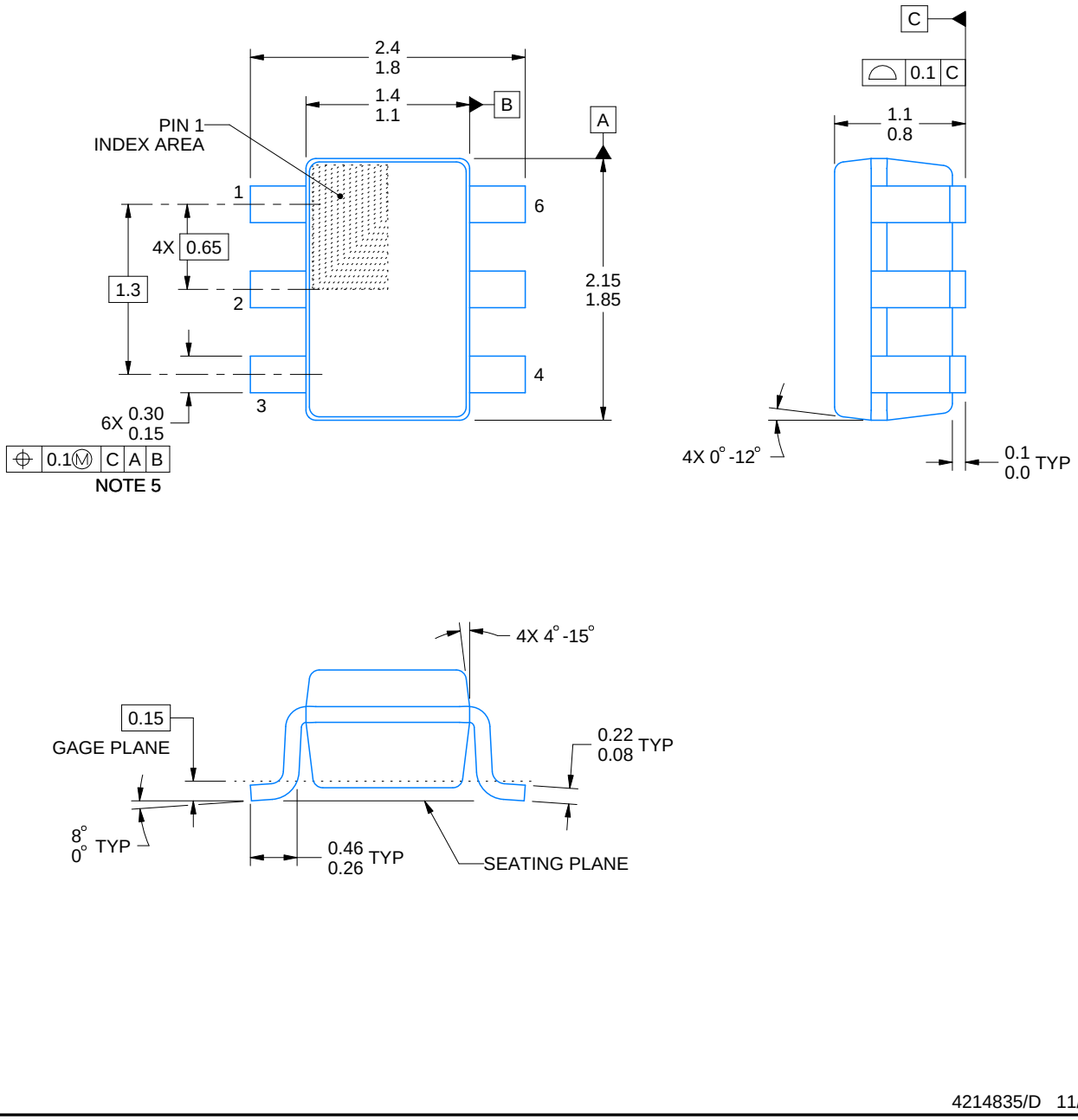
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DCK0006A

## SOT - 1.1 max height

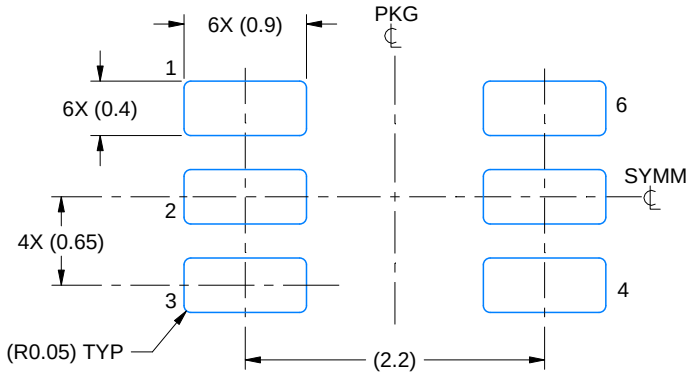
SMALL OUTLINE TRANSISTOR



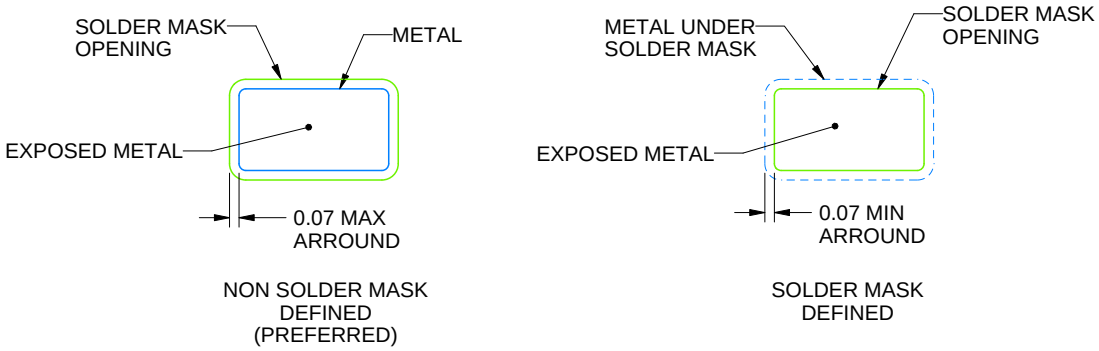

4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

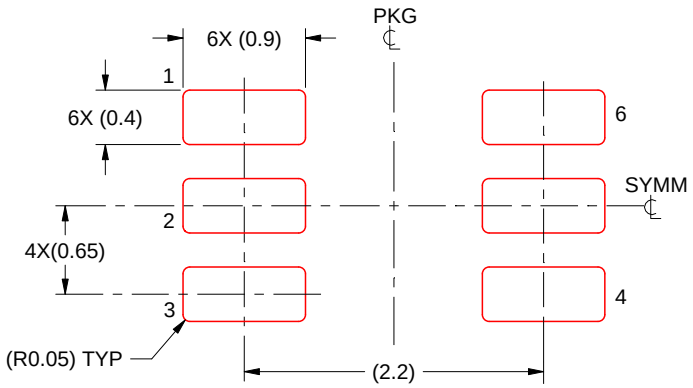



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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