

Single 3-Input Positive OR-AND Gate

Check for Samples: SN74LVC1G3208

FEATURES

- Available in the Texas Instruments NanoStar[™] and NanoFree[™] Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V_{CC}
- Max t_{pd} of 5 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input (V_{hys} = 250 mV Typ @ 3.3 V)
- Can Be Used in Three Combinations:
 - OR-AND Gate
 - OR Gate
 - AND Gate
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION

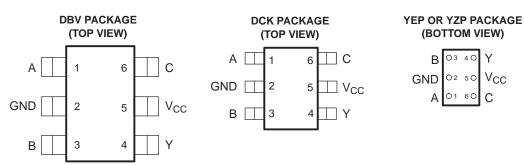
This device is designed for 1.65-V to 5.5-V $V_{\rm CC}$ operation.

The SN74LVC1G3208 device is a single 3-input positive OR-AND gate. It performs the Boolean function $Y = (A + B) \cdot C$ in positive logic.

By tying one input to GND or V_{CC} , the SN74LVC1G3208 device offers two more functions. When C is tied to V_{CC} , this device performs as a 2-input OR gate (Y = A + B). When A is tied to GND, the device works as a 2-input AND gate (Y = B \bullet C). This device also works as a 2-input AND gate when B is tied to GND (Y = A \bullet C).

NanoStar[™] and NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using $I_{\rm off}$. The $I_{\rm off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



See mechanical drawings for dimensions.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





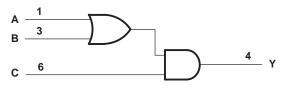
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Function Table⁽¹⁾

	INPUTS					
Α	В	С	Y			
Н	X	Н	Н			
X	Н	Н	Н			
X	X	L	L			
L	L	Н	L			

(1) X = Valid H or L

Logic Diagram (Positive Logic)



Function Selection Table

LOGIC FUNCTION	FIGURE
2-Input AND Gate	Figure 1
2-Input OR Gate	Figure 2
Y = (A + B) ● C	Figure 3

Logic Configurations

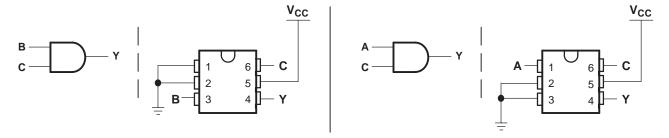


Figure 1. 2-Input AND Gate

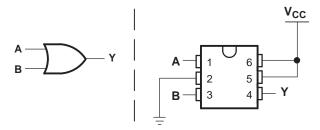


Figure 2. 2-Input OR Gate



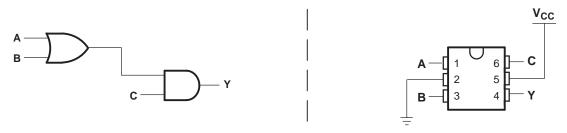


Figure 3. $Y = (A + B) \cdot C$

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾	-0.5	6.5	V	
Vo	Voltage range applied to any output in the	-0.5	6.5	V	
Vo	Voltage range applied to any output in the	-0.5	V _{CC} + 0.5	٧	
I _{IK}	Input clamp current	V _I < 0		-50	mA
lok	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
		DBV package		165	
θ_{JA}	Package thermal impedance (4)	DCK package		259	°C/W
		YEP or YZP package		123	
T _{stg}	Storage temperature range	-65	150	°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
	Cumply walte as	Operating	1.65	5.5	V	
V_{CC}	Supply voltage	Data retention only	1.5		V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
V	High level input valtage	V _{CC} = 2.3 V to 2.7 V	1.7		V	
V_{IH}	High-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2		V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.7 × V _{CC}			
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
\ /	Low lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
V_{IL}	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.8	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$		
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V_{CC}	V	
		V _{CC} = 1.65 V		-4		
		V _{CC} = 2.3 V		-8		
I _{OH}	High-level output current	V _{CC} = 3 V		-16	mA	
				-24		
		V _{CC} = 4.5 V		-32		
		V _{CC} = 1.65 V		4		
		V _{CC} = 2.3 V		8		
I _{OL}	Low-level output current	V _{CC} = 3 V		16	mA	
				24		
		V _{CC} = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10		
	,	V _{CC} = 5 V ± 0.5 V		5		
T _A	Operating free-air temperature		-40	125	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

		TEGT COMPLIANC	.,	-40°(C to 85°C		–40°C	to 85°C			
,	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	UNIT	
		I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.1			V _{CC} - 0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			1.2				
V _{OH}		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			1.9			V	
0		I _{OH} = -16 mA	3 V	2.4			2.4				
		I _{OH} = -24 mA	3 v	2.3			2.3				
		I _{OH} = -32 mA	4.5 V	3.8			3.8				
I _{OL} = 100 μA		I _{OL} = 100 μA	1.65 V to 5.5 V			0.1			0.1		
		I _{OL} = 4 mA	1.65 V			0.45			0.45		
V _{OL}		I _{OL} = 8 mA	2.3 V			0.3			0.3	V	
02		I _{OL} = 16 mA	2.1/			0.4			0.4		
		I _{OL} = 24 mA	3 V			0.55			0.55		
		I _{OL} = 32 mA	4.5 V			0.55			0.6		
I _I	A, B, or C inputs	V _I = 5.5 V or GND	0 to 5.5 V			±5			±5	μA	
I _{off}		V _I or V _O = 5.5 V	0			±10			±10	μA	
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			10			10	μA	
ΔI_{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V			500			500	μA	
Ci		V _I = V _{CC} or GND	3.3 V		3.5			3.5		pF	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 4)

						N74LVC -40°C to					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1. ± 0.15		V _{CC} = 2 ± 0.2		V _{CC} = 3 ± 0.3		V _{CC} = ± 0.5		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, or C	Υ	3.7	14	2.5	7	1.7	5	1.3	3.4	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 5)

			SN74LVC1G3208 -40°C to 85°C								
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 ± 0.15		V _{CC} = 2 ± 0.2		V _{CC} = 3 ± 0.3		V _{CC} = ± 0.5		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, or C	Υ	2.5	17.5	1.8	7.6	1.8	5.9	1.3	4	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 5)

			SN74LVC1G3208 -40°C to 125°C								
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 ± 0.15		V _{CC} = 2 ± 0.2		V _{CC} = 3 ± 0.3		V _{CC} = ± 0.5	5 V 5 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, or C	Υ	2.5	17.5	1.8	7.6	1.8	5.9	1.3	4.5	ns

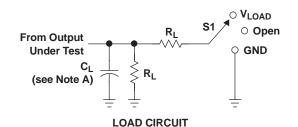
Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER		TEST	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 V$	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 V$	UNIT
		CONDITIONS	TYP	TYP	TYP	TYP	UNII
C_{pd}	Power dissipation capacitance	f = 10 MHz	15	15	16	17	pF

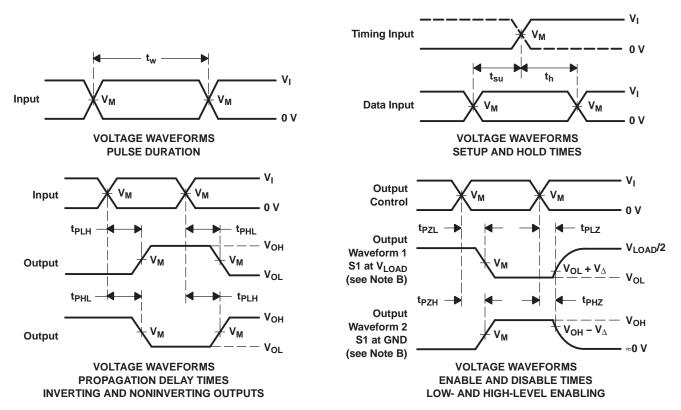


Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	INF	PUTS	.,	.,		_	.,	
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_Δ	
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V	
2.5 V \pm 0.2 V	V_{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.15 V	
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V	
5 V \pm 0.5 V	V_{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	15 pF	1 M Ω	0.3 V	



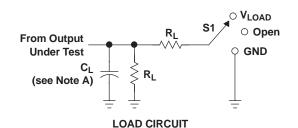
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

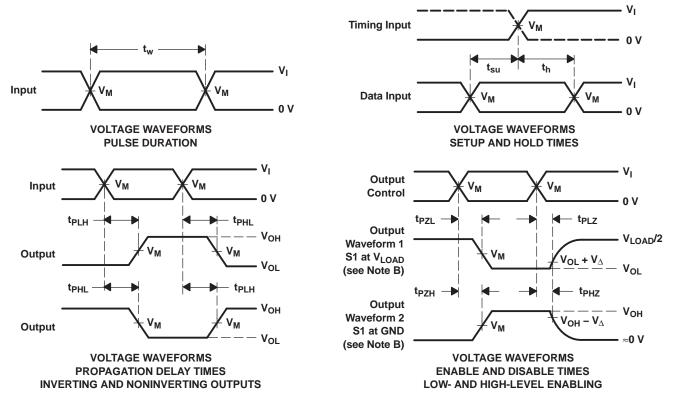


Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	INF	PUTS	V	V	•	_	.,	
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	V_Δ	
1.8 V \pm 0.15 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V	
2.5 V \pm 0.2 V	V_{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V	
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
5 V \pm 0.5 V	Vcc	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V	



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms





REVISION HISTORY

CI	hanges from Revision A (June 2005) to Revision B	Page
•	Updated document to new TI data sheet format.	1
•	Updated Features.	1
•	Removed Ordering Information table.	1
•	Added ESD warning.	2
•	Updated operating temperature range.	4

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
74LVC1G3208DBVRG4	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CDD5, CDDR)
74LVC1G3208DCKRG4.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
SN74LVC1G3208DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CDD5, CDDR)
SN74LVC1G3208DBVR.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CDD5, CDDR)
SN74LVC1G3208DBVT	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CDD5, CDDR)
SN74LVC1G3208DBVT.B	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CDD5, CDDR)
SN74LVC1G3208DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(DD5, DDJ, DDK, DD R)
SN74LVC1G3208DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(DD5, DDJ, DDK, DD R)
SN74LVC1G3208DCKT	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(DD5, DDJ, DDR)
SN74LVC1G3208DCKT.B	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(DD5, DDJ, DDR)
SN74LVC1G3208YZPR	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DDN
SN74LVC1G3208YZPR.B	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DDN

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G3208:

Automotive: SN74LVC1G3208-Q1

Enhanced Product : SN74LVC1G3208-EP

NOTE: Qualified Version Definitions:

- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G3208DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G3208DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G3208DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G3208DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G3208DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1G3208DCKT	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G3208DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G3208YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G3208DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G3208DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74LVC1G3208DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC1G3208DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74LVC1G3208DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74LVC1G3208DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1G3208DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1G3208YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

NanoFree Is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. NanoFree[™] package configuration.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
 For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025