SN74LVC1G3157-Q1 Automotive Single-Pole Double-Throw Analog Switch

1 Features

- Functional safety capable
  - Documentation available to aid functional safety system design
- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- ESD protection exceeds 2000V per MIL-STD-883, method 3015; exceeds 200V using machine model (C = 200pF, R = 0)
- 1.65V to 5.5V V_{CC} operation
- Useful for analog and digital applications
- Specified break-before-make switching
- Rail-to-rail signal handling
- High degree of linearity
- High speed, typically 0.5ns (V_{CC} = 3V, C_L = 50pF)
- Low ON-State resistance, typically approximately 6Ω (V_{CC} = 4.5V)
- Latch-up performance exceeds 100mA per JESD 78, Class II

2 Applications

- Advanced driver assistance systems (ADAS)

3 Description

The SN74LVC1G3157-Q1 device is a single-pole double-throw (SPDT) analog switch designed for 1.65V to 5.5V V_{CC} operation.

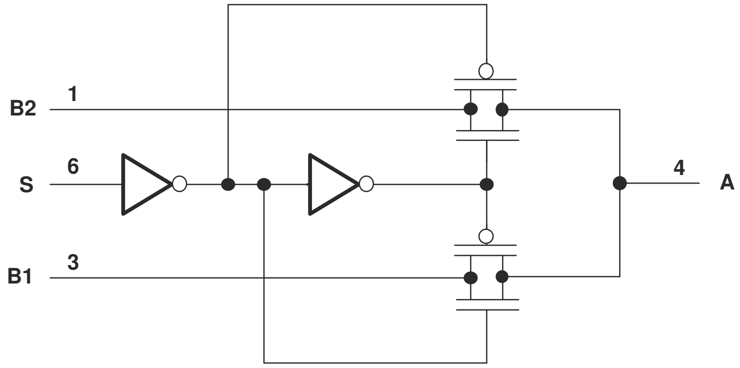
The SN74LVC1G3157 device can handle analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
SN74LVC1G3157-Q1	SOT-23 (6)	2.90mm × 1.60mm
	SC70 (6)	2.00mm × 1.25mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

Table of Contents

1 Features 1
2 Applications 1
3 Description 1
4 Pin Configuration and Functions 3
5 Specifications 4
  5.1 Absolute Maximum Ratings 4
  5.2 ESD Ratings 4
  5.3 Recommended Operating Conditions 5
  5.4 Thermal Information 5
  5.5 Electrical Characteristics 6
  5.6 Switching Characteristics 125C 7
  5.7 Analog Channel Specifications 8
  5.8 Typical Characteristics 9
6 Parameter Measurement Information 10
7 Detailed Description 16
  7.1 Overview 16
  7.2 Functional Block Diagram 16
  7.3 Feature Description 16
  7.4 Device Functional Modes 16
8 Application and Implementation 17
  8.1 Application Information 17
  8.2 Typical Application 17
9 Power Supply Recommendations 18
10 Layout 19
  10.1 Layout Guidelines 19
  10.2 Layout Example 19
11 Device and Documentation Support 20
  11.1 Documentation Support 20
  11.2 Receiving Notification of Documentation Updates 20
  11.3 Support Resources 20
  11.4 Trademarks 20
  11.5 Electrostatic Discharge Caution 20
  11.6 Glossary 20
12 Revision History 21
13 Mechanical, Packaging, and Orderable Information 21

4 Pin Configuration and Functions

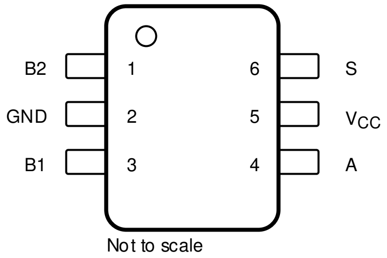


**Figure 4-1. DBV Package
6-Pin SOT-23
Top View**

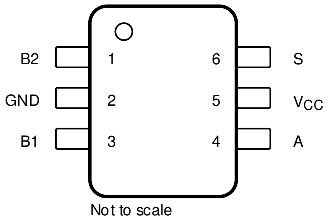


**Figure 4-2. DCK Package
6-Pin SC70
Top View**

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A	4	I/O	Common terminal
B1	3	I/O	First terminal
B2	1	I/O	Second terminal
GND	2	—	Ground
S	6	I	Select
V_{CC}	5	I	Power supply

(1) I = input, O = output, GND = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.5	6	V
V_{IN}	Control input voltage(2) (3)	-0.5	V_{DD} + 0.5V	V
$V_{I/O}$	Voltage range applied to any output in the high-impedance or power-off state(2) (3) (4) (5)	-0.5	6	V
I_{IK}	Control input clamp current $V_{IN} < 0$	-50		mA
$I_{I/O}$	I/O port diode current $V_{I/O} < 0$ or $V_{I/O} > V_{CC}$	-50		mA
$I_{I/O}$	On-state switch current(6) $V_{I/O}$ = 0 to V_{CC}	-128	128	mA
	Continuous current through V_{CC} or GND	-100	100	mA
T_J	Junction temperature		150	C
Storage temperature, T_{stg}		-65	150	C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(4) This value is limited to 5.5V maximum.
(5) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for $V_{I/O}$.
(6) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for $I_{I/O}$.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 1C		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	Other pins	±1000	V
			Corner pins (B2, B1, S, and A)	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1.65		5.5	V
$V_{I/O}$	Switch input or output voltage (Max of V_{CC})		0		V_{CC}	V
V_{IN}	Control input voltage		0		5.5	V
V_{IH}	High-level input voltage, control input (0.75*V_{CC})	V_{CC} = 1.65V to 1.95V	V_{CC}× 0.75			V
V_{IH}	High-level input voltage, control input (0.7*V_{CC})	V_{CC} = 2.3V to 5.5V	V_{CC}× 0.7			V
V_{IL}	Low-level input voltage, control input (0.25*V_{CC})	V_{CC} = 1.65V to 1.95V			V_{CC}× 0.25	V
V_{IL}	Low-level input voltage, control input (0.3*V_{CC})	V_{CC} = 2.3V to 5.5V			V_{CC}× 0.3	V
dt/dv	Input transition rise or fall rate	V_{CC} = 1.8 ± 0.15V			20	ns/V
		V_{CC} = 2.5 ± 0.2V			20	
		V_{CC} = 3.3V ± 0.3V			10	
		V_{CC} = 5V ± 0.5V			10	
T_A			-40		125	°C

(1) All unused inputs of the device must be held a V_{CC} or GND to ensure proper device operation. Refer to the *Implications of Slow or Floating CMOS Inputs* application note.

5.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G3157-Q1		UNIT
		DBV (SOT23)	DCK (SC70)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	258.2	286.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	182.8	224.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	142.8	143.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	118.4	124.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	142.2	142.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			V_{CC}	MIN	TYP[1]	MAX	UNIT
r_{on}	ON-state switch resistance[2]		See Figure 6-1 and Figure 5-1	V_I = 0V,	I_O = 4mA	1.65V		11	20	Ω
				V_I = 1.65V,	I_O = –4mA			15	50	
				V_I = 0V,	I_O = 8mA	2.3V		8	12	
				V_I = 2.3V,	I_O = –8mA			11	30	
				V_I = 0V,	I_O = 24mA	3V		7	9.5	
				V_I = 3V,	I_O = –24mA			9	20	
				V_I = 0V,	I_O = 30mA	4.5V		6	7.5	
				V_I = 2.4V,	I_O = –30mA			7	12	
				V_I = 4.5 ,	I_O = –30mA			7	15	
r_{range}	ON-state switch resistance over signal range[2] [3]		$0 \le V_{Bn} \le V_{CC}$ (see Figure 6-1 and Figure 5-1)		I_A = –4mA	1.65V			200	Ω
					I_A = –8mA	2.3V			75	
					I_A = –24mA	3V			25	
					I_A = –30mA	4.5V			15	
Δr_{on}	Difference in on-state resistance between switches[2] [4] [5]		See Figure 6-1	V_{Bn} = 1.15V,	I_A = –4mA	1.65V		0.5		Ω
				V_{Bn} = 1.6V,	I_A = –8mA	2.3V		0.1		
				V_{Bn} = 2.1V,	I_A = –24mA	3V		0.1		
				V_{Bn} = 3.15V,	I_A = –30mA	4.5V		0.1		
$r_{on(flat)}$	ON-state resistance flatness[2] [4] [6]		$0 \le V_{Bn} \le V_{CC}$		I_A = –4mA	1.65V		110		Ω
					I_A = –8mA	2.3V		26		
					I_A = –24mA	3V		9		
					I_A = –30mA	4.5V		4		
I_{off} [7]	OFF-state switch leakage current		$0 \le V_I, V_O \le V_{CC}$ (see Figure 6-2)			1.65V to 5.5V			±1	μA
								±0.05	±1[1]	
$I_{S(on)}$	ON-state switch leakage current		$V_I = V_{CC}$ or GND, V_O = Open (see Figure 6-3)			5.5V			±1	μA
									±0.1[1]	
I_{IN}	Control input current		$0 \le V_{IN} \le V_{CC}$			0V to 5.5V			±1	μA
								±0.05	±1[1]	
I_{CC}	Supply current		$V_{IN} = V_{CC}$ or GND			5.5V		1	10	μA
ΔI_{CC}	Supply-current change		$V_{IN} = V_{CC} – 0.6V$			5.5V			500	μA
C_{in}	Control input capacitance	S				5V		2.7		pF
$C_{io(off)}$	Switch I/O capacitance	Bn				5V		5.2		pF
$C_{io(on)}$	Switch I/O capacitance	Bn				5V		17.3		pF
		A						17.3		

(1) T_A = 25°C
(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages on the two (A or B) ports.
(3) Specified by design
(4) $\Delta r_{on} = r_{on(max)} – r_{on(min)}$ measured at identical V_{CC}, temperature, and voltage levels
(5) This parameter is characterized, but not tested in production.
(6) Flatness is defined as the difference between the maximum and minimum values of ON-state resistance over the specified range of conditions.
(7) I_{off} is the same as $I_{S(off)}$ (OFF-state switch leakage current).

5.6 Switching Characteristics 125C

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{pd} (1)	R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}	A or Bn	Bn or A	1.8V ± 0.15V			2	ns
				2.5V ± 0.2V			1.2	
				3.3V ± 0.3V			0.8	
				5V ± 0.5V			0.5	
t_{en} (2)	R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}	S	Bn	1.8V ± 0.15V	5		24	ns
				2.5V ± 0.2V	3.5		14	
				3.3V ± 0.3V	2.5		8	
				5V ± 0.5V	1.7		7	
t_{dis} (3)	R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}, V_{Δ} = 0.3V			1.8V ± 0.15V	3		13	
				2.5V ± 0.2V	2		7.5	
				3.3V ± 0.3V	1.5		6.5	
				5V ± 0.5V	0.8		5	
$T_{B\text{-}M}$ (4)	Break before make time			1.8V ± 0.15V	0.5			ns
				2.5V ± 0.2V	0.5			
				3.3V ± 0.3V	0.5			
				5V ± 0.5V	0.5			

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. The propagation delay is calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impednace).
(2) t_{en} is the slower of t_{PZL} or t_{PZH}.
(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ}.
(4) Specified by design

5.7 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
Frequency response (switch on)(1)	A or Bn	Bn or A	$R_L = 50\Omega$, f_{in} = sine wave	1.65V		300		MHz
				2.3V		300		
				3V		300		
				4.5V		300		
Crosstalk (between switches)(2)	B1 or B2	B2 or B1	$R_L = 50\Omega$, $f_{i\,n}$ = 10MHz (sine wave)	1.65V		-54		dB
				2.3V		-54		
				3V		-54		
				4.5V		-54		
Feed through attenuation (switch off)(2)	A or Bn	Bn or A	C_L = 5pF, $R_L = 50\Omega$, f_{in} = 10MHz (sine wave)	1.65V		-57		dB
				2.3V		-57		
				3V		-57		
				4.5V		-57		
Charge injection	S (Vs = VDD/2)	A	C_L = 0.1nF, $R_L = 1M\Omega$	3.3V		3		pC
				5V		7		
Total harmonic distortion	A or Bn	Bn or A	$V_I = 1.4V_{p\text{-}p}$, Vbias = Vcc/2, $R_L = 10k\Omega$, f_{in} = 600Hz to 20kHz (sine wave)	1.65V		0.5		%
			$V_I = 2.0\ V_{p\text{-}p}$, Vbias = Vcc/2, $R_L = 10k\Omega$, f_{in} = 600 Hz to 20kHz (sine wave)	2.3V		0.025		
			$V_I = 2.5V_{p\text{-}p}$, Vbias = Vcc/2, $R_L = 10k\Omega$, f_{in} = 600 Hz to 20kHz (sine wave)	3V		0.015		
			$V_I = 4.0V_{p\text{-}p}$, Vbias = Vcc/2, $R_L = 10k\Omega$, f_{in} = 600Hz to 20kHz (sine wave)	4.5V		0.01		

(1) Set fin to 0dBm and provide a bias of 0.4V. Increase fin frequency until the gain is 3dB below the insertion loss.
(2) Set fin to 0dBm and provide a bias of 0.4V.

5.8 Typical Characteristics

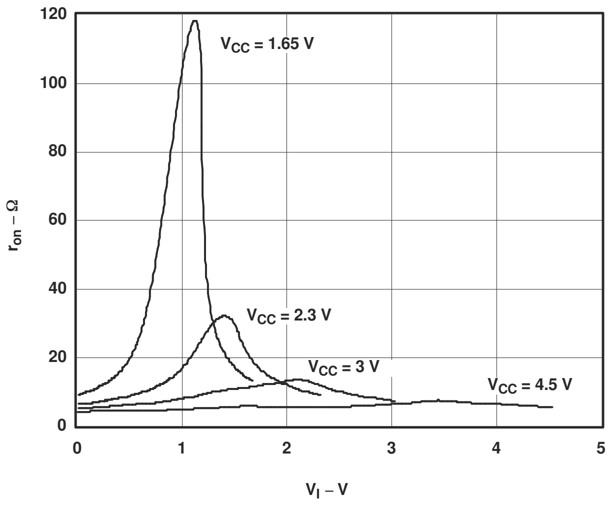


Figure 5-1. Typical R_{on} as a Function of Input Voltage (V_I) for V_I = 0 To V_{CC}

6 Parameter Measurement Information

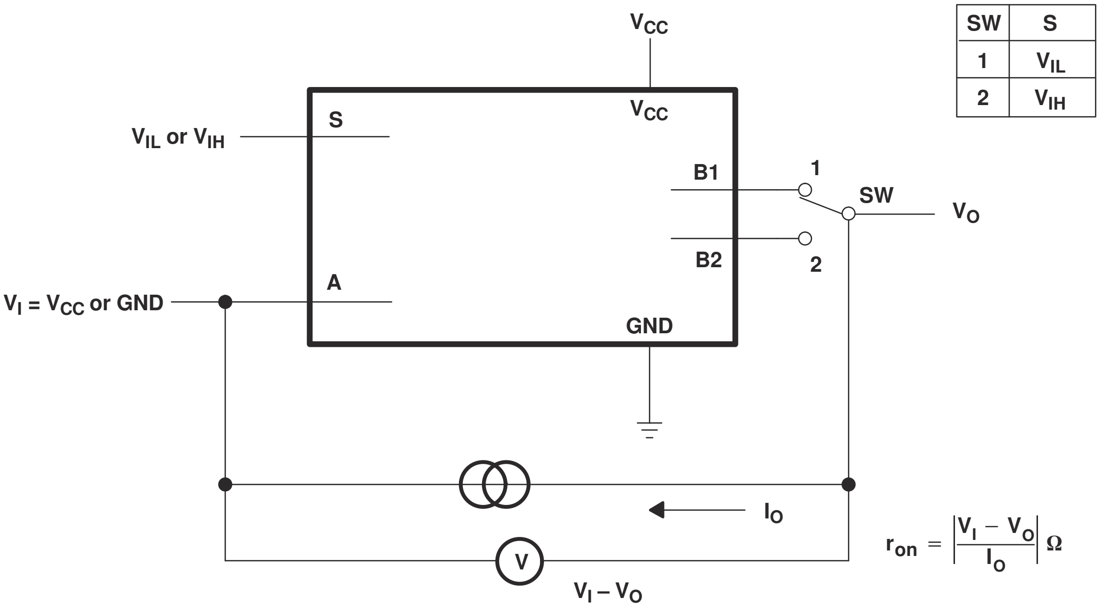
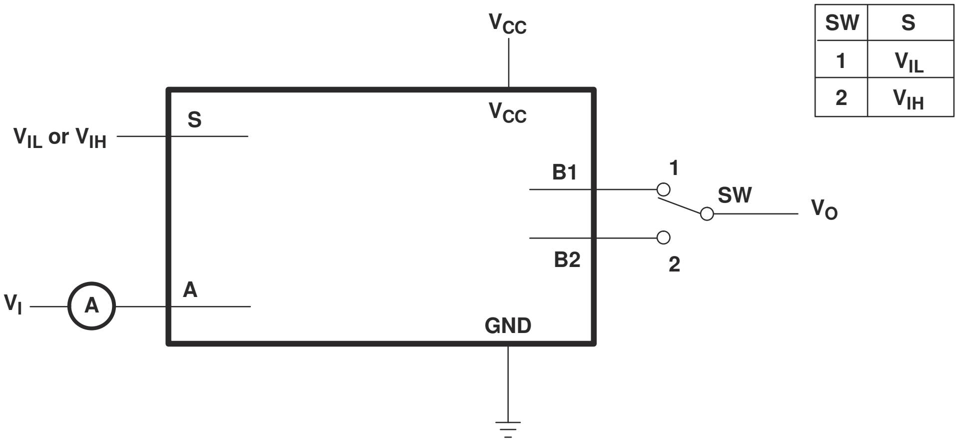


Figure 6-1. ON-State Resistance Test Circuit



Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 6-2. OFF-State Switch Leakage-Current Test Circuit

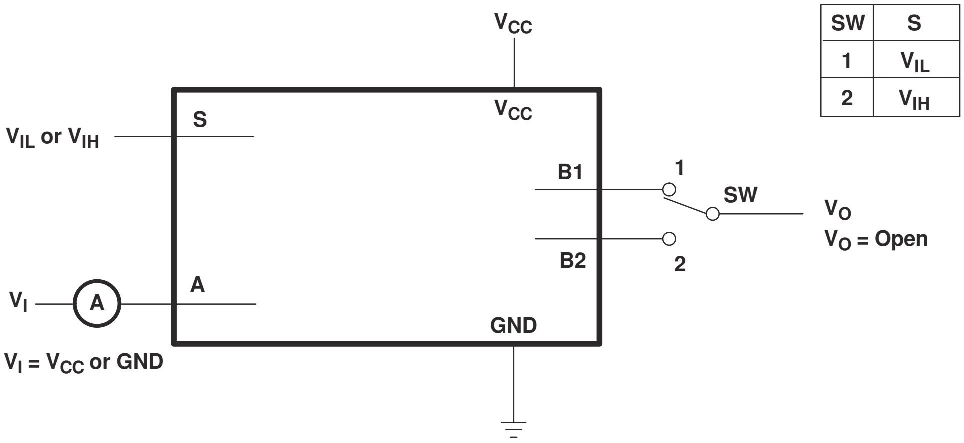
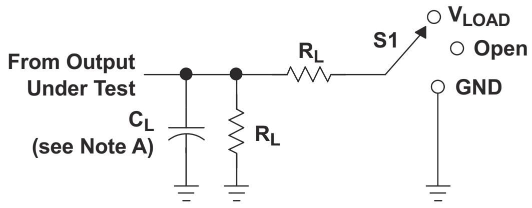


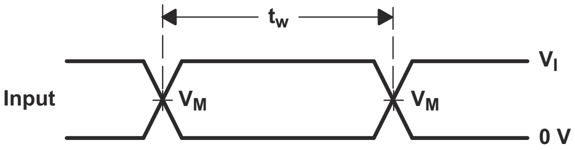
Figure 6-3. ON-State Switch Leakage-Current Test Circuit



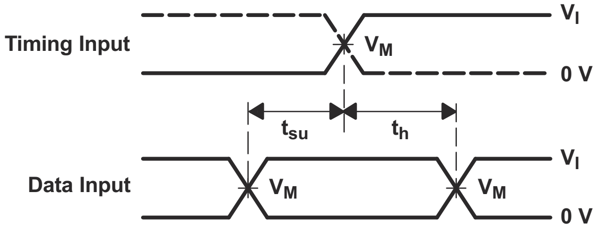
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

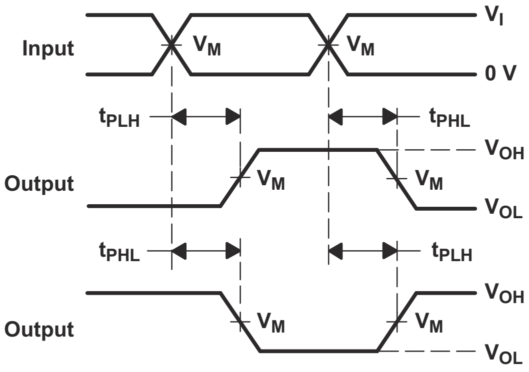
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



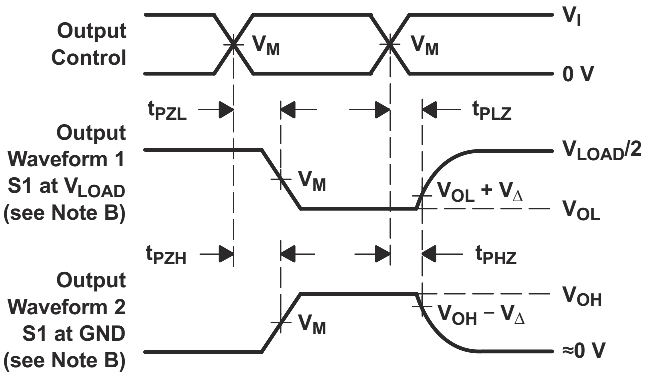
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



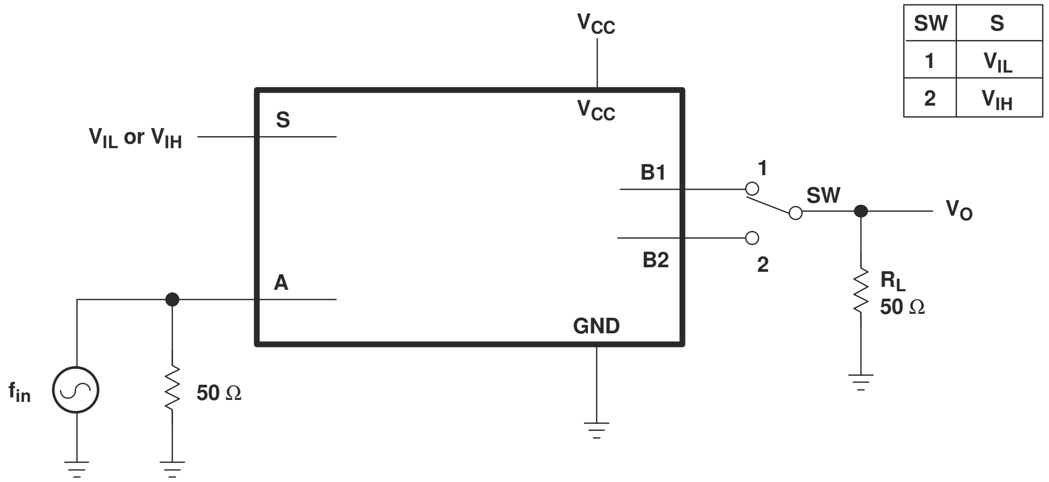
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

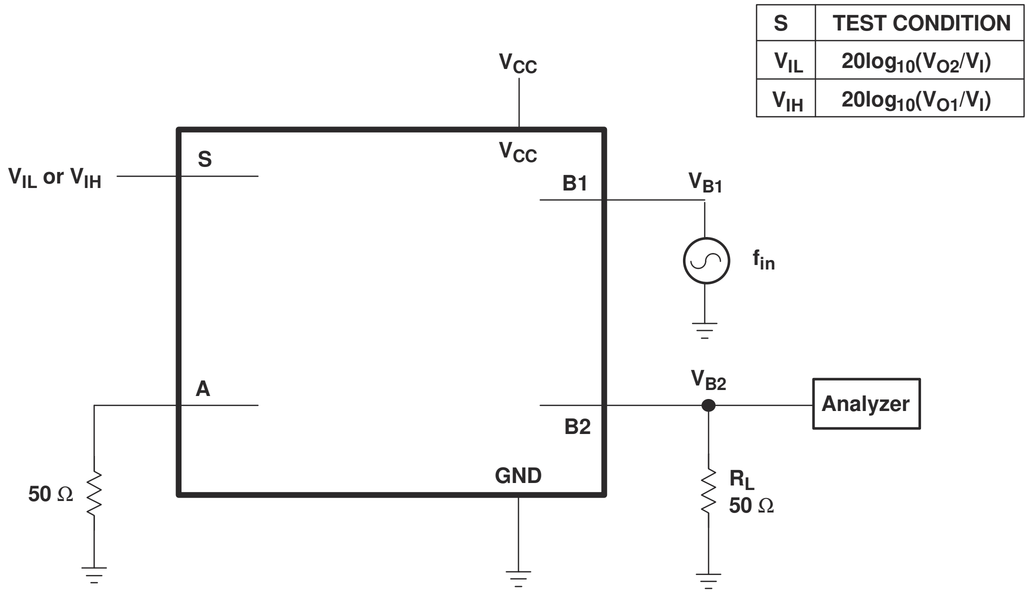
NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10-MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-4. Load Circuit and Voltage Waveforms



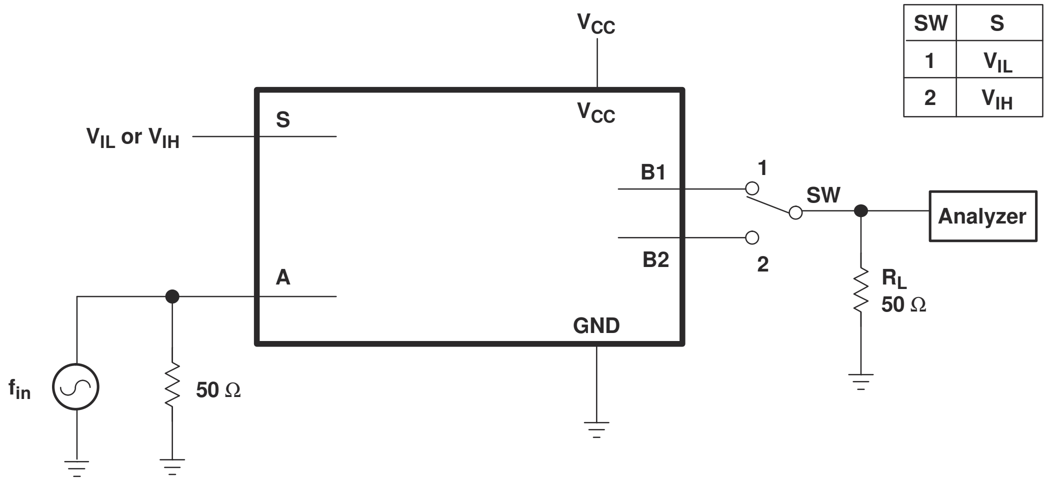
SW	S
1	V_{IL}
2	V_{IH}

Figure 6-5. Frequency Response (Switch On)



S	TEST CONDITION
V_{IL}	$20\log_{10}(V_{O2}/V_I)$
V_{IH}	$20\log_{10}(V_{O1}/V_I)$

Figure 6-6. Crosstalk (Between Switches)



SW	S
1	V_{IL}
2	V_{IH}

Figure 6-7. Feedthrough

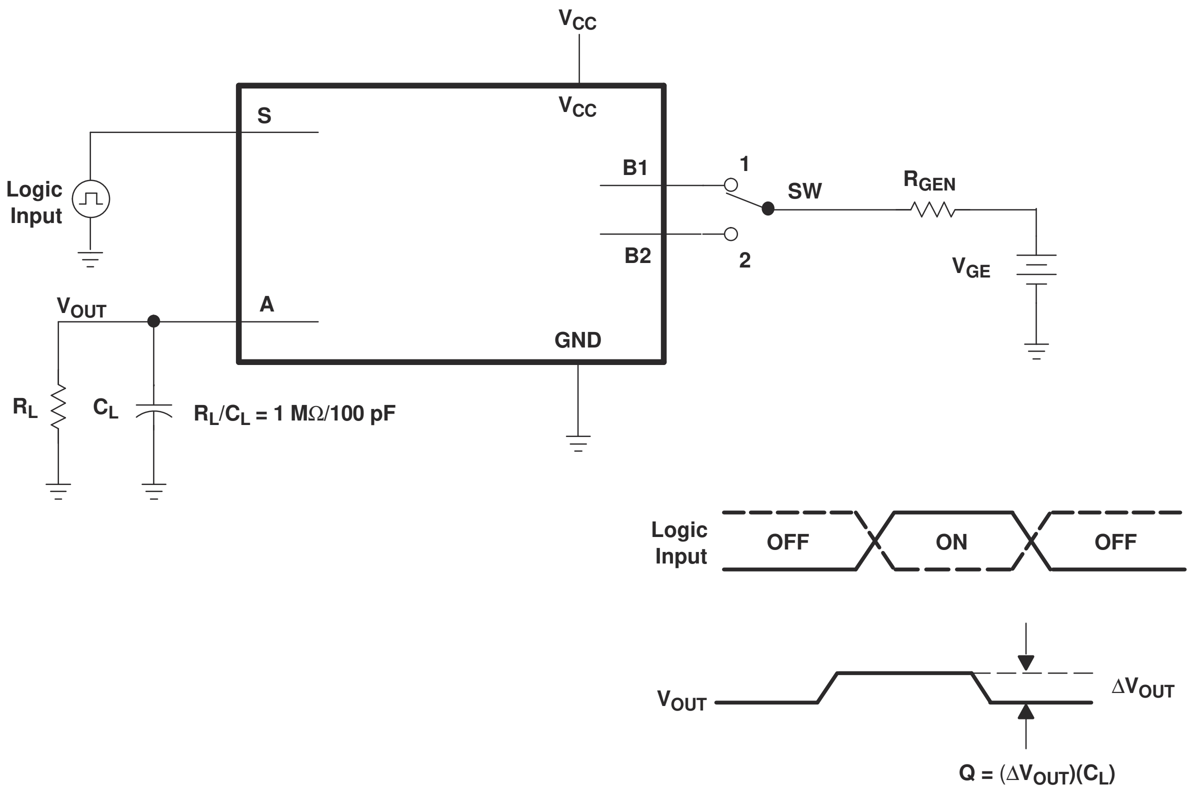
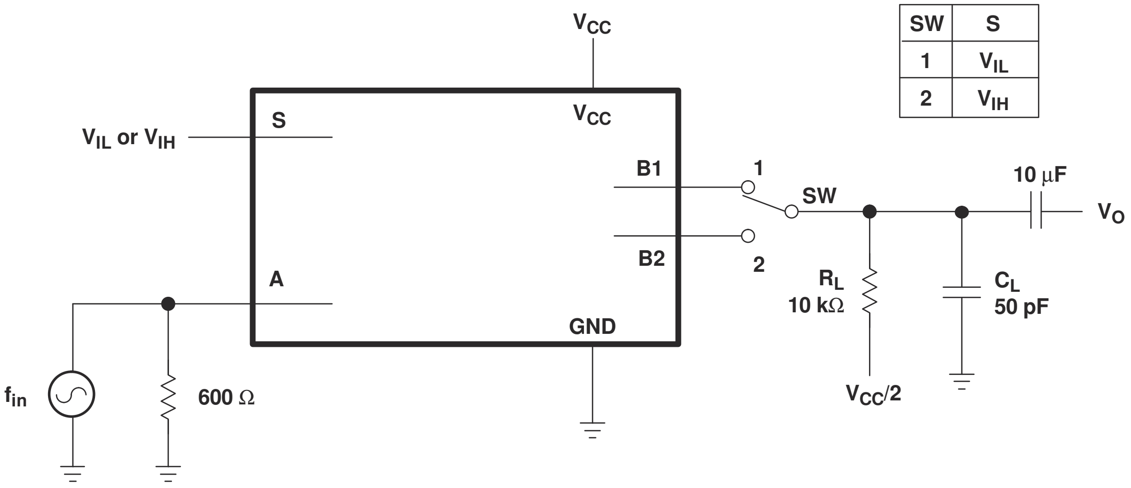


Figure 6-8. Charge-Injection Test



SW	S
1	V_{IL}
2	V_{IH}

V_{CC} = 1.65 V, V_I = 1.4 V_{P-P}
V_{CC} = 2.30 V, V_I = 2.0 V_{P-P}
V_{CC} = 3.00 V, V_I = 2.5 V_{P-P}
V_{CC} = 4.50 V, V_I = 4.0 V_{P-P}

Figure 6-9. Total Harmonic Distortion

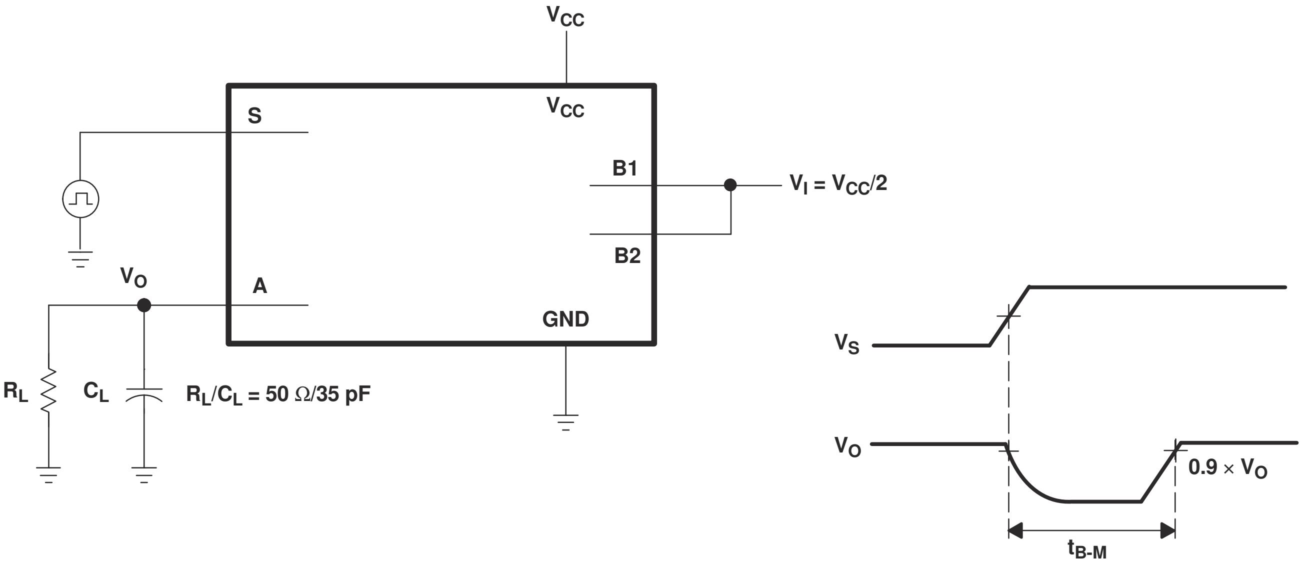


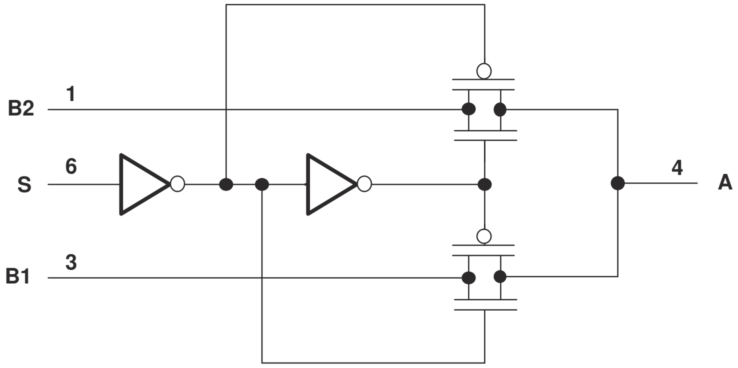
Figure 6-10. Break-Before-Make Internal Timing

7 Detailed Description

7.1 Overview

The SN74LVC1G3157-Q1 device is a single-pole double-throw (SPDT) analog switch designed for 1.65V to 5.5V V_{CC} operation. The SN74LVC1G3157-Q1 device can handle analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Feature Description

These devices are qualified for automotive applications. The 1.65V to 5.5V supply operation allows the device to function in many different systems comprised of different logic levels, allowing rail-to-rail signal switching. Either the B1 channel or the B2 channel is activated depending upon the control input. If the control input is low, B1 channel is selected. If the control input is high, B2 channel is selected.

7.4 Device Functional Modes

Table 7-1 lists the ON channel when one of the control inputs is selected.

Table 7-1. Function Table

CONTROL INPUTS	ON CHANNEL
L	B1
H	B2

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G3157-Q1 SPDT analog switch is flexible enough for use in a variety of circuits such as analog audio routing, power-up monitor, memory sharing and so on. For details on the applications, you can also view the SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches product overview.

8.2 Typical Application

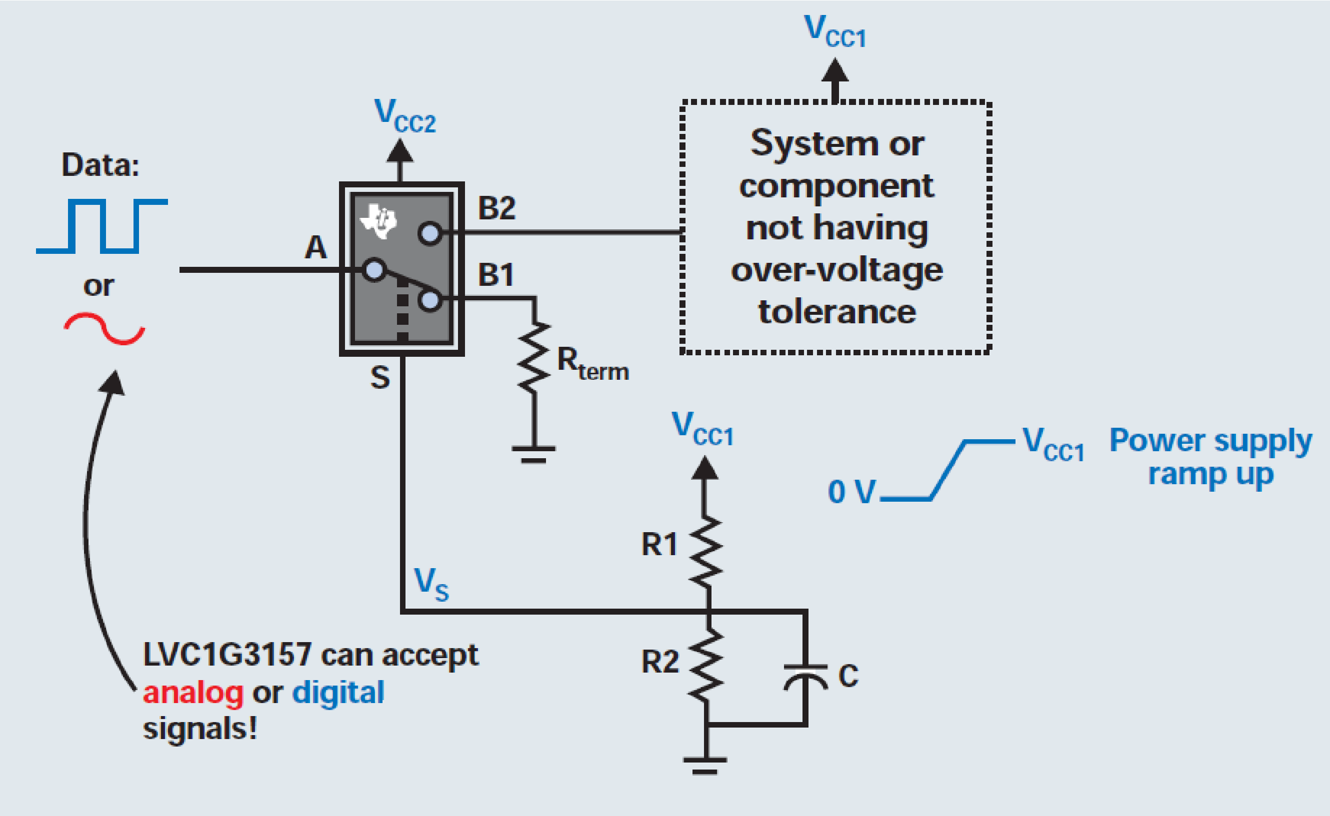


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

The inputs can be analog or digital, but TI recommends waiting until VCC has ramped to a level in *Section 5.3* before applying any signals. Appropriate termination resistors should be used depending on the type of signal and specification. The Select pin should not be left floating; either pull up or pull down with a resistor that can be overdriven by a GPIO.

8.2.2 Detailed Design Procedure

Using this circuit idea, a system designer can ensure a component or subsystem power has ramped up before allowing signals to be applied to its input. This is useful for integrated circuits that do not have overvoltage tolerant inputs. The basic idea uses a resistor divider on the VCC1 power rail, which is ramping up. The RC time constant of the resistor divider further delays the voltage ramp on the select pin of the SPDT bus switch. By carefully selecting values for R1, R2 and C, it is possible to ensure that VCC1 will reach its nominal value before the path from A to B2 is established, thus preventing a signal being present on an I/O before the device/system is powered up. To ensure the minimum desired delay is achieved, the designer should use Equation 1 to calculate the time required from a transition from ground (0V) to half the supply voltage (VCC1/2).

$$\text{Set}\left(\frac{R2}{R1+R2}\times V_{CC1} > V_{IH}\right)\text{of the select pin} \tag{1}$$

Choose Rs and C to achieve the desired delay.

When Vs goes high, the signal will be passed.

8.2.3 Application Curve

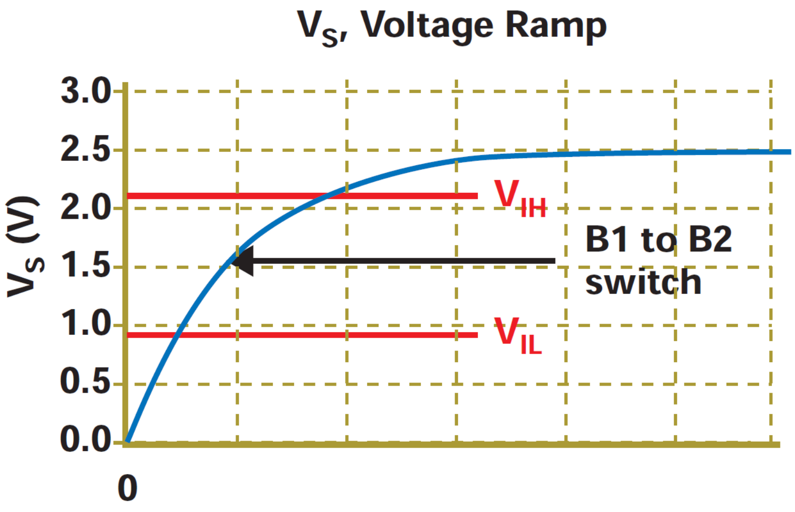


Figure 8-2. V_S Voltage Ramp

9 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the V_{CC} pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can be used to provide supply to this device from another voltage rail.

10 Layout

10.1 Layout Guidelines

TI recommends keeping signal lines as short as possible. TI also recommends incorporating microstrip or stripline techniques when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50Ω or 75Ω, as required by the application. Do not place this device too close to high-voltage switching components, as they may interfere with the device.

10.2 Layout Example

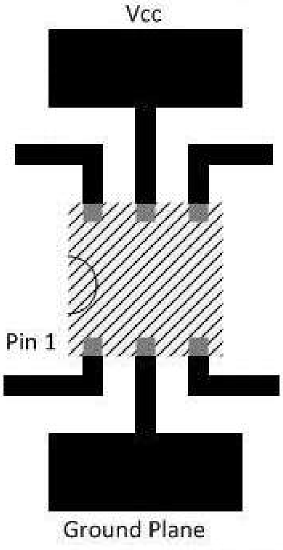


Figure 10-1. Recommended Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches* product overview
- Texas Instruments, *SN74LVC1G3157-Q1 Functional Safety, FIT Rate, FMD, and Pin FMA* report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (December 2021) to Revision I (June 2025)	Page
• Changed ABS max V_{CC} and $V_{I/O}$ voltage	4
• Updated thermal parameters for DBV and DCK	5
• Updated r_{range}	6
• Changed enable timing for minimum 1.8V, and maximum 3.3V and 5V	7
• Changed disable timing for maximum 3.3V and 5V	7
• Changed THD at 1.65V r_{range}	8

Changes from Revision G (April 2019) to Revision H (December 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added functional safety text to the data sheet	1

Changes from Revision F (March 2015) to Revision G (April 2019)	Page
• Changed the automotive *Features*	1
• Changed the *Pin Configuration* images	3

Changes from Revision E (April 2008) to Revision F (March 2015)	Page
• Added *ESD Rating*s table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
1P1G3157QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5O
1P1G3157QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5O
1P1G3157QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5O
1P1G3157QDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C5J, C5O)
1P1G3157QDCKRQ1.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C5J, C5O)
1P1G3157QDCKRQ1.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C5J, C5O)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G3157-Q1 :

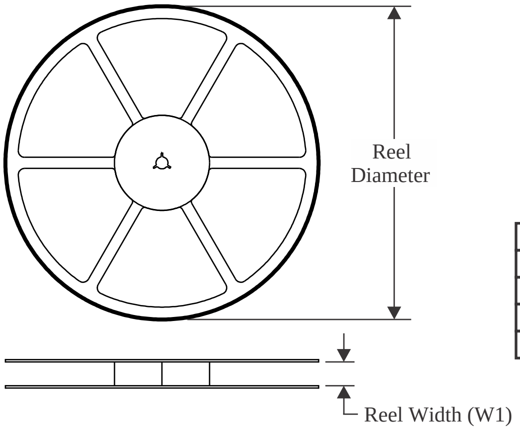
- Catalog : SN74LVC1G3157

NOTE: Qualified Version Definitions:

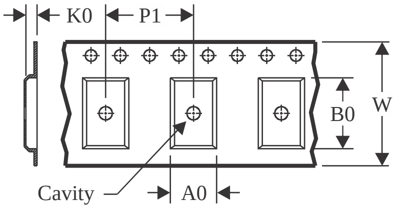
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

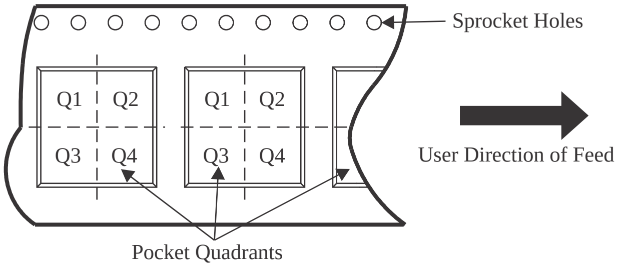


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

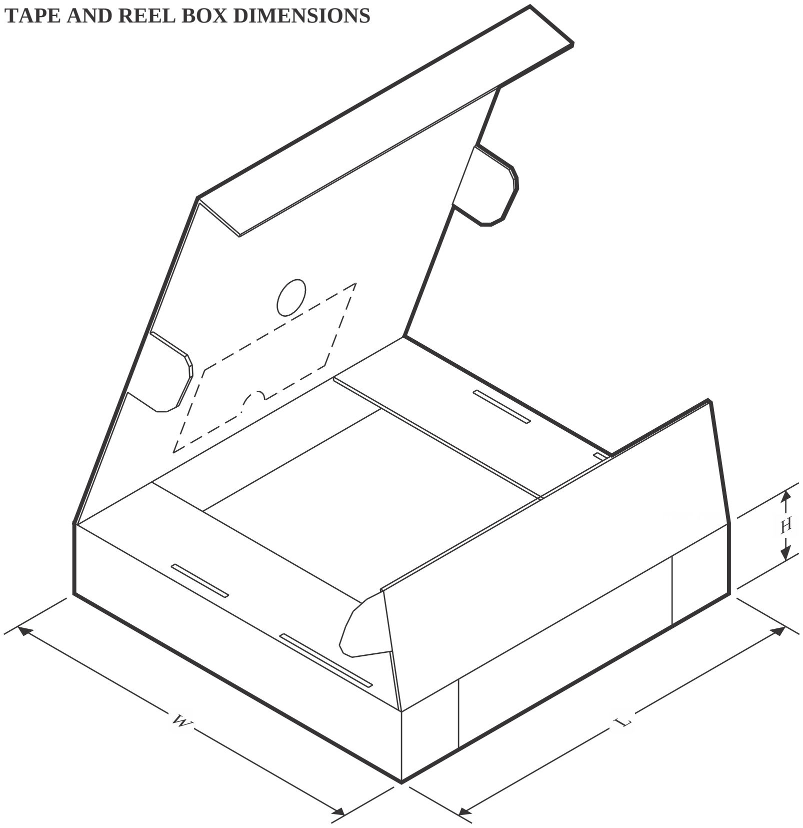
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

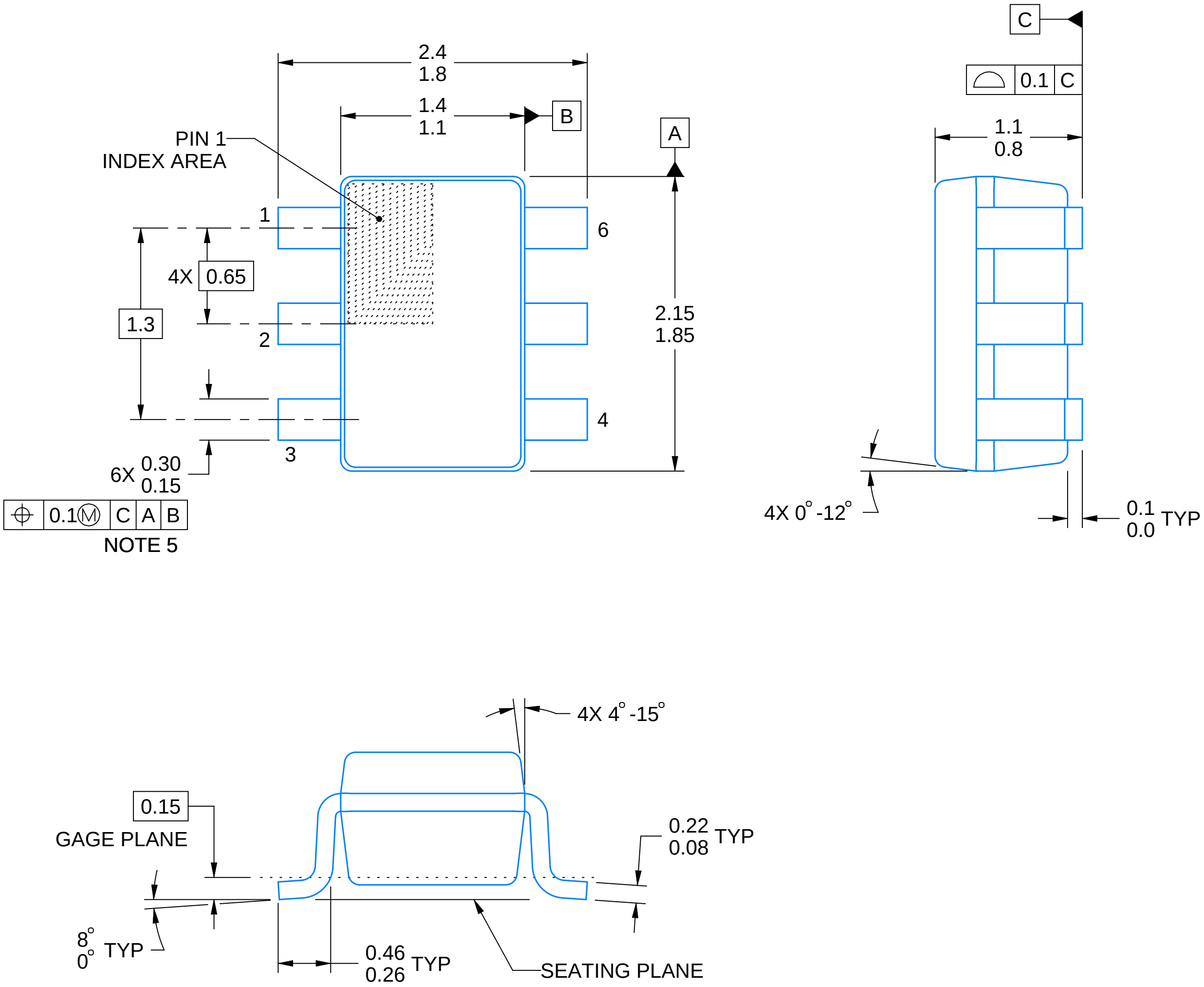
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
1P1G3157QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
1P1G3157QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

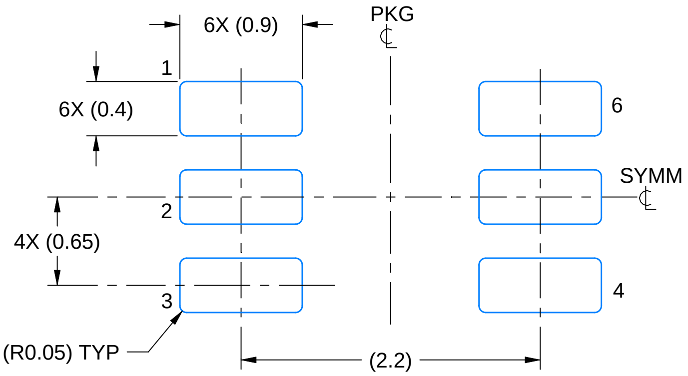
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
1P1G3157QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
1P1G3157QDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0



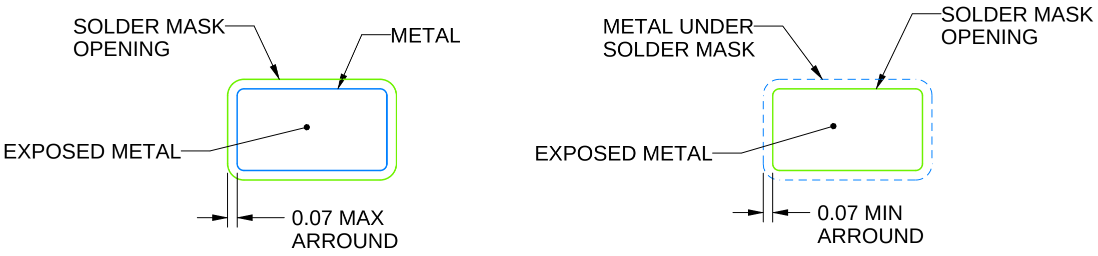
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



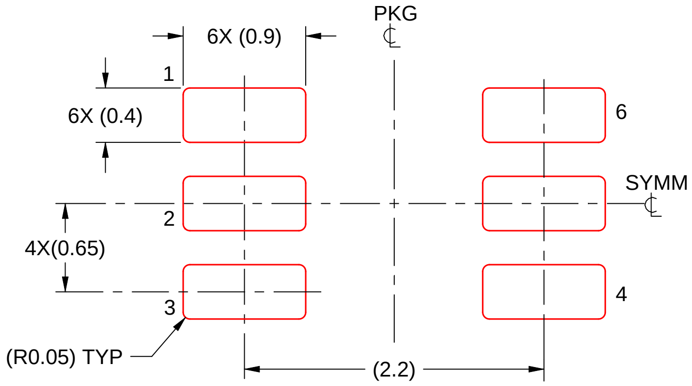
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

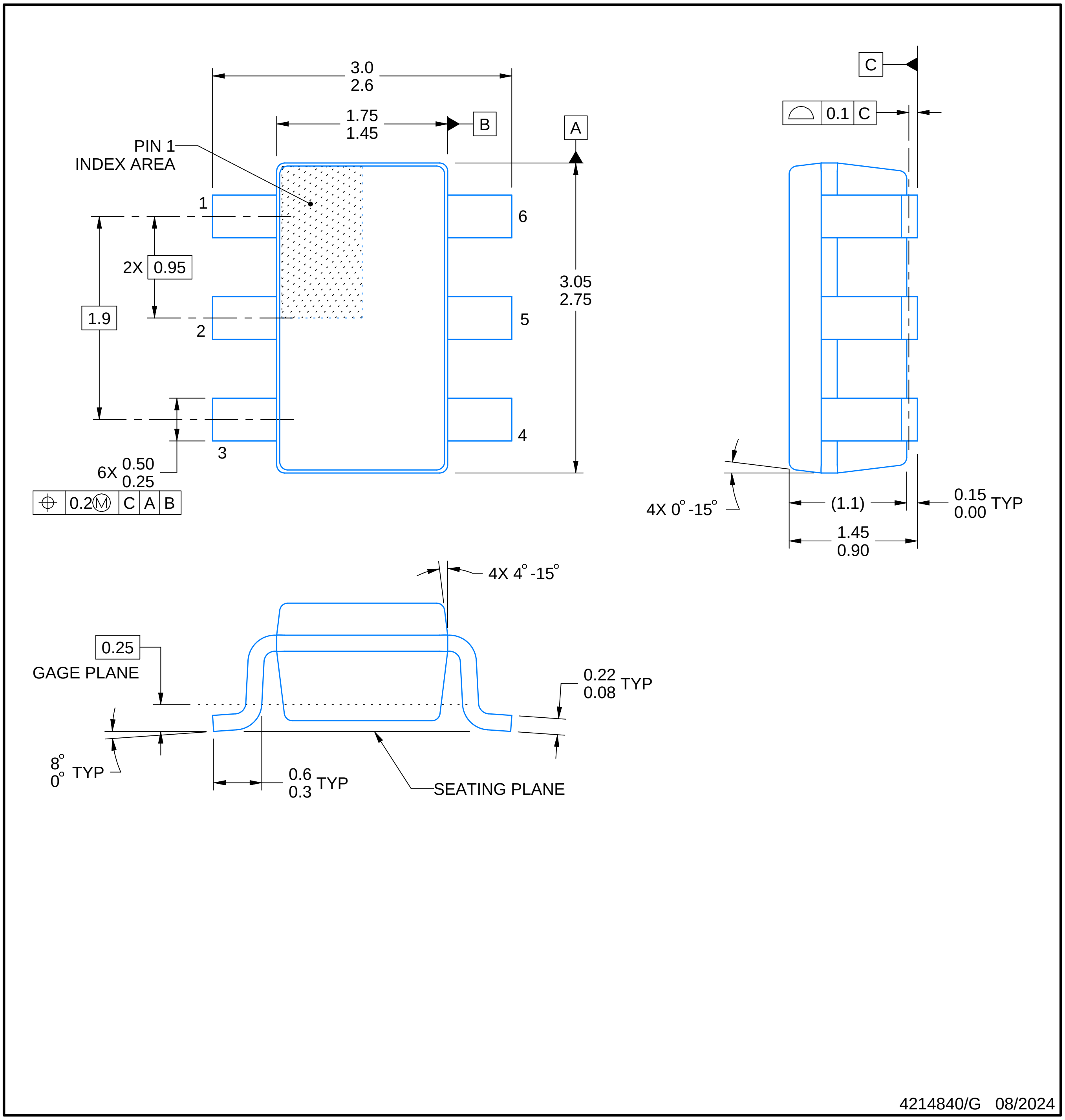
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

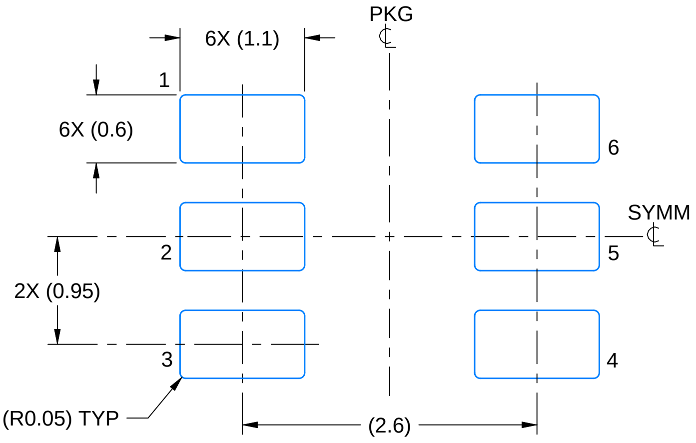
SMALL OUTLINE TRANSISTOR



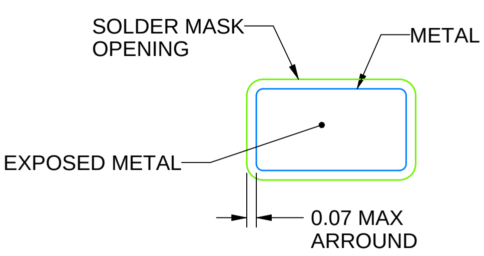
4214840/G 08/2024

NOTES:

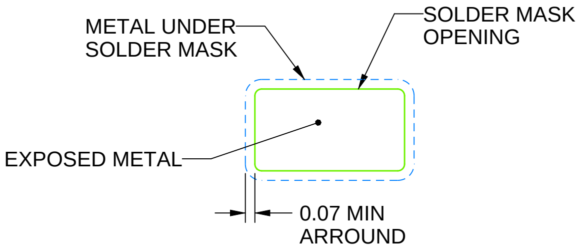
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

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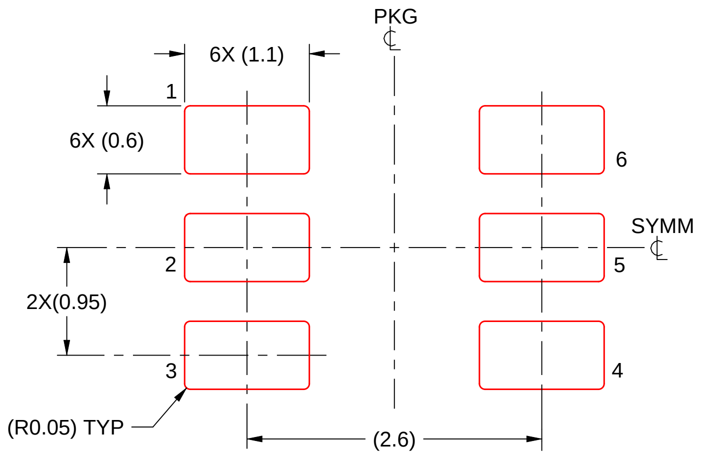
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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