

# SN74LVC1G29 2-of-3 Decoder/Demultiplexer

Check for Samples: SN74LVC1G29

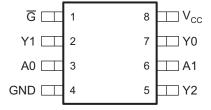
## **FEATURES**

- Available in the Texas Instruments
   NanoFree™ Package
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V<sub>CC</sub>
- Max t<sub>pd</sub> of 5.1 ns at 3.3 V
- Low Power Consumption, 10-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### YZP PACKAGE (BOTTOM VIEW)

		1
GND	0450	Y2
A0	0360	A1
Y1	0270	Y0
G	0180	$V_{cc}$

#### DCT PACKAGE (TOP VIEW)



See mechanical drawings for dimensions.

#### DESCRIPTION

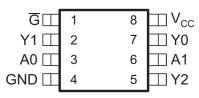
This decoder is designed for 1.65-V to 5.5-V  $V_{\rm CC}$  operation.

The SN74LVC1G29 device is a  $\underline{\hspace{0.1cm}}$  2-of-3 decoder/demultiplexer. When the enable ( $\overline{\hspace{0.1cm}}$ G) input signal is low, only one of the outputs is in the low state, depending on the input levels of A0 and A1. When  $\overline{\hspace{0.1cm}}$ G is high, Y0, Y1, and Y2 are high, regardless of the input states.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disable the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree<sup>™</sup> package technology is a major breakthrough in IC packaging concepts, using the die as the package.

# DCU PACKAGE (TOP VIEW)



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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



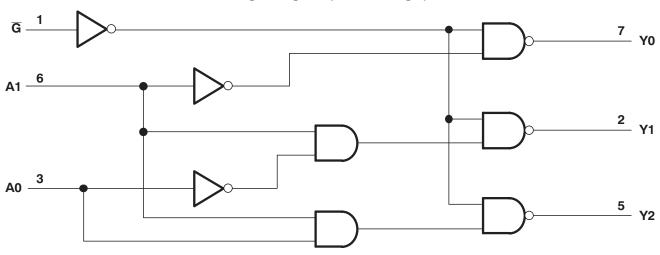


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## **Function Table**

	INPUTS			OUTPUTS	
G	<b>A</b> 1	A0	Y0	Y1	Y2
L	L	Х	L	Н	Н
L	Н	L	Н	L	Н
L	Н	Н	Н	Н	L
Н	Χ	Χ	Н	Н	Н

# **Logic Diagram (Positive Logic)**



# **Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range <sup>(2)</sup>		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power-off state (2)			6.5	V
Vo	Voltage range applied to any output in the high or lo	w state <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
		DCT package		220	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DCU package		227	°C/W
		YZP package		102	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.
- 4) The package thermal impedance is calculated in accordance with JESD 51-7.

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# **Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
,	Complement	Operating	1.65	5.5	V
√ <sub>CC</sub>	Supply voltage	Data retention only	1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
,	I Pak Jawa Canada adha na	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3.0 V to 3.6 V	2		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
,	Lavo lavol Spant valta as	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	V
$V_{IL}$	Low-level input voltage	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		0.8	V
	Supply voltage  High-level input voltage  Low-level input voltage  Input voltage  Output voltage  High-level output current  Low-level output current  v Input transition rise or fall rate  Operating free-air temperature	V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
ОН	High-level output current	evel output current		-16	mΑ
		V <sub>CC</sub> = 3 V		-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
OL	Low-level output current			16	mΑ
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/\
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

<sup>(1)</sup> All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



# **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
	$I_{OH} = -100 \ \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1			
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
<b>V</b>	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V
$V_{OH}$	$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V
	$I_{OH} = -24 \text{ mA}$	3 V	2.3			
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
<b>V</b>	I <sub>OL</sub> = 8 mA	2.3 V			0.3	V
$V_{OL}$	I <sub>OL</sub> = 16 mA	2.1/			0.4	V
	I <sub>OL</sub> = 24 mA	3 V	2.3 V 1.9 3 V 2.4 2.3 4.5 V 3.8 V to 5.5 V 6.65 V 2.3 V 3 V 4.5 V 0 5.5 V 0 V to 5.5 V to 5.5 V	0.55		
	$_{OH} = -4 \text{ mA}$ 1.65 V 1.2 $_{OH} = -8 \text{ mA}$ 2.3 V 1.9 $_{OH} = -16 \text{ mA}$ 3 V 2.4 $_{OH} = -24 \text{ mA}$ 3.8 $_{OH} = -32 \text{ mA}$ 4.5 V 3.8 $_{OL} = 100 \text{ μA}$ 1.65 V to 5.5 V 1.65 V 1		0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1	μΑ
I <sub>off</sub>	$V_1$ or $V_0 = 5.5 \text{ V}$	0			±10	μΑ
I <sub>CC</sub>	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ
$\Delta I_{CC}$	One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND	3 V to 5.5 V		·	500	μΑ
Cı	$V_I = V_{CC}$ or GND	3.3 V		3.5		pF

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

# **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L$  = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or $\overline{G}$	Υ	2.5	15.4	1.5	7.1	1	5.1	0.5	4.2	ns

# **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.	1.8 V 15 V			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or $\overline{G}$	Υ	2.5	15.8	1.5	7.5	1	6.1	0.5	5.1	ns

# **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

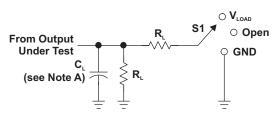
	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	V <sub>CC</sub> = 3.3 V TYP	V <sub>CC</sub> = 5 V TYP	UNIT
_	Power dissipation	G to Y1	f 40 MH=	17	17	18	19	pF
C <sub>pd</sub>	capacitance	A1 to Yn	f = 10 MHz	33	33	33	35	pΕ

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Product Folder Links: SN74LVC1G29



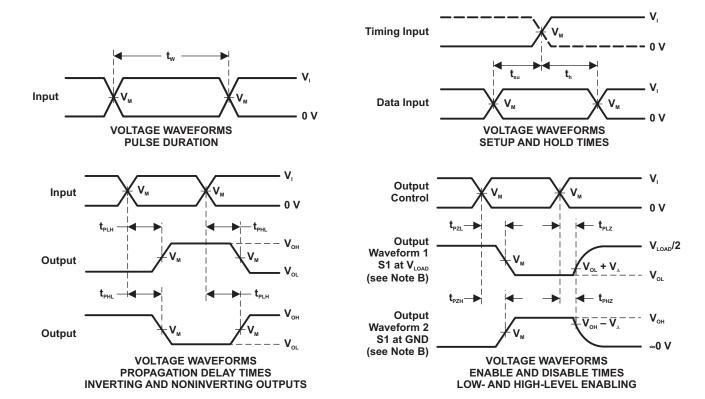
#### **Parameter Measurement Information**



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
$t_{_{\mathrm{PLZ}}}/t_{_{\mathrm{PZL}}}$	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

LOAD CIRCUIT

.,	INI	PUTS		v	C,	_	.,
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	V <sub>M</sub> V <sub>LOAD</sub>		R <sub>∟</sub>	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 M</b> Ω	0.15 V
2.5 V ± 0.2 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 M</b> Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	<b>1 M</b> Ω	0.3 V
5 V ± 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 M</b> Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

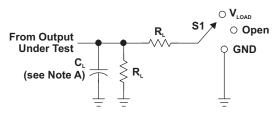
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $\dot{t}_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{\mbox{\tiny PZL}}$  and  $t_{\mbox{\tiny PZH}}$  are the same as  $t_{\mbox{\tiny en}}.$
- G.  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  are the same as  $t_{\text{pd}}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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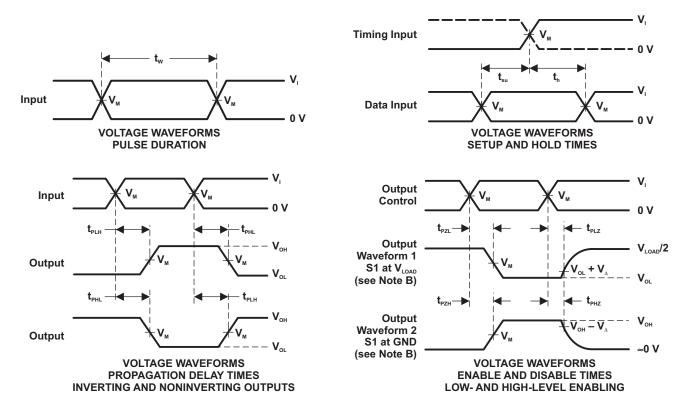
### **Parameter Measurement Information (continued)**



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
$t_{_{\mathrm{PLZ}}}/t_{_{\mathrm{PZL}}}$	<b>V</b> <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

LOAD CIRCUIT

.,	INI	PUTS		V		-	.,
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	<b>V</b> <sub>LOAD</sub>	C <sub>L</sub>	$R_{\scriptscriptstyle L}$	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V ± 0.2 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	500 $\Omega$	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V ± 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	500 $\Omega$	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $\dot{t}_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{\text{PZL}}$  and  $t_{\text{PZH}}$  are the same as  $t_{\text{en}}$ .
- G.  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  are the same as  $t_{\text{pd}}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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# **REVISION HISTORY**

Changes from Revision B (January 2007) to Revision C					
•	Updated document to new TI data sheet format.	1			
•	Deleted Ordering Information table.	1			
•	Updated Features.	1			
•	Added ESD warning.	<u>2</u>			

Product Folder Links : SN74LVC1G29

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74LVC1G29DCTR	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(2WD5, C29) (R, Z)
SN74LVC1G29DCTR.B	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2WD5, C29) (R, Z)
SN74LVC1G29DCUR	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(C29J, C29Q, C29R)
SN74LVC1G29DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(C29J, C29Q, C29R)
SN74LVC1G29DCUT	Active	Production	VSSOP (DCU)   8	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(C29J, C29Q, C29R)
SN74LVC1G29DCUT.B	Active	Production	VSSOP (DCU)   8	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(C29J, C29Q, C29R)
SN74LVC1G29DCUT1G4.B	Active	Production	VSSOP (DCU)   8	250   SMALL T&R	-	Call TI	Call TI	-40 to 85	
SN74LVC1G29YZPR	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D9N
SN74LVC1G29YZPR.B	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D9N

<sup>(1)</sup> **Status:** For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

www.ti.com 10-Nov-2025

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**PACKAGE MATERIALS INFORMATION** 

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# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G29DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1G29DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G29DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G29DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G29YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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#### \*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G29DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC1G29DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC1G29DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC1G29DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC1G29YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0





### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



# NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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