SN74LVC1G175B-Q1 Automotive Single D-Type Flip-Flop With Asynchronous Clear

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
- Operating range from 1.1V to 5.5V
- 5.5V tolerant input pins
- Supports standard pinouts
- Latch-up performance exceeds 100mA per JESD 78

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED

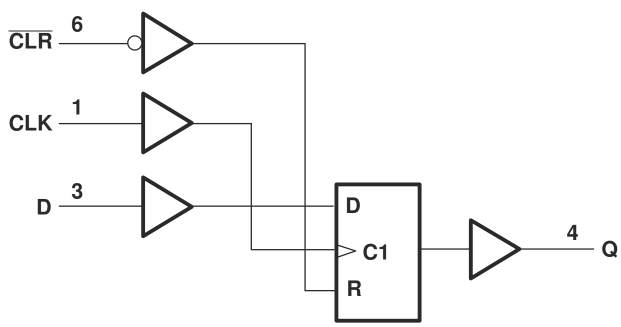
3 Description

The SN74LVC1G175B-Q1 device is a single D-type flip-flop with asynchronous clear ($\overline{CLR}$) input. When $\overline{CLR}$ is HIGH, data from the input pin (D) transfers to the output pin (Q) on the rising edge of the clock (CLK). When $\overline{CLR}$ is LOW, the Q is forced into the LOW state, regardless of the clock edge or data on D.

Package Information

PART NUMBER	PACKAGE[(1)]	PACKAGE SIZE[(2)]	BODY SIZE[(3)]
SN74LVC1G175B-Q1	DBV (SOT-23, 6)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC70, 6)	2mm × 2.1mm	2mm × 1.25mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram

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4 Pin Configuration and Functions

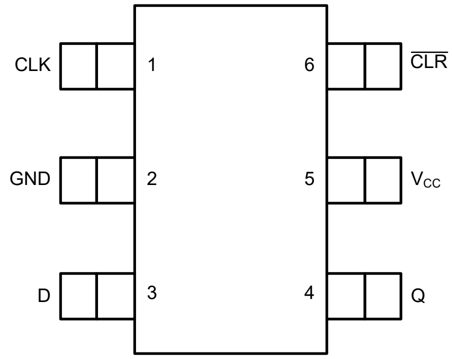


Figure 4-1. DBV or DCK Package, 6-Pin SOT-23 or SOT-SC70 (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CLK	1	I	Clock input
GND	2	G	Ground Pin
D	3	I	Data input
Q	4	O	Output
V_{CC}	5	P	Positive supply
$\overline{CLR}$	6	I	Asynchronous clear pin

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range[2]		-0.5	6.5	V
V_O	Output voltage range[2]		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	(High or low state)	0	V_{CC}	V
V_{IH}	High-level input voltage	V_{CC} = 1.1V to 1.95V	0.65x Vcc		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3.0V to 3.6V	2		
		V_{CC} = 4.5V to 5.5V	0.7x Vcc		
V_{IL}	Low-Level input voltage	V_{CC} = 1.1V to 1.95V		0.35x Vcc	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3.0V to 3.6V		0.8	
		V_{CC} = 4.5V to 5.5V		0.3x Vcc	
I_{OH}	High-level output current	V_{CC} = 1.65V		-4	mA
		V_{CC} = 2.3V		-8	
		V_{CC} = 3.0V		-16	
				-24	
		V_{CC} = 4.5V		-32	

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3.0V		16	
				24	
		V_{CC} = 4.5V		32	
Δt/Δv	Input transition rise or fall rate	V_{cc} = 1.2V to 2.5V		20	ns/V
		V_{cc} = 3.3V ± 0.3V		10	
		V_{cc} = 5.0V ± 0.5V		5	
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC[1]						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23, 6)	6	357.1	263.7	264.4	195.6	262.2	-	°C/W
DCK (SOT-SC70, 6)	6	371.0	297.5	258.6	195.6	256.2	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH}= –100μA	1.1V to 5.5V	V_{CC} - 0.1			V_{CC} - 0.1			V
	I_{OH}= –4mA	1.65V	1.2			1.2			V
	I_{OH}= –8mA	2.3V	1.9			1.9			V
	I_{OH}= –12mA	2.7V	2.2			2.2			V
	I_{OH}= –16mA	3V	2.4			2.4			V
	I_{OH}= –24mA	3V	2.3			2.3			V
	I_{OH}= –32mA	4.5V	3.8			3.8			V
V_{OL}	I_{OL}= 100μA	1.1V to 5.5V			0.1			0.15	V
	I_{OL}= 4mA	1.65V			0.24			0.45	V
	I_{OL}= 8mA	2.3V			0.3			0.3	V
	I_{OL}= 12mA	2.7V			0.4			0.4	V
	I_{OL}= 16mA	3V			0.4			0.4	V
	I_{OL}= 24mA	3V			0.55			0.55	V
	I_{OL}= 32mA	4.5V			0.55			0.55	V
I_I	V_I = V_{CC} or GND	V_{CC} = 0V to 5.5V			±1			±5	μA
I_{OFF}	V_I or V_O = V_{CC}	V_{CC} = 0V			±1			±10	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 1.1V to 5.5V			1			10	μA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	3.0V to 5.5V			500			500	μA
C_I	V_I = V_{CC} or GND	3.3V		3.5			3.5		pF

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
C_O	$V_O = V_{CC}$ or GND	3.3V		6.3					pF

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
f_{clock}	Clock frequency		1.2V ± 0.1V			32	MHz
			1.5V ± 012V			70	
			1.8V ± 0.15V			110	
			2.5V ± 0.2V			196	
			3.3V ± 0.3V			262	
			5V ± 0.5V			353	
t_W	Pulse duration	$\overline{CLR}$ low	1.2V ± 0.1V	6.4			ns
			1.5V ± 012V	2.5			
			1.8V ± 0.15V	2			
			2.5V ± 0.2V	1.1			
			3.3V ± 0.3V	1.1			
			5V ± 0.5V	1.1			
		CLK high or low	1.2V ± 0.1V	8.7			
			1.5V ± 012V	3.2			
			1.8V ± 0.15V	2.6			
			2.5V ± 0.2V	1.5			
			3.3V ± 0.3V	1.1			
			5V ± 0.5V	1.1			
t_{SU}	Setup time before CLK↑	Data before CLK↑	1.2V ± 0.1V	8.6			ns
			1.5V ± 012V	4.6			
			1.8V ± 0.15V	2.8			
			2.5V ± 0.2V	1.5			
			3.3V ± 0.3V	1			
			5V ± 0.5V	0.6			
		$\overline{CLR}$ Inactive	1.2V ± 0.1V	0			
			1.5V ± 012V	0			
			1.8V ± 0.15V	0			
			2.5V ± 0.2V	0			
			3.3V ± 0.3V	0			
			5V ± 0.5V	0			
t_H	Hold time	Data after CLK↑	1.2V ± 0.1V	2			ns
			1.5V ± 012V	1			
			1.8V ± 0.15V	1			
			2.5V ± 0.2V	1			
			3.3V ± 0.3V	1			
			5V ± 0.5V	1			

5.7 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	CLK	Q	C_L = 15pF	1.2V ± 0.1V			66.4	ns
				1.5V ± 0.12V			14.1	
				1.8V ± 0.15V			9.3	
				2.5V ± 0.2V			5.4	
				3.3V ± 0.3V			4	
				5V ± 0.5V			3.7	
			C_L = 30pF	1.8V ± 0.15V			74.5	
				2.5V ± 0.2V			15.1	
			C_L = 50pF	3.3V ± 0.3V			10	
				5V ± 0.5V			5.8	
t_{pd}	$\overline{CLR}$	Q	C_L = 15pF	1.2V ± 0.1V			4.8	ns
				1.5V ± 0.12V			4.8	
				1.8V ± 0.15V			8.7	
				2.5V ± 0.2V			5.2	
				3.3V ± 0.3V			3.9	
				5V ± 0.5V			2.7	
			C_L = 30pF	1.8V ± 0.15V			9.4	
				2.5V ± 0.2V			5.7	
			C_L = 50pF	3.3V ± 0.3V			4.7	
				5V ± 0.5V			3.1	
C_{pd}			f = 10MHz	1.8V		16.2		pF
				2.5V		17.3		
				3.3V		18.5		
				5V		20.4		

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

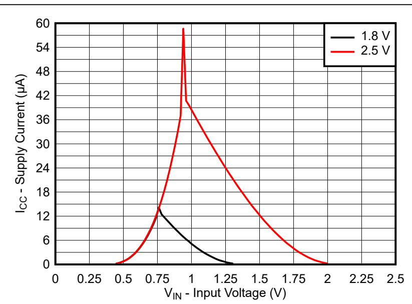


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

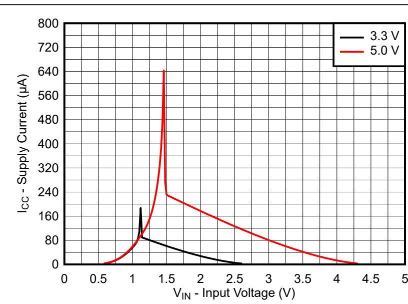


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

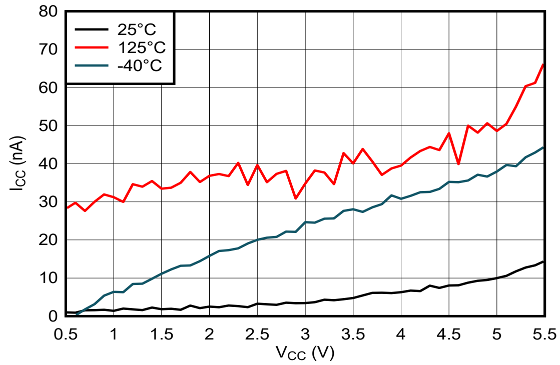


Figure 5-3. Supply Current Across Supply Voltage

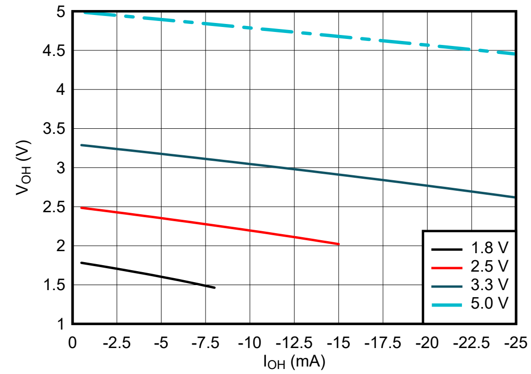


Figure 5-4. Output Voltage vs Current in HIGH State

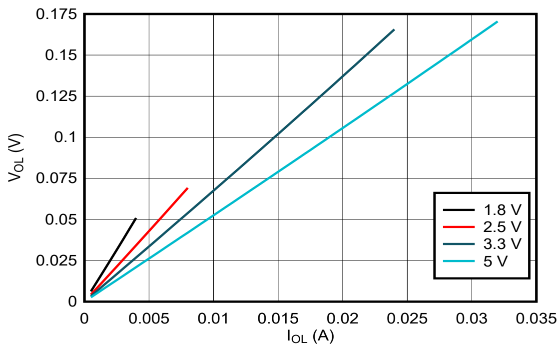


Figure 5-5. Output Voltage vs Current in LOW State

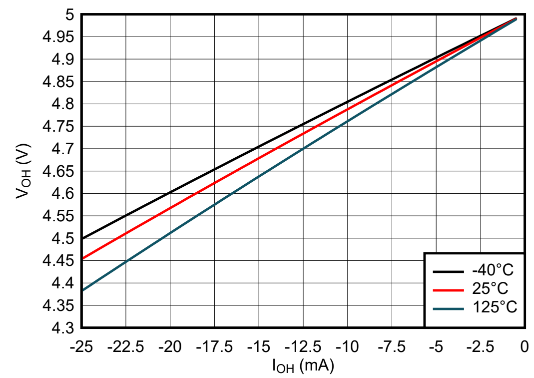


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

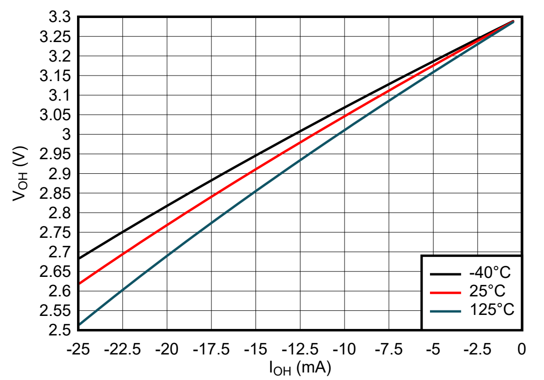


Figure 5-7. Output Voltage vs Current in HIGH State; 3.3V Supply

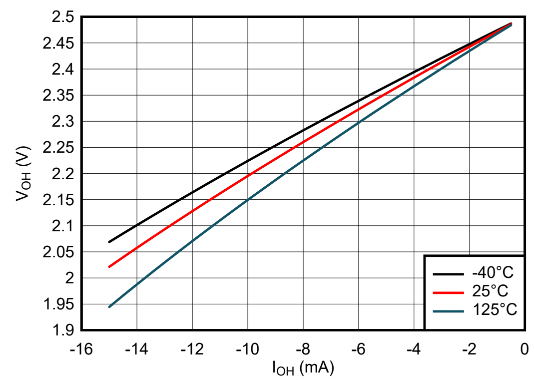


Figure 5-8. Output Voltage vs Current in HIGH State; 2.5V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

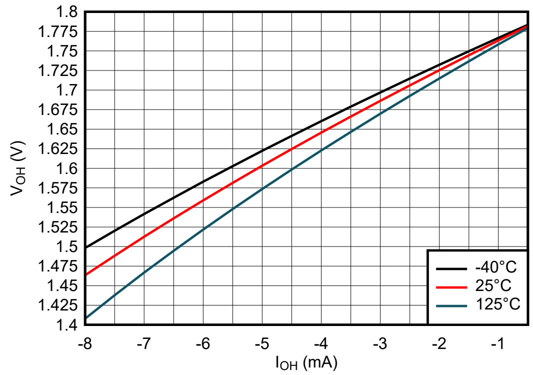


Figure 5-9. Output Voltage vs Current in HIGH State; 1.8V Supply

6 Parameter Measurement Information

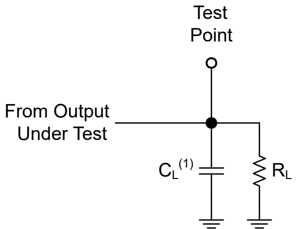
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.

Table 6-1. Push-Pull Outputs

V_{CC}	V_t	R_L	C_L	ΔV
1.2V ± 0.1V	$V_{CC}/2$	2kΩ	15pF	0.1V
1.5V ± 0.12V	$V_{CC}/2$	2kΩ	15pF	0.1V
1.8V ± 0.15V	$V_{CC}/2$	1kΩ	15pF/30pF	0.15V
2.5V ± 0.2V	$V_{CC}/2$	500Ω	15pF/30pF	0.15V
3.3V ± 0.3V	1.5V	500Ω	15pF/50pF	0.3V
5.0V ± 0.5V	1.5V	500Ω	15pF/50pF	0.3V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

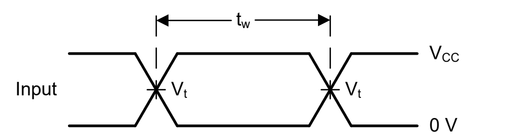


Figure 6-2. Voltage Waveforms, Pulse Duration

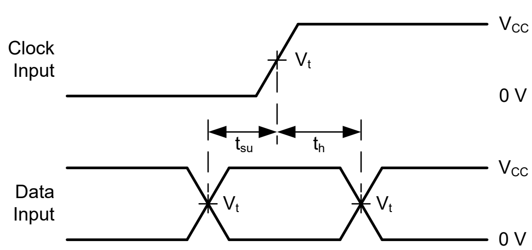
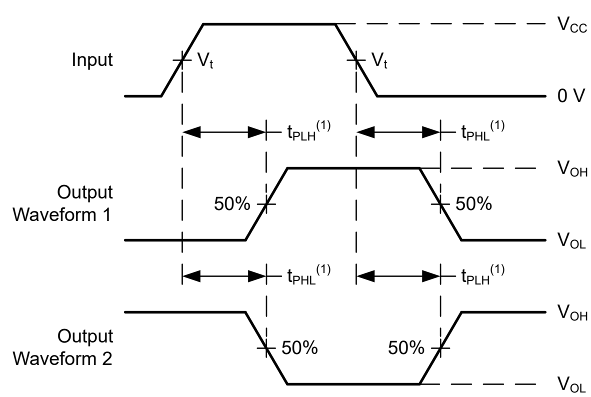
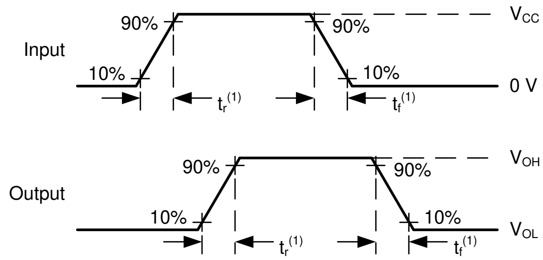


Figure 6-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-5. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74LVC1G175B-Q1 device is a single D-type flip-flop with asynchronous clear ($\overline{\text{CLR}}$) input. When $\overline{\text{CLR}}$ is HIGH, data from the input pin (D) is transferred to the output pin (Q) on the clock's (CLK) rising edge. When $\overline{\text{CLR}}$ is LOW, the Q is forced into the LOW state, regardless of the clock edge or data on D.

7.2 Functional Block Diagram

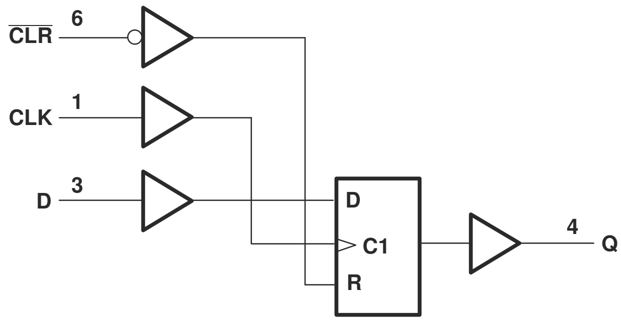


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.3.4 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

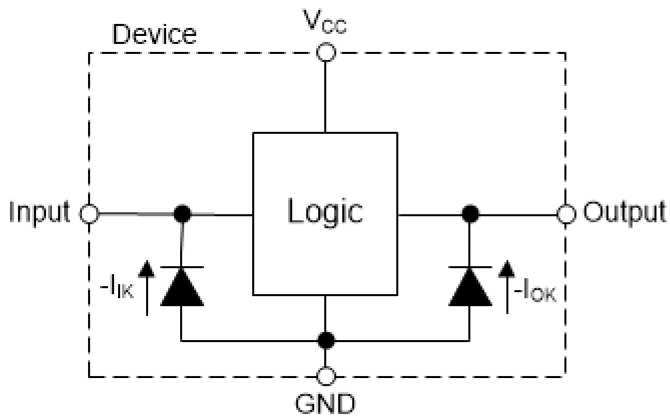


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Function Table lists the functional modes for SN74LVC1G175B-Q1.

Table 7-1. Function Table

INPUTS(1)			OUTPUT Q(2)
$\overline{CLR}$	CLK	D	
H	↑	L	L
H	↑	H	H
H	H or L	X	Q_0
L	X	X	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Multiple SN74LVC1G175B-Q1 devices can be used in tandem to create a shift register of arbitrary length. In this example, we use four SN74LVC1G175B-Q1 devices to form a 4-bit serial shift register. By connecting all CLK inputs to a common clock pulse and tying each output of one device to the next, we can store and load 4-bit values on demand. We demonstrate loading the 4 bit value *1101* into memory by setting *Serial Input Data* to each desired memory bit, and by sending a clock pulse for each bit, we sequentially move all stored bits from left to right
(A → B → C → D)

8.2 Typical Application

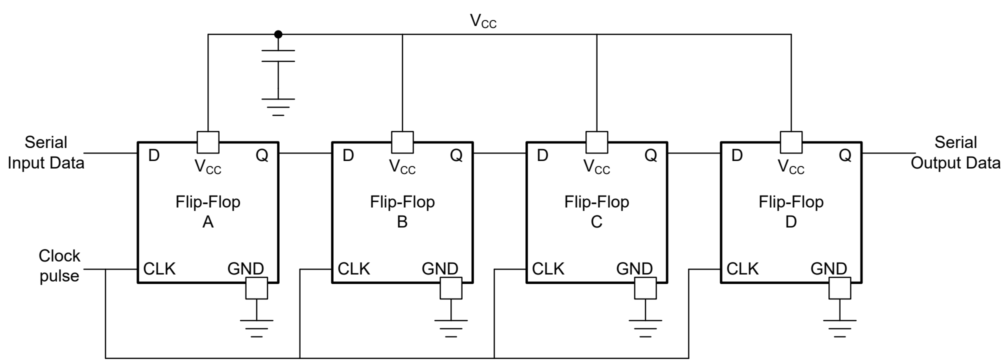


Figure 8-1. 4-Bit Serial Shift Register

8.2.1 Design Requirements

The SN74LVC1G175B-Q1 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that can exceed maximum limits.

The SN74LVC1G175B-Q1 allows switching control of analog and digital signals with a digital control signal. All input signals must remain as close as possible to either 0V or V_{CC} for peak operation.

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC1G175B-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC1G175B-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC1G175B-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, do not exceed 50pF.

The SN74LVC1G175B-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC1G175B-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC1G175B-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5V at any valid V_{CC}.
2. Recommended output conditions:
   - Load currents not exceeding ±50mA.

3. Frequency selection criterion:
   - The effects of frequency upon the device's power consumption should be studied in the *CMOS Power Consumption and CPD Calculation* application note.
   - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the *Layout* section.

8.2.3 Application Curves

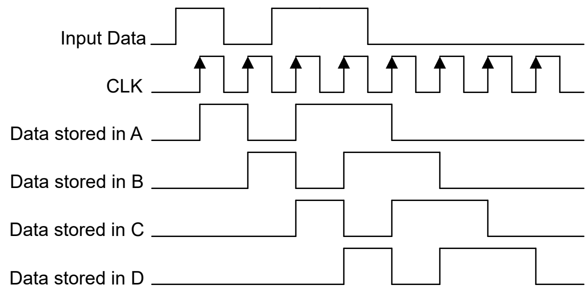


Figure 8-2. Application Timing Chart

Table 8-1. Stored Data Values

Serial Input Data	Stored A	Stored B	Stored C	Stored D
1	0	0	0	0
0	1	0	0	0
1	0	1	0	0
1	1	0	1	0
0	1	1	0	1

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each V_{CC} terminal has a good bypass capacitor to prevent power disturbance. For the SN74LVC1G175B-Q1, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  – Place near the positive supply terminal of the device
  – Provide an electrically short ground return path
  – Use wide traces to minimize impedance
  – Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  – 8mil to 12mil trace width
  – Lengths less than 12cm to minimize transmission line effects
  – Avoid 90° corners for signal traces
  – Use an unbroken ground plane below signal traces
  – Flood fill areas around signal traces with ground
  – Parallel traces must be separated by at least 3x dielectric thickness
  – For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

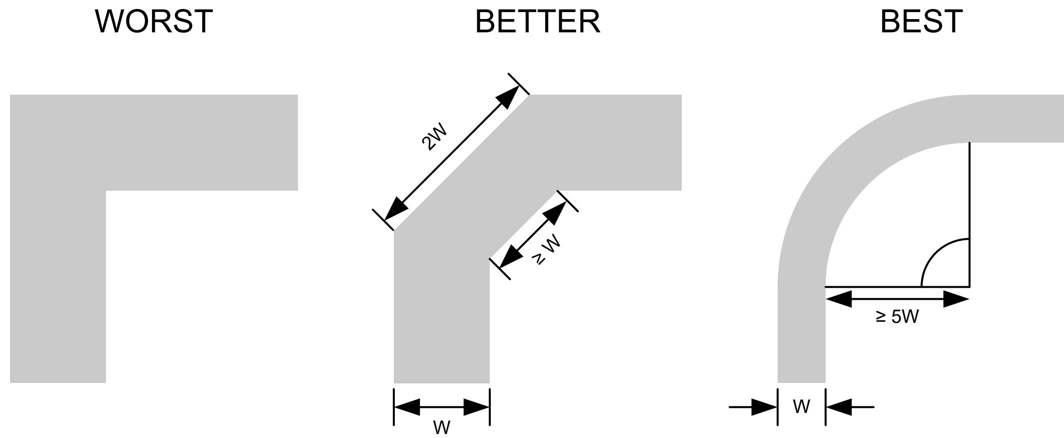


Figure 8-3. Example Trace Corners for Improved Signal Integrity

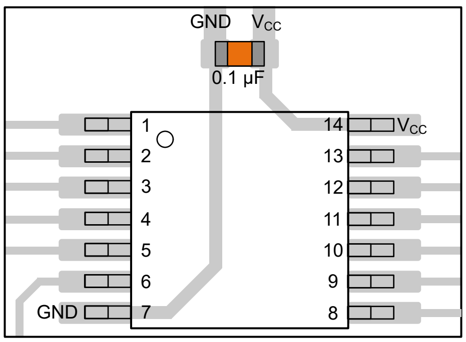


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

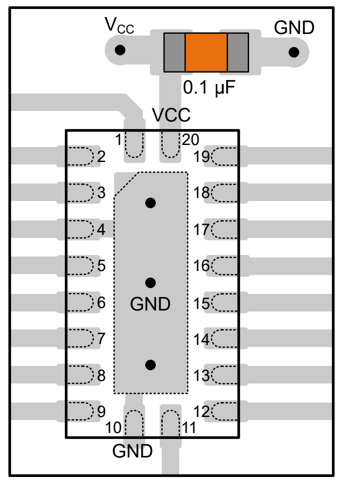


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

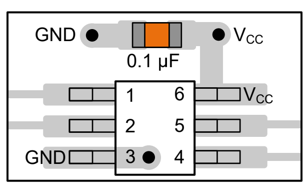


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

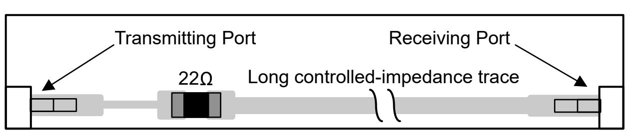


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.