

SN74LVC1G11 Single 3-Input Positive-AND Gate

1 Features

- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
 - ±2000V human-body model (A114-A)
 - ±1000V charged-device model (C101)
- Available in the Texas Instruments NanoFree™ package
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Maximum t_{pd} of 4.1ns at 3.3V
- Low power consumption, 10µA maximum I_{CC}
- ±24mA output drive at 3.3V
- I_{off} supports partial-power-down mode operation

2 Applications

- AV Receivers
- DLP Front Projection System
- Digital Picture Frames
- Digital Radio
- Digital Still Cameras
- Digital Video Cameras (DVC)
- Embedded PCs
- E-Books
- Ethernet Switches
- GPS: Personal Navigation Devices
- Handset: Smartphones
- High-Speed Data Acquisition and Generation
- Military: Radar and Sonar
- Mobile Internet Devices
- Notebook PC and Netbooks
- Network-Attached Storage (NAS)
- Power Line Communication Modems
- Server PSU
- STB, DVR, and Streaming Media
- Speakers: USB
- Tablets: Enterprise
- Video Broadcasting and Infrastructure: Scalable Platform and IP-Based Multi-Format Transcoders
- Wireless Headsets, Keyboards, and Mice

3 Description

The SN74LVC1G11 performs the Boolean function $Y = A \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE ⁽²⁾
SN74LVC1G11	DBV (SOT-23, 6)	2.90 mm × 1.60 mm
	DCK (SC70, 6)	2.00 mm × 1.25 mm
	DRY (SON, 6)	1.45 mm × 1.00 mm
	DSF (SON, 6)	1.00 mm × 1.00 mm
	YZP (DSBGA, 6)	1.41 mm × 0.91 mm

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

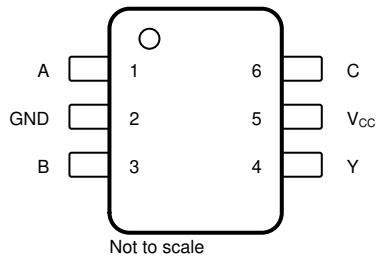


Figure 4-1. DBV or DCK Package, 6-Pin SOT-23 or SOT-SC70 (Top View)

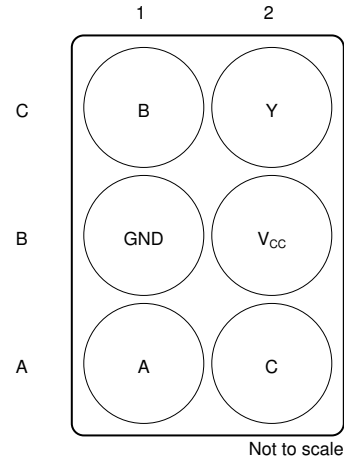


Figure 4-2. YZP Package 6-Pin DSBGA (Bottom View)

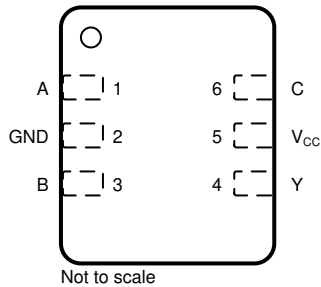
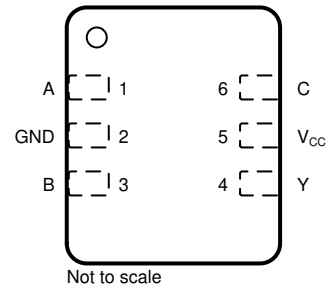


Figure 4-3. DRY Package 6-Pin SON (Top View)



See mechanical drawings for dimensions.

Figure 4-4. DSF Package 6-Pin SON Top View

Table 4-1. Pin Functions

NAME	PIN		I/O ⁽¹⁾	DESCRIPTION
	SOT-23, SOT-SC70, SON, SON	DSBGA		
A	1	A1	I	A Input
B	3	C1	I	B Input
C	6	A2	I	C Input
GND	2	B1	—	Ground
V _{CC}	5	B2	—	Power Supply
Y	4	C2	O	Y Output

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	−0.5	6.5	V
V _I	Input voltage ⁽²⁾	−0.5	6.5	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	−0.5	6.5	V
V _O	Voltage applied to any output in the high or low state ⁽²⁾ (3)	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current V _I < 0		−50	mA
I _{OK}	Output clamp current V _O < 0		−50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾.

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		−4	mA
		V _{CC} = 2.3 V		−8	
		V _{CC} = 3 V		−16	
				−24	
		V _{CC} = 4.5 V		−32	

over operating free-air temperature range (unless otherwise noted)⁽¹⁾.

		MIN	MAX	UNIT
I_{OL} Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
	$V_{CC} = 2.3\text{ V}$		8	
	$V_{CC} = 3\text{ V}$		16	
			24	
	$V_{CC} = 4.5\text{ V}$		32	
$\Delta t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$		20	ns/V
	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		10	
	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		10	
T_A Operating free-air temperature	BGA package	–40	85	°C
	All other packages	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G11					UNIT
		DBV (SOT-23)	DCK (SC70)	DRY (SON)	YZP (DSBGA)	DSF (SON)	
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	195.9	260.1	424.6	105.8	413.7	°C/W
$R_{\theta JCTop}$	Junction-to-case (top) thermal resistance	177.4	98.1	309	1.6	226.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	63.1	292	10.8	317	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	61.3	2.2	135.4	3.1	37.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.3	62.4	292	10.8	317	°C/W
$R_{\theta JCbott}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -100\text{ }\mu\text{A}$	1.65 V to 5.5 V	$V_{CC} - 0.1$			V
	$I_{OH} = -4\text{ mA}$	1.65 V	1.2			
	$I_{OH} = -8\text{ mA}$	2.3 V	1.9			
	$I_{OH} = -16\text{ mA}$	3 V	2.4			
	$I_{OH} = -24\text{ mA}$		2.3			
	$I_{OH} = -32\text{ mA}$	4.5 V	3.8			
V_{OL}	$I_{OL} = 100\text{ }\mu\text{A}$	1.65 V to 5.5 V			0.1	V
	$I_{OL} = 4\text{ mA}$	1.65 V			0.45	
	$I_{OL} = 8\text{ mA}$	2.3 V			0.3	
	$I_{OL} = 16\text{ mA}$	3 V			0.4	
	$I_{OL} = 24\text{ mA}$				0.55	
	$I_{OL} = 32\text{ mA}$	4.5 V			0.55	
I_I All inputs	$V_I = 5.5\text{ V}$ or GND	0 to 5.5 V			±5	μA
I_{off}	V_I or $V_O = 5.5\text{ V}$	0			±10	μA
I_{CC}	$V_I = 5.5\text{ V}$ or GND, $I_O = 0$	1.65 V to 5.5 V			10	μA
ΔI_{CC}	One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		3.5		pF

5.6 Switching Characteristics, $C_L = 15 \text{ pF}$

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A, B, or C	Y	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	2.6	15.2	ns
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.6	5.6	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.2	4.1	
			$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	1	3.1	

5.7 Switching Characteristics, $C_L = 30 \text{ pF}$ or 50 pF

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A, B, or C	Y	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	2.9	17.2	ns
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.4	6.2	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.3	4.9	
			$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	1	3.5	

5.8 Switching Characteristics, $C_L = 30 \text{ pF}$ or 50 pF

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

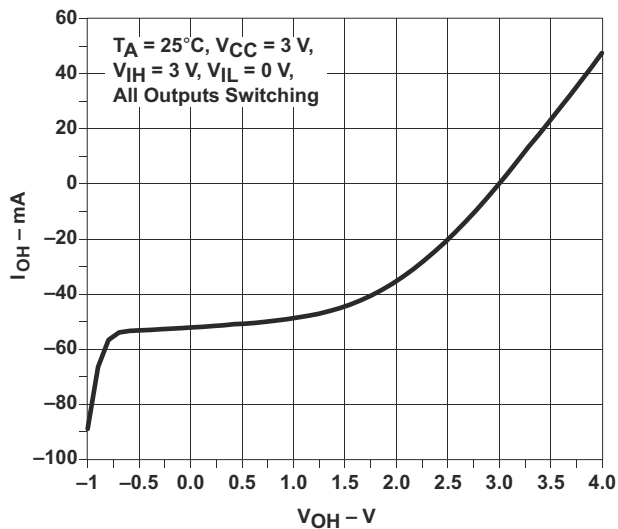
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	A, B, or C	Y	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	2.9	20	ns
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.4	7.8	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.3	6.2	
			$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	1	4.6	

5.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

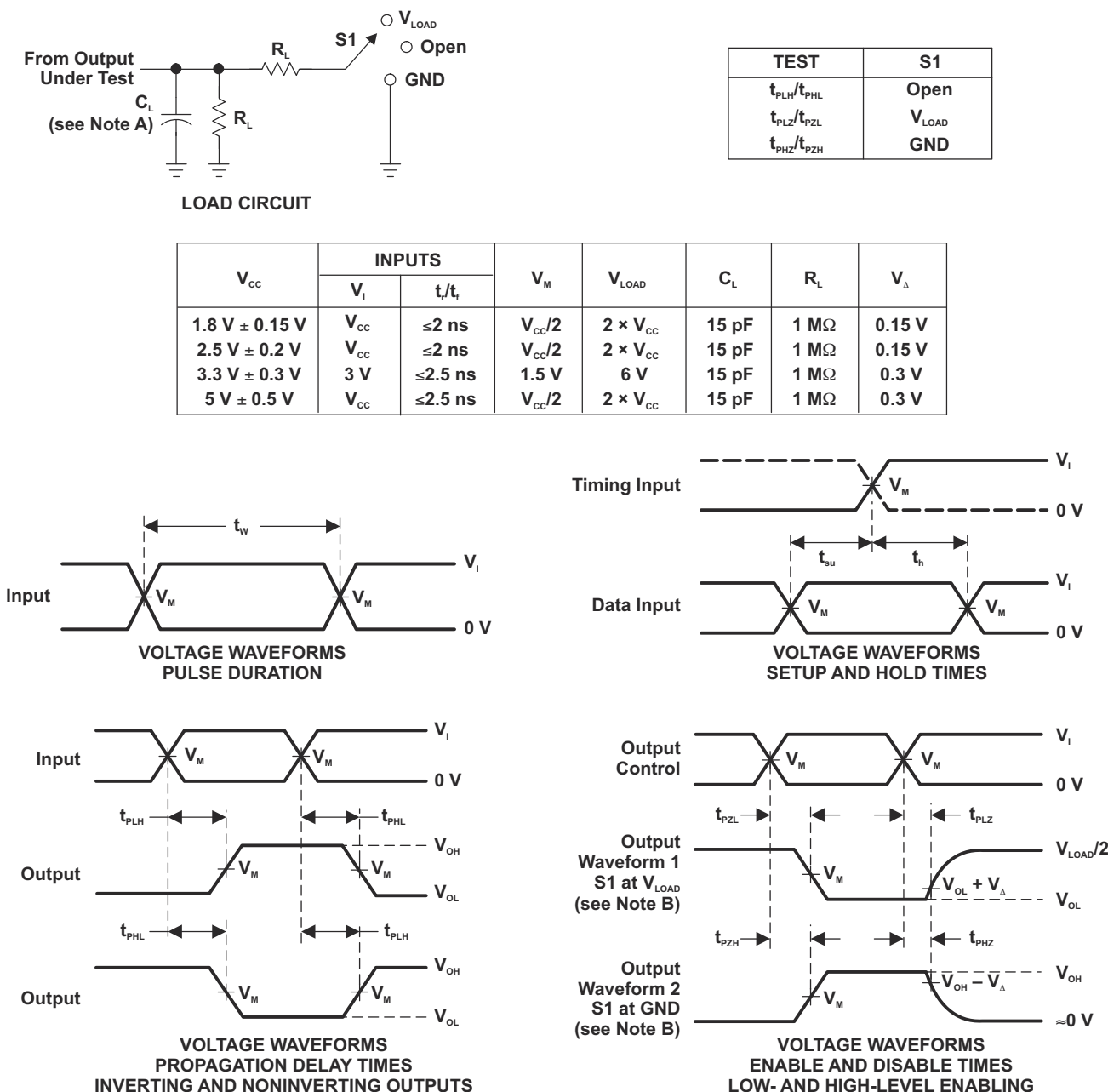
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$f = 10 \text{ MHz}$	$V_{CC} = 1.8 \text{ V}$	18	pF
		$V_{CC} = 2.5 \text{ V}$	19	
		$V_{CC} = 3.3 \text{ V}$	20	
		$V_{CC} = 5 \text{ V}$	23	

5.10 Typical Characteristics



**Figure 5-1. Output Current Drive
vs HIGH-level Output Voltage**

6 Parameter Measurement Information



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{on} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

This 3-input AND gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G11 device features a three-input AND gate. The output state is determined by eight patterns of 3-bit input. All inputs can be connected to V_{CC} or GND.

This device is fully-specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram



Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The SN74LVC1G11 device has a wide operating V_{CC} range of 1.65 V to 5.5 V, which allows use in a broad range of systems. The 5.5-V I/Os allow down translation and also allow voltages at the inputs when $V_{CC} = 0$ V.

7.4 Device Functional Modes

[Table 7-1](#) lists the functional modes of SN74LVC1G11.

Table 7-1. Function Table

INPUTS			OUTPUT Y
A	B	C	
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G11 device offers logical AND configuration for many design applications. This example describes basic power sequencing using the AND gate configuration. Power sequencing is often used in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. In the application below, the power-good signals from the supplies tell the MCU to continue an operation.

8.2 Typical Application

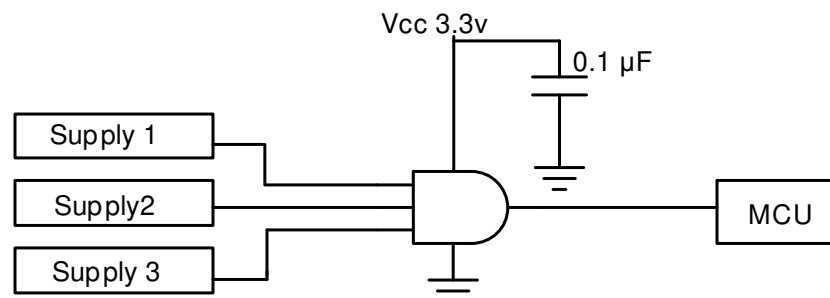


Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

- Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid V_{CC} .
- Recommended output conditions:
 - Load currents must not exceed ± 50 mA.
- Frequency selection criterion:
 - [Figure 8-2](#) illustrates the effects of frequency on output current.
 - Added trace resistance and capacitance can reduce maximum frequency capability. Follow the layout practices listed in the [Layout](#) section.

8.2.2 Detailed Design Procedure

The SN74LVC1G11 device uses CMOS technology and has balanced output drive. Avoid bus contentions that can drive currents that can exceed maximum limits.

The SN74LVC1G11 allows for performing the logical AND function with digital signals. Maintain input signals as close as possible to either 0 V or V_{CC} for optimal operation.

8.2.3 Application Curve

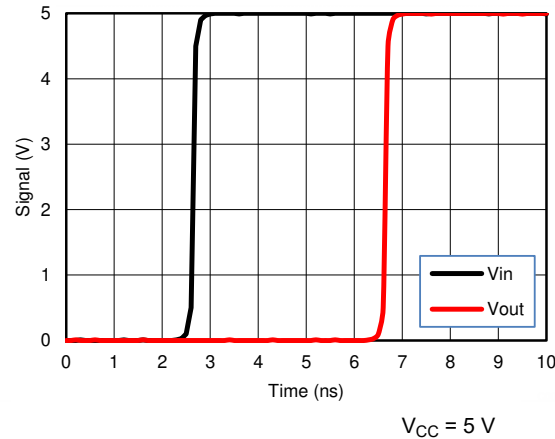


Figure 8-2. Simulated Input-to-Output Voltage Response Showing Propagation Delay

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#) table.

To prevent power disturbance, ensure good bypass capacitance for each V_{CC} terminal. For devices with a single-supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. Place the bypass capacitor as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions (or parts of functions) of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or when only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected, because the undefined voltages at the outside connections result in undefined operational states. [Figure 8-3](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted, which does not disable the input section of the I/Os. Therefore, the I/Os cannot float when disabled.

8.4.2 Layout Example

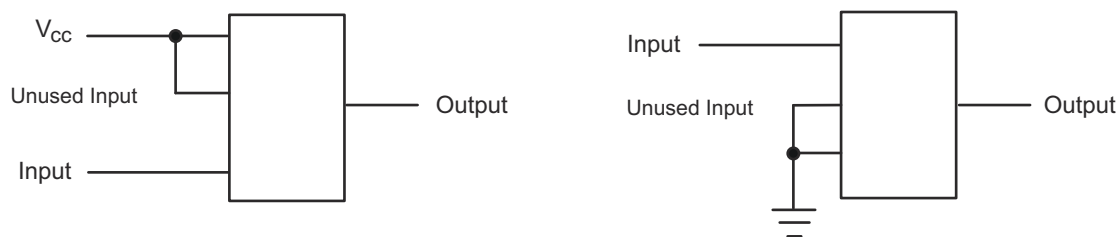


Figure 8-3. Layout Diagrams

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation see the following:

- [Implications of Slow or Floating CMOS Inputs](#) , SCBA004
- [Selecting the Right Texas Instruments Signal Switch](#) , SZZA030

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

NanoFree™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (November 2016) to Revision I (November 2024)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document.....	1
• Updated DCK package pinout drawing.....	3
• Deleted duplicate <i>Load Circuit and Voltage Waveforms</i> drawing.....	8

Changes from Revision G (December 2015) to Revision H (November 2016)	Page
• Deleted 200-V Machine Model from <i>Features</i>	1
• Changed pinout images to improve clarity of pin names and pin numbers.....	3
• Added DSBGA pin numbers to <i>Pin Functions</i> table	3
• Added Operating free-air temperature, T _A for BGA package.....	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G11DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C115, C11F, C11K, C11R)
SN74LVC1G11DBVR.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C115, C11F, C11K, C11R)
SN74LVC1G11DBVRE4	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C11F
SN74LVC1G11DBVRG4	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C11F
SN74LVC1G11DBVRG4.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C11F
SN74LVC1G11DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C35, C3F, C3J, C3K, C3R)
SN74LVC1G11DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C35, C3F, C3J, C3K, C3R)
SN74LVC1G11DCKRE4	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C35
SN74LVC1G11DCKRG4	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C35
SN74LVC1G11DCKRG4.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C35
SN74LVC1G11DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3
SN74LVC1G11DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3
SN74LVC1G11DRYRG4	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3
SN74LVC1G11DRYRG4.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3
SN74LVC1G11DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3
SN74LVC1G11DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3
SN74LVC1G11DSFRG4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3
SN74LVC1G11DSFRG4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3
SN74LVC1G11YZPR	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C3N
SN74LVC1G11YZPR.B	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C3N

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G11 :

- Automotive : [SN74LVC1G11-Q1](#)
- Enhanced Product : [SN74LVC1G11-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G11DBVR	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G11DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G11DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G11DCKRG4	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G11DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G11DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G11DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G11DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G11YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G11DBVR	SOT-23	DBV	6	3000	208.0	191.0	35.0
SN74LVC1G11DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G11DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74LVC1G11DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G11DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G11DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G11DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G11DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G11YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

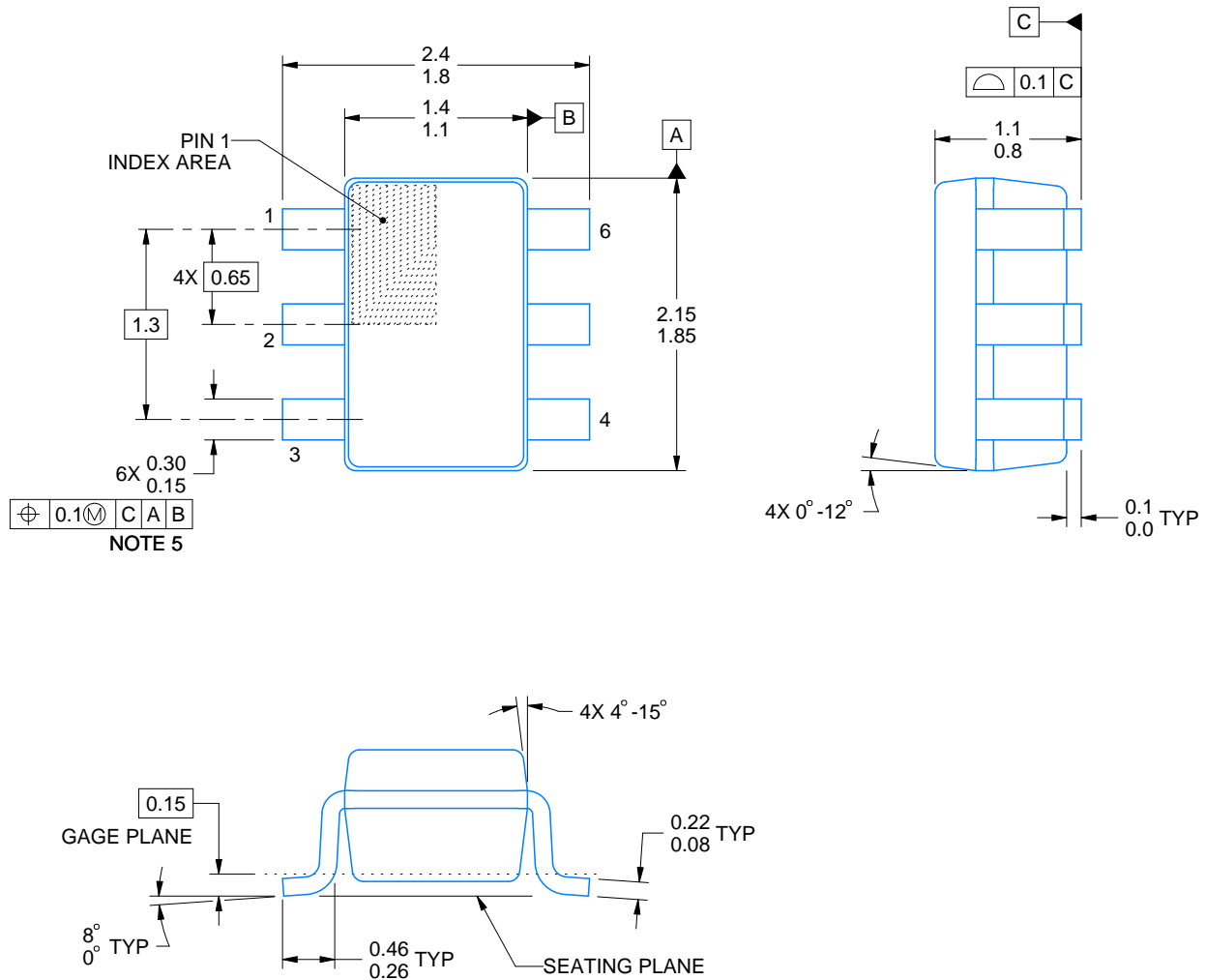
DCK0006A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.

EXAMPLE BOARD LAYOUT

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G



USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

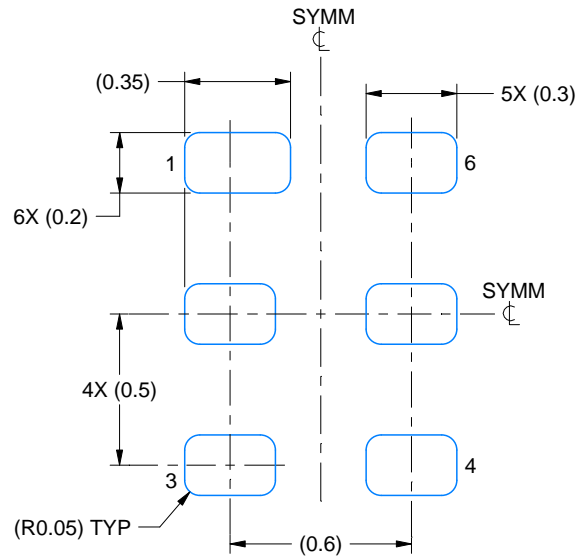
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

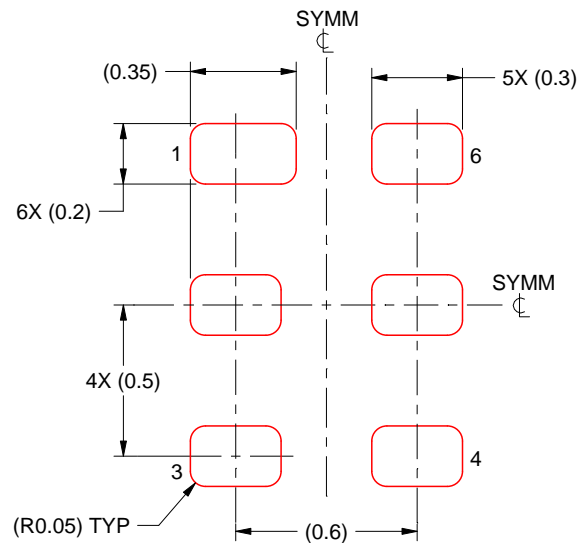
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

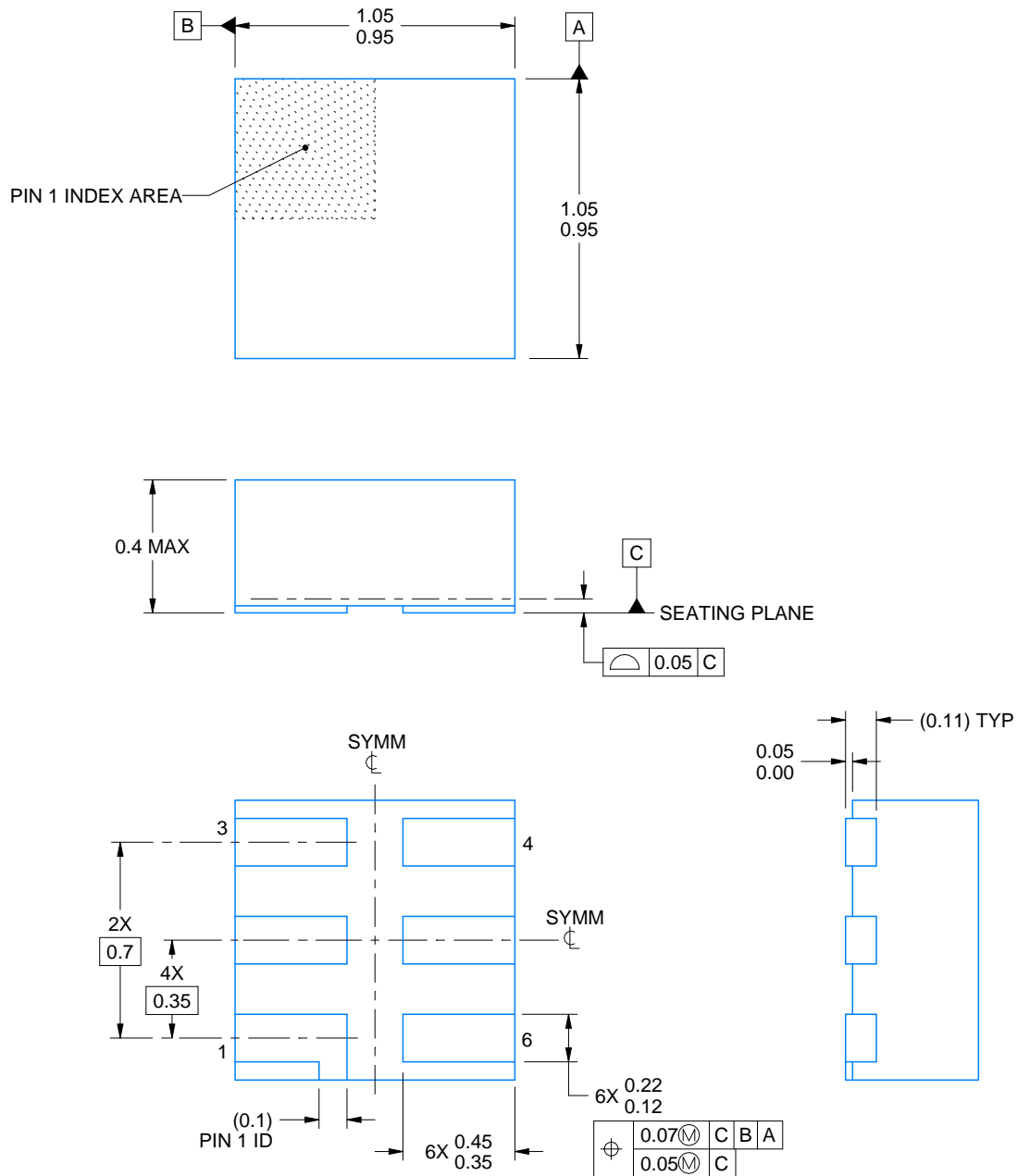


DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

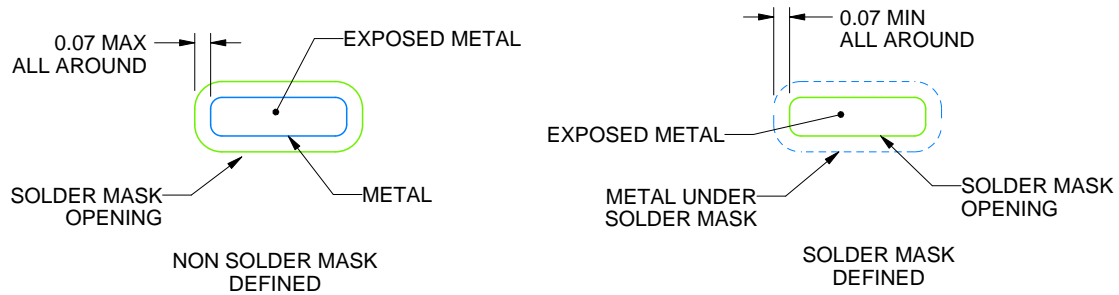
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



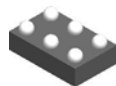
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

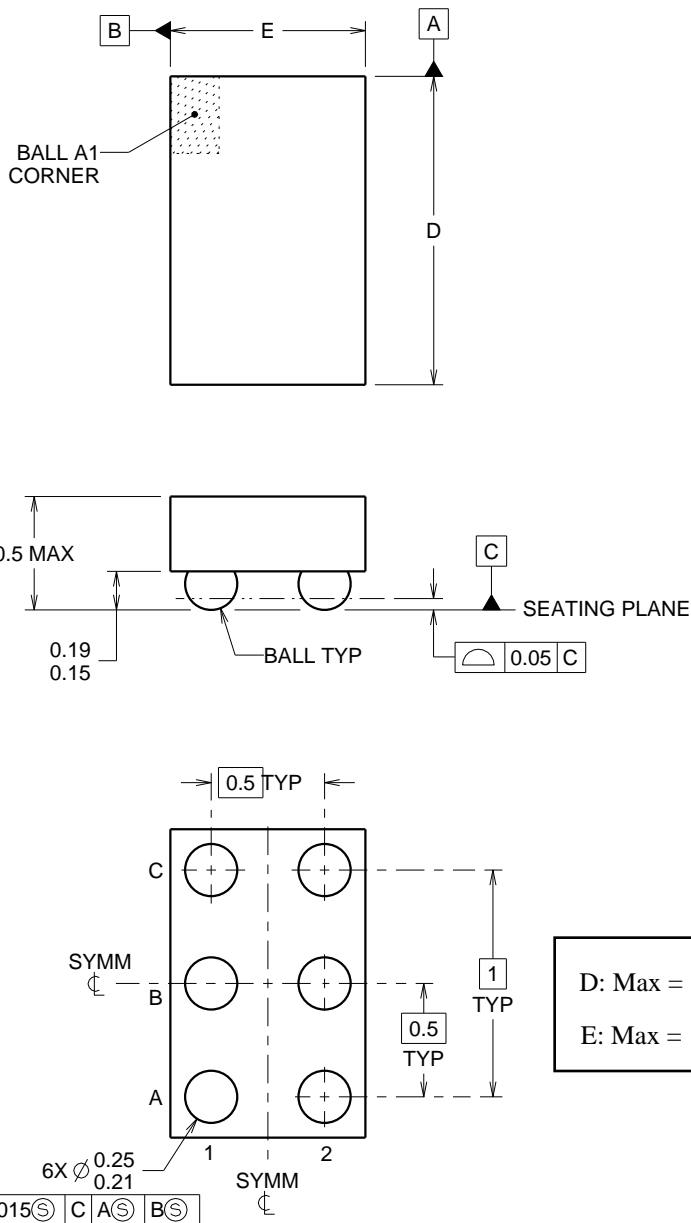
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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