

Single 3-Input Positive AND-OR Gate

Check for Samples: [SN74LVC1G0832](#)

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V_{CC}
- Max t_{pd} of 5 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input ($V_{hys} = 250$ mV Typ @ 3.3 V)
- Can Be Used in Three Combinations:
 - AND-OR Gate
 - AND Gate
 - OR Gate
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION

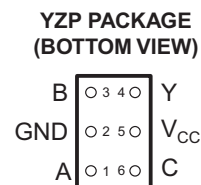
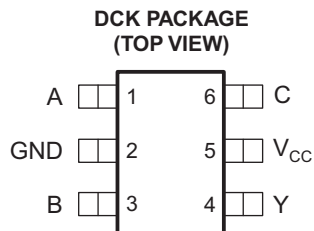
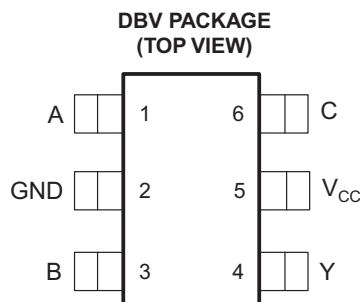
This device is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G0832 device is a single 3-input positive AND-OR gate. It performs the Boolean function $Y = (A \cdot B) + C$ in positive logic.

By tying one input to GND or V_{CC} , the SN74LVC1G0832 device offers two more functions. When C is tied to GND, this device performs as a 2-input AND gate ($Y = A \cdot B$). When A is tied to V_{CC} , the device works as a 2-input OR gate ($Y = B + C$). This device also works as a 2-input OR gate when B is tied to V_{CC} ($Y = A + C$).

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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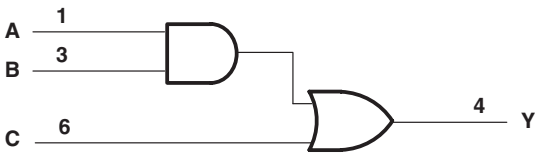
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Function Table⁽¹⁾

| INPUTS | | | OUTPUT Y |
|--------|---|---|-------------|
| A | B | C | |
| X | X | H | H |
| H | H | X | H |
| X | L | L | L |
| L | X | L | L |

(1) X = Valid H or L

Logic Diagram (Positive Logic)



Function Selection Table

| LOGIC FUNCTION | FIGURE |
|-------------------------|--------------------------|
| 2-Input AND Gate | Figure 1 |
| 2-Input OR Gate | Figure 2 |
| $Y = (A \bullet B) + C$ | Figure 3 |

Logic Configurations

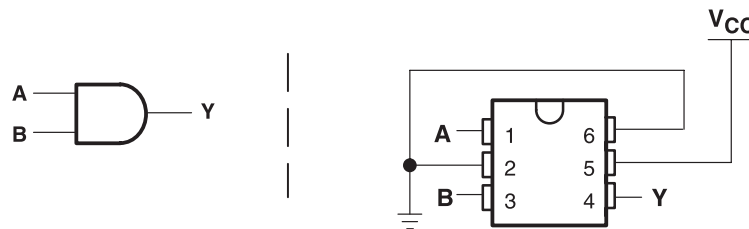


Figure 1. 2-Input AND Gate

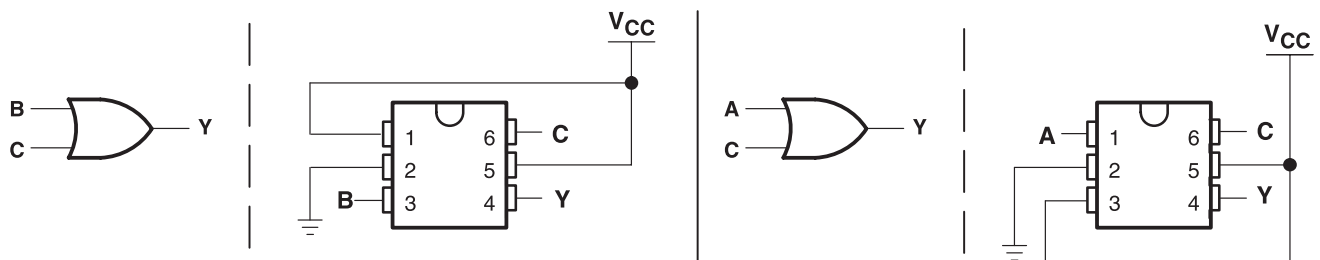


Figure 2. 2-Input OR Gate



Figure 3. $Y = (A \cdot B) + C$

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-------------|----------------|--------|
| V_{CC} | Supply voltage range | –0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | –0.5 | 6.5 | V |
| V_O | Voltage range applied to Y output in the high-impedance or power-off state ⁽²⁾ | –0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | –0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | | –50 mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | –50 mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DBV package | | 215 |
| | | DCK package | | 259 |
| | | YZP package | | 123 |
| T_{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------|------------------------------------|---|------------------------|------------------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | 5.5 | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | 5.5 | |
| | | V _{CC} = 3 V to 3.6 V | 2 | 5.5 | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | 5.5 | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0 | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0 | | |
| | | V _{CC} = 3 V to 3.6 V | 0 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 0 | | |
| V _O | Output voltage | | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | mA |
| | | V _{CC} = 2.3 V | | –8 | |
| | | V _{CC} = 3 V | | –16 | |
| | | V _{CC} = 4.5 V | | –32 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 3 V | | 16 | |
| | | V _{CC} = 4.5 V | | 32 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | V _{CC} = 3.3 V ± 0.3 V | | 10 | |
| | | V _{CC} = 5 V ± 0.5 V | | 5 | |
| T _A | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | –40°C to 85°C | | | –40°C to 125°C | | | UNIT |
|------------------|---------------------------|--|-----------------|-----------------------|--------------------|------|-----------------------|--------------------|-----|------|
| | | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | |
| V _{OH} | I _{OH} = –100 μA | V _I = 5.5 V or GND | 1.65 V to 5.5 V | V _{CC} – 0.1 | | | V _{CC} – 0.1 | | | V |
| | I _{OH} = –4 mA | | 1.65 V | | | 1.2 | | | | |
| | I _{OH} = –8 mA | | 2.3 V | | | 1.9 | | | | |
| | I _{OH} = –16 mA | | 3 V | | | 2.4 | | | | |
| | 2.3 | | | | | | | | | |
| | I _{OH} = –32 mA | | 4.5 V | | | 3.8 | | | | |
| V _{OL} | I _{OL} = 100 μA | V _I = 5.5 V or GND | 1.65 V to 5.5 V | 0.1 | | | 0.1 | | | V |
| | I _{OL} = 4 mA | | 1.65 V | | | 0.45 | | | | |
| | I _{OL} = 8 mA | | 2.3 V | | | 0.3 | | | | |
| | I _{OL} = 16 mA | | 3 V | | | 0.4 | | | | |
| | 0.55 | | | | | | | | | |
| | I _{OL} = 32 mA | | 4.5 V | | | 0.55 | | | | |
| I _I | A, B, or C inputs | V _I = 5.5 V or GND | 0 to 5.5 V | ±5 | | | ±5 | | | μA |
| I _{off} | | V _I or V _O = 5.5 V | 0 | ±10 | | | ±10 | | | μA |
| I _{CC} | | V _I = 5.5 V or GND, I _O = 0 | 1.65 V to 5.5 V | 10 | | | 10 | | | μA |
| ΔI _{CC} | | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 3 V to 5.5 V | 500 | | | 500 | | | μA |
| C _i | | V _I = V _{CC} or GND | 3.3 V | 7 | | | | | | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 4](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC1G0832 –40°C to 85°C | | | | | | | | UNIT |
|-----------------|-----------------|----------------|-------------------------------------|-----|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
| | | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A, B, or C | Y | 3.7 | 14 | 2.4 | 7 | 1.7 | 5 | 1.2 | 3.4 | ns |

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see [Figure 5](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC1G0832 –40°C to 85°C | | | | | | | | UNIT |
|-----------------|-----------------|----------------|-------------------------------------|------|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
| | | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A, B, or C | Y | 2.5 | 17.5 | 1.8 | 7.6 | 1.8 | 5.9 | 1.3 | 4 | ns |

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see [Figure 5](#))

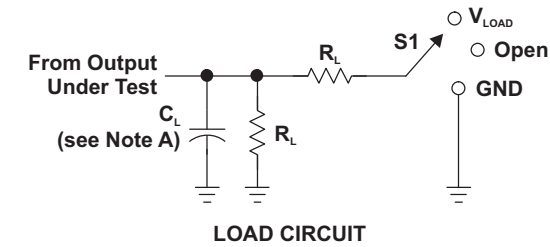
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC1G0832 –40°C to 125°C | | | | | | | | UNIT |
|-----------------|-----------------|----------------|-------------------------------------|------|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
| | | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A, B, or C | Y | 2.5 | 17.5 | 1.8 | 7.6 | 1.8 | 5.9 | 1.3 | 4.5 | ns |

Operating Characteristics

$T_A = 25^\circ\text{C}$

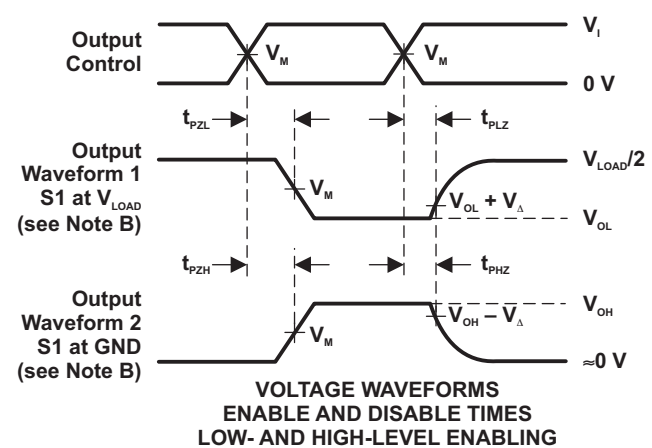
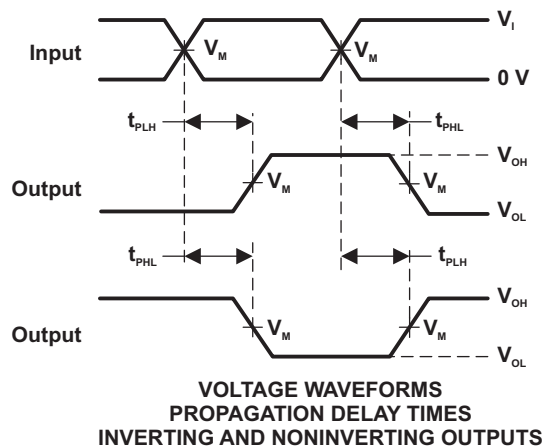
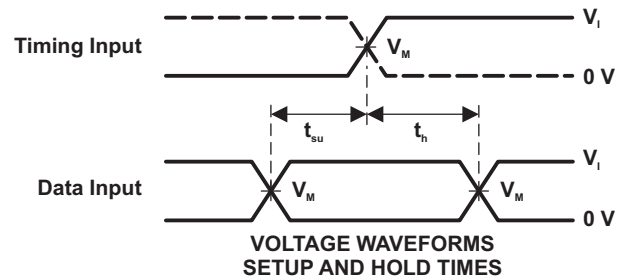
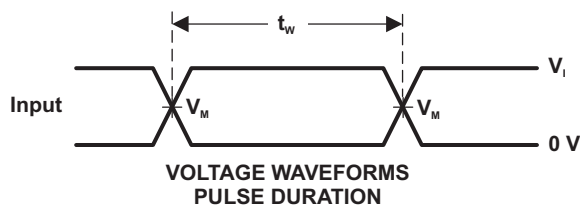
| PARAMETER | | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|-----------|-------------------------------|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | | TYP | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance | $f = 10\text{ MHz}$ | 15 | 15 | 16 | 18 | pF |

Parameter Measurement Information



| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

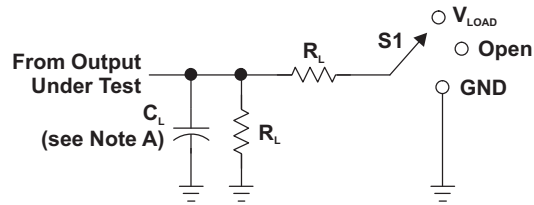
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 1 M Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.3 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

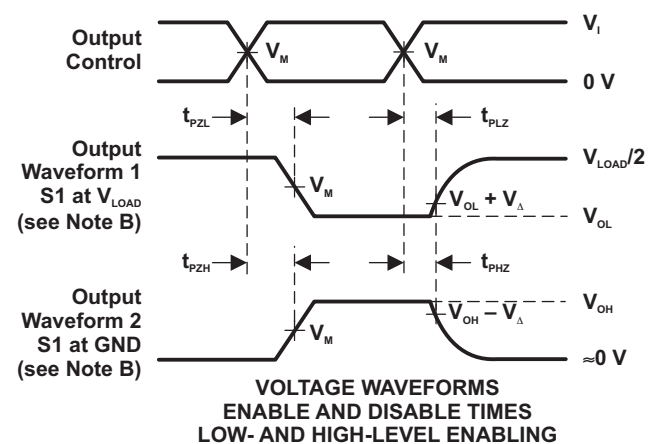
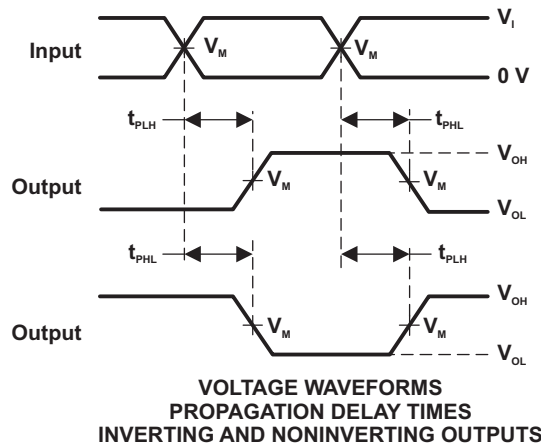
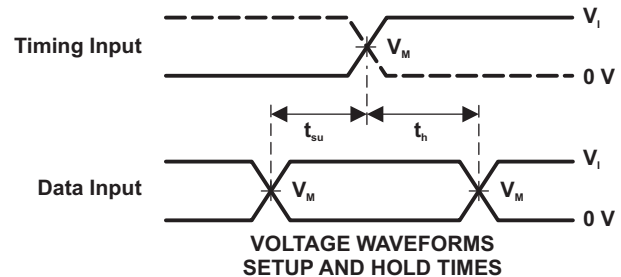
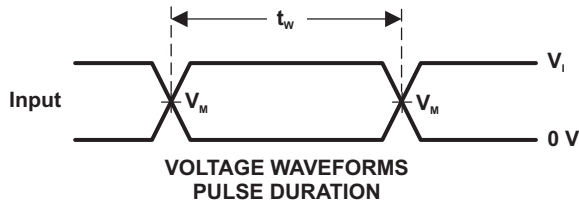
Parameter Measurement Information (continued)



LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_i | t_i/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

REVISION HISTORY

| Changes from Revision C (January 2007) to Revision D | Page |
|--|------|
| • Updated document to new TI data sheet format. | 1 |
| • Updated Features. | 1 |
| • Added ESD warning. | 2 |
| • Updated operating temperature range. | 5 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| 74LVC1G0832DCKRG4.B | Active | Production | SC70 (DCK) 6 | 3000 LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| SN74LVC1G0832DBVR | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CDCR |
| SN74LVC1G0832DBVR.B | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CDCR |
| SN74LVC1G0832DBVT | Active | Production | SOT-23 (DBV) 6 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CDCR |
| SN74LVC1G0832DBVT.B | Active | Production | SOT-23 (DBV) 6 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CDCR |
| SN74LVC1G0832DCKR | Active | Production | SC70 (DCK) 6 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (DCJ, DCR) |
| SN74LVC1G0832DCKR.B | Active | Production | SC70 (DCK) 6 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (DCJ, DCR) |
| SN74LVC1G0832DCKT | Active | Production | SC70 (DCK) 6 | 250 SMALL T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (DCJ, DCR) |
| SN74LVC1G0832DCKT.B | Active | Production | SC70 (DCK) 6 | 250 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (DCJ, DCR) |
| SN74LVC1G0832YZPR | Active | Production | DSBGA (YZP) 6 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | DCN |
| SN74LVC1G0832YZPR.B | Active | Production | DSBGA (YZP) 6 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | DCN |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G0832DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G0832DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G0832DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G0832DCKT | SC70 | DCK | 6 | 250 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G0832DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G0832YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G0832DBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G0832DBVT | SOT-23 | DBV | 6 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G0832DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G0832DCKT | SC70 | DCK | 6 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G0832DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G0832YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

EXAMPLE BOARD LAYOUT

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

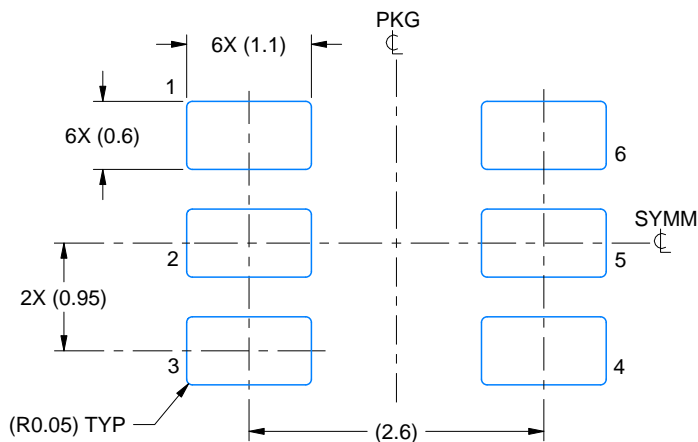
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

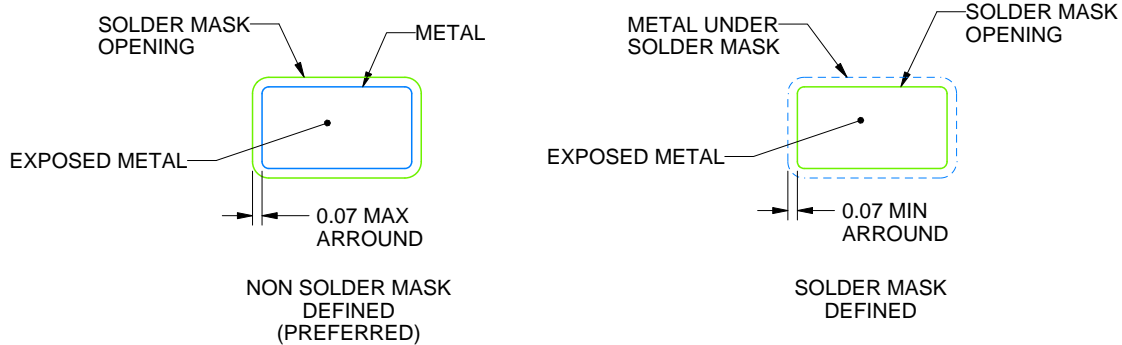
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

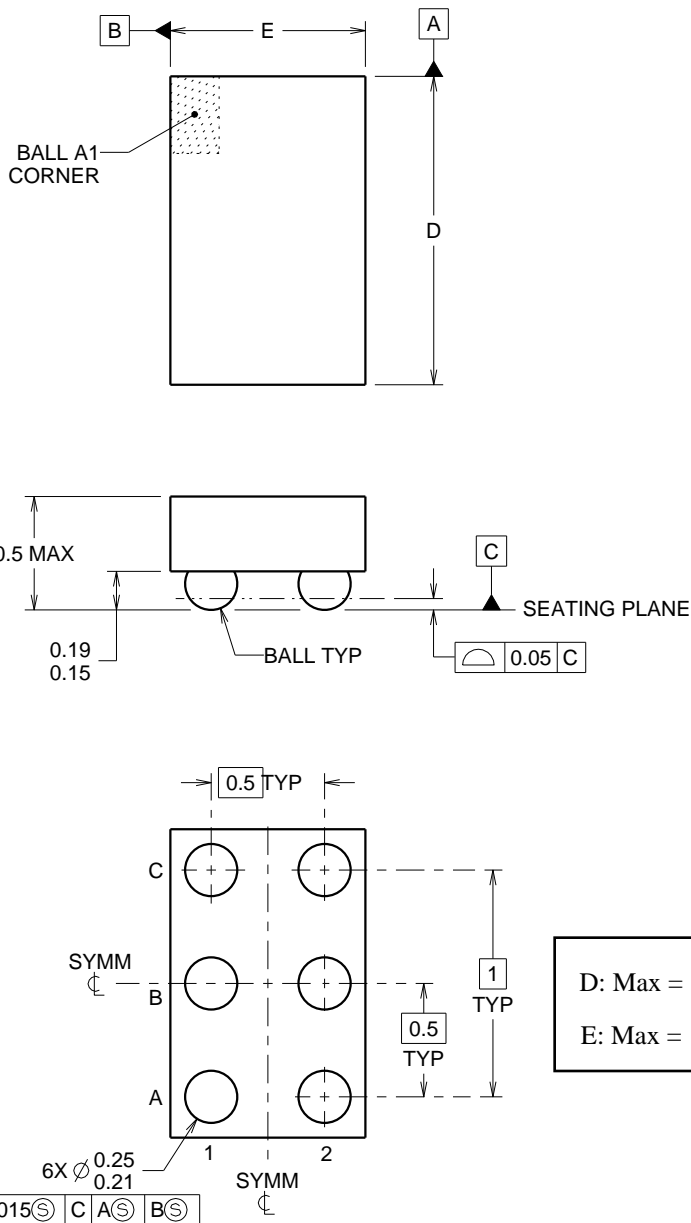
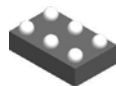


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

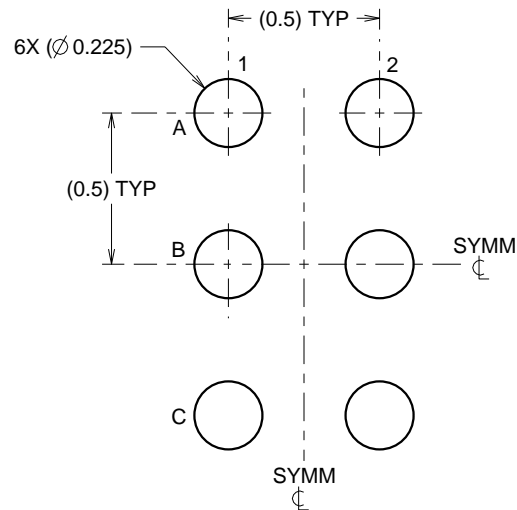
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

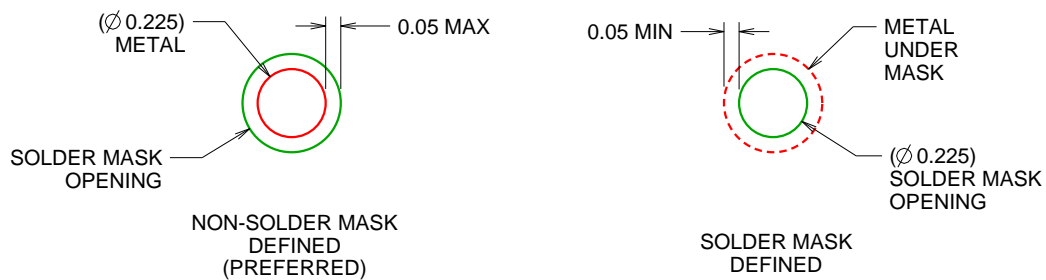
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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