SN74LVC16T245 16-bit Dual-Supply Bus Transceiver With Configurable Level-Shifting / Voltage Translation and Tri-State Outputs

1 Features

- Control Inputs V_{IH}/V_{IL} Levels are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input is at GND, Both Ports are in the High-Impedance State
- Overvoltage-Tolerant Inputs and Outputs Allow Mixed Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22

2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

3 Description

This 16-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

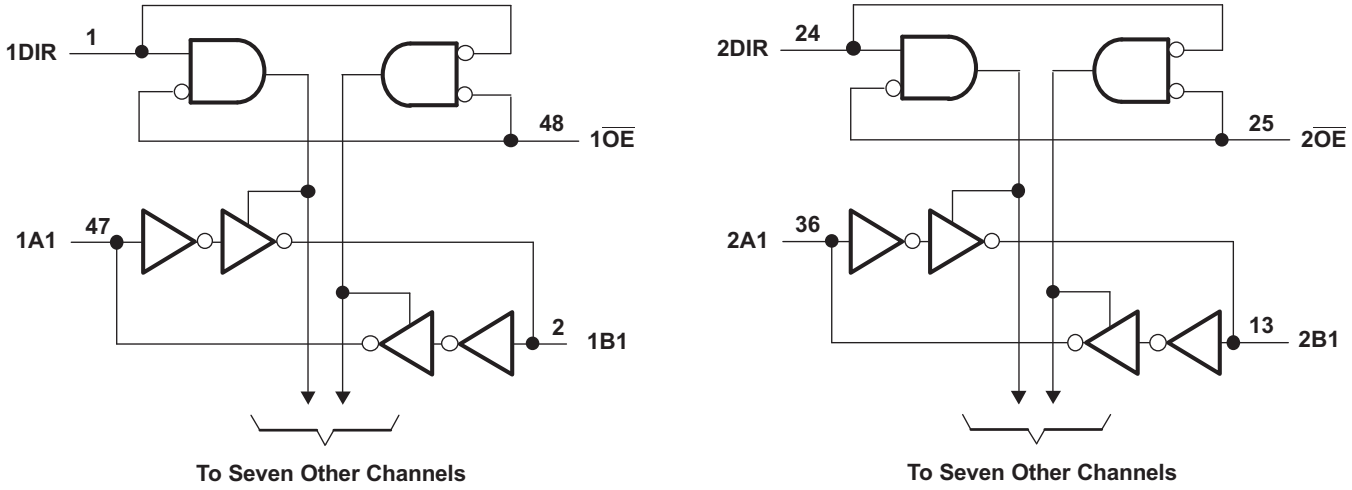
The SN74LVC16T245 device is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC16T245	TSSOP (48)	12.50 mm × 6.10 mm
	TVSOP (48)	9.70 mm × 4.40 mm
	SSOP (48)	15.88 mm × 7.49 mm
	BGA MICROSTAR JUNIOR (56)	7.00 mm × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

Changes from Revision A (October 2005) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Description (continued)

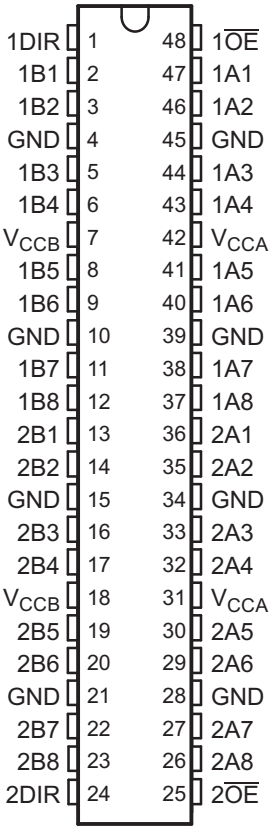
The SN74LVC16T245 control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

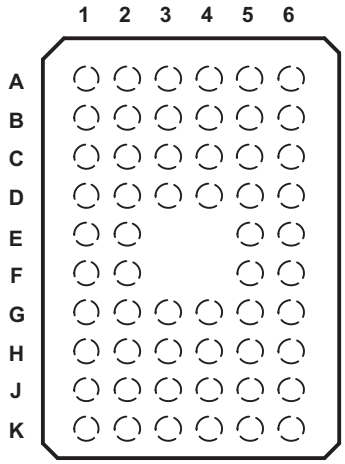
The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6 Pin Configuration and Functions

DGG and DGV Packages
48-Pin TSSOP and TVSOP
(Top View)



GQL and ZQL Packages
56-Pin BGA
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DGG / DGV	GQL / ZQL		
1A1	47	B5	I/O	Input/Output. Referenced to V_{CCA}
1A2	46	B6	I/O	Input/Output. Referenced to V_{CCA}
1A3	44	C5	I/O	Input/Output. Referenced to V_{CCA}
1A4	43	C6	I/O	Input/Output. Referenced to V_{CCA}
1A5	41	D5	I/O	Input/Output. Referenced to V_{CCA}
1A6	40	D6	I/O	Input/Output. Referenced to V_{CCA}
1A7	38	E5	I/O	Input/Output. Referenced to V_{CCA}
1A8	37	E6	I/O	Input/Output. Referenced to V_{CCA}
1B1	2	B2	I/O	Input/Output. Referenced to V_{CCB}
1B2	3	B1	I/O	Input/Output. Referenced to V_{CCB}
1B3	5	C2	I/O	Input/Output. Referenced to V_{CCB}
1B4	6	C1	I/O	Input/Output. Referenced to V_{CCB}
1B5	8	D2	I/O	Input/Output. Referenced to V_{CCB}
1B6	9	D1	I/O	Input/Output. Referenced to V_{CCB}
1B7	11	E2	I/O	Input/Output. Referenced to V_{CCB}
1B8	12	E1	I/O	Input/Output. Referenced to V_{CCB}
1DIR	1	A1	I	Direction-control signal

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	DGG / DGV	GQL / ZQL		
$1\overline{OE}$	48	A6	I	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to V_{CCA}
2A1	36	F6	I/O	Input/Output. Referenced to V_{CCA}
2A2	35	F5	I/O	Input/Output. Referenced to V_{CCA}
2A3	33	G6	I/O	Input/Output. Referenced to V_{CCA}
2A4	32	G5	I/O	Input/Output. Referenced to V_{CCA}
2A5	30	H6	I/O	Input/Output. Referenced to V_{CCA}
2A6	29	H5	I/O	Input/Output. Referenced to V_{CCA}
2A7	27	J6	I/O	Input/Output. Referenced to V_{CCA}
2A8	26	J5	I/O	Input/Output. Referenced to V_{CCA}
2B1	13	F1	I/O	Input/Output. Referenced to V_{CCB}
2B2	14	F2	I/O	Input/Output. Referenced to V_{CCB}
2B3	16	G1	I/O	Input/Output. Referenced to V_{CCB}
2B4	17	G2	I/O	Input/Output. Referenced to V_{CCB}
2B5	19	H1	I/O	Input/Output. Referenced to V_{CCB}
2B6	20	H2	I/O	Input/Output. Referenced to V_{CCB}
2B7	22	J1	I/O	Input/Output. Referenced to V_{CCB}
2B8	23	J2	I/O	Input/Output. Referenced to V_{CCB}
2DIR	24	K1	I	Direction-control signal
$2\overline{OE}$	25	K6	I	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to V_{CCA}
GND	4	B3	—	Ground
		B4		
	10	D3		
	15	D4		
	21	G3		
	28	G4		
	34	J3		
	45	J4		
NC(1)	—	A2	—	
		A3		
		A4		
		A5		
		K2		
		K3		
		K4		
		K5		
V_{CCA}	31	C4	—	A-port supply. 1.65 V ≤ V_{CCA} ≤ 5.5 V
	42	H4		
V_{CCB}	7	C3	—	B-port supply. 1.65 V ≤ V_{CCB} ≤ 5.5 V
	18	H3		

(1) NC – No internal connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)	I/O ports (A port)	–0.5	6.5	V
		I/O ports (B port)	–0.5	6.5	
		Control inputs	–0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	6.5	V
		B port	–0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA}, V_{CCB}, and GND			±100	mA
T_J	Junction temperature		-40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input (V_I) and output (V_O) negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

See (1)(2)(3)(4)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs(5)	1.65 V to 1.95 V		V_{CCI} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCI} × 0.7		
V_{IL}	Low-level input voltage	Data inputs(5)	1.65 V to 1.95 V			V_{CCI} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCI} × 0.3	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCA})(6)	1.65 V to 1.95 V		V_{CCA} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCA} × 0.7		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCA})(6)	1.65 V to 1.95 V			V_{CCA} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCA} × 0.3	
V_I	Input voltage	Control inputs			0	5.5	V
$V_{I/O}$	Input/output voltage	Active state			0	V_{CCO}	V
		Tri-State			0	5.5	
I_{OH}	High-level output current			1.65 V to 1.95 V		–4	mA
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–24	
				4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) All unused data inputs of the device must be held at V_{CCA} or GND to ensure proper device operation.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(6) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

7.4 Thermal Information

THERMAL METRIC[1]		SN74LVC16T245				UNIT
		DL (SSOP)	DGG (TSSOP)	DGV (TVSOP)	GQL / ZQL (BGA)	
		48 PINS	48 PINS	48 PINS	56 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.9	60	82.5	64.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.5	13.9	34.2	16.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.5	27.1	45.1	30.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.1	0.5	2.7	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.9	26.8	44.6	64.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1] [2]

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100 µA, $V_I = V_{IH}$	1.65 V to 4.5 V	1.65 V to 4.5 V				V_{CCO} – 0.1		V
		I_{OH} = –4 mA, $V_I = V_{IH}$	1.65 V	1.65 V				1.2		
		I_{OH} = –8 mA, $V_I = V_{IH}$	2.3 V	2.3 V				1.9		
		I_{OH} = –24 mA, $V_I = V_{IH}$	3 V	3 V				2.4		
		I_{OH} = –32 mA, $V_I = V_{IH}$	4.5 V	4.5 V				3.8		
V_{OL}		I_{OL} = 100 µA, $V_I = V_{IL}$	1.65 V to 4.5 V	1.65 V to 4.5 V					0.1	V
		I_{OL} = 4 mA, $V_I = V_{IL}$	1.65 V	1.65 V					0.45	
		I_{OL} = 8 mA, $V_I = V_{IL}$	2.3 V	2.3 V					0.3	
		I_{OL} = 24 mA, $V_I = V_{IL}$	3 V	3 V					0.55	
		I_{OL} = 32 mA, $V_I = V_{IL}$	4.5 V	4.5 V					0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±2	µA
I_{off}	A or B port	V_I or V_O = 0 to 5.5 V	0 V	0 to 5.5 V			±1		±2	µA
			0 to 5.5 V	0 V			±1		±2	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±2	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					20	µA
			5 V	0 V					20	
			0 V	5 V					–2	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					20	µA
			5 V	0 V					–2	
			0 V	5 V					20	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					30	µA
ΔI_{CCA}	A port	One A port at V_{CCA} – 0.6 V, DIR at V_{CCA}, B port = open	3 V to 5.5 V	3 V to 5.5 V					50	µA
	DIR	DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND							50	
ΔI_{CCB}	B port	One B port at V_{CCB} – 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V					50	µA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	3.3 V	3.3 V		4			5	pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
C_{io}	A or B port	$V_O = V_{CCA/B}$ or GND	3.3 V	3.3 V		8.5			10	pF

7.6 Switching Characteristics: V_{CCA} = 1.8 V ±0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B	1.7	21.9	1.3	9.2	1	7.4	0.8	7.1	ns
t_{PLH} / t_{PHL}	B	A	0.9	23.8	0.8	23.6	0.7	23.4	0.7	23.4	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A	1.6	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B	2.4	32.2	1.9	13.1	1.7	12	1.3	10.3	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A	0.4	24	0.4	23.8	0.4	23.7	0.4	23.7	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B	1.8	32	1.6	16	1.2	12.6	0.9	10.8	ns

7.7 Switching Characteristics: V_{CCA} = 2.5 V ±0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B	1.6	21.4	1.2	9	0.8	6.2	0.6	4.8	ns
t_{PLH} / t_{PHL}	B	A	1.2	9.3	1	9.1	1	8.9	0.9	8.8	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A	1.4	9	1.4	9	1.4	9	1.4	9	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B	2.3	29.6	1.8	11	1.7	9.3	0.9	6.9	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A	1	10.9	1	10.9	1	10.9	1	10.9	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B	1.7	28.2	1.6	12.9	1.2	9.4	1	6.9	ns

7.8 Switching Characteristics: V_{CCA} = 3.3 V ±0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B	1.5	21.2	1.1	8.8	0.8	6.1	0.5	4.4	ns
t_{PLH} / t_{PHL}	B	A	0.9	7.2	0.8	6.2	0.7	6.1	0.6	6	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A	1.6	8.2	1.6	8.2	1.6	6.2	1.6	8.2	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B	2.1	29	1.7	10.3	1.5	8.6	0.8	6.3	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A	0.8	7.8	0.8	7.8	0.8	7.8	0.8	7.8	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B	1.6	27.7	1.4	12.4	1.1	8.5	0.9	8.4	ns

7.9 Switching Characteristics: V_{CCA} = 5 V ±0.5 V

over recommended operating free-air temperature range, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ±0.15 V		V_{CC} = 2.5 V ±0.2 V		V_{CC} = 3.3 V ±0.3 V		V_{CC} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B	1.6	21.4	1	8.8	0.7	6	0.4	4.2	ns
t_{PLH} / t_{PHL}	B	A	0.7	6.8	0.4	4.8	0.3	4.5	0.3	4.3	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A	0.3	5.4	0.3	5.4	0.3	5.4	0.3	6.4	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B	2	28.7	1.6	9.7	1.4	8	0.7	5.7	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A	0.7	5.5	0.7	5.5	0.7	5.5	0.7	5.5	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B	1.6	27.6	1.3	11.4	1	8.1	0.9	6	ns

7.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	2	2	2	3	pF
	B-port input, A-port output		18	19	19	22	
C_{pdB} (1)	A-port input, B-port output		18	19	20	22	
	B-port input, A-port output		2	2	2	2	

(1) Power dissipation capacitance per transceiver. Refer to the TI application report, *CMOS Power Consumption and Cpd Calculation*, SCAA035

7.11 Typical Characteristics

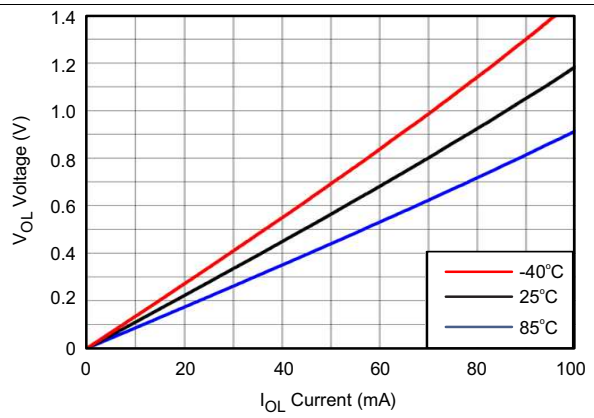


Figure 1. V_{OL} Voltage vs I_{OL} Current

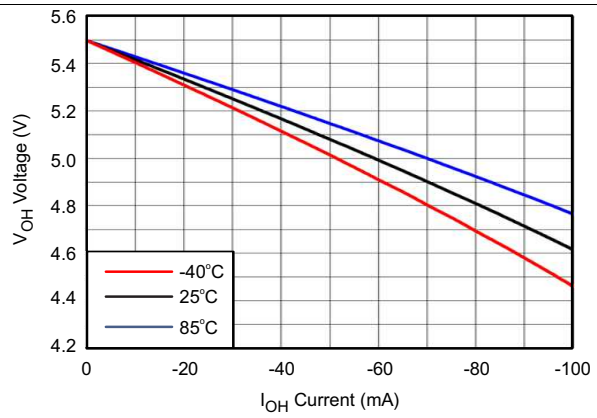
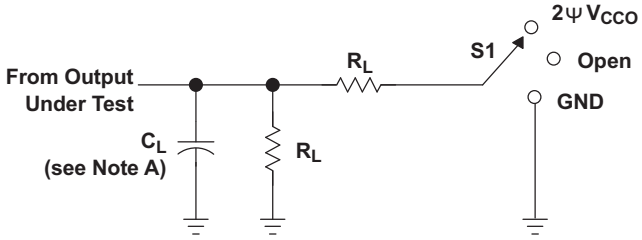


Figure 2. V_{OH} Voltage vs I_{OH} Current

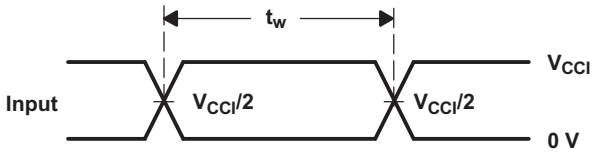
8 Parameter Measurement Information



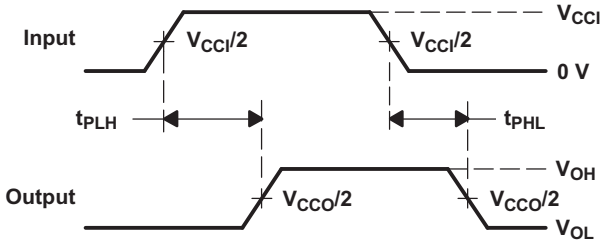
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2\psi V_{CCO}$
t_{PHZ}/t_{PZH}	GND

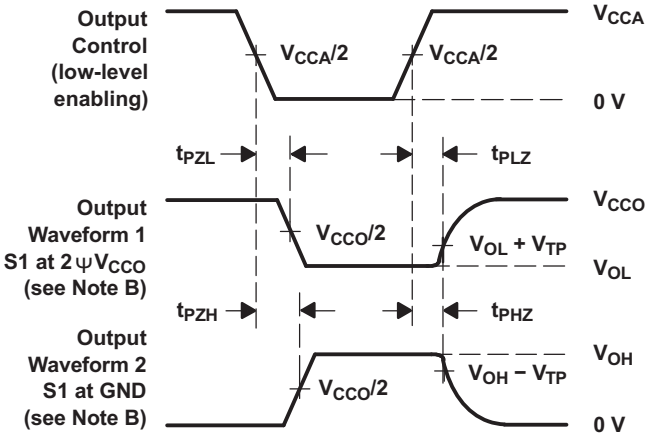
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.
F. V_{CCI} is the V_{CC} associated with the input port.
G. V_{CCO} is the V_{CC} associated with the output port.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

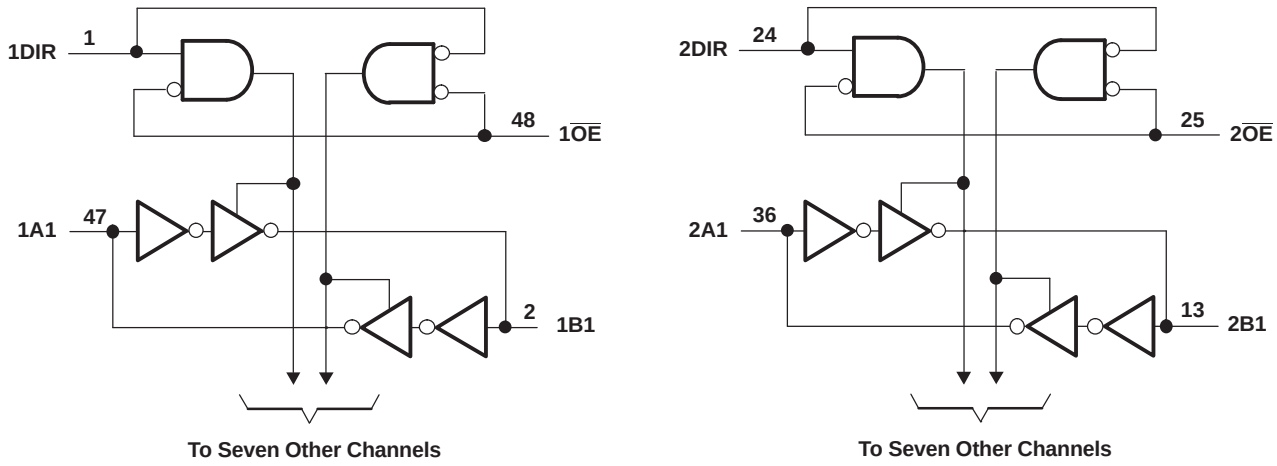
9.1 Overview

The SN74LVC16T245 is a 16-bit, dual-supply noninverting bidirectional voltage level translation. Pins A and control pins (DIR and $\overline{OE}$) are supported by V_{CCA} and pins B are supported by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.65 V to 5.5 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both A and B are in the high-impedance state.

This device is fully specified for partial-power-down applications using off output current (I_{off}).

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are put in a high-impedance state.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.65 V to 5.5 V making the device suitable for translating between any of the low voltage nodes (1.8-V, 2.5-V, and 3.3-V).

9.3.2 Support High-Speed Translation

SN74LVC16T245 can support high data rate application. Data rates can be calculated form the maximum propagation delay. This is also dependant on the output load. For example, for a 3.3-V to 5-V conversion, the maximum frequency is 200 MHz.

9.3.3 Partial-Power-Down Mode Operation

This device is fully specified for partial-power-down applications using off output current (I_{off}). I_{off} will prevent backflow current by disabling I/O output circuits when device is in partial power-down mode.

9.3.4 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND, both ports will be in a high-impedance state (I_{OZ} shown in *Electrical Characteristics*). This prevents false logic levels from being presented to either bus.

9.4 Device Functional Modes

The functional modes for the SN74LVC16T245 device are shown in Table 1.

Table 1. Function Table(1)
(Each Transceiver)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LVC16T245 device can be used in level-shifting applications for interfacing devices and addressing mixed voltage incompatibility. The SN74LVC16T245 device is ideal for data transmission where direction is different for each channel.

10.1.1 Enable Times

Calculate the enable times for the SN74LV16T245 using the following formulas:

t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A) (1)

t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A) (2)

t_{PZH} (DIR to B) =t_{PLZ} (DIR to A) + t_{PLH} (A to B) (3)

t_{PZL} (DIR to B) = t_{PHZ}(DIR to A) + t_{PHL} (A to B) (4)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC16T245 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

10.2 Typical Application

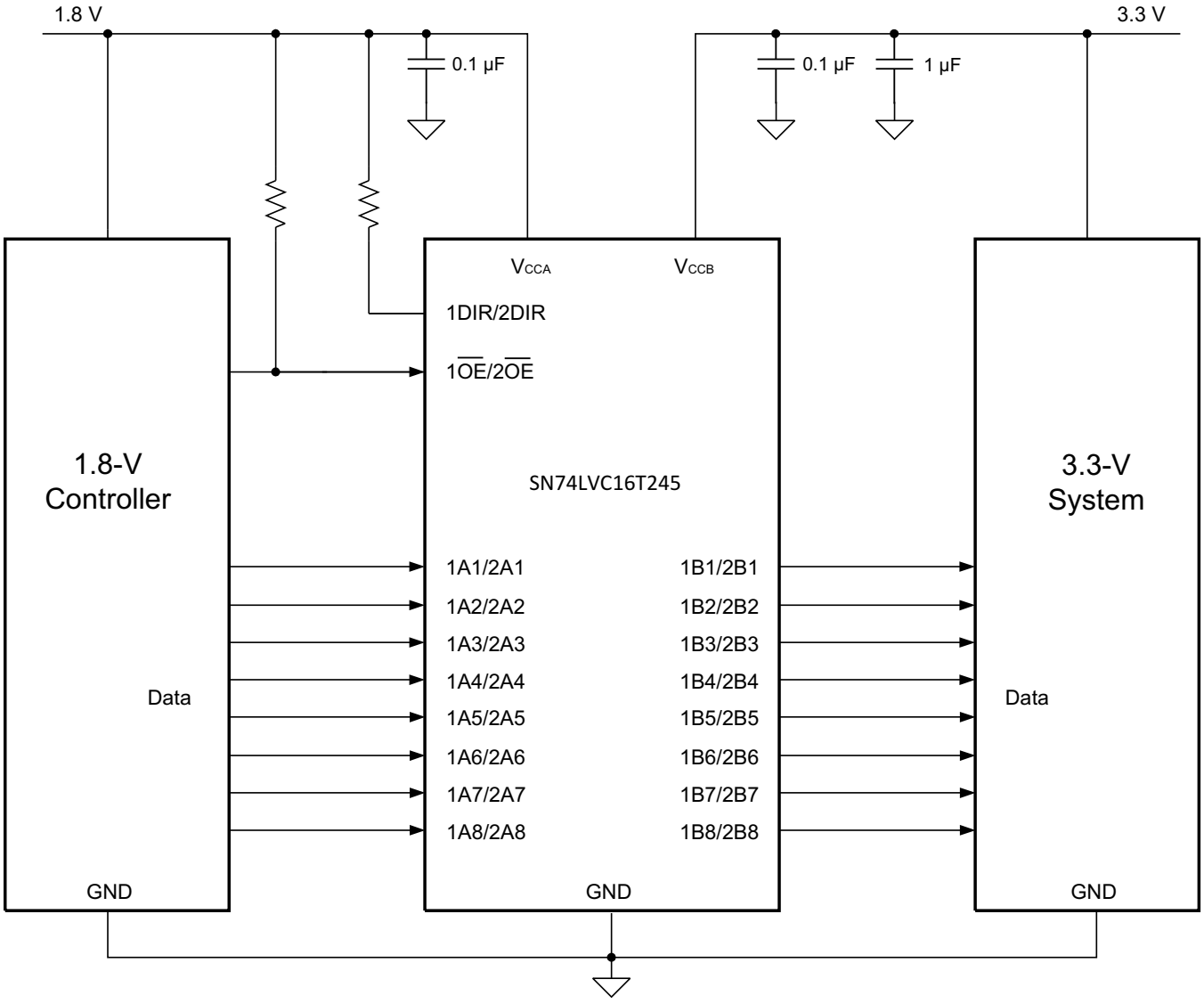


Figure 4. Typical Application Schematic

10.2.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. It is important that unused data inputs not be floating, as this can cause excessive internal leakage on the input CMOS structure. Make sure to tie any unused input and output ports directly to ground. For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	1.65 V to 5.5 V
Output voltage	1.65 V to 5.5 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LVC16T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LVC16T245 device is driving to determine the output voltage range.

10.2.3 Application Curve

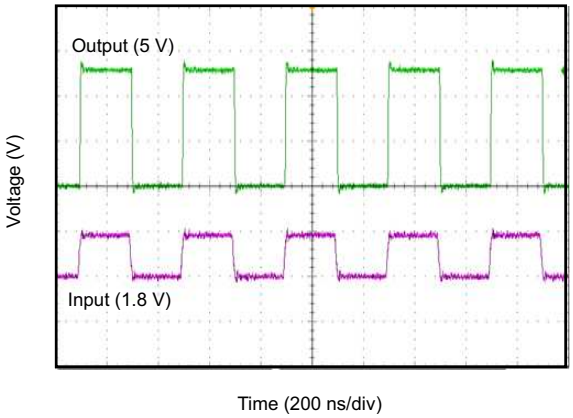


Figure 5. Translation Up (1.8 V to 5 V) at 2.5 MHz

11 Power Supply Recommendations

The SN74LVC16T245 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V and V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. The A port and B port are designed to track V_{CCA} and V_{CCB}, respectively, allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V and 3.3-V voltage nodes.

The output-enable $\overline{OE}$ input circuit is supplied by V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit-board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

12.2 Layout Example

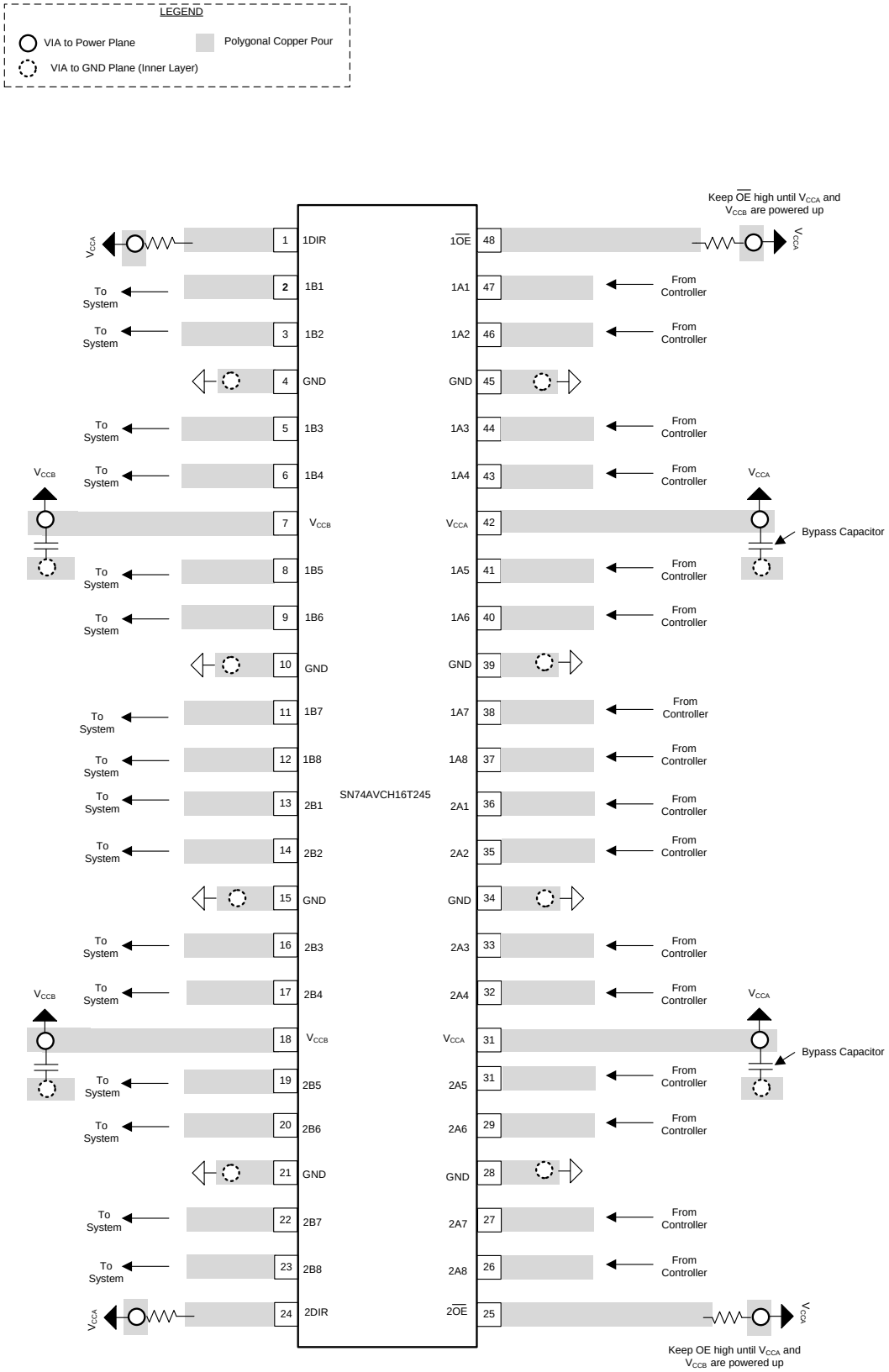


Figure 6. SN74LVC16T245 Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *CMOS Power Consumption and Cpd Calculation*, SCAA035
- *Implications of Slow or Floating CMOS Inputs*, SCBA004

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC16T245DGGRE4	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245
74LVC16T245DGGRG4	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245
74LVC16T245DGVRG4	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LDT245
SN74LVC16T245DGGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245
SN74LVC16T245DGGR.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245
SN74LVC16T245DGVR	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LDT245
SN74LVC16T245DGVR.B	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LDT245
SN74LVC16T245DL	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245
SN74LVC16T245DL.B	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245
SN74LVC16T245DLR	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245
SN74LVC16T245DLR.B	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245
SN74LVC16T245DLRG4	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245
SN74LVC16T245DLRG4.B	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC16T245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC16T245 :

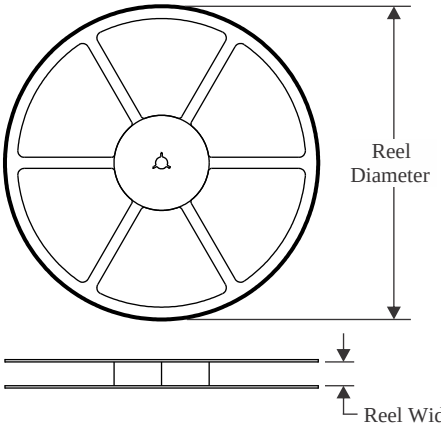
- Enhanced Product : SN74LVC16T245-EP

NOTE: Qualified Version Definitions:

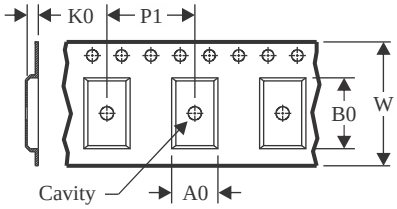
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

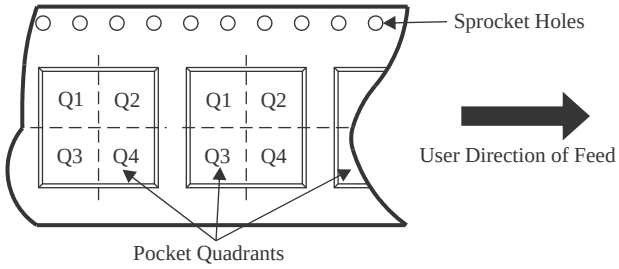


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

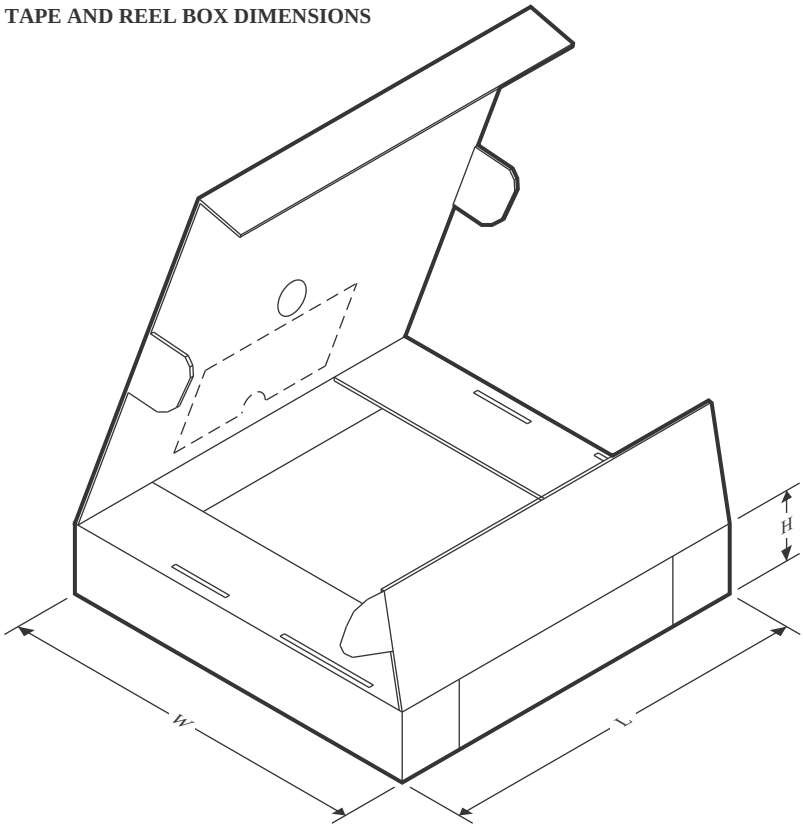
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC16T245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVC16T245DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVC16T245DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVC16T245DLRG4	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

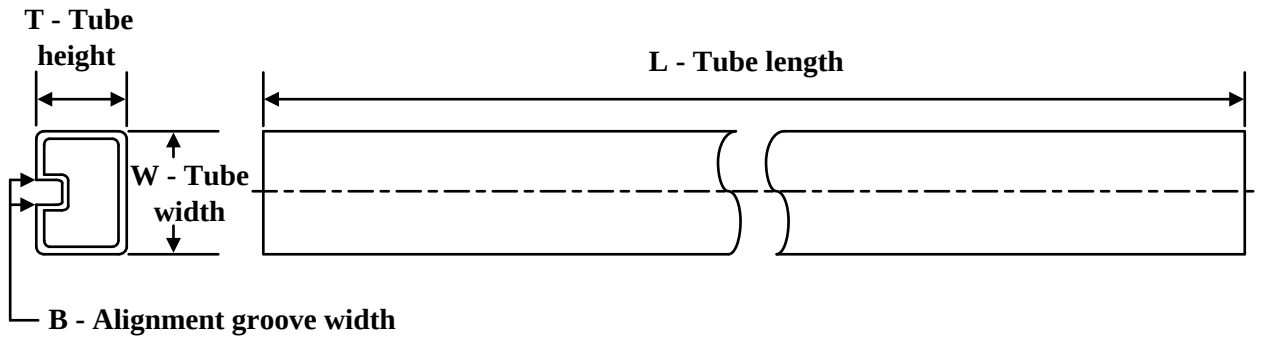
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC16T245DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVC16T245DGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74LVC16T245DLR	SSOP	DL	48	1000	356.0	356.0	53.0
SN74LVC16T245DLRG4	SSOP	DL	48	1000	356.0	356.0	53.0

TUBE

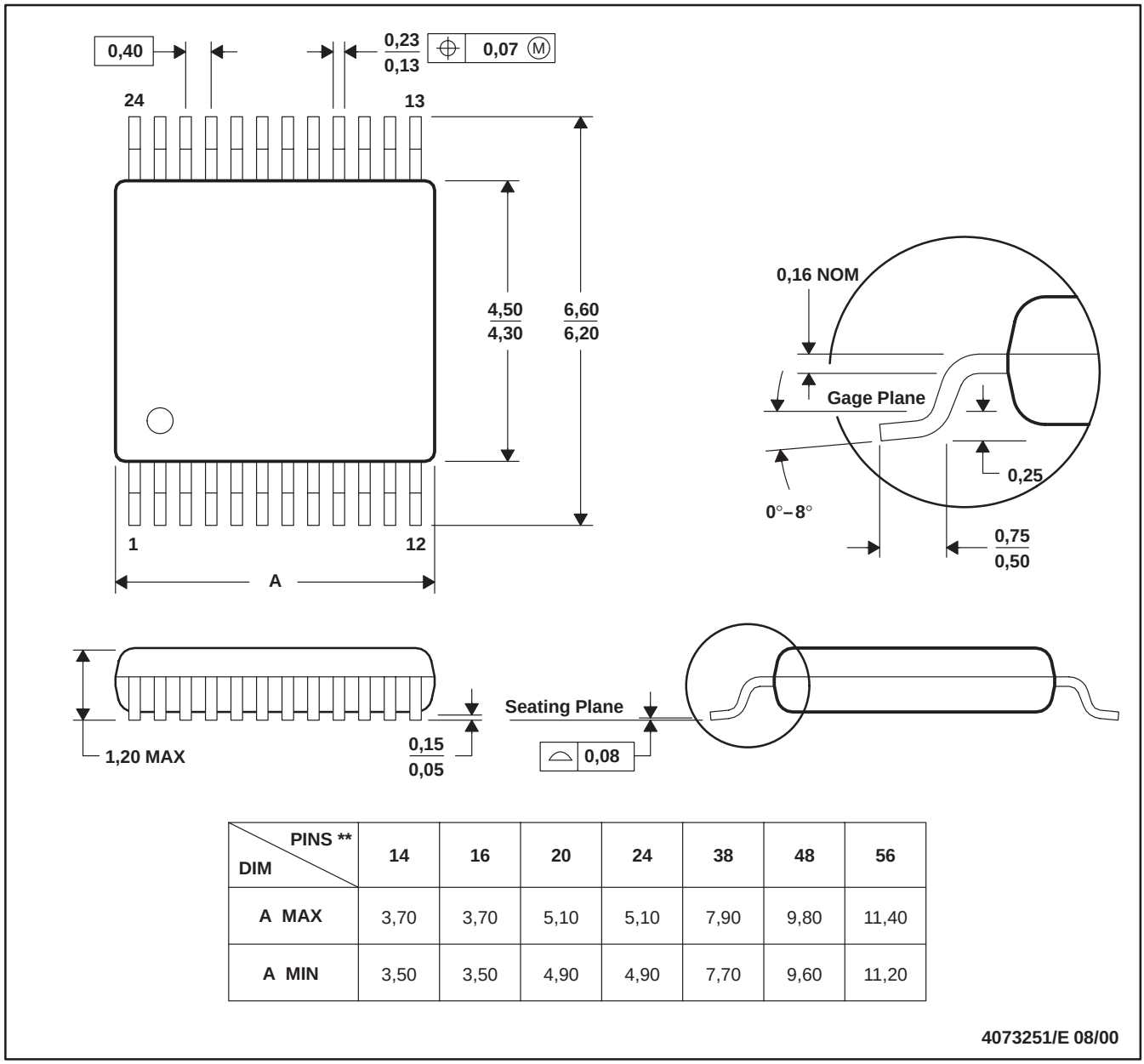


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC16T245DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVC16T245DL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

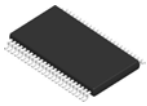
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

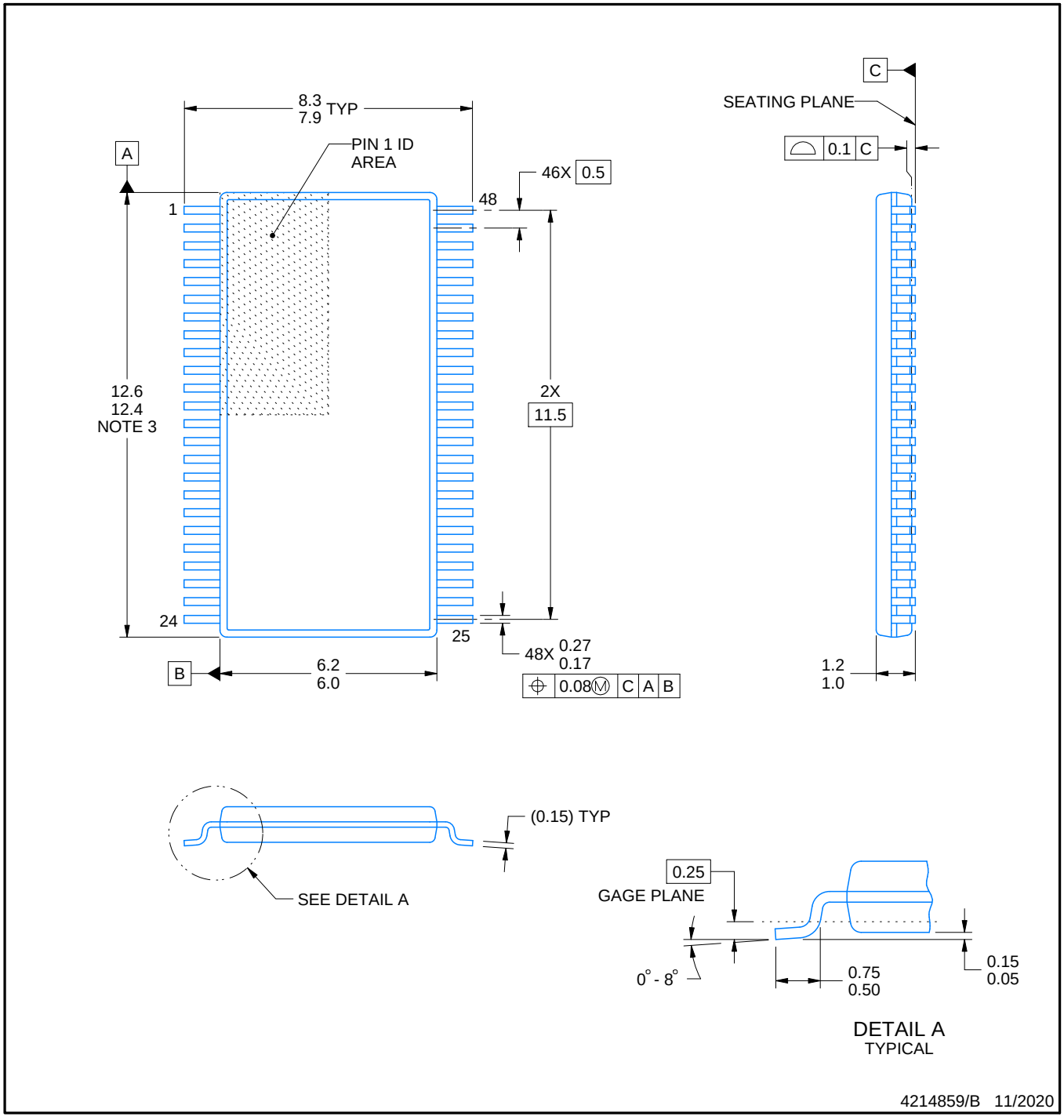


PACKAGE OUTLINE

DGG0048A

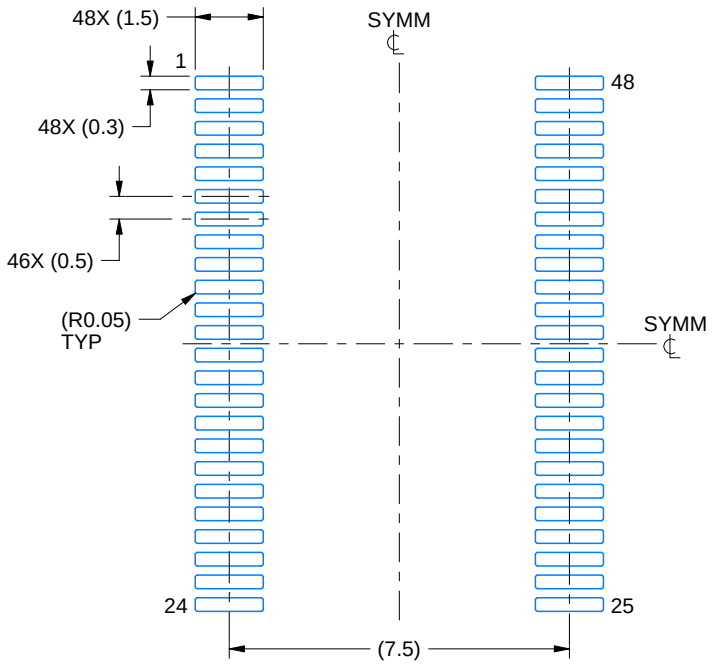
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

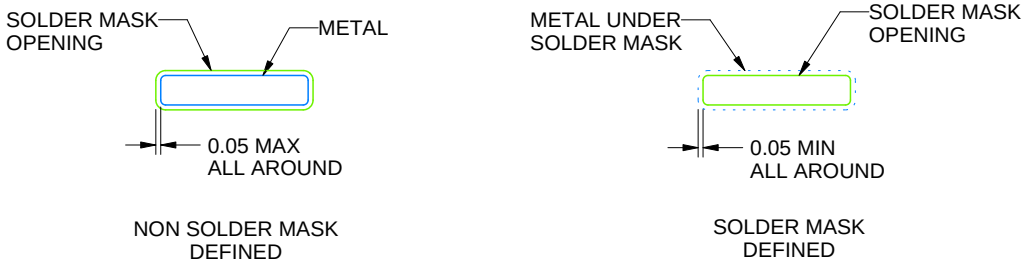


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

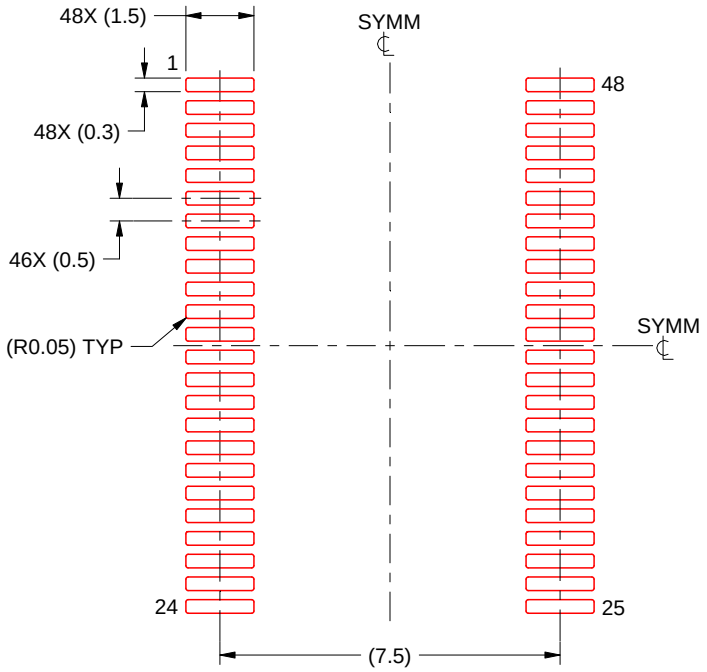


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

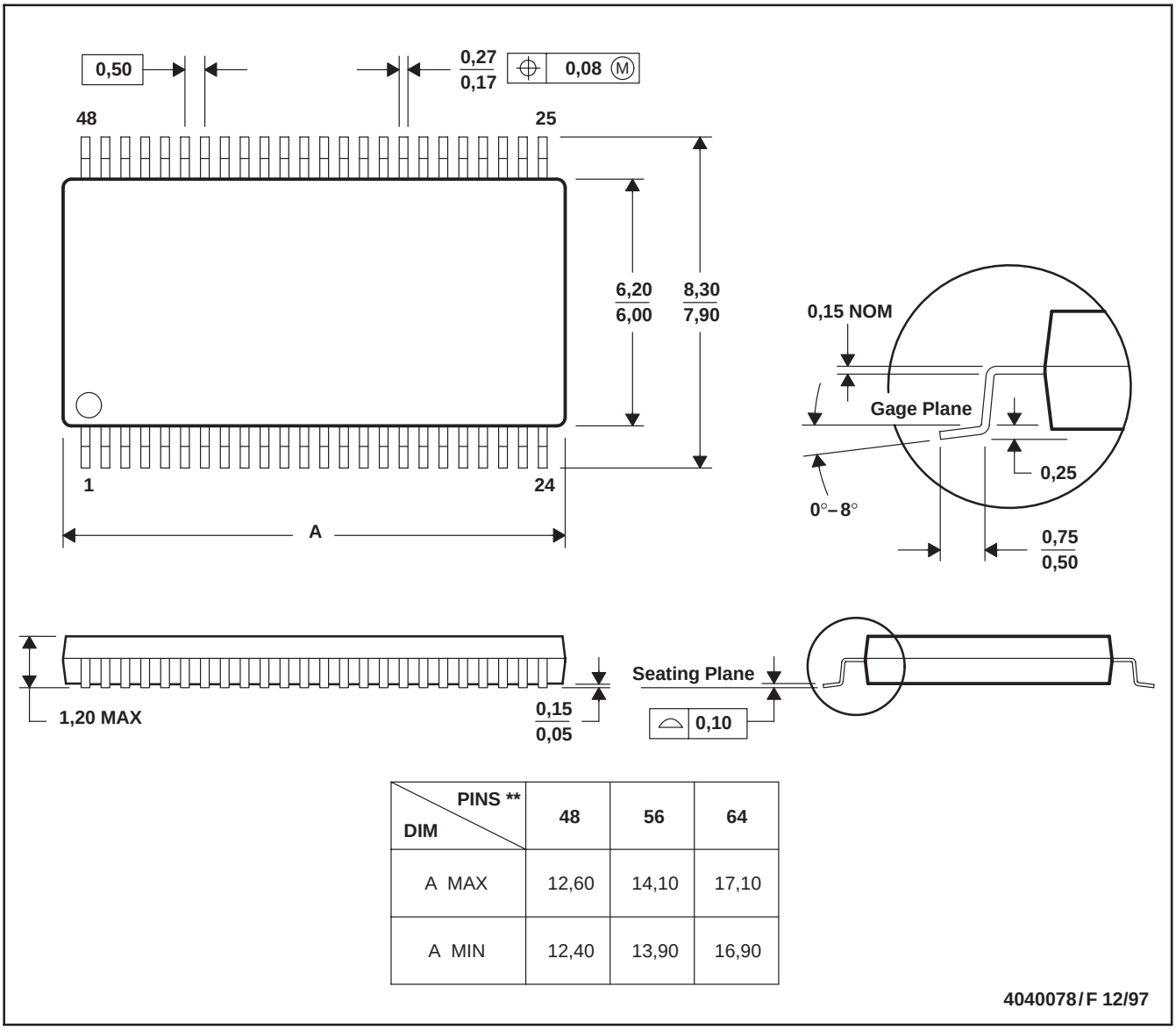
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

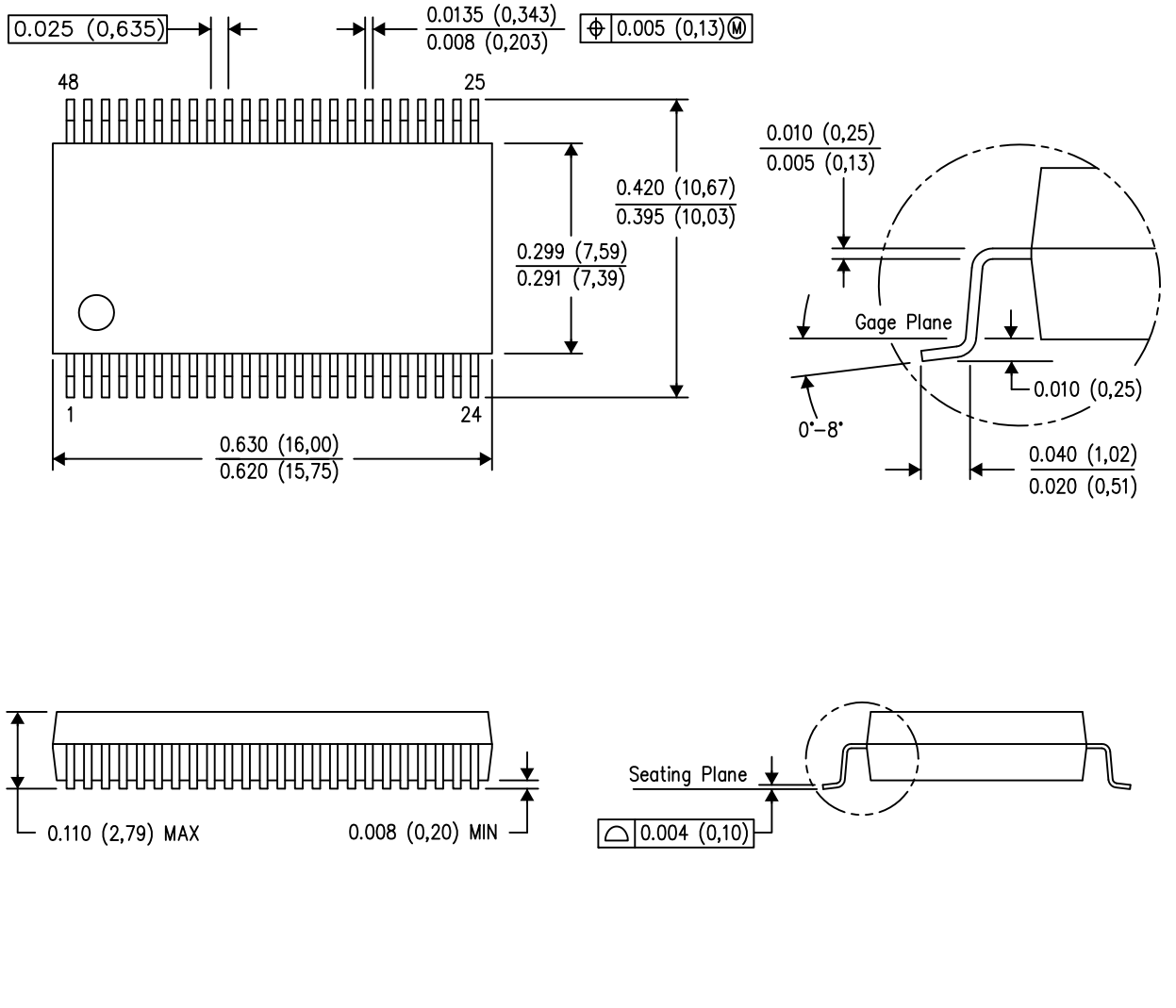
48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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