











SN74LVC1404

SCES469F - AUGUST 2003 - REVISED MARCH 2020

SN74LVC1404 Oscillator Driver for Crystal Oscillator or Ceramic Resonator

Features

- Available in the Texas Instruments NanoFree™ package
- Supports 5-V V_{CC} operation
- Inputs accept voltages to 5.5 V
- One buffered inverter with Schmitt-trigger input and two unbuffered inverters
- Integrated solution for oscillator applications
- Suitable for commonly used clock frequencies:
 - 15 kHz, 3.58 MHz, 4.43 MHz, 13 MHz, 25 MHz, 26 MHz, 27 MHz, 28 MHz
- Control input to disable the oscillator circuit
- Low power consumption (10-µA Max I_{CC}) in standby state
- ±24-mA Output Drive at 3.3 V
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100 mA Per JESD 78, Class II
- ESD protection exceeds JESD 22
 - 2000-V Human-body model (A114-A)
 - 200-V Machine model (A115-A)
 - 1000-V Charged-device model (C101)

Applications

- Servers
- PCs and notebooks
- Network switches
- Wearable health and fitness devices
- Telecom infrastructures
- Electronic points-of-sale

3 Description

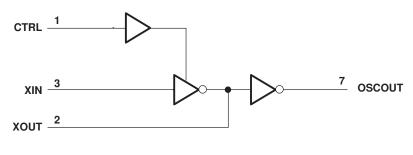
The SN74LVC1404 device consists of one inverter with a Schmitt-trigger input and two unbuffered inverters. It is designed for 1.65-V to 5.5-V V_{CC} operation.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1404DCT	SM8 (8)	2.95 mm × 2.80 mm
SN74LVC1404DCU	VSSOP (8)	2.30 mm × 2.00 mm
SN74LVC1404YZP	DSBGA (8)	1.88 mm × 0.88 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



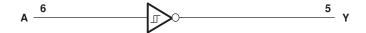




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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

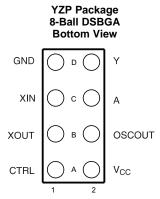
С	hanges from Revision E (June 2014) to Revision F	Page
•	Formatted pinout figures for search capability	3
•	Corrected pin numbering for the DSBGA package to match the mechanical drawing	3
•	Changed ESD Ratings table format to comply with JEDEC standards	4
•	Added YZP T _A MIN /MAX specs and package thermal information	5

Cł	nanges from Revision D (January 2007) to Revision E	Page
•	Updated document to new TI data sheet format	1
•	Removed Ordering Information table.	1
•	Added Applications.	1
•	Added Device Information table.	1
•	Added Handling Ratings table.	4
•	Changed MAX ambient temperature to 125°C.	5
•	Added Thermal Information table.	5
•	Added Typical Characteristics.	7



6 Pin Configuration and Functions





See mechanical drawings for dimensions.

Drawings not to scale

Pin Functions

PIN	PIN NO.		1/0	DESCRIPTION
DCT/DCU	YZP	NAME	2	DESCRIPTION
1	A1	CTRL	-	OSC Control
2	B1	XOUT	0	Crystal Connection Out
3	C1	XIN	_	Crystal Connection In
4	D1	GND	-	Ground
5	D2	Υ	0	Schmitt Trigger Output
6	C2	Α	_	Schmitt Trigger Input
7	B2	OSCOUT	0	Oscillator Output
8	A2	VCC	_	Power Supply

Product Folder Links: SN74LVC1404



Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range (2)	XIN, A, CTRL inputs	-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power-off state (2)	Y output	-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state (2)(3)	XOUT, OSCOUT	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _{stg}	Storage Temperature Range		-65	150	°C
TJ	Junction Temperature			150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

	-		MAX	UNIT
V	Flootrootatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed. The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V	Cupality valtage	Operating	1.65	5.5	V
V_{CC}	Supply voltage	Data retention only	1.5		V
VI	Input voltage (XIN, CTRL, A inputs)		0	5.5	V
Vo	Output voltage (XOUT, OSCOUT, Y outputs)		0	V_{CC}	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
I_{OH}	High-level output current (OSCOUT, XOUT, Y outputs)	V 2.V		-16	-
		$V_{CC} = 3 V$		-24	
		V _{CC} = 4.5 V		-32	
	$V_{CC} = 1.65 \text{ V}$ $V_{CC} = 2.3 \text{ V}$	V _{CC} = 1.65 V		4	
			8		
I_{OL}	Low-level output current (OSCOUT, XOUT, Y outputs)	V - 2 V		16	mA
		V _{CC} = 3 V	V _{CC} = 3 V		
		V _{CC} = 4.5 V		32	
I _{OL} (2)	Low-level output current (XOUT)	V _{CC} = 1.65 V		2	mA
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		20	
Δt/Δν	Input transition vice and fall time (CTDL input)	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		20	20/1
ΔΨΔν	Input transition rise and fall time (CTRL input)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		V _{CC} = 5 V ± 0.5 V		5	
т	Operating free air temperature	DCU, DCT	-40	125	°C
T_A	Operating free-air temperature	YZP	-40	85	-0

 ⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
 (2) CTRL = Low, XIN = GND

7.4 Thermal Information

	THERMAL METRIC ⁽¹⁾	DCT	DCU	YZP	LINUT
	THERMAL METRIC**	8 PINS	8 PINS	8 BALLS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.8	198.4	97.5	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115.3	73.5	1.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	97.3	77.1	26.3	°C/W
ΨЈТ	Junction-to-top characterization parameter	40.9	6.1	0.5	
ΨЈВ	Junction-to-board characterization parameter	96.3	76.7	26.2	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

Product Folder Links: SN74LVC1404



7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARA	AMETER	TEST CONDITIONS	V _{cc}	MIN TYP ⁽¹⁾	MAX	UNIT	
			1.65 V	0.79	1.16		
V_{T+}			2.3 V	1.11	1.56		
Positive- going	A input		3 V	1.5	1.87	V	
threshold			4.5 V	2.16	2.74		
			5.5 V	2.61	3.33		
			1.65 V	0.39	0.62		
V_{T-}			2.3 V	0.58	0.87		
Negative- going	A input		3 V	0.84	1.14	V	
threshold			4.5 V	1.41	1.79		
			5.5 V	1.87	2.29		
			1.65 V	0.37	0.62		
ΔV_{T}			2.3 V	0.48	0.77		
hysteresis	A input		3 V	0.56	0.87	V	
$(V_{T+} - V_{T-})$			4.5 V	0.71	1.04		
			5.5 V	0.71	1.11		
		I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} – 0.1			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		V	
v (2)		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			
		I _{OH} = -16 mA	3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2.3				
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
		I _{OL} = 100 μA	1.65 V to 5.5 V		0.1		
		I _{OL} = 4 mA	1.65 V		0.45		
v (2)		I _{OL} = 8 mA	2.3 V		0.3		
V _{OL} (=)		I _{OL} = 16 mA	3 V		0.4	V	
V _{OH} ⁽²⁾		I _{OL} = 24 mA	3 V		0.55		
		I _{OL} = 32 mA	4.5 V	0.58 0.87 0.84 1.14 1.41 1.79 1.87 2.29 0.37 0.62 0.48 0.77 0.56 0.87 0.71 1.04 0.71 1.11 V V _{CC} - 0.1 1.9 2.4 2.3 3.8 V 0.1 0.45 0.3 0.4 0.55 V 0.1 0.65 V 0.65 ±5 V 10 µA ±10 V 500 µA 500 µA			
	XOUT	$I_{OL} = 100 \mu A$ CTRL = Low, XIN = GND	1.65 V to 5.5 V		0.1		
V_{OL}	X001	$I_{OL} = 2 \text{ mA}$	1.65 V		0.65	V	
I _I	All inputs	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V		±5	μΑ	
l _{off}	Y output	V_I or $V_O = 0$ to 5.5 V	0		±10	μΑ	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	1.65 V to 5.5 V		10	μΑ	
Δl _{CC}	CTRL and A inputs	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500	μA	
C _i	CTRL and A inputs	$V_I = V_{CC}$ or GND	3.3 V	3.5		pF	
	XIN			6	6		

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⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) $V_{IL} = 0 \text{ V}$ and $V_{IH} = V_{CC}$ for XOUT and OSCOUT; the standard V_{T+} and V_{T-} levels should be applied for the Y output.



7.6 Switching Characteristics, $C_L = 15 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = : ± 0.2		V _{CC} = 0.3			UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Α	Υ	2.8	15.1	1.6	5.7	1.5	4.6	0.9	4.4	
4	XIN —	XOUT	1.7	9.6	1	3.2	1.1	2.4	0.9	1.8	
t _{pd}		OSCOUT	2.6	17.2	2	5.6	2	4.1	1.5	3.2	ns
		XOUT	3	28.2	1.8	14.4	1.5	12.2	1.1	10.2	

7.7 Switching Characteristics, $C_L = 30 \text{ pF}$ or 50 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = : ± 0.2		V _{CC} = 3 ± 0.3		V _{CC} = ± 0.5		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Α	Υ	3	17.3	1.8	7.4	1.8	6.4	1	5.3	
4	XIN	XOUT	1.2	15.8	0.8	5.8	1	5.4	0.6	4.6	no
t _{pd}	AIN	OSCOUT	3.5	25.7	2.6	7.1	2.8	7.8	2	6.7	ns
	CTRL	XOUT	3.3	24.5	2.1	12	1.9	12.7	1.1	11.2	

7.8 Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	V _{CC} = 5 V TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	25	26	29	39	pF

7.9 Typical Characteristics

Figure 1 shows the open-loop-gain characteristics of the unbuffered inverter of the LVC1404 (that is, between XIN and XOUT). The device provides a high gain over a wide range of frequencies.

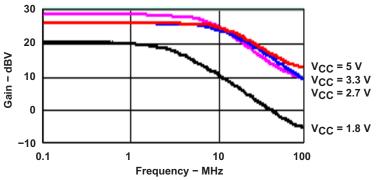


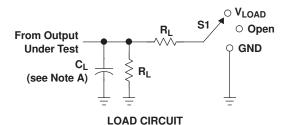
Figure 1. Open-Loop-Gain Characteristics

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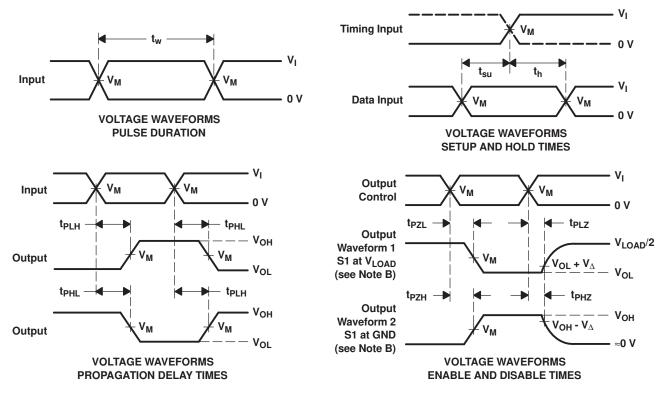


8 Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open V _{LOAD} GND

.,	INF	PUTS	.,	N RL	RL	R_L	V	
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	(Except t _{PZ})	(t _{PZ})	$oldsymbol{V}_\Delta$
1.8 V \pm 0.15 V	v _{cc}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 Μ Ω	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	1 Μ Ω	1 k Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 Μ Ω	1 k Ω	0.3 V
5 V \pm 0.5 V	V _{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	15 pF	1 Μ Ω	1 k Ω	0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

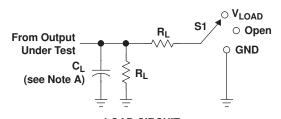
Figure 2. Load Circuit and Voltage Waveforms

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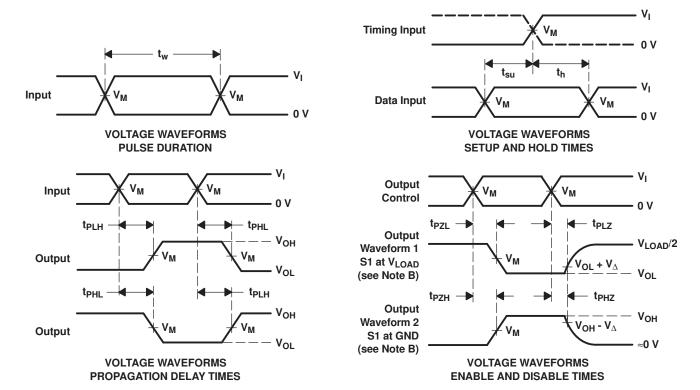
Parameter Measurement Information (continued)



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V_{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD	CIRCUIT

V	INI	PUTS	V V 0 D		, , , , , , , , , , , , , , , , , , ,		V
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	RL	V_{Δ}
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{CC}	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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9 Detailed Description

9.1 Overview

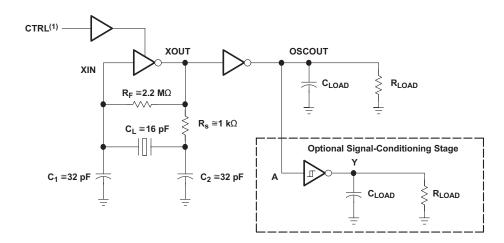
The SN74LVC1404 device consists of one inverter with a Schmitt-trigger input and two unbuffered inverters. It is designed for 1.65-V to 5.5-V V_{CC} operation.

XIN and XOUT pins can be connected to a crystal or resonator in oscillator applications. The SN74LVC1404 device provides an additional unbuffered inverter (OSCOUT) and a Schmitt-trigger input inverter for signal conditioning (see the *Functional Block Diagram*). The control (CTRL) input disables the oscillator circuit to reduce power consumption. The oscillator circuit is disabled and the XOUT output is set to low level when CTRL is low. To ensure the oscillator circuit remains disabled during power up or power down, CTRL should be connected to GND through a pulldown resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

9.2 Functional Block Diagram



9.3 Feature Description

- · Wide operating voltage range
 - Operates from 1.65 V to 5.5 V
- Has buffered output and un-buffered output from oscillator
- Schmitt-trigger buffer
 - Allows for extra buffering of the oscillator output
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V

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9.4 Device Functional Modes

Table 1. Function Table

INP	JTS	OUTPUTS		
CTRL	XIN	XOUT	OSCOUT	
Н	L	Н	Г	
Н	Н	L	Н	
L	X	L	Н	

Table 2. Function Table

INPUT A	OUTPUT Y
L	Н
Н	L

Product Folder Links: SN74LVC1404



10 Application and Implementation

10.1 Application Information

Figure 4 shows a typical application of the SN74LVC1404 device in a Pierce oscillator circuit. The output voltage can be conditioned further by connecting OSCOUT to the Schmitt-trigger input inverter. The Schmitt-trigger input inverter produces a rail-to-rail voltage waveform. The recommended load for the crystal, shown in this example, is 16 pF. The value of the recommended load (C_L) can be found in the crystal manufacturer's data sheet. Values

10.2 Typical Application

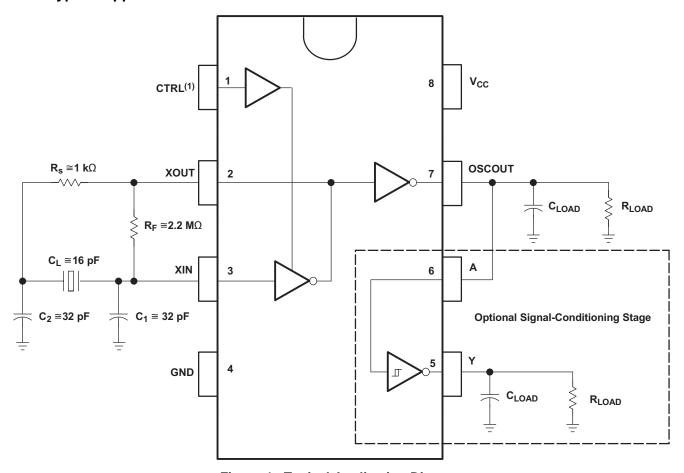


Figure 4. Typical Application Diagram

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Typical Application (continued)

10.2.1 Design Requirements

- The open-loop gain of the unbuffered inverter decreases as power-supply voltage decreases. This decreases
 the closed-loop gain of the oscillator circuit. The value of R_s can be decreased to increase the closed-loop
 gain, while maintaining the power dissipation of the crystal within the maximum limit.
- R_s and C₂ form a low-pass filter and reduce spurious oscillations. Component values can be adjusted, based on the desired cutoff frequency.
- C₂ can be increased over C₁ to increase the phase shift and help in start-up of the oscillator. Increasing C₂
 may affect the duty cycle of the output voltage.
- At high frequency, phase shift due to R_s becomes significant. In this case, R_s can be replaced by a capacitor to reduce the phase shift.

10.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the Recommended Operating Conditions table.
 - Specified high and low levels: See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{\rm CC}$.
- 2. Recommended Output Conditions
 - Load currents should not exceed 50 mA per output and 100 mA total for the part.
 - Outputs should not be pulled above V_{CC}.

10.2.2.1 Testing

After the selection of proper component values, the oscillator circuit should be tested, using these components, to ensure that the oscillator circuit shows required performance over the recommended operating conditions.

- Without a crystal, the oscillator circuit should not oscillate. To check this, the crystal can be replaced by its equivalent parallel-resonant resistance.
- When the power-supply voltage drops, the closed-loop gain of the oscillator circuit reduces. Ensure that the circuit oscillates at the appropriate frequency at the lowest V_{CC} and highest V_{CC}.
- Ensure that the duty cycle, start-up time, and frequency drift over time is within the system requirements.

Product Folder Links: SN74LVC1404



Typical Application (continued)

10.2.3 Application Curves

10.2.3.1 LVC1404 in 25-MHz Crystal-Oscillator Circuit

 $C_1 \approx C_2 = 30 \text{ pF} \tag{1}$

 X_{C2} = 200 Ω (capacitive reactance at resonance frequency, that is, 25 MHz) (2)

 $V_{CC} = 3.3 \text{ V} \tag{3}$

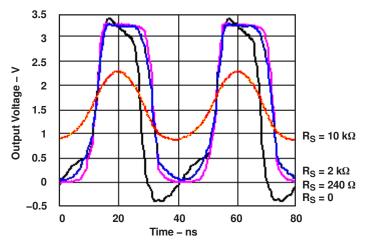


Figure 5. Effect of R_S on Oscillator Waveform (Frequency = 25 MHz)

Table 3. Effect of R_S on Duty Cycle and I_{CC} (Frequency = 25 MHz)

R _S (Ω)	I _{CC} (mA)	Positive Duty Cycle (%)
0	22.2	43
240	11.1	45.9
2 k	7.3	47.3
10 k	8.6	46.7

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10.2.3.2 LVC1404 in 10-MHz Crystal-Oscillator Circuit

$$C_1 \approx C_2 = 30 \text{ pF} \tag{4}$$

 $X_{C2} = 480 \Omega$ (capacitive reactance at resonance frequency, that is, 10 MHz) (5)

 $V_{CC} = 3.3 \text{ V}$ (6)

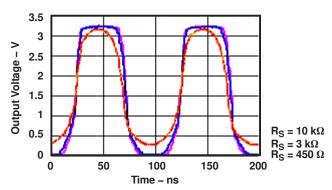


Figure 6. Effect of R_S on Oscillator Waveform (Frequency = 10 MHz)

Table 4. Effect of R_S on Duty Cycle and I_{CC} (Frequency = 10 MHz)

R _S (Ω)	I _{CC} (mA)	Positive Duty Cycle (%)
450	6.9	40
3 k	8.4	47.6
10 k	15.1	43.9

10.2.3.3 LVC1404 in 2-MHz Crystal-Oscillator Circuit

$$C_1 \approx C_2 = 30 \text{ pF} \tag{7}$$

$$X_{C2} = 2.4 \text{ k}\Omega$$
 (capacitive reactance at resonance frequency, that is, 2 MHz) (8)

$$V_{CC} = 3.3 \text{ V} \tag{9}$$

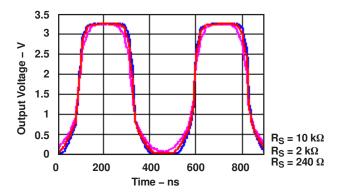


Figure 7. Effect of R_S on Oscillator Waveform (Frequency = 2 MHz)

Table 5. Effect of R_S on Duty Cycle and I_{CC} (Frequency = 2 MHz)

R _S (Ω)	I _{CC} (mA)	Positive Duty Cycle (%)
240	11.1	45.9
2 k	7.3	47.3
10 k	8.6	46.7

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10.2.3.4 LVC1404 in 100-kHz Crystal-Oscillator Circuit

 $C_1 \approx C_2 = 30 \text{ pF} \tag{10}$

 $X_{C2} = 48 \text{ k}\Omega$ (capacitive reactance at resonance frequency, that is, 100 kHz) (11)

 $V_{CC} = 3.3 \text{ V} \tag{12}$

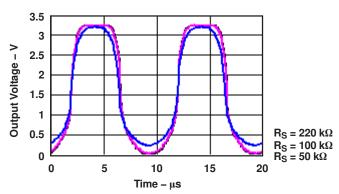


Figure 8. Effect of R_S on Oscillator Waveform (Frequency = 100 kHz)

Table 6. Effect of R_S on Duty Cycle and I_{CC} (Frequency = 100 kHz)

R _S (Ω)	I _{CC} (mA)	Positive Duty Cycle (%)
50 k	9	46.4
100 k	9.5	46.1
220 k	13.7	44.3

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11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ f is recommended; if there are multiple V_{CC} pins, then 0.01 μ f or 0.022 μ f is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ f and a 1 μ f are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 9 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{\rm CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

12.2 Layout Example

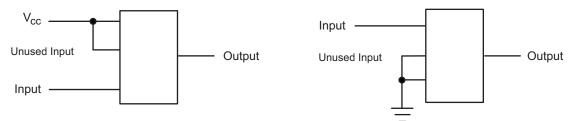


Figure 9. Layout Diagram

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Product Folder Links: SN74LVC1404



13 Device and Documentation Support

13.1 Trademarks

NanoFree is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74LVC1404

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74LVC1404DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(2W85, CA4) (R, Z)
									` '
SN74LVC1404DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2W85, CA4) (R, Z)
SN74LVC1404DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CA4J, CA4R)
SN74LVC1404DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CA4J, CA4R)
SN74LVC1404DCUR1G4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
SN74LVC1404YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	44N
SN74LVC1404YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	44N

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 9-Nov-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	-
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1404DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1404DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1404DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1404YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1404DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC1404DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC1404DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC1404YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





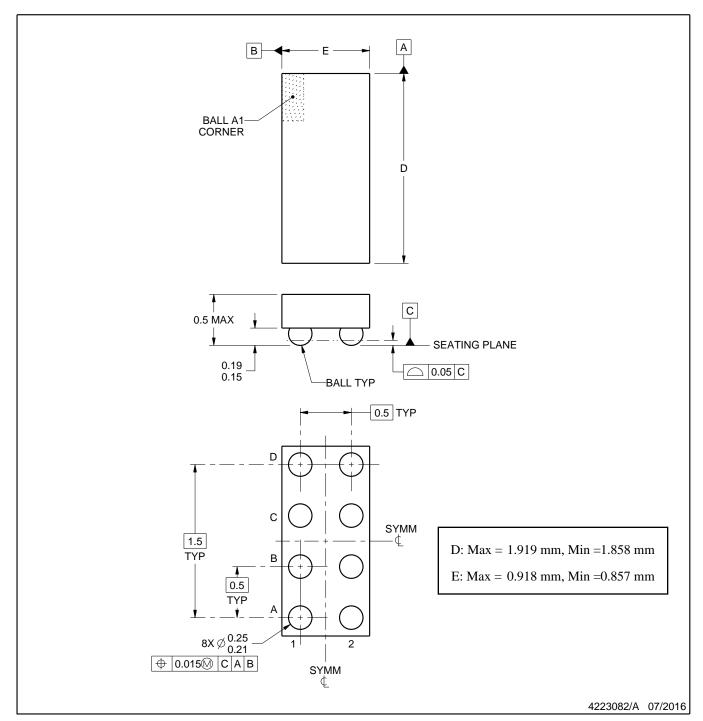
NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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