









SN74LVC126A SCAS339U - MARCH 1994 - REVISED JULY 2024

# SN74LVC126A Quadruple Bus Buffer Gate With 3-State Outputs

#### 1 Features

- Operates from 1.65V to 3.6V
- Specified from -40°C to +125°C
- Inputs accept voltages up to 5.5V
- Maximum t<sub>pd</sub> of 4.7ns at 3.3V
- Typical V<sub>OLP</sub> (output ground bounce), <0.8V at  $V_{CC} = 3.3V$ ,  $T_A = 25^{\circ}C$
- Typical V<sub>OHV</sub> (output V<sub>OH</sub> undershoot), >2V at  $V_{CC}$  = 3.3V,  $T_A$  = 25°C
- Latch-up performance exceeds 250mA per JESD 17

# 2 Applications

- **AV Receivers**
- Audio Docks: Portable
- Blu-ray Players and Home Theaters
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom, Server, and AC-DC Supplies (Single-Controller, Analog, and Digital)
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

#### 3 Description

The SN74LVC126A device is a quadruple bus buffer gate designed for 1.65V to 3.6V V<sub>CC</sub> operation.

The SN74LVC126A device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

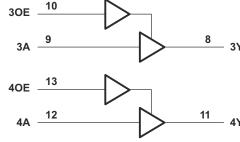
To ensure the high-impedance state during power up or power down, OE must be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V and 5V system environment.

#### **Package Information**

PART NUMBER	PACKAGE (1)	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE(3)
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm x 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.2mm x 7.8mm	6.20mm × 5.30mm
SN74LVC126A	DGV (TVSOP, 14)	3.60mm × 6.4mm	3.60mm × 4.40mm
	NS (SOP, 14)	10.2mm x 7.8mm	10.20mm × 5.30mm
	PW (TSSOP, 14)	5mm x 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm	3.50mm × 3.50mm

- For more information, see Mechanical, Packaging, and Orderable Information.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



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**Simplified Schematic** 



# **Table of Contents**

1 Features2 Applications	1	7.4 Device Functional Modes  8 Application and Implementation	. 11
3 Description		8.1 Application Information	
4 Pin Configuration and Functions	3	8.2 Typical Application	. 11
5 Specifications	4	8.3 Power Supply Recommendations	12
5.1 Absolute Maximum Ratings	4	8.4 Layout	. 12
5.2 ESD Ratings	4	9 Device and Documentation Support	14
5.3 Recommended Operating Conditions	4	9.1 Documentation Support	. 14
5.4 Thermal Information	5	9.2 Receiving Notification of Documentation Updates	14
5.5 Electrical Characteristics	6	9.3 Support Resources	. 14
5.6 Switching Characteristics	7	9.4 Trademarks	14
5.7 Typical Characteristics	8	9.5 Electrostatic Discharge Caution	14
6 Parameter Measurement Information	9	9.6 Glossary	14
7 Detailed Description	10	10 Revision History	. 14
7.1 Overview	10	11 Mechanical, Packaging, and Orderable	
7.2 Functional Block Diagram		Information	. 14
7.3 Feature Description	10		



# **4 Pin Configuration and Functions**

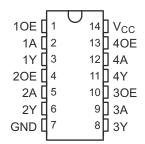


Figure 4-1. SN74LVC126A D, DB, DGV, NS, or PW Package; 14-Pin SOIC, SSOP, TVSOP, SOP or TSSOP (Top View)

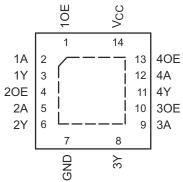


Figure 4-2. SN74LVC126A BQA or RGY Package;14-Pin WQFN or VQFN (Top View)

**Table 4-1. Pin Functions** 

	PIN	I/O <sup>(1)</sup>	DESCRIPTION
NO.	NAME	1/0(1)	DESCRIPTION
1	10E	I	Output enable 1
2	1A	I	Gate 1 input
3	1Y	0	Gate 1 output
4	20E	I	Output enable 2
5	2A	I	Gate 2 input
6	2Y	0	Gate 2 output
7	GND	_	Ground pin
8	3Y	0	Gate 3 output
9	3A	I	Gate 3 input
10	30E	I	Output enable 3
11	4Y	0	Gate 4 output
12	4A	I	Gate 4 input
13	40E	1	Output Enable 4
14	V <sub>CC</sub>		Power pin
Therma	l pad	_	Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable



## **5 Specifications**

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	6.5	V
V <sub>I</sub> <sup>(2)</sup>	Input voltage	nput voltage		6.5	V
V <sub>O</sub> <sup>(2)</sup> <sup>(3)</sup>	Output voltage			V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GNI	D		±100	mA
P <sub>tot</sub>	Power dissipation	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}^{(4)}$ (5)		500	mW
T <sub>J</sub>	Maximum junction temperature	·		150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in *Recommended Operating Conditions*.
- (4) For the D package: above 70°C, the value of Ptot derates linearly with 8 mW/K.
- (5) For the DB, NS, and PW packages: above 60°C, the value of Ptot derates linearly with 5.5 mW/K.

### 5.2 ESD Ratings

			VALUE	UNIT
\/		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	\/
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. This rating was tested on the D (SOIC) package.

### **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
.,	Cumply voltage	Operating	1.65		3.6	V
V <sub>CC</sub>	Supply voltage	Data retention only	1.5			V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>			
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7			V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2			
		V <sub>CC</sub> = 1.65 V to 1.95 V			0.35 × V <sub>CC</sub>	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V			0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V			0.8	
VI	Input voltage		0		5.5	V
Vo	Output voltage		0		V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65 V			-4	
	High lavel autout access	V <sub>CC</sub> = 2.3 V			-8	А
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V			-12	mA
		V <sub>CC</sub> = 3 V			-24	

Product Folder Links: SN74LVC126A

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. This rating was tested on the D (SOIC) package.



# 5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
		V <sub>CC</sub> = 1.65 V			4	
	La. Low-level output current	V <sub>CC</sub> = 2.3 V			8	m A
$I_{OL}$ Low-level output current			12	mA		
		V <sub>CC</sub> = 3 V			4 8	
Δt/Δν	Input transition rise or fall rate				10	ns/V
T <sub>A</sub>	Operating free-air temperature		-40		125	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*.

#### 5.4 Thermal Information

				5	SN74LVC126	Α			
1	THERMAL METRIC(1)		D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	UNIT
		14 PINS	14 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	102.3 <sup>(3)</sup>	127.8 <sup>(2)</sup>	112.2 <sup>(2)</sup>	140.9 <sup>(2)</sup>	123.8 <sup>(2)</sup>	150.8 <sup>(2)</sup>	92.1 <sup>(3)</sup>	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	96.8	81.9	64.2	59.9	51.7	78.3	91.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	70.9	84.4	59.6	70.2	52.7	93.8	66.7	°C/W
ΨЈТ	Junction-to-top characterization parameter	16.6	39.6	28.3	9.1	20.7	38.2	20	°C/W
ΨЈВ	Junction-to-board characterization parameter	70.9	83.9	59.1	69.5	52.3	93.2	66.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	50.1	N/A	N/A	N/A	N/A	N/A	50.1	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

<sup>(2)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>(3)</sup> The package thermal impedance is calculated in accordance with JESD 51-5.



#### 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	DITIONS		MIN	TYP N	IAX	UNIT	
	100 00 10 10 10 10 10 10 10 10 10 10 10		T <sub>A</sub> = 25°C	V <sub>CC</sub> - 0.2				
	$I_{OH} = -100 \mu A$ , $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$		$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	V <sub>CC</sub> - 0.3				
			T <sub>A</sub> = 25°C	1.29				
	$I_{OH} = -4 \text{ mA}, V_{CC} = 1.65 \text{ V}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	1.2				
			$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$	1.05				
			T <sub>A</sub> = 25°C	1.9				
	$I_{OH} = -8 \text{ mA}, V_{CC} = 2.3 \text{ V}$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	1.7				
$V_{OH}$			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	1.55	,		V	
	\ <u>\</u>	- 0.7.7	T <sub>A</sub> = 25°C	2.2				
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	2.05				
	I <sub>OH</sub> = -12 mA		T <sub>A</sub> = 25°C	2.4				
	Vcc	= 3 V	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	2.25				
			T <sub>A</sub> = 25°C	2.3	,			
	$I_{OH}$ = -24 mA, $V_{CC}$ = 3 V		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	2.2				
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	2				
			T <sub>A</sub> = 25°C			0.1		
	$I_{OL}$ = 100 $\mu$ A, $V_{CC}$ = 1.65 V to 3.6 V		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			0.2		
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			0.3		
			T <sub>A</sub> = 25°C		(	).24		
	$I_{OL} = 4 \text{ mA}, V_{CC} = 1.65 \text{ V}$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		(	).45		
						0.6		
$V_{OL}$	I <sub>OL</sub> = 8 mA, V <sub>CC</sub> = 2.3 V		T <sub>A</sub> = 25°C			0.3	V	
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			0.7		
					(	).75		
	1 - 40 - 10 - 10 - 10 - 10 - 10 - 10 - 1		T <sub>A</sub> = 25°C			0.4		
	$I_{OL} = 12 \text{ mA}, V_{CC} = 2.7 \text{ V}$	$I_{OL}$ = 12 mA, $V_{CC}$ = 2.7 V				0.6		
			T <sub>A</sub> = 25°C		(	).55		
	$I_{OL} = 24 \text{ mA}, V_{CC} = 3 \text{ V}$		$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			8.0		
			T <sub>A</sub> = 25°C			±1		
I <sub>I</sub>	$V_I = 5.5 \text{ V or GND}, V_{CC} = 3.6 \text{ V}$		T <sub>A</sub> = -40°C to +85°C			±5	μΑ	
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			±20		
			T <sub>A</sub> = 25°C			±1		
l <sub>oz</sub>	$V_O = V_{CC}$ or GND, $V_{CC} = 3.6 \text{ V}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			±10	μΑ	
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			±20		
			T <sub>A</sub> = 25°C			1		
I <sub>CC</sub>	$V_I = V_{CC}$ or GND, $I_O = 0$ , $V_{CC} = 3.6$ V		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			10	μΑ	
			$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			40		
Al	One input at $V_{CC} = 0.6 \text{ V}$ , other inputs a	at V <sub>CC</sub> or	T <sub>A</sub> = 25°C			500	^	
ΔI <sub>CC</sub>	GND, V <sub>CC</sub> = 2.7 V to 3.6 V		$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$		5	000	μΑ	
Ci	$V_I = V_{CC}$ or GND, $V_{CC} = 3.3 \text{ V}$				4.5		pF	
Co	$V_O = V_{CC}$ or GND, $V_{CC} = 3.3 \text{ V}$				7		pF	



### **5.5 Electrical Characteristics (continued)**

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST (	CONDITIONS		MIN 7	ГҮР МАХ	UNIT
Power			V <sub>CC</sub> = 1.8 V		20		
		Outputs enabled	V <sub>CC</sub> = 2.5 V		21		
	dissination	r gate f = 10 MHz, T <sub>A</sub> = 25°C	011000	V <sub>CC</sub> = 3.3 V		22	pF
C <sub>pd</sub>	capacitance		Outputs disabled	V <sub>CC</sub> = 1.8 V		2	
	per gate			V <sub>CC</sub> = 2.5 V		3	
			dicabled	V <sub>CC</sub> = 3.3 V		4	

# **5.6 Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted; see Parameter Measurement Information)

PARAMETER	TES	TEST CONDITIONS			TYP	MAX	UNIT
			T <sub>A</sub> = 25°C	1	4.2	9.3	
		V <sub>CC</sub> = 1.8 V ± 0.15 V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			9.8	
			T <sub>A</sub> = -40°C to +125°C		-	11.3	
			T <sub>A</sub> = 25°C	1	2.7	6.7	
t <sub>pd</sub>		V <sub>CC</sub> = 2.5 V ± 0.2 V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			7.2	
	From A (input) to Y (output)	100 =10 1 = 11= 1	T <sub>A</sub> = -40°C to +125°C			9.3	ne
	From A (input) to 1 (output)		T <sub>A</sub> = 25°C	1	2.9	5	ns
		V <sub>CC</sub> = 2.7 V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	-		5.2	
		VCC - 2.1 V	T <sub>A</sub> = -40°C to +125°C			6.5	
			T <sub>A</sub> = 25°C	1	2.5	4.5	
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			4.7	
			T <sub>A</sub> = -40°C to +125°C			6	
		V <sub>CC</sub> = 1.8 V ± 0.15 V	T <sub>A</sub> = 25°C	1	4.8	9.5	1
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			10	
			T <sub>A</sub> = -40°C to +125°C			11.5	
			T <sub>A</sub> = 25°C	1	2.8	7.8	
		V <sub>CC</sub> = 2.5 V ± 0.2 V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			8.3	
	From OE (input) to Y (output)	100 =10 1 = 11= 1	T <sub>A</sub> = -40°C to +125°C			10.4	ns
en	rioni OE (input) to 1 (output)		T <sub>A</sub> = 25°C	1	3.1	6.1	115
		V <sub>CC</sub> = 2.7 V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			6.3	
			T <sub>A</sub> = -40°C to +125°C			8	l
			T <sub>A</sub> = 25°C	1	2.5	5.5	
		V <sub>CC</sub> = 3.3 V ± 0.3 V	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			5.7	
		- 5.5 V 1 5.5 V	T <sub>A</sub> = -40°C to +125°C			7.5	



### **5.6 Switching Characteristics (continued)**

over recommended operating free-air temperature range (unless otherwise noted; see *Parameter Measurement Information*)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
			T <sub>A</sub> = 25°C	1	4.4	12.1	
		V <sub>CC</sub> = 1.8 V ± 0.15 V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			12.6	
			T <sub>A</sub> = -40°C to +125°C			14.1	
			T <sub>A</sub> = 25°C	1	2.7	8.2	
t <sub>dis</sub>		V <sub>CC</sub> = 2.5 V ± 0.2 V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			8.7	
	From OE (input) to Y (output)		T <sub>A</sub> = -40°C to +125°C			10.8	ns
		V <sub>CC</sub> = 2.7 V	T <sub>A</sub> = 25°C	1	2.7	6.5	
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			6.7	
			T <sub>A</sub> = -40°C to +125°C			8.5	
			T <sub>A</sub> = 25°C	1.3	2.3	5.8	
		V <sub>CC</sub> = 3.3 V ± 0.3 V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			6	
		0.0 1 2 0.0 1	T <sub>A</sub> = -40°C to +125°C			7.5	
			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			1	
t <sub>sk(o)</sub>	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		T <sub>A</sub> = -40°C to +125°C			1.5	ns

# **5.7 Typical Characteristics**

T<sub>A</sub> = 25°C

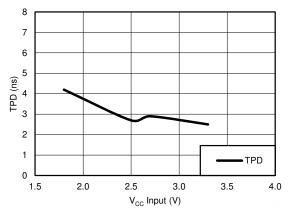


Figure 5-1. TPD vs  $V_{\text{CC}}$ 

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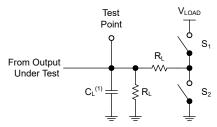
#### **6 Parameter Measurement Information**

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1MHz,  $Z_O = 50\Omega$ ,  $t_t \leq$  2.5ns.

The outputs are measured individually with one input transition per measurement.

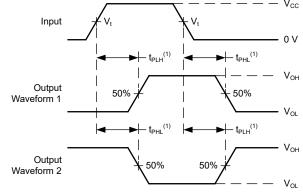
TEST	S1	S2	$R_L$	CL	ΔV	V <sub>LOAD</sub>
t <sub>PLH</sub> , t <sub>PHL</sub>	OPEN	OPEN	500Ω	50pF	_	_
t <sub>PLZ</sub> , t <sub>PZL</sub>	CLOSED	OPEN	500Ω	50pF	0.3V	2×V <sub>CC</sub>
t <sub>PHZ</sub> , t <sub>PZH</sub>	OPEN	CLOSED	500Ω	50pF	0.3V	_

V <sub>CC</sub>	V <sub>t</sub>	R <sub>L</sub>	CL	ΔV	V <sub>LOAD</sub>
1.8V ± 0.15V	V <sub>CC</sub> /2	1kΩ	30pF	0.15V	2×V <sub>CC</sub>
2.5V ± 0.2V	V <sub>CC</sub> /2	500Ω	30pF	0.15V	2×V <sub>CC</sub>
2.7V	1.5V	500Ω	50pF	0.3V	6V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V	6V



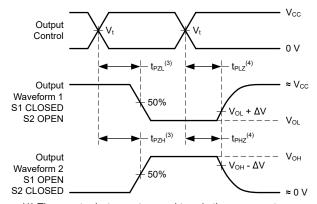
(1) C<sub>L</sub> includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



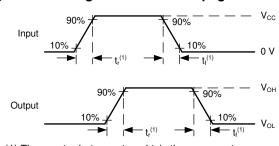
(1) The greater between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  is the same as  $t_{\text{pd}}$ .

Figure 6-2. Voltage Waveforms Propagation Delays



- (1) The greater between  $t_{\text{PZL}}$  and  $t_{\text{PZH}}$  is the same as  $t_{\text{en}}$ .
- (2) The greater between  $t_{\text{PLZ}}$  and  $t_{\text{PHZ}}$  is the same as  $t_{\text{dis}}$ .

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

## 7 Detailed Description

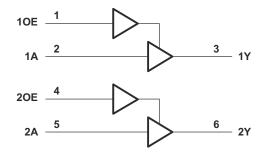
### 7.1 Overview

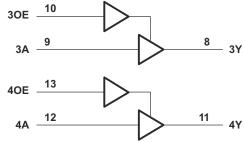
The SN74LVC126A quadruple buffer is designed for 1.65-V to 3.6-V V<sub>CC</sub> operation and features tri-state outputs.

The SN74LVC126A devices perform the Boolean function Y = A in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as down-translators in a mixed 3.3-V or 5-V system environment.

### 7.2 Functional Block Diagram





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#### 7.3 Feature Description

The SN74LVC126A device features four independent buffers with 3-state outputs, and is designed to operate from a  $V_{CC}$  of 1.65 V to 3.6 V. When the output enable (OE) input is low, the corresponding output is disabled and enters a high-impedance state. This device also features high-tolerance inputs, allowing for voltage translation in mixed voltage systems. Wide operating temperature range enables this device to be used in any application, including rugged or extreme environments.

#### 7.4 Device Functional Modes

The SN74LVC126A's 3-state outputs allow the outputs to be disabled using the output enable (OE) pin. To ensure the high-impedance state during power up and power down, OE must be tied to GND through a pulldown resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

Table 7-1. Function Table (Each Buffer)

INP	OUTPUT				
OE	Α	Υ			
Н	Н	Н			
Н	L	L			
L	Х	Hi-Z			

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## 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The SN74LVC126A device is a high-drive, CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to translate up to 5.5 V or down to  $V_{\rm CC}$ .

#### 8.2 Typical Application

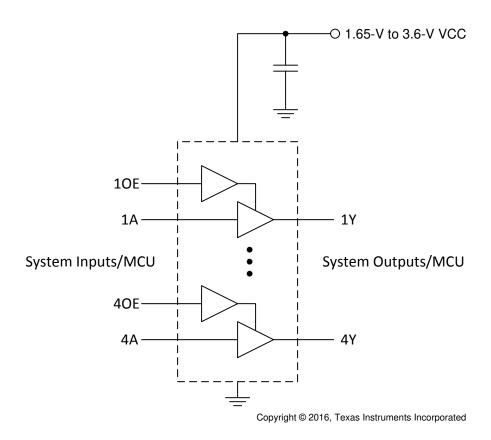


Figure 8-1. Typical Buffer Application and Supply Voltage

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads; therefore, routing and load conditions must be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
  - Rise time and fall time specifications: See (Δt/ΔV) in Recommended Operating Conditions.
  - Specified high and low levels: See (V<sub>IH</sub> and V<sub>IL</sub>) in Recommended Operating Conditions.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V<sub>CC</sub>.
- 2. Recommended Output Conditions
  - Load currents must not exceed 25 mA per output and 50 mA total for the part.
  - Outputs must not be pulled above 5.5 V.

#### 8.2.3 Application Curve

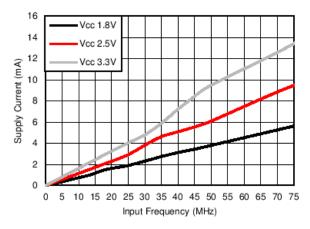


Figure 8-2. Supply Current vs Input Frequency

#### 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating in the *Recommended Operating Conditions*.

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and a 1  $\mu$ F are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

#### 8.4 Layout

#### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 8-3 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

Product Folder Links: SN74LVC126A



### 8.4.2 Layout Example

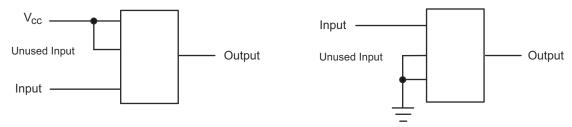


Figure 8-3. Layout Diagram



### 9 Device and Documentation Support

#### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004)

#### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 9.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### Changes from Revision T (May 2024) to Revision U (July 2024)

Page

Updated RθJA values: D = 98.4 to 127.8, NS = 93.9 to 123.8, PW = 127.7 to 150.8, RGY = 35 to 92.1;
 Updated D, NS, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W 5

#### Changes from Revision S (February 2017) to Revision T (May 2024)

Page

- Added BQA package to Package Information table, Pin Configuration and Functions section, and Thermal
   Information table

#### 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74LVC126A

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7-Oct-2025

### **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC126ABQAR	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LVC126ABQAR.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LVC126AD	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126AD.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADBR	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADBR.B	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADGVR	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADGVR.B	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADRE4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADT	Active	Production	SOIC (D)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADT.B	Active	Production	SOIC (D)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ANSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ANSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ANSR.B	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126APW	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APW.B	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWG4	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWRE4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWT	Active	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWT.B	Active	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A

7-Oct-2025



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Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74LVC126ARGYR	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A
SN74LVC126ARGYR.A	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A
SN74LVC126ARGYR.B	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A
SN74LVC126ARGYRG4	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74LVC126A:

Automotive: SN74LVC126A-Q1

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



# **PACKAGE OPTION ADDENDUM**

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NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC126ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC126ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC126ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC126ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC126ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC126APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC126APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC126ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74LVC126ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



www.ti.com 11-Nov-2025



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC126ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC126ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVC126ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LVC126ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC126ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVC126ADT	SOIC	D	14	250	213.0	191.0	35.0
SN74LVC126ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC126APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC126APWT	TSSOP	PW	14	250	353.0	353.0	32.0
SN74LVC126ARGYR	VQFN	RGY	14	3000	360.0	360.0	36.0
SN74LVC126ARGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 11-Nov-2025

### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC126AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC126AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC126APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC126APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC126APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
   The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



### **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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