

SN74LVC125A-Q1 Automotive Quadruple Bus Buffer Gate With 3-State Outputs

1 Features

- Qualified for automotive applications
- Operates from 1.65V to 3.6V
- Specified from -40°C to 125°C
- Inputs accept voltages to 5.5V
- Max t_{pd} of 4.8ns at 3.3V
- Typical V_{OLP} (output ground bounce) <0.8V at V_{CC} $= 3.3V, T_A = 25$ °C
- Typical V_{OHV} (output V_{OH} undershoot) >2V at V_{CC} $= 3.3V, T_A = 25^{\circ}C$
- Latch-up performance exceeds 250mA per JESD

2 Description

This quadruple bus buffer gate is designed for 1.65V to 3.6V V_{CC} operation.

PART NUMBER PACKAGE ⁽¹⁾		PACKAGE SIZE(2)	BODY SIZE(3)		
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm		
SN74LVC125A-Q1	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.91mm		
	PW (TSSOP, 14)	5.00mm × 6.4mm	5.00mm × 4.40mm		

- For more information, see Section 10. (1)
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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3 Pin Configuration and Functions

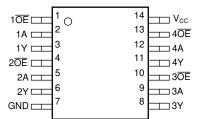


Figure 3-1. D Package, 14-Pin SOIC; PW Package, TSSOP-14 PIN (Top View)

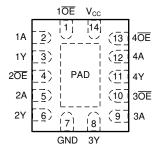


Figure 3-2. BQA Package, 14-Pin WQFN (Top View)

Table 3-1. Pin Functions

P	PIN	I/O	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
1 OE	1	Input	Output Enable
1A	2	Input	Input A
1Y	3	Output	Output Y
2 OE	4	Input	Output Enable
2A	5	Input	Input A
2Y	6	Output	Output Y
GND	7	_	Ground
3Y	8	Output	Output Y
3A	9	Input	Input A
3 OE	10	Input	Output Enable
4Y	11	Output	Output Y
4A	12	Input	Input A
4 OE	13	Input	Output Enable
V _{CC}	14	_	Positive Supply



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range		-0.5	6.5	V
Vo	Output voltage range ⁽¹⁾ (2)		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _{stg}	Storage temperature range		-65	150	°C
P _{tot}	Power dissipation ⁽³⁾ (4)	T _A = -40°C to 125°C		500	mW

- (1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (2) The value of V_{CC} is provided in the recommended operating conditions table.
- (3) For the D package: above 70°C, the value of Ptot derates linearly with 8 mW/K.
- (4) For the PW package: above 60°C, the value of Ptot derates linearly with 5.5 mW/K.

4.2 ESD Ratings

	PARAMETER DEFINITION		VALUE	UNIT
\/·	Electrostatic	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
V _(ESD)	discharge	Charged device model (CDM), per AEC Q100-011	±1000	\ \ \

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			T _A = 2	T _A = 25°C		-40°C to 125°C	
			MIN	MAX	MIN	MAX	UNIT
.,	Cumply valtage	Operating	1.65	3.6	1.65	3.6	V
V_{CC}	Supply voltage	Data retention only	1.5		1.5		V
		V _{CC} = 1.65V to 1.95V	0.65 × V _{CC}		0.65 × V _{CC}		
V_{IH}	High-level input voltage	V _{CC} = 2.3V to 2.7V	1.7		1.7		V
		V _{CC} = 2.7V to 3.6V	2		2		
		V _{CC} = 1.65V to 1.95V		0.35 × V _{CC}	(0.35 × V _{CC}	
V_{IL}	Low-level input voltage	V _{CC} = 2.3V to 2.7V		0.7		0.7	V
		V _{CC} = 2.7V to 3.6V		0.8		0.8	
VI	Input voltage	<u>'</u>	0	5.5	0	5.5	V
Vo	Output voltage		0	V _{CC}	0	V _{CC}	V
		V _{CC} = 1.65V		-4		-4	
	Lligh lovel output ourrent	V _{CC} = 2.3V		-8		-8	mA
I _{OH}	High-level output current	V _{CC} = 2.7V		-12		-12	mA
		V _{CC} = 3V		-24		-24	
		V _{CC} = 1.65V		4		4	
	Low level output ourrent	V _{CC} = 2.3V		8		8	mA
I _{OL}	Low-level output current	V _{CC} = 2.7V		12		12	
		V _{CC} = 3V		24		24	mA

Product Folder Links: SN74LVC125A-Q1

over operating free-air temperature range (unless otherwise noted)(1)

	T _A = 25°C	-40°C to 125°C	UNIT
	MIN MA	X MIN MAX	ONII
Δt/Δv Input transition rise or fall rate		8 8	ns/V

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC(1)		BQA (WQFN)	D (SOIC)	PW (TSSOP)	UNIT
			14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.3	127.8	150.8	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	R TEST CONDITIONS	V	T _A =	25°C	-40°C to 125°C		UNIT
PARAIVIETER		V _{cc}	MIN	TYP MAX	MIN	MAX	UNII
	I _{OH} = -100μA	1.65V to 3.6 V	V _{CC} - 0.2		V _{CC} - 0.2		
	I _{OH} = -4mA	1.65V	1.29		1.1		
\\	I _{OH} = -8mA	2.3V	1.9		1.75		V
V _{OH}	I - 12mA	2.7V	2.2		2.1		V
	I _{OH} = -12mA	3V	2.4		2.35		
	I _{OH} = -24mA	3V	2.3		2.1		
	I _{OL} = 100μA	1.65V to 3.6 V		0.1		0.2	
	I _{OL} = 4mA	1.65V		0.24		0.45	
V _{OL}	I _{OL} = 8mA	2.3V		0.3		0.7	V
	I _{OL} = 12mA	2.7V		0.4		0.5	
	I _{OL} = 24mA	3V		0.55		0.7	
I	V _I = 5.5 V or GND	3.6V		±1		±10	μΑ
I _{OZ}	V _O = V _{CC} or GND	3.6V		±1		±10	μΑ
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6V		1		20	μΑ
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7V to 3.6 V		500		500	μΑ
C _i	V _I = V _{CC} or GND	3.3V		5			pF

4.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	V _{CC}	T _A = 25°C			T _A = 25°C -40°C to 125°C	UNIT	
PARAMETER	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	UNII
	Δ.	V	2.7V	1	3	5.3	1	7	
t _{pd}	A	Ť	3.3V ± 0.3V	1	2.5	4.6	1	6	ns
	ŌĒ	V	2.7V	1	3.3	6.4	1	8.5	no
t _{en}	OE .	Ť	3.3V ± 0.3V	1	2.4	5.2	1	7	ns
	ŌĒ	V	2.7V	1	2.5	4.8	1	6.5	no
t _{dis}	OE	Y	3.3V ± 0.3V	1	2.4	4.4	1	6	ns
t _{sk(o)}			3.3V ± 0.3V					1.5	ns



4.7 Operating Characteristics

T_A = 25°C

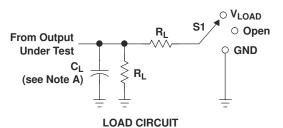
	PARAMETER	TEST CONDITIONS	V _{cc}	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	f = 10MHz	3.3V	15	pF

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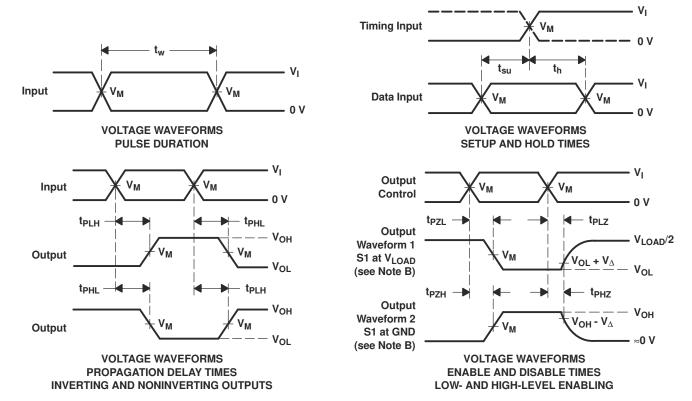


5 Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	V _{LOAD} GND

	INPUT						
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R_L	V_{Δ}
2.7 V 3.3 V ± 0.3 V	2.7 V 2.7 V	≤ 2.5 ns ≤ 2.5 ns	1.5 V 1.5 V	6 V 6 V	50 pF 50 pF	500 Ω 500 Ω	0.3 V 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

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6 Detailed Description

6.1 Overview

The SN74LVC125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

6.2 Functional Block Diagram

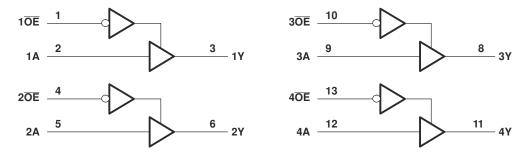


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Function Table (Each Buffer)

INP	UTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	X	z

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 4.3 table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ f is recommended; if there are multiple VCC pins, then 0.01 μ f or 0.022 μ f is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ f and a 1 μ f are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Section 7.2.2 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

7.2.2 Layout Example

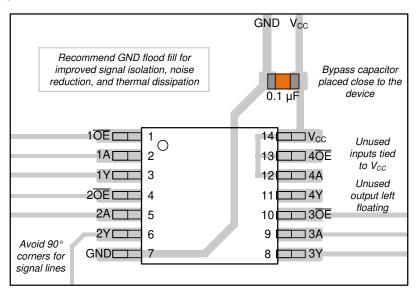


Figure 7-1. Example layout for the SN74LVC125A-Q1

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

	PARTS	PARTS PRODUCT FOLDER SAME		TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SI	N74LVC125A-Q1	Click here	Click here	Click here	Click here	Click here	

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Notifications to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision D (May 2024) to Revision E (December 2024) **Page** Updated RθJA values: D = 86 to 127.8, all values in °C/W5 Changes from Revision C (February 2024) to Revision D (May 2024) **Page** Updated RθJA values: PW = 113 to 150.8, all values in °C/W5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74LVC125A-Q1

www.ti.com 23-May-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
CLVC125AQPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ
CLVC125AQPWRG4Q1.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ
SN74LVC125AQDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ
SN74LVC125AQDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ
SN74LVC125AQDRQ1.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ
SN74LVC125AQPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ
SN74LVC125AQPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ
SN74LVC125AQPWRQ1.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ
SN74LVC125AWBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125Q
SN74LVC125AWBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC125A-Q1:

Catalog: SN74LVC125A

● Enhanced Product: SN74LVC125A-EP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC125AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125AWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1



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*All dimensions are nominal

7 til dillionolono di o mominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC125AQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC125AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC125AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC125AWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

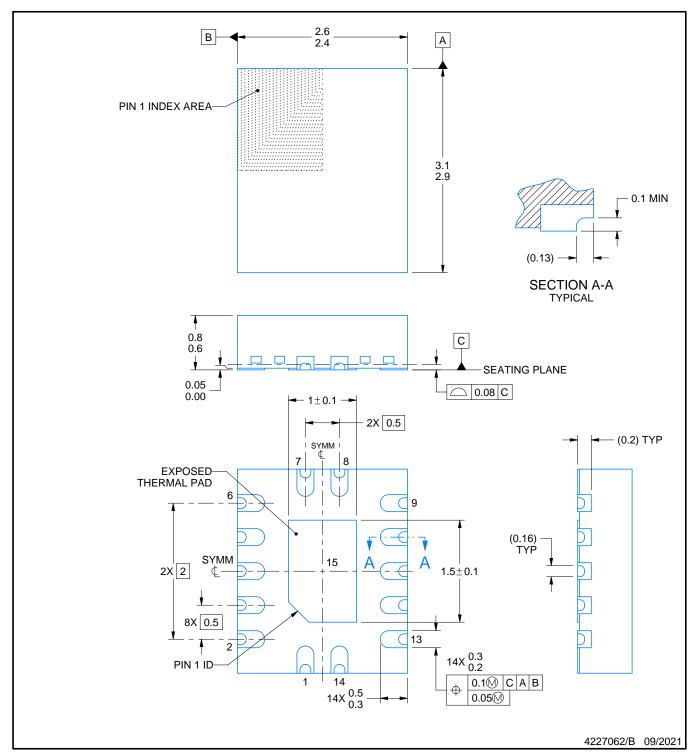
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD

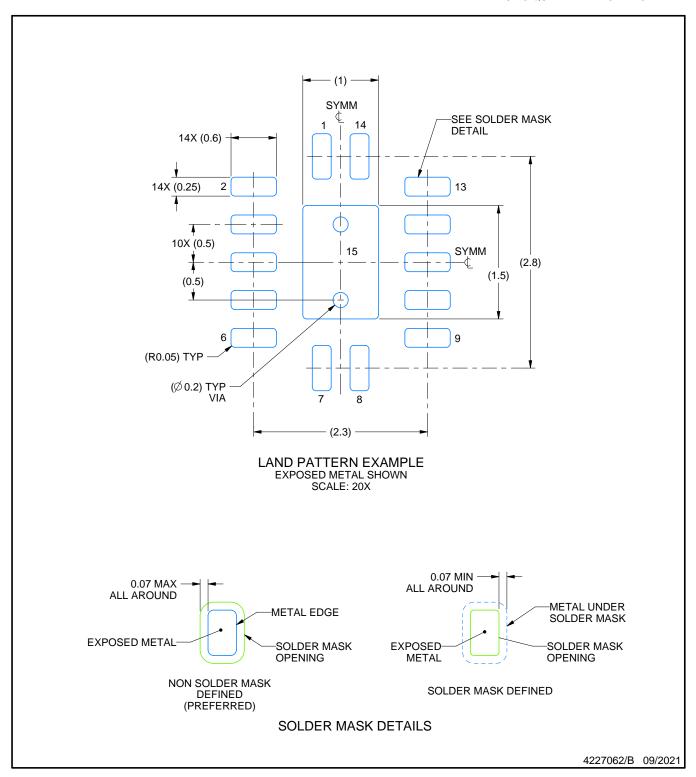


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

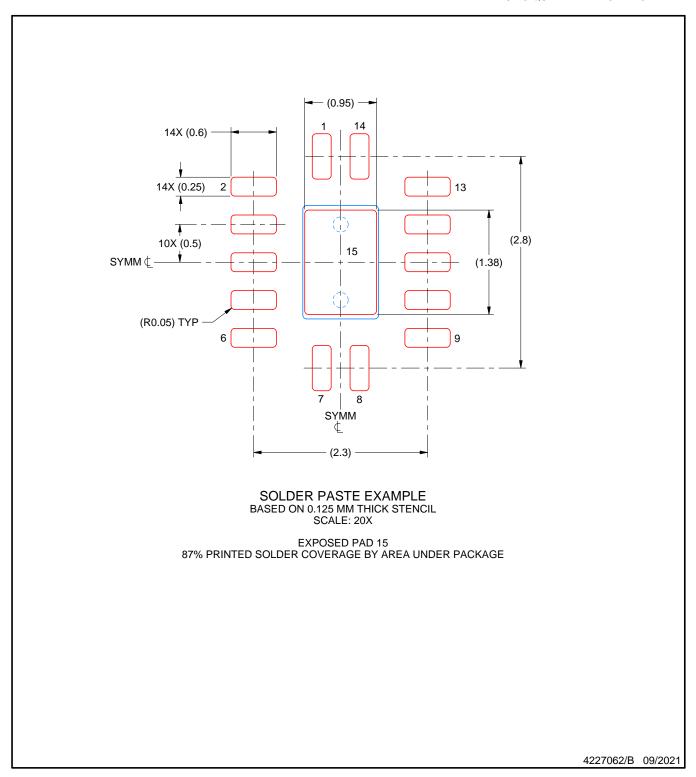


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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