SN74LV8T596 8-bit Serial-Load Shift Register with Open-Drain Output and Logic-Level Shifter

1 Features

- *Latching logic with known power-up state* provides consistent start-up behavior
- Wide operating range of 1.65V to 5.5V
- 5.5V tolerant input pins
- *LVxT enhanced inputs* combined with *open-drain outputs* provide maximum voltage translation flexibility:
  - Over 6.67Mbps operation, (R_{PU} = 1kΩ, C_L = 30pF)
  - Up translation from 1.2V to 5V with 1.8V supply
  - Down translation from 5V to 0.8V or even less with any valid supply
- Supports standard function pinout
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Digital signage
- Controlling an indicator LED
- Increase the number of outputs on a microcontroller

3 Description

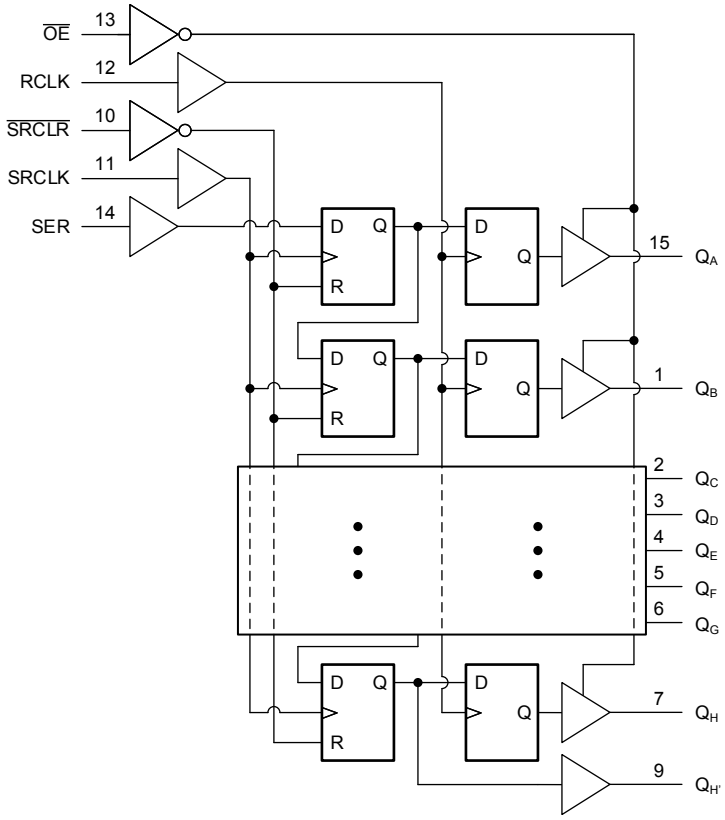
The SN74LV8T596 device contains an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. All inputs include Schmitt-triggers, eliminating any erroneous data outputs due to slow-edged or noisy input signals. The storage register has parallel open-drain outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and a serial output ($Q_{H'}$) for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in a high impedance state. The operation of the $\overline{OE}$ input does not impact the internal register data

The input is designed with a reduced threshold circuit to support up translation when the supply voltage is larger than the input voltage. Additionally, the 5V tolerant input pins enable down translation when the input voltage is larger than the supply voltage. The output level is always referenced to the supply voltage (V_{CC}) and supports 1.8V, 2.5V, 3.3V, and 5V CMOS levels.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM) (3)
SN74LV8T596	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Simplified Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

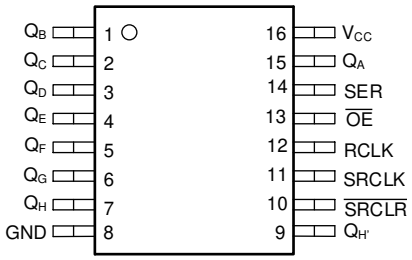


Figure 4-1. PW Package, 16-Pin TSSOP (Top View)

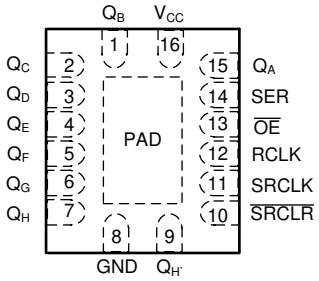


Figure 4-2. BQB Package, 16-Pin WQFN (Transparent Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Q_B	1	O	Q_B output (open-drain)
Q_C	2	O	Q_C output (open-drain)
Q_D	3	O	Q_D output (open-drain)
Q_E	4	O	Q_E output (open-drain)
Q_F	5	O	Q_F output (open-drain)
Q_G	6	O	Q_G output (open-drain)
Q_H	7	O	Q_H output (open-drain)
GND	8	G	Ground
$Q_{H'}$	9	O	Serial output, can be used for cascading (push-pull)
$\overline{SRCLR}$	10	I	Shift register clear, active low
SRCLK	11	I	Shift register clock, rising edge triggered
RCLK	12	I	Output register clock, rising edge triggered
$\overline{OE}$	13	I	Output enable, active low
SER	14	I	Serial input
Q_A	15	O	Q_A output (open-drain)
V_{CC}	16	P	Positive supply
Thermal Pad[2]		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power
(2) BQB package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±75	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 2V	1.1		V
		V_{CC} = 2.25V to 2.75V	1.28		
		V_{CC} = 3V to 3.6V	1.45		
		V_{CC} = 4.5V to 5.5V	2		
V_{IL}	Low-Level input voltage	V_{CC} = 1.65V to 2V		0.51	V
		V_{CC} = 2.25V to 2.75V		0.65	
		V_{CC} = 3V to 3.6V		0.75	
		V_{CC} = 4.5V to 5.5V		0.8	
I_O	Output current	V_{CC} = 1.65V to 2V		±8	mA
		V_{CC} = 2.25V to 2.75V		±15	
		V_{CC} = 3.3V to 5.0V		±25	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.65V to 5.0V		20	ns/V
$Δt/ΔV_{CC}$	Safe supply ramp rate for POR	V_{CC} = 1.65V to 5.5V	6		µs/V

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		BQB (WQFN)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.6	135.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.6	70.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.4	81.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.1	22.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.4	80.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	56.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	I_{OL} = 50µA	1.65V to 5.5V			0.1			0.1	V
	I_{OL} = 2mA	1.65V to 2V		0.1[1]	0.2			0.25	
	I_{OL} = 3mA	2.25V to 2.75V		0.1[1]	0.15			0.2	
	I_{OL} = 5.5mA	3V to 3.6V		0.2[1]	0.2			0.25	
	I_{OL} = 8mA	4.5V to 5.5V		0.3[1]	0.3			0.35	
I_I	V_I = 0V or V_{CC}	0V to 5.5V			±0.1			±1	µA
I_{CC}	V_I = 0V or V_{CC}, I_O = 0; open on loading	1.65V to 5.5V			2			20	µA
ΔI_{CC}	One input at 0.3V or 3.4V, other inputs at 0 or V_{CC}, I_O = 0	5.5V			1.35			1.5	mA
	One input at 0.3V or 1.1V, other inputs at 0 or V_{CC}, I_O = 0	1.8V			10			20	µA
C_I	V_I = V_{CC} or GND	5V		4	10			10	pF
C_O	V_O = V_{CC} or GND	5V		3					pF
C_{PD}	No load, F = 1MHz	5V		129					pF
V_{POR}	V_{CC} ramp rate of 6µs/V to 100ms/V	1.65V to 5.5V			1.5			1.5	V

(1) Typical value at nearest nominal voltage (1.8V, 2.5V, 3.3V, and 5V)

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	T_A = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_H	Hold time	SER after SRCLK↑	1.8V	0		0		0		ns
t_{SU}	Setup time	SER before SRCLK↑	1.8V	7.9		9.8		9.8		ns
t_{SU}	Setup time	SRCLK↑ before RCLK↑	1.8V	8.1		10.1		10.1		ns

5.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	T_A = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{SU}	Setup time	SRCLR high (inactive) before SRCLK↑	1.8V	2.2		3		3		ns
t_{SU}	Setup time	SRCLR low before RCLK↑	1.8V	8.9		11.2		11.2		ns
t_W	Pulse duration	RCLK or SRCLK high or low	1.8V	5.9		7		7		ns
t_W	Pulse duration	RCLR or SCRCLR low	1.8V	6.5		8.3		8.3		ns
t_H	Hold time	SER after SRCLK↑	2.5V	0		0		0		ns
t_{SU}	Setup time	SER before SRCLK↑	2.5V	4.6		5.9		5.9		ns
t_{SU}	Setup time	SRCLK↑ before RCLK↑	2.5V	3.9		5.3		5.3		ns
t_{SU}	Setup time	SRCLR high (inactive) before SRCLK↑	2.5V	1.1		1.7		1.7		ns
t_{SU}	Setup time	SRCLR low before RCLK↑	2.5V	5.1		6.6		6.6		ns
t_W	Pulse duration	RCLK or SRCLK high or low	2.5V	4.3		4.3		4.3		ns
t_W	Pulse duration	RCLR or SCRCLR low	2.5V	4.3		5.2		5.2		ns
t_H	Hold time	SER after SRCLK↑	3.3V	0		0		0		ns
t_{SU}	Setup time	SER before SRCLK↑	3.3V	3.2		4		4		ns
t_{SU}	Setup time	SRCLK↑ before RCLK↑	3.3V	2.5		3.2		3.2		ns
t_{SU}	Setup time	SRCLR high (inactive) before SRCLK↑	3.3V	0.7		1		1		ns
t_{SU}	Setup time	SRCLR low before RCLK↑	3.3V	3.6		4.5		4.5		ns
t_W	Pulse duration	RCLK or SRCLK high or low	3.3V	4.3		4.3		4.3		ns
t_W	Pulse duration	RCLR or SCRCLR low	3.3V	4.3		4.3		4.3		ns
t_H	Hold time	SER after SRCLK↑	5V	0		0		0		ns
t_{SU}	Setup time	SER before SRCLK↑	5V	1.3		1.8		1.8		ns
t_{SU}	Setup time	SRCLK↑ before RCLK↑	5V	1.6		2.1		2.1		ns
t_{SU}	Setup time	SRCLR high (inactive) before SRCLK↑	5V	0.5		0.7		0.7		ns
t_{SU}	Setup time	SRCLR low before RCLK↑	5V	1.6		2.1		2.1		ns
t_W	Pulse duration	RCLK or SRCLK high or low	5V	4.3		4.3		4.3		ns
t_W	Pulse duration	RCLR or SCRCLR low	5V	4.3		4.3		4.3		ns

5.7 Switching Characteristics

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
F_{MAX}	-	-	C_L = 15pF	1.8V	46.3	60		39.4			39.4			MHz
t_{PZL}	OE	Q	C_L = 15pF	1.8V		11.9	27.9	1		31.5	1		31.5	ns
t_{PZH}	OE	Q	C_L = 15pF	1.8V		9.4	21	1		24.4	1		24.4	ns
t_{PLZ}	OE	Q	C_L = 15pF	1.8V		8.3	20.2	1		21.9	1		21.9	ns
t_{PHZ}	OE	Q	C_L = 15pF	1.8V		8.3	22.1	1		24.7	1		24.7	ns
t_{PLH}	RCLK	Q_A-Q_H	C_L = 15pF	1.8V		9.4	27	1		28.5	1		29.4	ns
t_{PHL}	RCLK	Q_A-Q_H	C_L = 15pF	1.8V		9.4	23.9	1		26.8	1		26.8	ns
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15pF	1.8V		9.9	20.4	1		23.5	1		23.5	ns
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 15pF	1.8V		9.9	23.9	1		26.9	1		26.9	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15pF	1.8V		9.9	24.5	1		27.8	1		27.8	ns
F_{MAX}	-	-	C_L = 50pF	1.8V	38.11	48		32.6			32.6			MHz

5.7 Switching Characteristics (continued)

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PZL}	OE	Q	C_L = 50pF	1.8V		14.9	51.3	1		56.6	1		56.6	ns
t_{PZH}	OE	Q	C_L = 50pF	1.8V		12.5	25.8	1		29.8	1		29.8	ns
t_{PLZ}	OE	Q	C_L = 50pF	1.8V		7.5	28.5	1		29.3	1		29.3	ns
t_{PHZ}	OE	Q	C_L = 50pF	1.8V		7.7	31	1		33.1	1		33.1	ns
t_{PLH}	RCLK	Q_A-Q_H	C_L = 50pF	1.8V		12.3	52.3	1		53.6	1		54.2	ns
t_{PHL}	RCLK	Q_A-Q_H	C_L = 50pF	1.8V		12.3	28.9	1		32.1	1		32.1	ns
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50pF	1.8V		14.1	25.2	1		28.7	1		28.7	ns
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 50pF	1.8V		14.1	28.8	1		32.1	1		32.1	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50pF	1.8V		14.1	29.5	1		33	1		33	ns
F_{MAX}	-	-	C_L = 15pF	2.5V	66.2	85.8		56.4			56.4			MHz
t_{PZL}	OE	Q	C_L = 15pF	2.5V		9.1	15.7	1		18.8	1		18.8	ns
t_{PZH}	OE	Q	C_L = 15pF	2.5V		7.3	12.4	1		15.2	1		15.2	ns
t_{PLZ}	OE	Q	C_L = 15pF	2.5V		6.4	22.7	1		24.2	1		24.2	ns
t_{PHZ}	OE	Q	C_L = 15pF	2.5V		6.4	13	1		15.1	1		15.1	ns
t_{PLH}	RCLK	Q_A-Q_H	C_L = 15pF	2.5V		7.3	22.2	1		23.2	1		23.9	ns
t_{PHL}	RCLK	Q_A-Q_H	C_L = 15pF	2.5V		7.3	12.9	1		15.7	1		15.7	ns
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15pF	2.5V		7.6	12.1	1		14.6	1		14.6	ns
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 15pF	2.5V		7.6	13.1	1		15.8	1		15.8	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15pF	2.5V		7.6	14.3	1		17.2	1		17.2	ns
F_{MAX}	-	-	C_L = 50pF	2.5V	58.8	68.6		46.6			46.6			MHz
t_{PZL}	OE	Q	C_L = 50pF	2.5V		11.5	28.6	1		34	1		34	ns
t_{PZH}	OE	Q	C_L = 50pF	2.5V		9.6	15.7	1		18.9	1		18.9	ns
t_{PLZ}	OE	Q	C_L = 50pF	2.5V		5.7	49.9	1		50.7	1		50.7	ns
t_{PHZ}	OE	Q	C_L = 50pF	2.5V		5.9	19.3	1		21	1		21	ns
t_{PLH}	RCLK	Q_A-Q_H	C_L = 50pF	2.5V		9.5	47.6	1		48.5	1		49.1	ns
t_{PHL}	RCLK	Q_A-Q_H	C_L = 50pF	2.5V		9.5	16.8	1		19.7	1		19.7	ns
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50pF	2.5V		10.8	15.1	1		17.9	1		17.9	ns
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 50pF	2.5V		10.8	16.8	1		19.7	1		19.7	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50pF	2.5V		10.8	18	1		21.1	1		21.1	ns
F_{MAX}	-	-	C_L = 15pF	3.3V	94.5	122.5		80.5			80.5			MHz
t_{PZL}	OE	Q	C_L = 15pF	3.3V		7	11.5	1		13.9	1		13.9	ns
t_{PZH}	OE	Q	C_L = 15pF	3.3V		5.6	9.2	1		11.1	1		11.1	ns
t_{PLZ}	OE	Q	C_L = 15pF	3.3V		4.9	8.2	1		9.2	1		9.2	ns
t_{PHZ}	OE	Q	C_L = 15pF	3.3V		4.9	9.8	1		11.2	1		11.2	ns
t_{PLH}	RCLK	Q_A-Q_H	C_L = 15pF	3.3V		5.6	20.9	1		21.7	1		22.2	ns
t_{PHL}	RCLK	Q_A-Q_H	C_L = 15pF	3.3V		5.6	9	1		11	1		11	ns
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15pF	3.3V		5.9	9.3	1		11	1		11	ns
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 15pF	3.3V		5.9	9.1	1		11.1	1		11.1	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15pF	3.3V		5.9	10.3	1		12.4	1		12.4	ns
F_{MAX}	-	-	C_L = 50pF	3.3V	84	98		66.5			66.5			MHz
t_{PZL}	OE	Q	C_L = 50pF	3.3V		8.8	21.1	1		25.2	1		25.2	ns
t_{PZH}	OE	Q	C_L = 50pF	3.3V		7.4	11.7	1		14	1		14	ns

5.7 Switching Characteristics (continued)

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLZ}	OE	Q	C_L = 50pF	3.3V		4.4	12.9	1		13.7	1		13.7	ns
t_{PHZ}	OE	Q	C_L = 50pF	3.3V		4.6	15.2	1		16.2	1		16.2	ns
t_{PLH}	RCLK	Q_A-Q_H	C_L = 50pF	3.3V		7.3	46.3	1		47	1		47.3	ns
t_{PHL}	RCLK	Q_A-Q_H	C_L = 50pF	3.3V		7.3	12.2	1		14.3	1		14.3	ns
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50pF	3.3V		8.3	11.4	1		13.5	1		13.5	ns
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 50pF	3.3V		8.3	12.2	1		14.4	1		14.4	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50pF	3.3V		8.3	13.4	1		15.7	1		15.7	ns
F_{MAX}	-	-	C_L = 15pF	5V	135	175		115			115			MHz
t_{PZL}	OE	Q	C_L = 15pF	5V		5.4	8.2	1		9.9	1		9.9	ns
t_{PZH}	OE	Q	C_L = 15pF	5V		4.3	6.3	1		7.6	1		7.6	ns
t_{PLZ}	OE	Q	C_L = 15pF	5V		3.8	6.1	1		6.8	1		6.8	ns
t_{PHZ}	OE	Q	C_L = 15pF	5V		3.8	7.5	1		8.4	1		8.4	ns
t_{PLH}	RCLK	Q_A-Q_H	C_L = 15pF	5V		4.3	21.3	1		21.8	1		22.2	ns
t_{PHL}	RCLK	Q_A-Q_H	C_L = 15pF	5V		4.3	6.8	1		8.1	1		8.1	ns
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15pF	5V		4.5	8	1		9.1	1		9.1	ns
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 15pF	5V		4.5	6.9	1		8.3	1		8.3	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15pF	5V		4.5	7	1		8.5	1		8.5	ns
F_{MAX}	-	-	C_L = 50pF	5V	120	140		95			95			MHz
t_{PZL}	OE	Q	C_L = 50pF	5V		6.8	15.4	1		18.2	1		18.2	ns
t_{PZH}	OE	Q	C_L = 50pF	5V		5.7	8.3	1		9.9	1		9.9	ns
t_{PLZ}	OE	Q	C_L = 50pF	5V		3.4	9.1	1		9.8	1		9.8	ns
t_{PHZ}	OE	Q	C_L = 50pF	5V		3.5	11.2	1		11.9	1		11.9	ns
t_{PLH}	RCLK	Q_A-Q_H	C_L = 50pF	5V		5.6	46.3	1		46.5	1		46.9	ns
t_{PHL}	RCLK	Q_A-Q_H	C_L = 50pF	5V		5.6	9.3	1		10.9	1		10.9	ns
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50pF	5V		6.4	9.5	1		10.9	1		10.9	ns
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 50pF	5V		6.4	9.3	1		10.9	1		10.9	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50pF	5V		6.4	9.4	1		11.1	1		11.1	ns

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.9	-0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

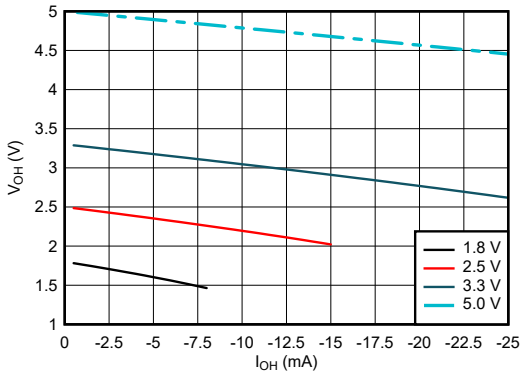


Figure 5-1. Output Voltage vs Current in HIGH State

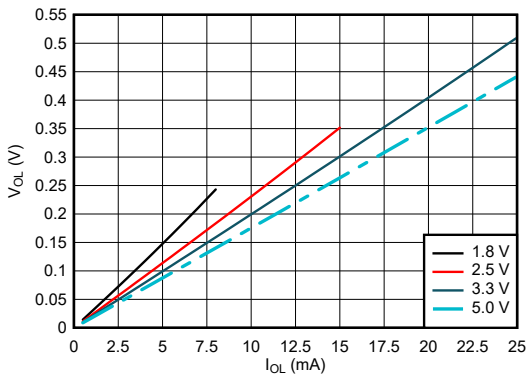


Figure 5-2. Output Voltage vs Current in LOW State

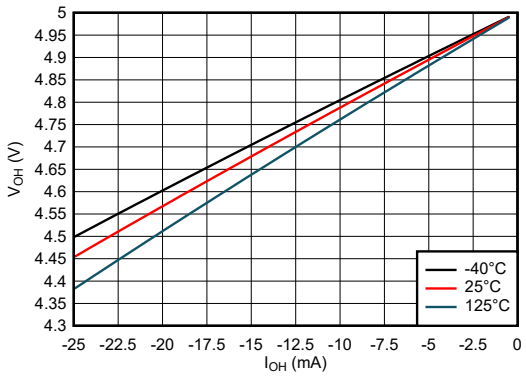


Figure 5-3. Output Voltage vs Current in HIGH State; 5V Supply

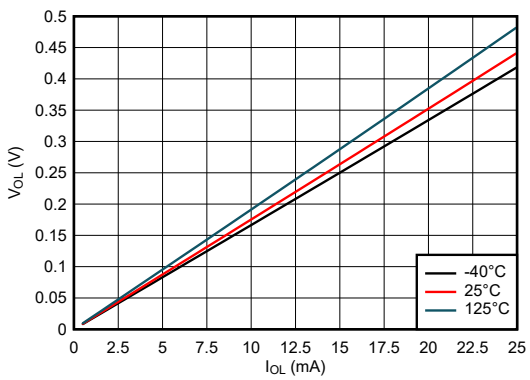


Figure 5-4. Output Voltage vs Current in LOW State; 5V Supply

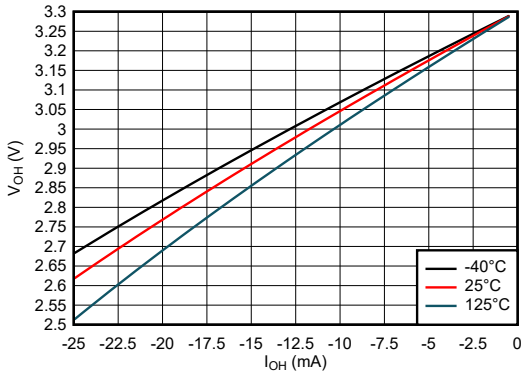


Figure 5-5. Output Voltage vs Current in HIGH State; 3.3V Supply

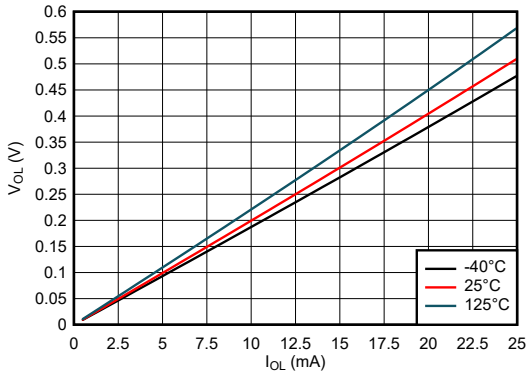


Figure 5-6. Output Voltage vs Current in LOW State; 3.3V Supply

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

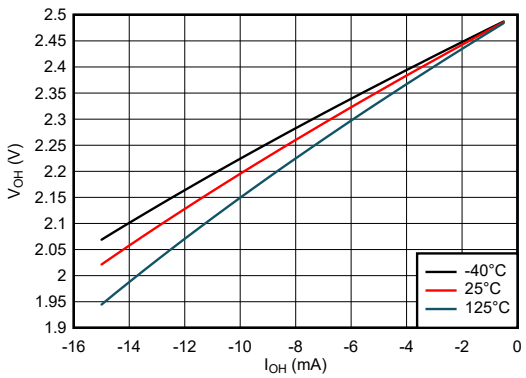


Figure 5-7. Output Voltage vs Current in HIGH State; 2.5V Supply

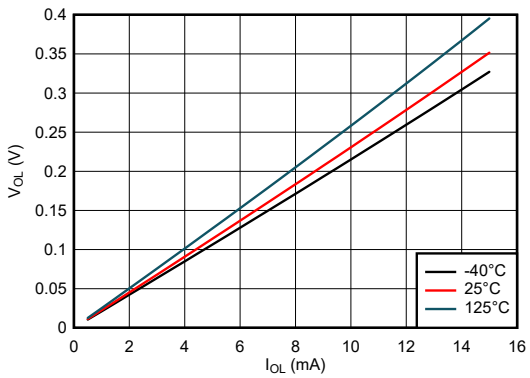


Figure 5-8. Output Voltage vs Current in LOW State; 2.5V Supply

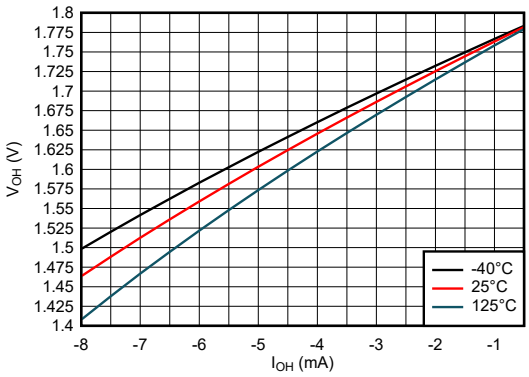


Figure 5-9. Output Voltage vs Current in HIGH State; 1.8V Supply

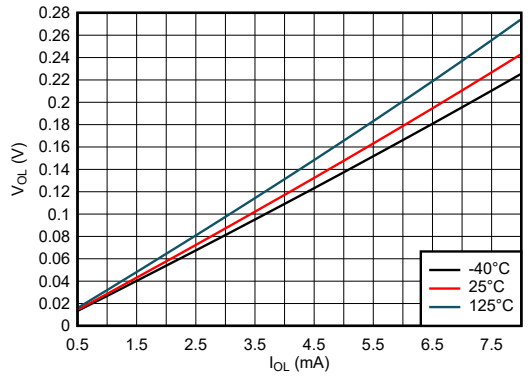


Figure 5-10. Output Voltage vs Current in LOW State; 1.8V Supply

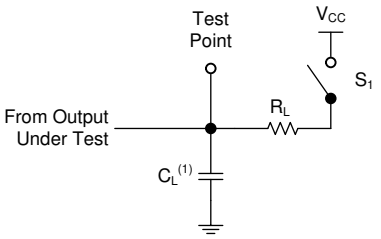
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.

TEST	S1	R_L	C_L	ΔV	V_{CC}
t_{PLZ}, t_{PZL}	CLOSED	1kΩ	15pF, 50pF	0.15V	≤ 2.5V
t_{PLZ}, t_{PZL}	CLOSED	1kΩ	15pF, 50pF	0.3V	> 2.5V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Open-Drain Outputs

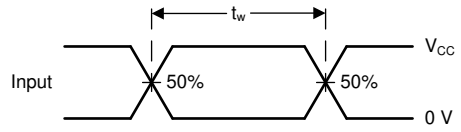


Figure 6-2. Voltage Waveforms, Pulse Duration

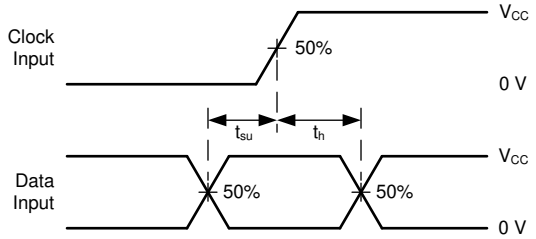
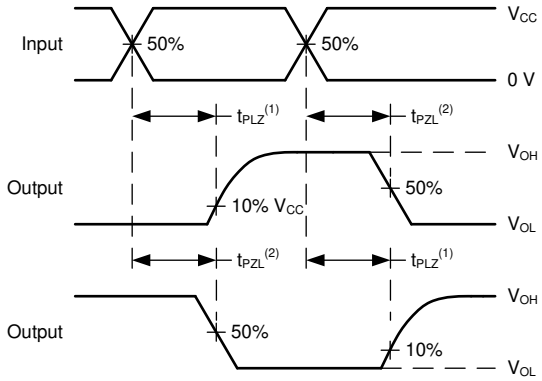


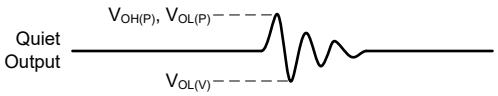
Figure 6-3. Voltage Waveforms, Setup and Hold Times



(1) t_{PLZ} is the same as t_{dis}.

(2) t_{PZL} is the same as t_{en}.

Figure 6-4. Voltage Waveforms Propagation Delays



Noise values measured with all other outputs simultaneously switching.

Figure 6-5. Voltage Waveforms, Noise

7 Detailed Description

7.1 Overview

The SN74LV8T596 is an 8-bit shift register that feeds an 8-bit D-type storage register. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, then the shift register always is one clock pulse ahead of the storage register. All inputs include Schmitt-triggers allowing for slow input transitions and providing more noise margin. Outputs Q_A through Q_H are open-drain which require a pull-up resistor to output a High. The serial output $Q_{H'}$ is push-pull.

7.2 Functional Block Diagram

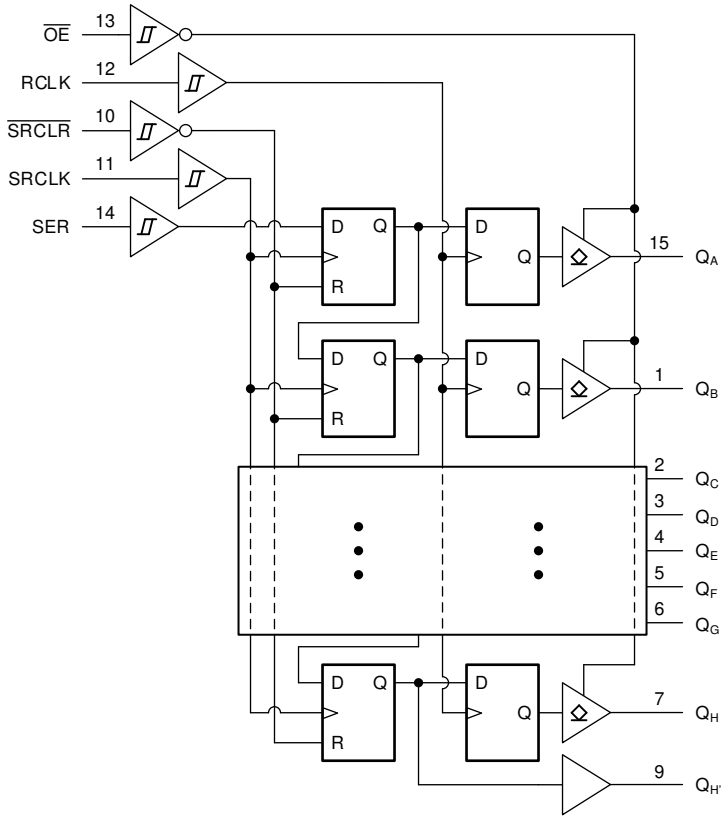


Figure 7-1. Logic Diagram (Positive Logic) for SN74LV8T596

7.3 Feature Description

7.3.1 Open-Drain CMOS Outputs

This device includes open-drain CMOS outputs. Open-drain outputs can only drive the output low. When in the high logical state, open-drain outputs will be in a high-impedance state. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage; the output voltage is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused open-drain CMOS outputs should be left disconnected.

7.3.2 Latching Logic with Known Power-Up State

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory. In typical logic devices, the output state of each latching circuit is unknown after power is initially applied; however, this device includes an added Power On Reset (POR) circuit which sets the states of all included latching circuits during the power-up ramp prior to the device starting normal functionality.

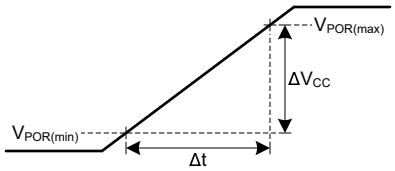


Figure 7-2. Supply (V_{CC}) Ramp Characteristics for Known Power-Up State

Figure 7-2 shows a correct supply voltage turn-on ramp and defines values used in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

Prior to starting the power-on ramp, the supply must be completely off ($V_{CC} \leq V_{POR(min)}$).

The supply voltage must ramp at a rate within the range provided in the *Recommended Operating Conditions* table.

The output state of each latching logic circuit only remains stable as long as power is applied to the device ($V_{CC} \geq V_{POR(max)}$).

Variation from these recommendations will result in the device having an unknown power-up state.

7.3.3 LVxT Enhanced Input Voltage

The SN74LV8T596 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. For proper functionality, input signals must remain at or above the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. Figure 7-3 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Input signals must transition between valid logic states quickly, as defined by the input transition rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. For more details, see the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.

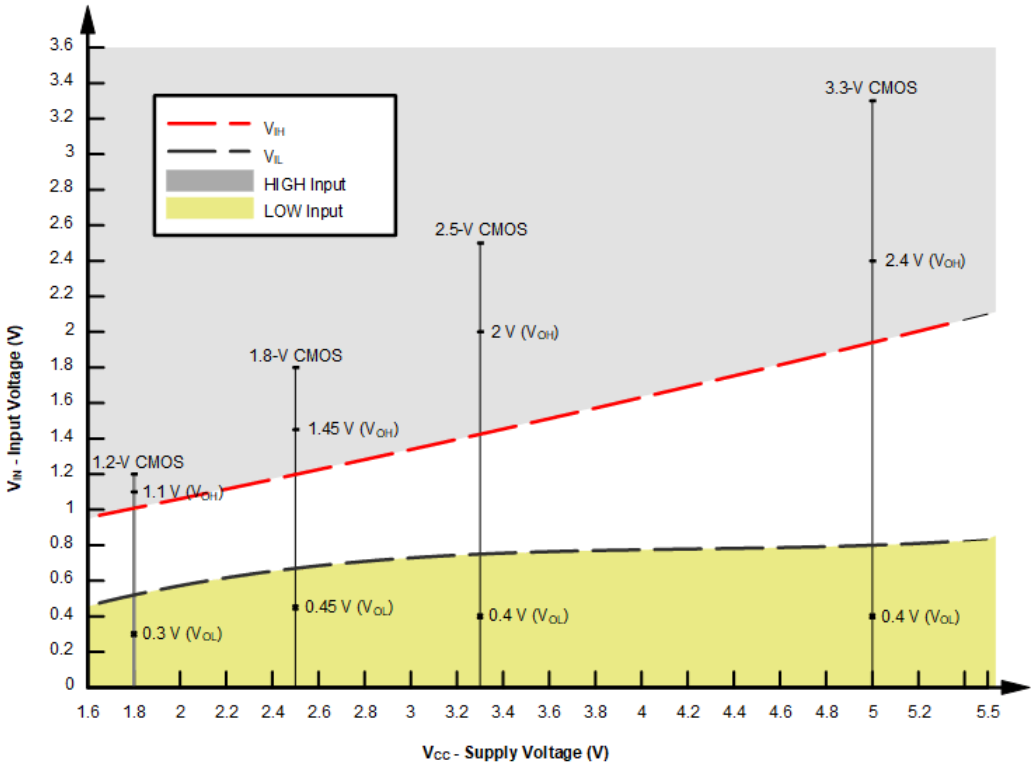


Figure 7-3. LVxT Input Voltage Levels

7.3.4 Clamp Diode Structure

As Figure 7-4 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

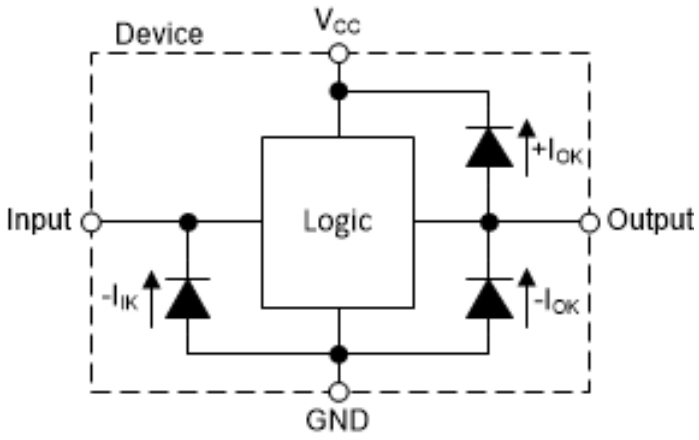


Figure 7-4. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LV8T596.

Table 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	H	↑	X	Shift-register data is stored in the storage register.
X	↑	H	↑	X	Data in shift register is stored in the storage register, the data is then shifted through.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74LV8T596 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74LV8T596 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The OE pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74LV8T596 can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many SN74LV8T596 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register. An RC circuit can be connected to the $\overline{\text{SRCLR}}$ pin as shown in the Figure 8-1 to initialize the shift register to all zeros. With the $\overline{\text{OE}}$ pin pulled up with a resistor, this process can be performed while the outputs are in a high impedance state eliminating any erroneous data causing issues with the displays.

8.2 Typical Application

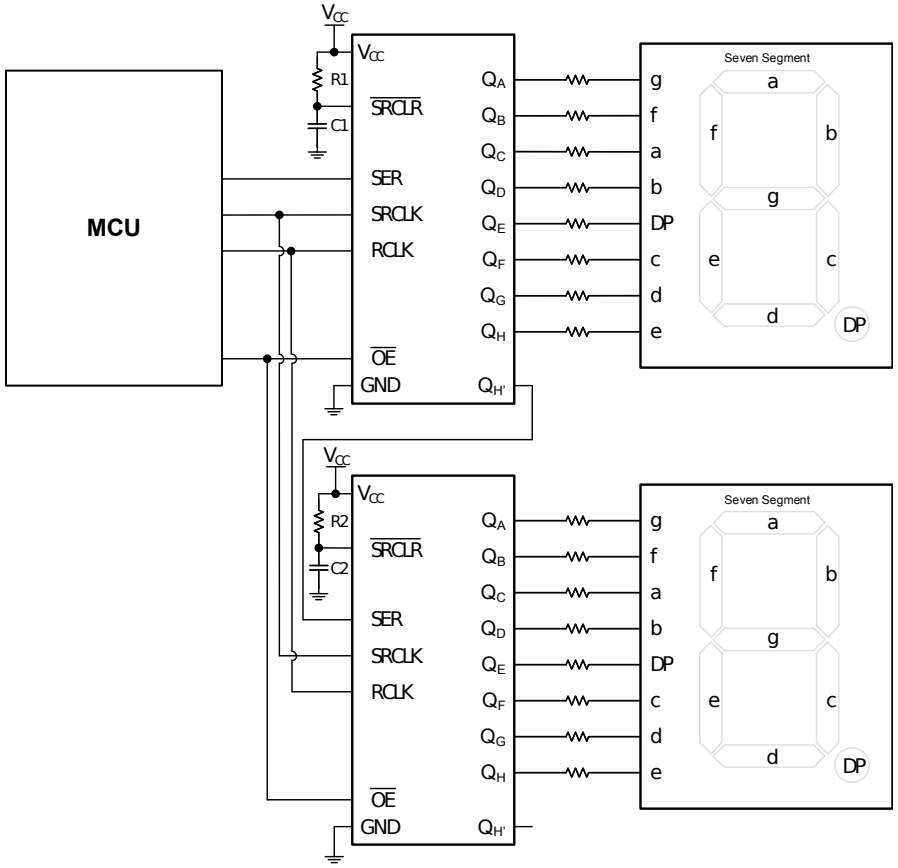


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current (I_{CC}) listed in the *Electrical Characteristics* and any transient current required for switching. is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV8T596 plus the maximum supply current (I_{CC}) listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LV8T596 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LV8T596 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL}. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74LV8T596, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10kΩ resistor value is often used due to these factors.

The SN74LV8T596 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

For additional information regarding the inputs for this device, refer to the *Feature Description*.

8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

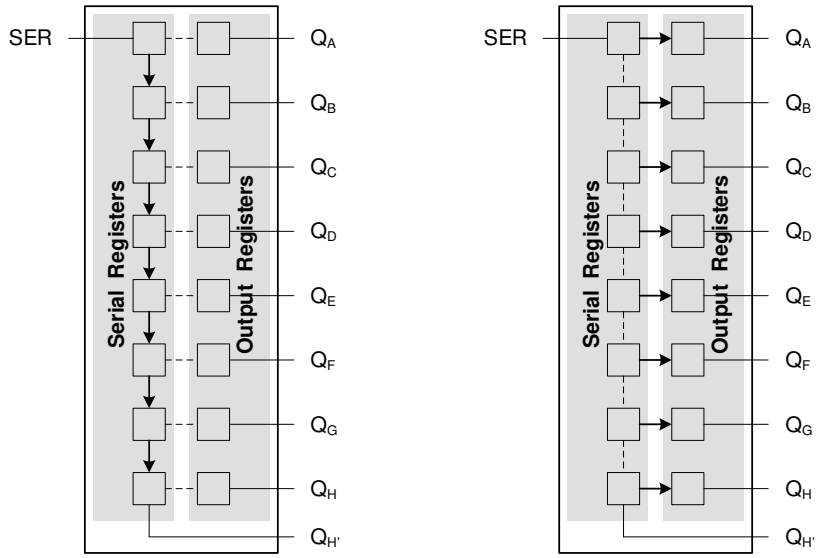
Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV8T596 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves



SRCLK rising edge shifts data in the serial registers only

RCLK rising edge shifts data to the output registers

Figure 8-2. Simplified Functional Diagram Showing Clock Operation

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. As shown in the following layout example, install the bypass capacitor as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

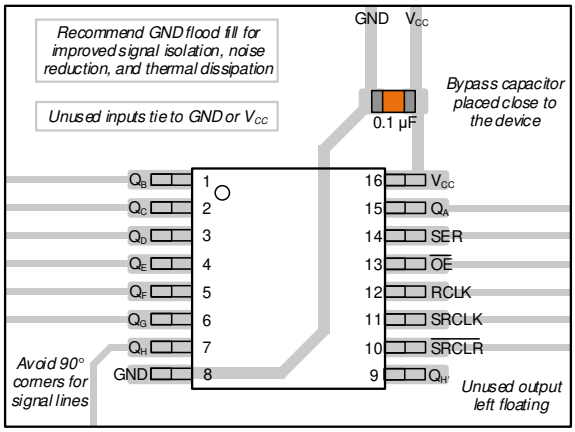


Figure 8-3. Example Layout for the SN74LV8T596 in TSSOP

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
March 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV8T596BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT596
SN74LV8T596BQBR.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT596
SN74LV8T596PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LVT596
SN74LV8T596PWR.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVT596

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LV8T596 :

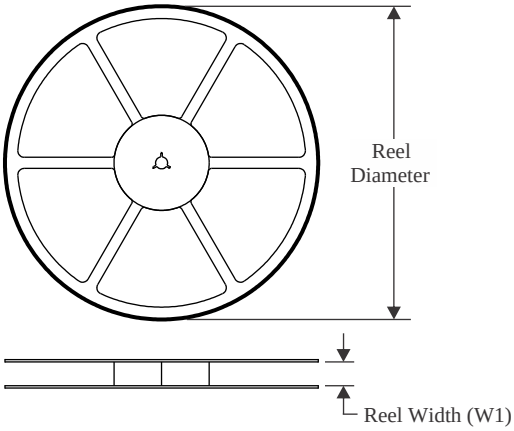
- Automotive : SN74LV8T596-Q1

NOTE: Qualified Version Definitions:

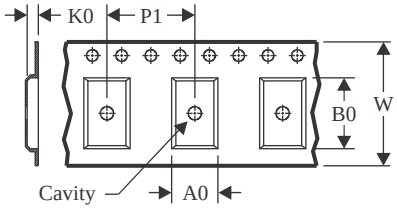
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

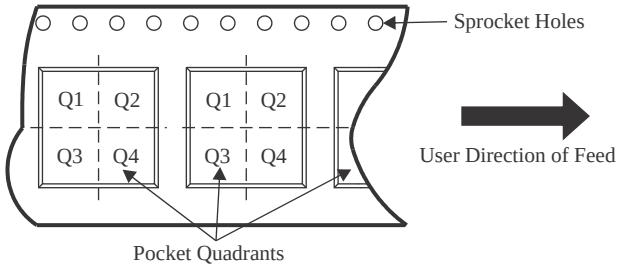


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

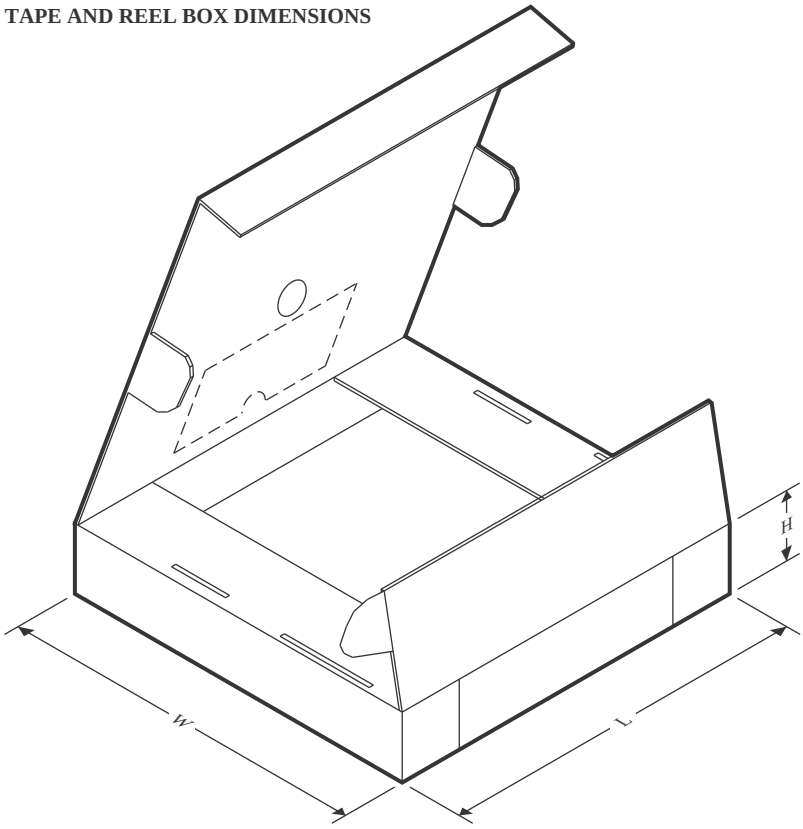
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV8T596BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74LV8T596PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV8T596BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74LV8T596PWR	TSSOP	PW	16	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

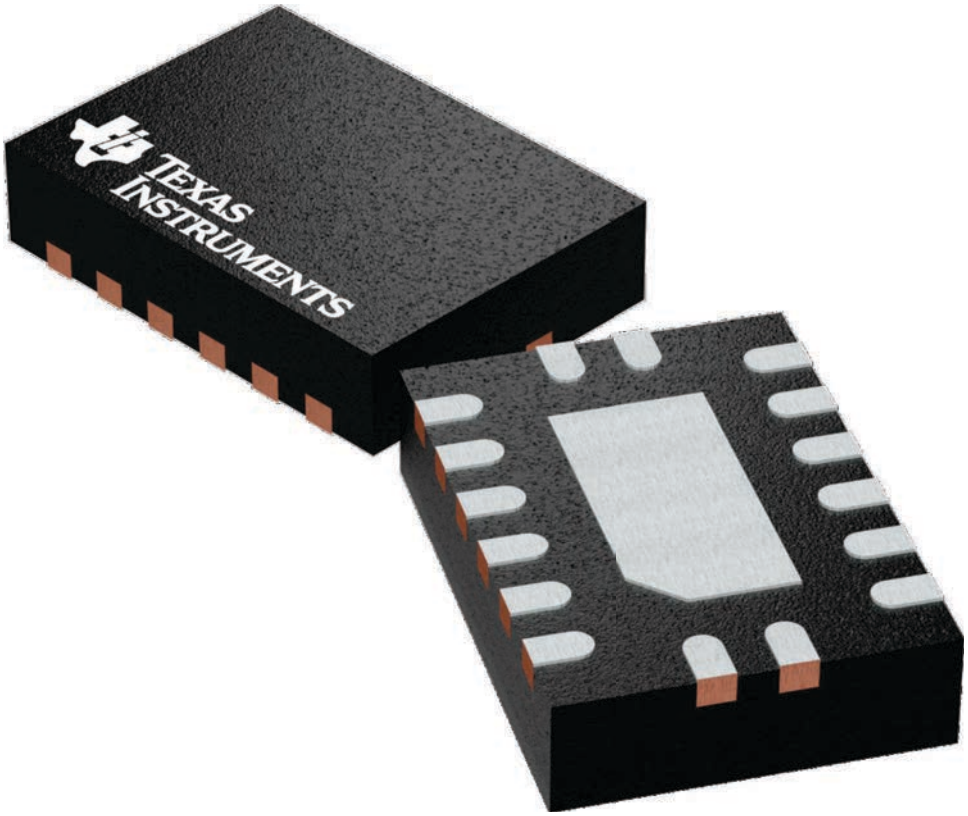
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



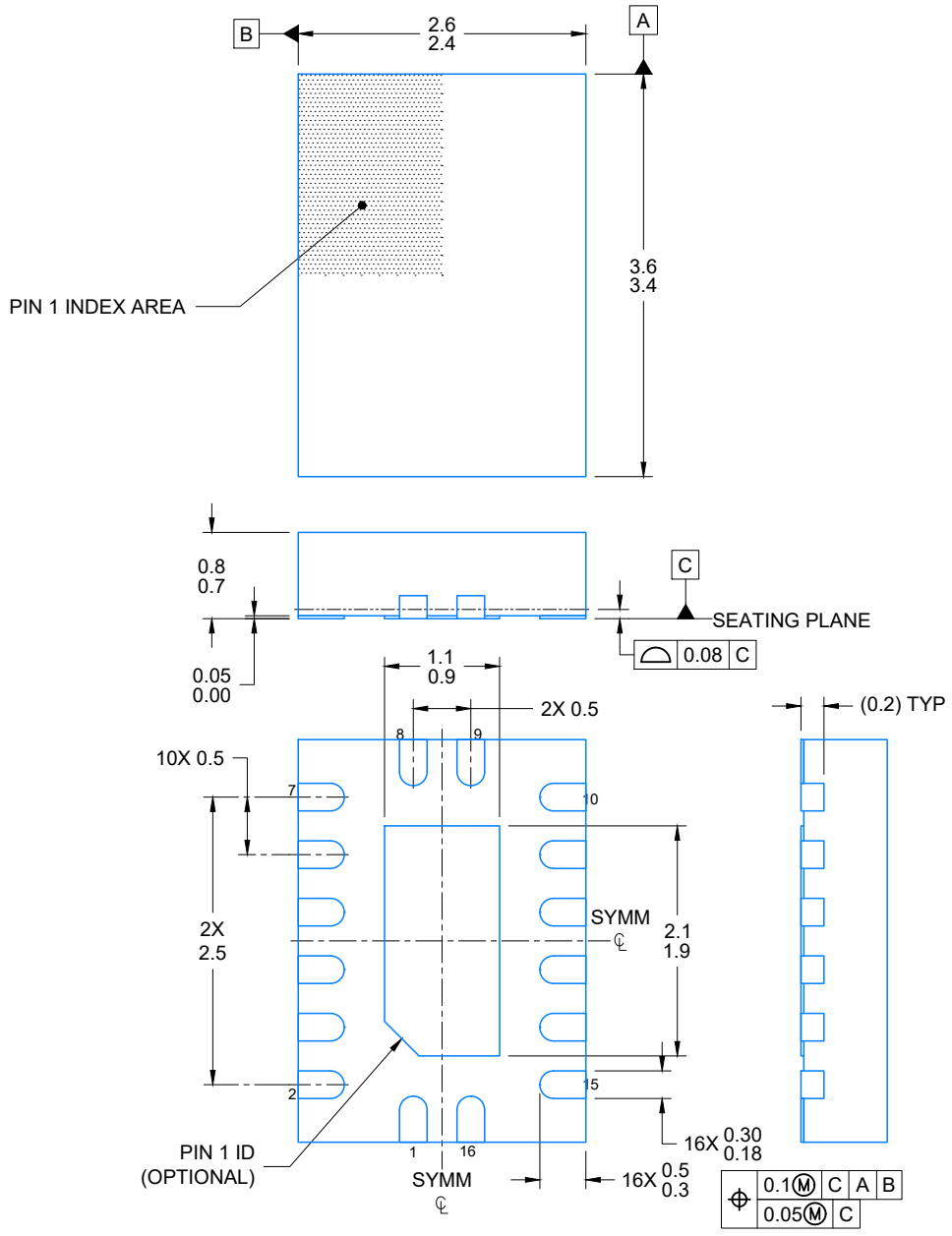
4226161/A

PACKAGE OUTLINE

BQB0016A

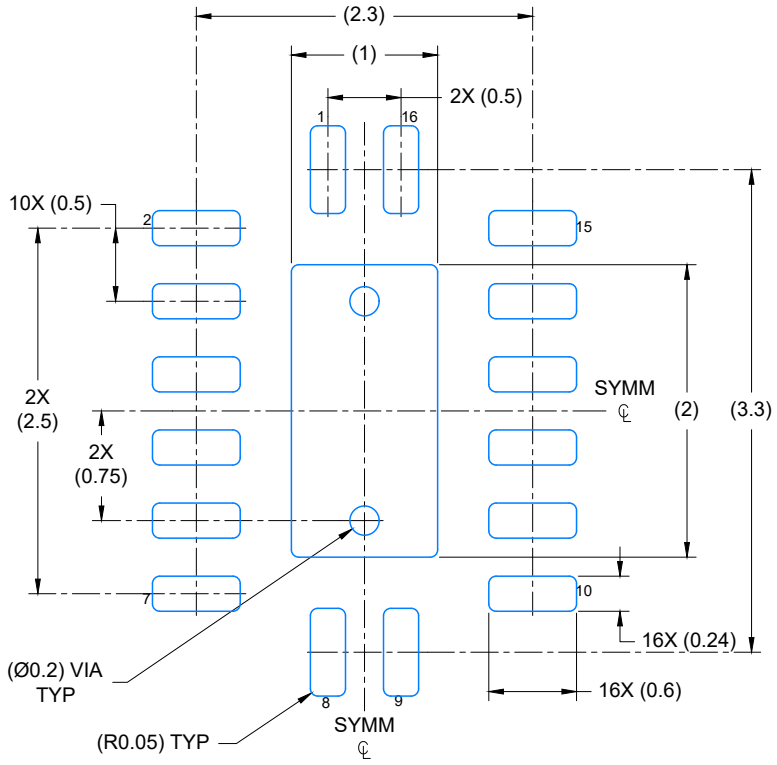
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

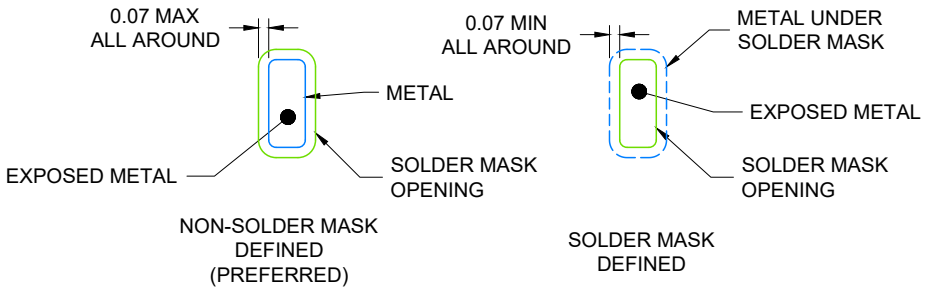


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



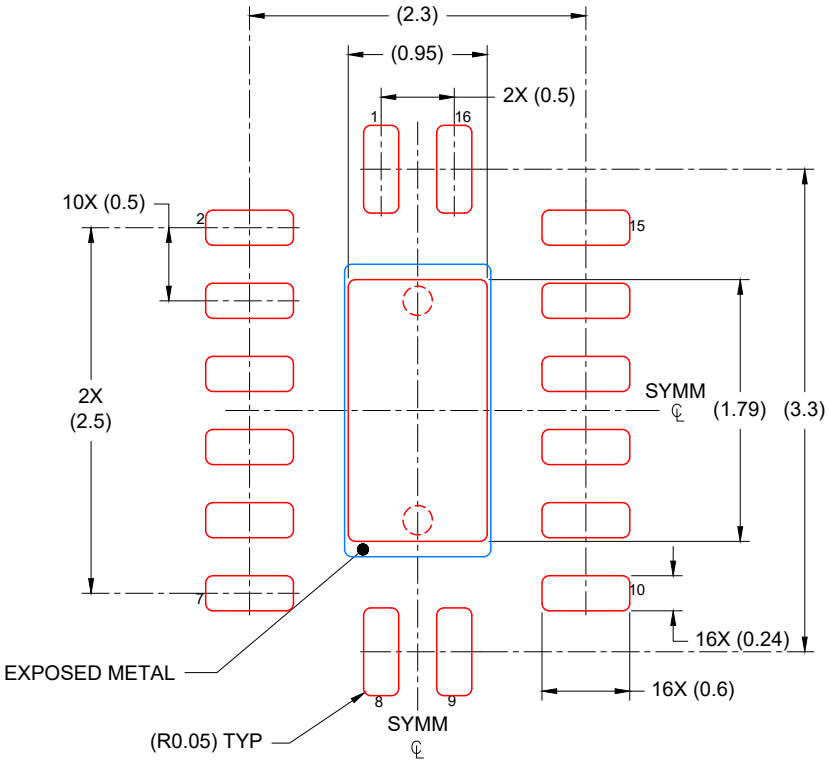
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

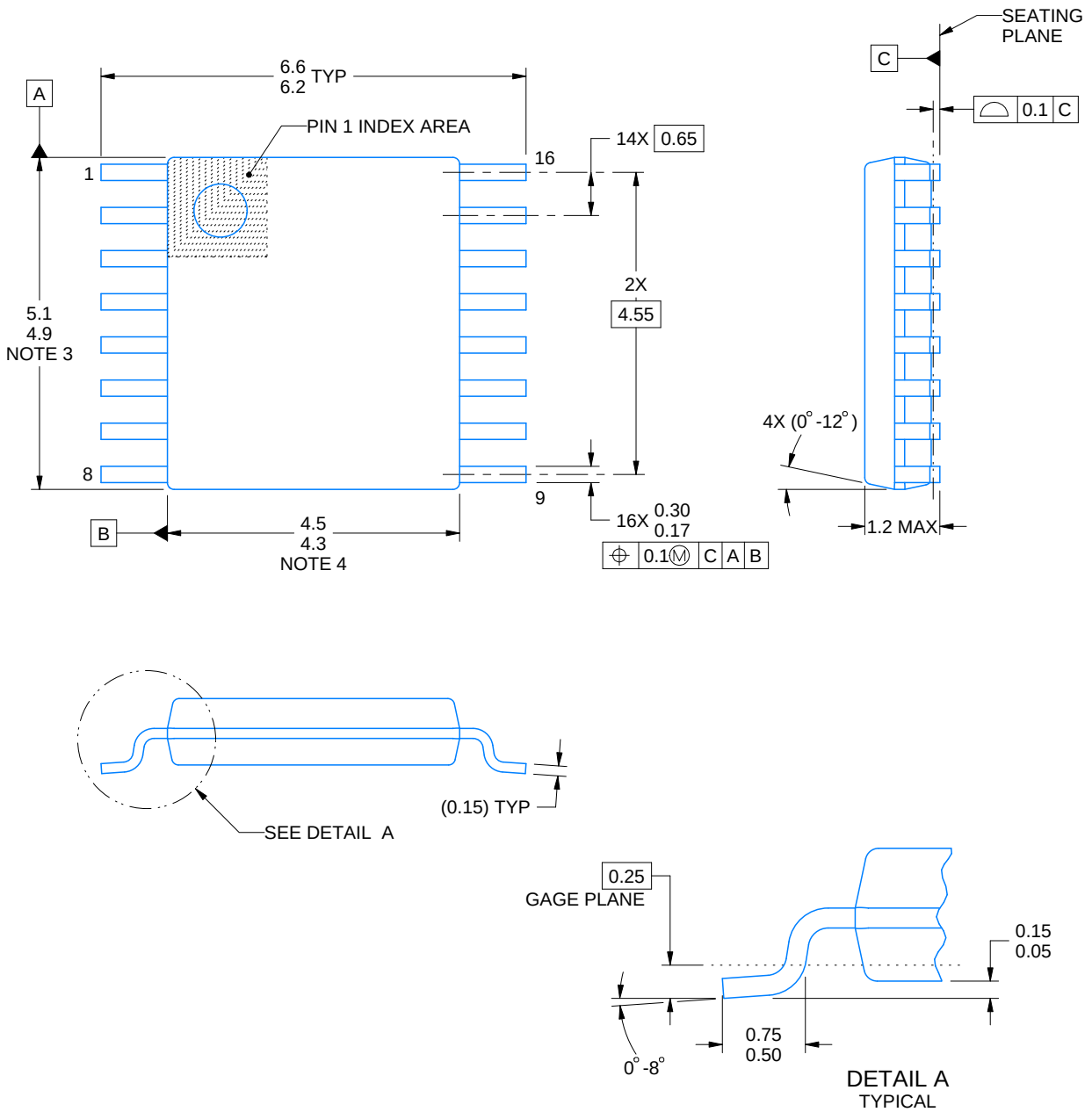
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

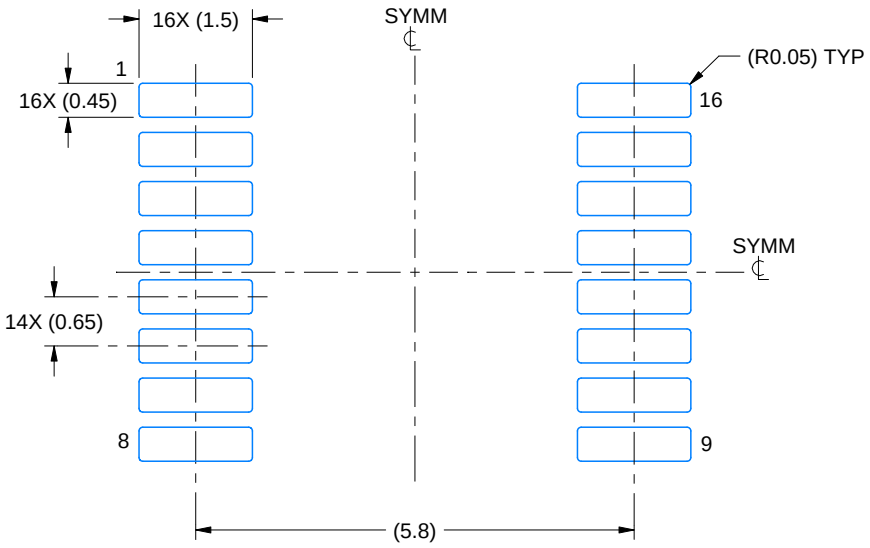
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



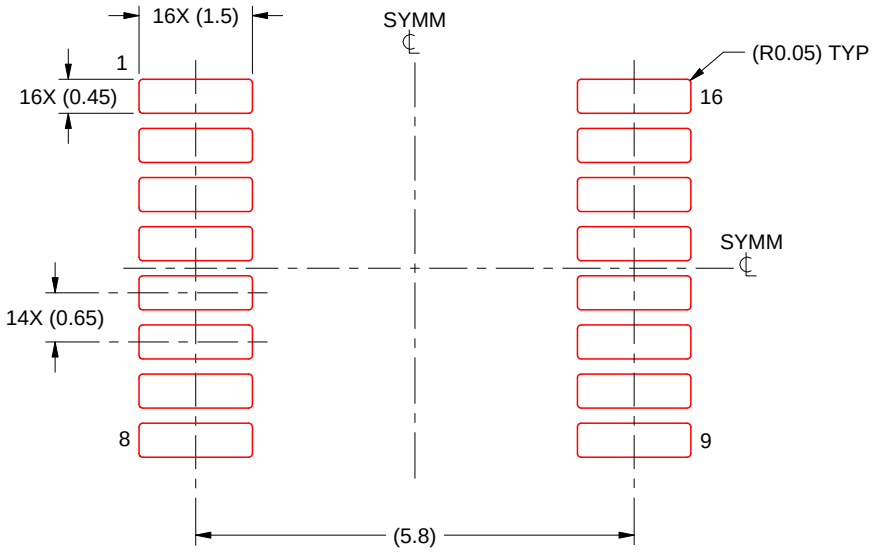
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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