SN74LV4051A-Q1 Automotive 8-Channel Analog Multiplexer or Demultiplexer

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- 1.65V to 5.5V V_{CC} operation
- Supports mixed-mode voltage operation on all ports
- High on-off output-voltage ratio
- Low crosstalk between switches
- Individual switch controls
- Extremely low input current
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Applications

- Automotive infotainment and cluster
- Telematics, eCall

3 Description

This 8-channel CMOS analog multiplexer and demultiplexer is designed for 1.65V to 5.5V V_{CC} operation.

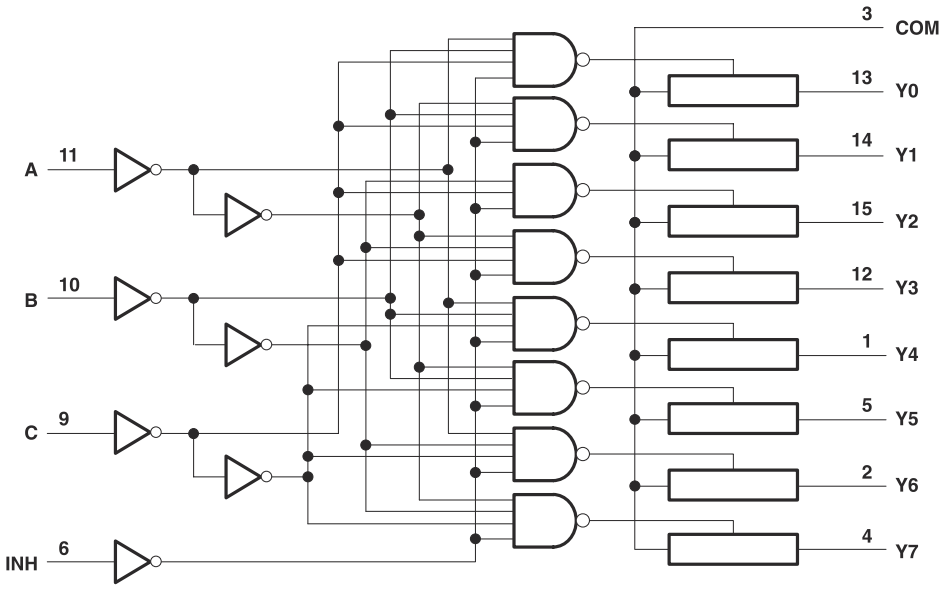
The SN74LV4051A-Q1 handles analog and digital signals. Each channel permits signals with amplitudes up to 5.5V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74LV4051A-Q1	PW (TSSOP, 16)	5mm × 6.4mm
	D (SOIC, 16)	9.9mm × 6mm
	DYY (SOT-23-THIN, 16)	4.2mm x 3.26mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

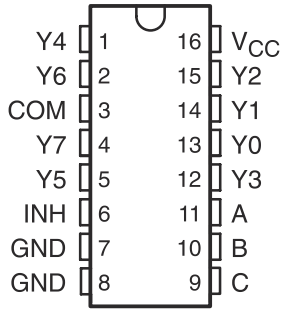


Figure 4-1. D, PW or DYY Package, 16-Pin SOIC, TSSOP, or SOT-23-THIN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Y4	1	I[2]	Input to mux
Y6	2	I[2]	Input to mux
COM	3	O[2]	Output of mux
Y7	4	I[2]	Input to mux
Y5	5	I[2]	Input to mux
INH	6	I[2]	Enables the outputs of the device. Logic low level with turn the outputs on, high level will turn them off.
GND	7	—	Ground
GND	8	—	Ground
C	9	I	Selector line for outputs (see *Section 7.4* for specific information)
B	10	I	Selector line for outputs (see *Section 7.4* for specific information)
A	11	I	Selector line for outputs (see *Section 7.4* for specific information)
Y3	12	I[2]	Input to mux
Y0	13	I[2]	Input to mux
Y1	14	I[2]	Input to mux
Y2	15	I[2]	Input to mux
Vcc	16	I	Device power input

(1) I = input, O = output
(2) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins Y0-Y7 may be considered outputs (O) and the COM pin may be considered inputs (I).

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7.0	V
V_I	Logic input voltage range		–0.5	7.0	V
V_{IO}	Switch I/O voltage range(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0	–20		mA
I_{IOK}	Switch IO diode clamp current	V_{IO} < 0 or V_{IO} > V_{CC}	–50	50	mA
I_T	Switch continuous current	V_{IO} = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(3) This value is limited to 5.5 V maximum

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	All pins	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information: SN74LV4051A-Q1

THERMAL METRIC (1)		SN74LV4051A-Q1 PW (TSSOP) 16 PINS	SN74LV4051A-Q1 DYY (SOT) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140.2	199.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	121.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.7	129.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.4	24.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	97.3	126.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1(2)		5.5	V
V_{IH}	High-level input voltage, logic control inputs	V_{CC} = 1.65	1.2		5.5	V
		V_{CC} = 2 V	1.5		5.5	
		V_{CC} = 2.3 V to 2.7 V	V_{CC} x 0.7		5.5	
		V_{CC} = 3 V to 3.6 V	V_{CC} x 0.7		5.5	
		V_{CC} = 4.5 V to 5.5 V	V_{CC} x 0.7		5.5	
V_{IL}	Low-level input voltage, logic control inputs	V_{CC} = 1.65 V	0		0.4	V
		V_{CC} = 2	0		0.5	
		V_{CC} = 2.3V to 2.7V	0		V_{CC} x 0.3	
		V_{CC} = 3 V to 3.6 V	0		V_{CC} x 0.3	
		V_{CC} = 4.5 V to 5.5 V	0		V_{CC} x 0.3	
V_I	Logic control input voltage		0		5.5	V
V_{IO}	Switch input or output voltage		0		V_{CC}	V
Δt/ΔV	Logic input transition rise or fall rate	V_{CC} = 1.0 V to 2.0 V			500	ns/V
		V_{CC} = 2.0 V to 2.7 V			200	
		V_{CC} = 3 V to 3.6 V			100	
		V_{CC} = 4.5 V to 5.5 V			20	
T_A	Ambient temperature		–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) When using a V_{CC} of ≤1.2 V, it is recommended to use these devices only for transmitting digital signals.When supply voltage is near 1.2 V the analog switch ON resistance becomes very non-linear

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T_A	V_{CC}	MIN	TYP	MAX	UNIT
r_{ON}	ON-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL}	25°C	1.65 V		60	150	Ω
			–40°C to 85°C				225	
			–40°C to 125°C				225	
			25°C	2.3 V		38	180	
			–40°C to 85°C				225	
			–40°C to 125°C				225	
			25°C	3 V		30	150	
			–40°C to 85°C				190	
			–40°C to 125°C				190	
			25°C	4.5 V		22	75	
			–40°C to 85°C				100	
			–40°C to 125°C				100	

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$r_{ON(p)}$	Peak ON-state resistance	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	25°C	1.65 V		220	600	Ω
			–40°C to 85°C				700	
			–40°C to 125°C				700	
			25°C	2.3 V		113	500	
			–40°C to 85°C				600	
			–40°C to 125°C				600	
			25°C	3 V		54	180	
			–40°C to 85°C				225	
			–40°C to 125°C				225	
			25°C	4.5 V		31	100	
			–40°C to 85°C				125	
			–40°C to 125°C				125	
Δr_{ON}	Difference in ON-state resistance between switches	I_T = 2 mA, V_I = GND to V_{CC}, V_{INH} = V_{IL}	25°C	1.65 V		3	40	Ω
			–40°C to 85°C				40	
			–40°C to 125°C				40	
			25°C	2.3 V		2.1	30	
			–40°C to 85°C				40	
			–40°C to 125°C				40	
			25°C	3 V		1.4	20	
			–40°C to 85°C				30	
			–40°C to 125°C				30	
			25°C	4.5 V		1.3	15	
			–40°C to 85°C				20	
			–40°C to 125°C				20	
I_{IH} I_{IL}	Control input current	V_I = 5.5 V or GND	25°C	0 to 5.5 V	-0.1		0.1	µA
			–40°C to 85°C		-1		1	
			–40°C to 125°C		-2		2	
$I_{S(off)}$	OFF-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_{INH} = V_{IH}	25°C	5.5 V	-0.1		0.1	µA
			–40°C to 85°C		-1		1	
			–40°C to 125°C		-2		2	
$I_{S(on)}$	ON-state switch leakage current	V_I = V_{CC} or GND, V_{INH} = V_{IL}	25°C	5.5 V	-0.1		0.1	µA
			–40°C to 85°C		-1		1	
			–40°C to 125°C		-2		2	
I_{CC}	Supply current	V_I = V_{CC} or GND V_{INH} = 0 V	25°C	5.5 V		0.01		µA
			–40°C to 85°C				20	
			–40°C to 125°C				40	
C_{IC}	Control input capacitance	f = 10 MHz	25°C	3.3 V		2		pF
C_{IS}	Common terminal capacitance	f = 10 MHz	25°C	3.3 V		23.4		pF
C_{OS}	Switch ternminal capacitance	f = 10 MHz	25°C	3.3 V		5.7		pF
C_F	Feedthrough capacitance	f = 10 MHz	25°C	3.3 V		0.5		pF

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T_A	V_{CC}	MIN	TYP	MAX	UNIT
C_{PD}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	25°C	3.3 V		5.9		pF

5.6 Timing Characteristics V_{CC} = 2.5 V ± 0.2 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF	25°C		1.9	10	ns
					–40°C to 85°C			16	
					–40°C to 125°C			18	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF	25°C		6.6	18	ns
					–40°C to 85°C			23	
					–40°C to 125°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF	25°C		7.4	18	ns
					–40°C to 85°C			23	
					–40°C to 125°C			25	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF	25°C		3.8	12	ns
					–40°C to 85°C			18	
					–40°C to 125°C			20	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF	25°C		7.8	28	ns
					–40°C to 85°C			35	
					–40°C to 125°C			35	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF	25°C		11.5	28	ns
					–40°C to 85°C			35	
					–40°C to 125°C			35	

5.7 Timing Characteristics V_{CC} = 3.3 V ± 0.3 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF	25°C		2.5	9	ns
					–40°C to 85°C			12	
					–40°C to 125°C			14	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF	25°C		5.5	20	ns
					–40°C to 85°C			25	
					–40°C to 125°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF	25°C		8.8	20	ns
					–40°C to 85°C			25	
					–40°C to 125°C			25	

5.8 Timing Characteristics V_{CC} = 5 V ± 0.5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF	25°C		1.5	6	ns
					–40°C to 85°C			8	
					–40°C to 125°C			10	

5.8 Timing Characteristics V_{CC} = 5 V ± 0.5 V (continued)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF	25°C		4	14	ns
					–40°C to 85°C			18	
					–40°C to 125°C			18	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF	25°C		6.2	14	ns
					–40°C to 85°C			18	
					–40°C to 125°C			18	

5.9 AC Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	SN74LV4051	C_L = 50 pF, R_L = 600 Ω, F_{in} = 1 MHz (sine wave)	V_{CC} = 2.3 V		20		MHz
					V_{CC} = 3 V		25		
					V_{CC} = 4.5 V		35		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	ALL	C_L = 50 pF, R_L = 600 Ω, F_{in} = 1 MHz (sine wave)	V_{CC} = 2.3 V		–45		dB
					V_{CC} = 3 V		–45		
					V_{CC} = 4.5 V		–45		
Crosstalk (between any switches)	COM or Yn	Yn or COM	ALL	C_L = 50 pF, R_L = 600 Ω, F_{in} = 1 MHz (sine wave)	V_{CC} = 2.3 V		20		mV
					V_{CC} = 3 V		35		
					V_{CC} = 4.5 V		60		
Sine-wave distortion	COM or Yn	Yn or COM	ALL	C_L = 50 pF, R_L = 10 kΩ, F_{in} = 1 kHz (sine wave)	V_I = 2 V_{p-p} V_{CC} = 2.3 V		0.1		%
					V_I = 2.5 V_{p-p} V_{CC} = 3 V		0.1		
					V_I = 4 V_{p-p} V_{CC} = 4.5 V		0.1		

6 Parameter Measurement Information

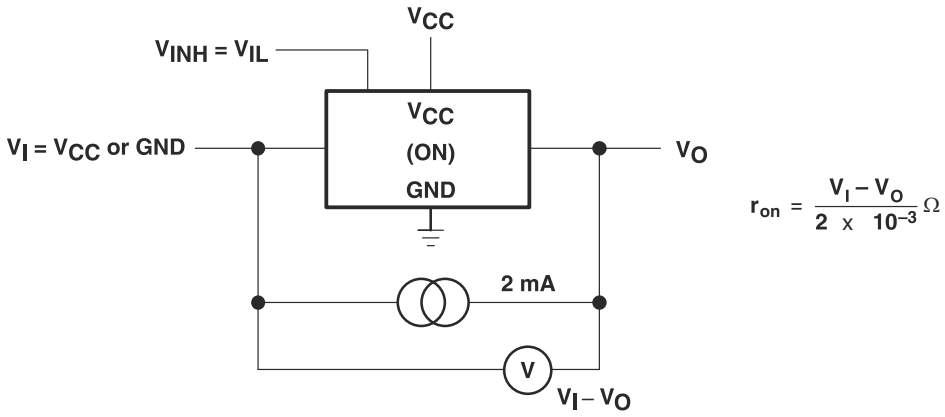


Figure 6-1. On-State Resistance Test Circuit

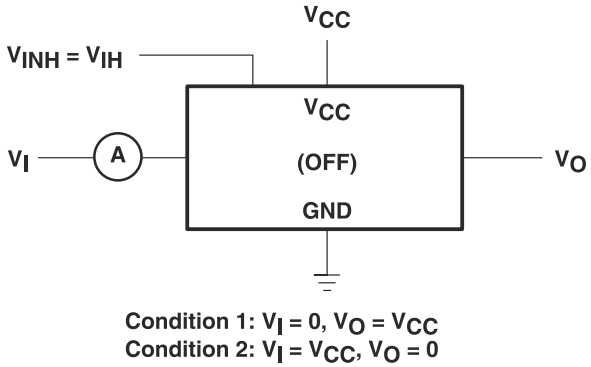


Figure 6-2. Off-State Switch Leakage-Current Test Circuit

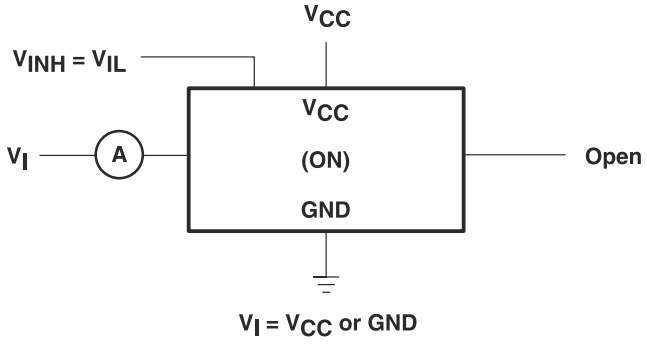


Figure 6-3. On-State Switch Leakage-Current Test Circuit

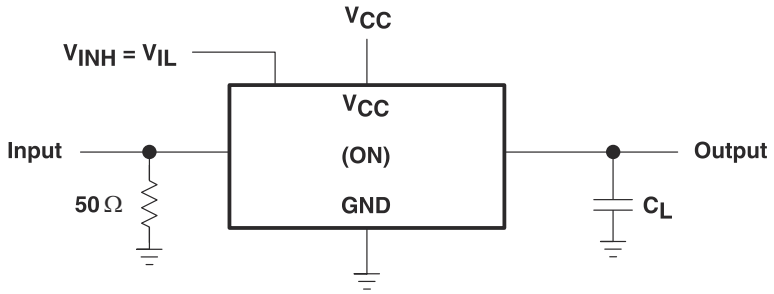
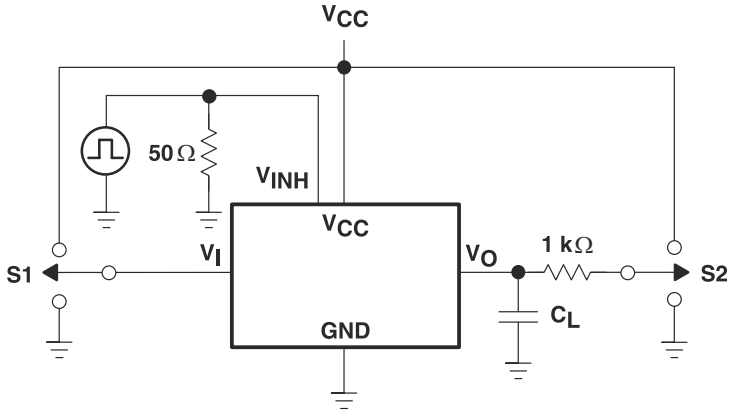
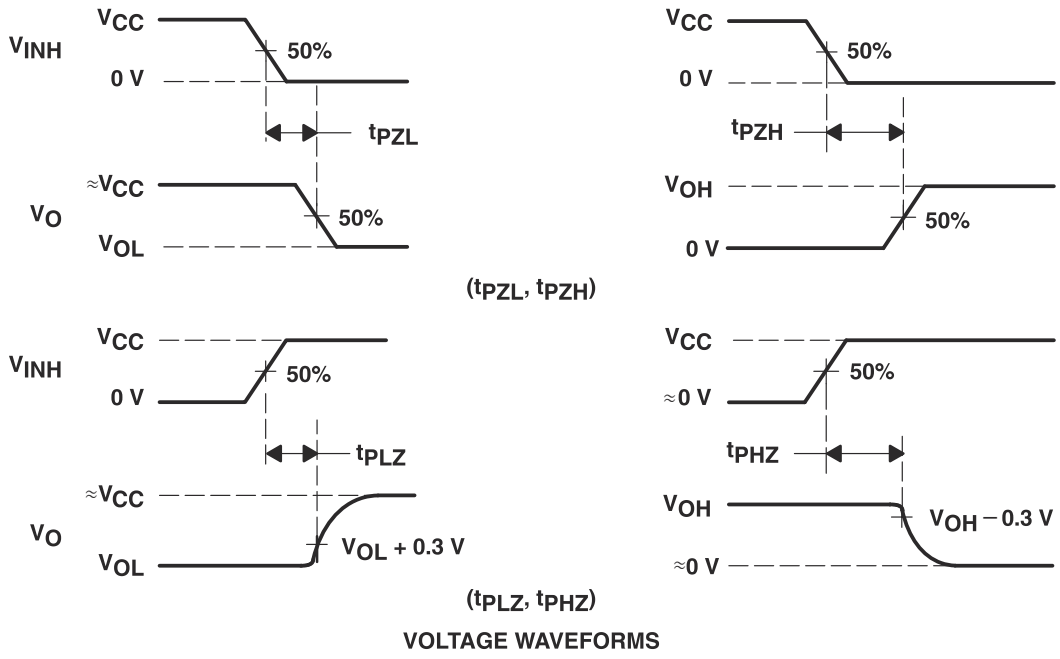


Figure 6-4. Propagation Delay Time, Signal Input to Signal Output



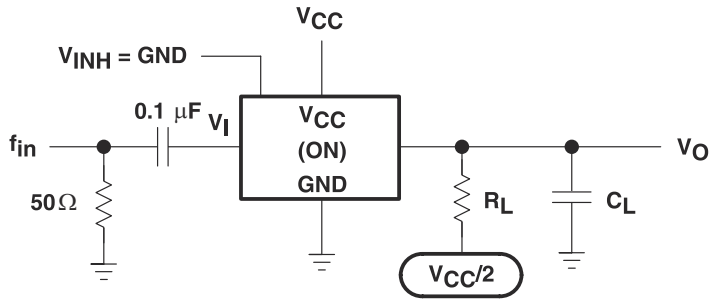
TEST	S1	S2
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	GND V_{CC}	V_{CC} GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 6-5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6-6. Frequency Response (Switch On)

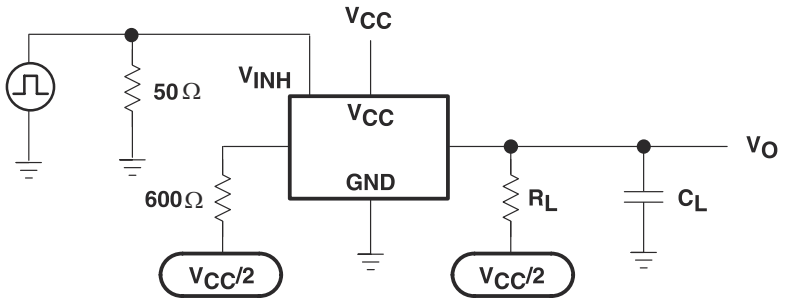


Figure 6-7. Crosstalk (Control Input, Switch Output)

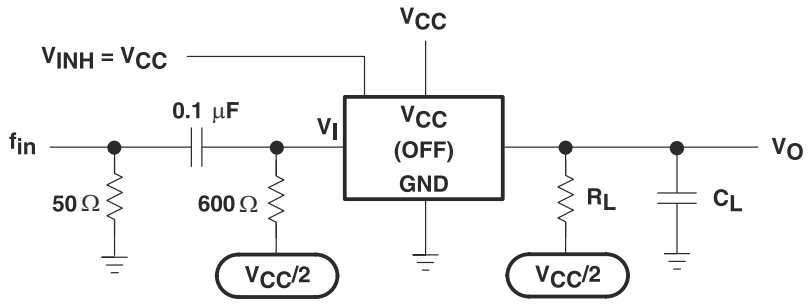


Figure 6-8. Feedthrough Attenuation (Switch Off)

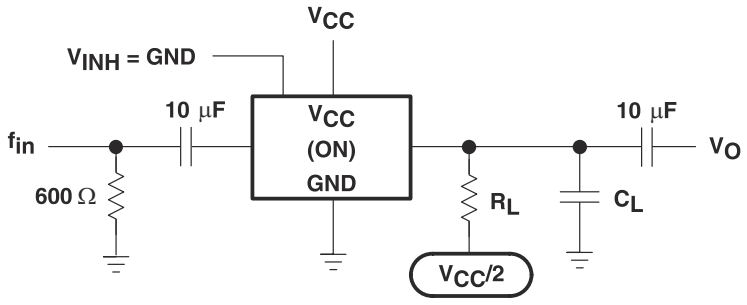


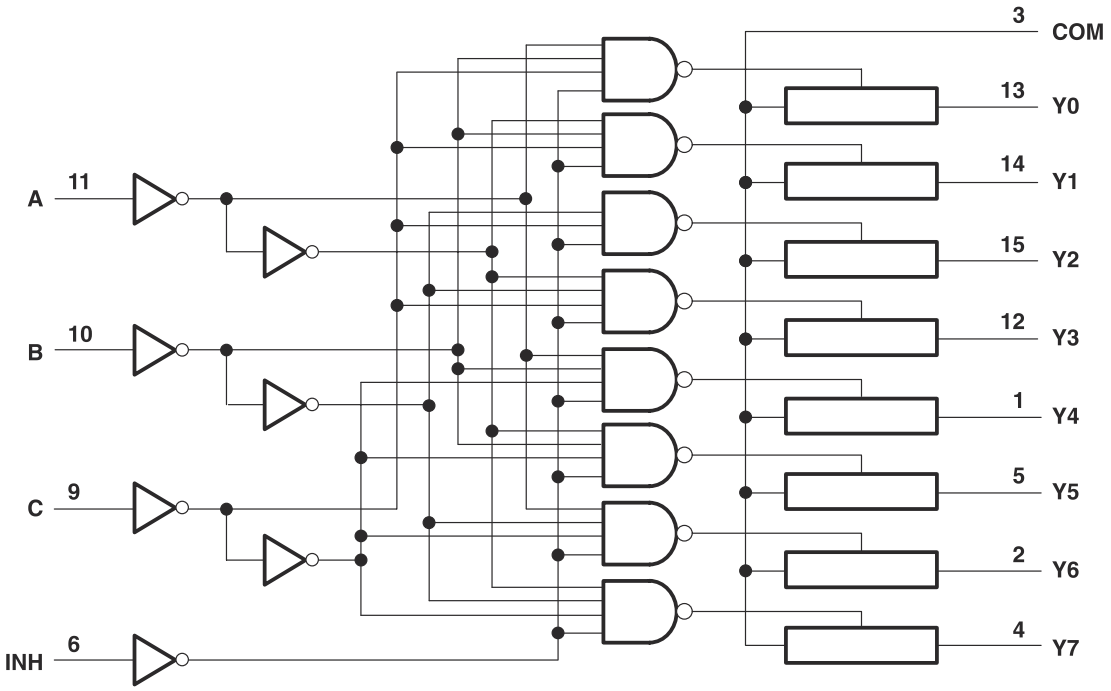
Figure 6-9. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

This device is an 8-channel analog multiplexer. A multiplexer is used when several signals must share the same device or resource. This device allows the selection of one of these signals at a time, for analysis or propagation.

7.2 Functional Block Diagram



7.3 Feature Description

This device contains one 8-channel multiplexer for use in a variety of applications, and can also be configured as demultiplexer by using the COM pin as an input and the Yx pins as outputs. This device is qualified for automotive applications and has an extended temperature range of –40°C to 125°C (maximum depends on package type).

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A multiplexer is used in applications where multiple signals share a resource. In the example below, several different sensors are connected to the analog-to-digital converter (ADC) of a microcontroller unit (MCU).

8.2 Typical Application

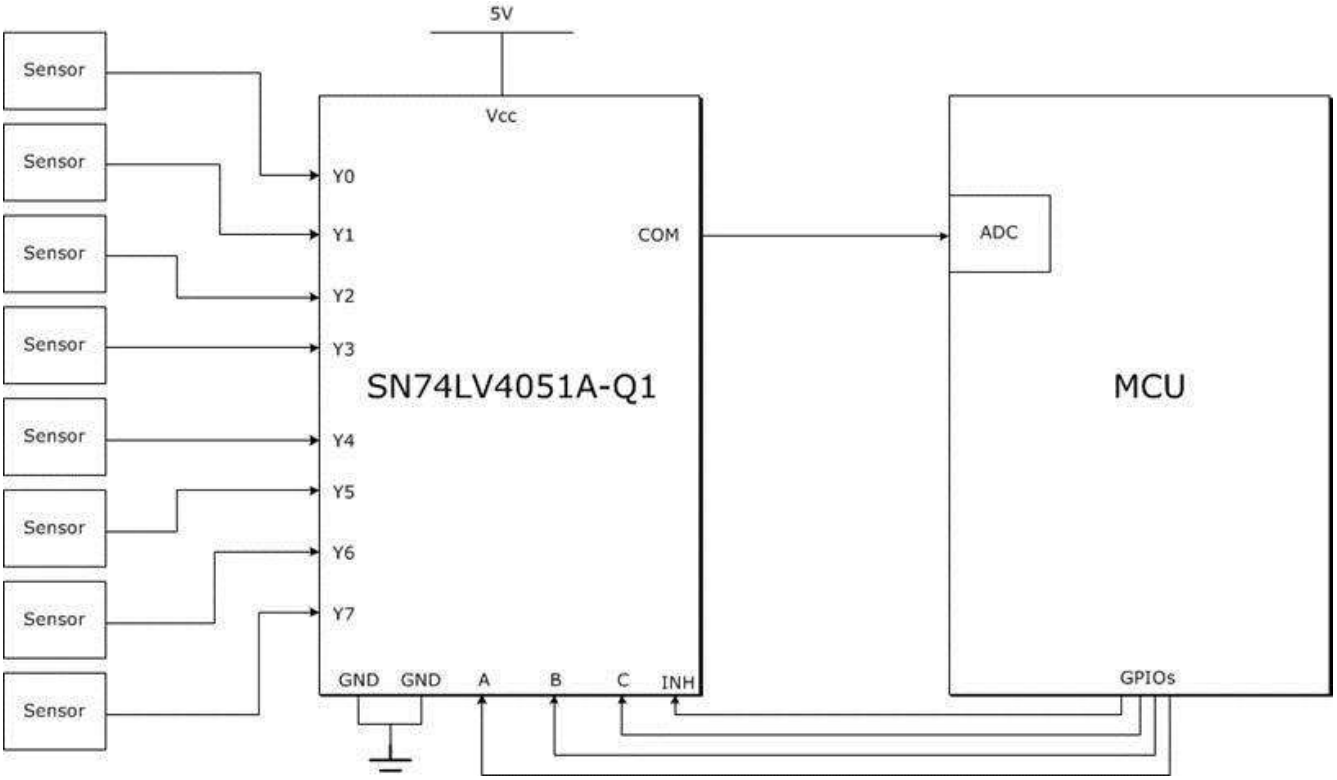


Figure 8-1. Example of Multiplexer Use With Analog Sensors and the ADC of an MCU

8.2.1 Design Requirements

Designing with the SN74LV4051A-Q1 device requires a stable input voltage between 2 V (see *Recommended Operating Conditions* for details) and 5.5V. Another important design consideration are the characteristics of the signal being multiplexed—ensure no important information is lost due to timing or incompatibility with this device.

8.2.2 Detailed Design Procedure

Processing eight different analog signals would normally require eight separate ADCs, but Figure 8-1 shows how to achieve this using only one ADC and four GPIOs (general-purpose input/outputs).

8.3 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the Vcc pin of this device. If this is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher voltage rail.

8.4 Layout

8.4.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are more than 1 inch long. These traces must be designed with a characteristic impedance of either 50Ω or 75Ω, as required by the application. Do not place this device too close to high-voltage switching components, as they may cause interference.

8.4.2 Layout Example

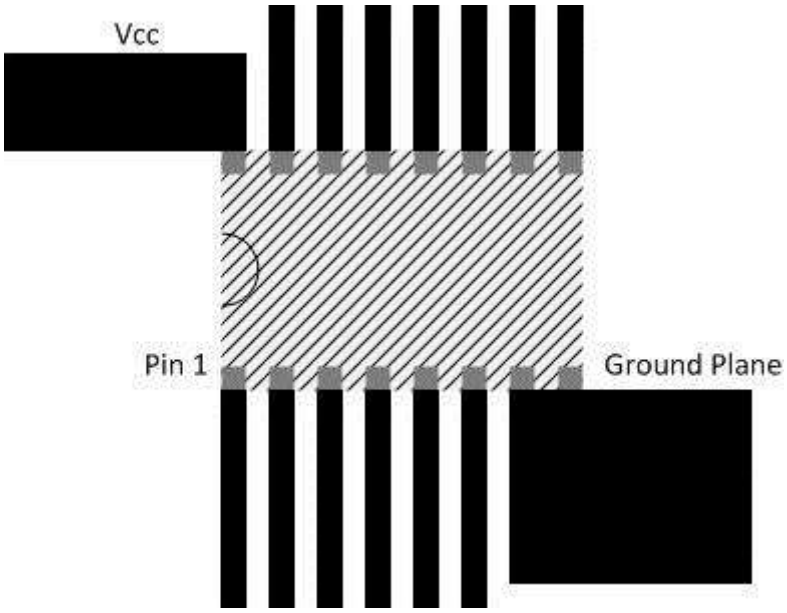


Figure 8-2. Layout Schematic

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (September 2024) to Revision H (October 2024)	Page
• Added 50mA to the Switch IO diode clamp current	4

Changes from Revision F (June 2024) to Revision G (September 2024)	Page
• Added DYY package and size	1
• Added DYY package	3
• Added new VIH and VIL Specifications at 1.65V Vcc	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CLV4051ATDWRG4Q1	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ
CLV4051ATDWRG4Q1.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ
CLV4051ATPWRG4Q1	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 105	L4051AQ
SN74LV4051AQDYYRQ1	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4051Q
SN74LV4051AQDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4051Q
SN74LV4051AQPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4051AQ1
SN74LV4051AQPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4051AQ1
SN74LV4051ATDRQ1	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ
SN74LV4051ATDRQ1.A	NRND	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ
SN74LV4051ATDWRQ1	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ
SN74LV4051ATDWRQ1.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ
SN74LV4051ATPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ
SN74LV4051ATPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4051A-Q1 :

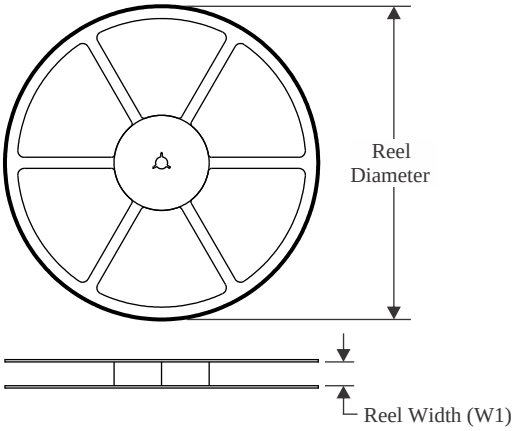
- Catalog : SN74LV4051A
- Enhanced Product : SN74LV4051A-EP

NOTE: Qualified Version Definitions:

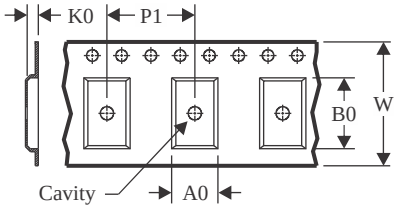
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

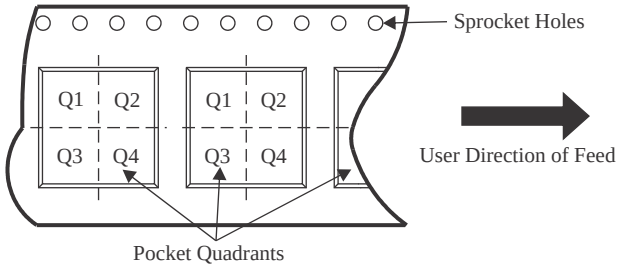


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

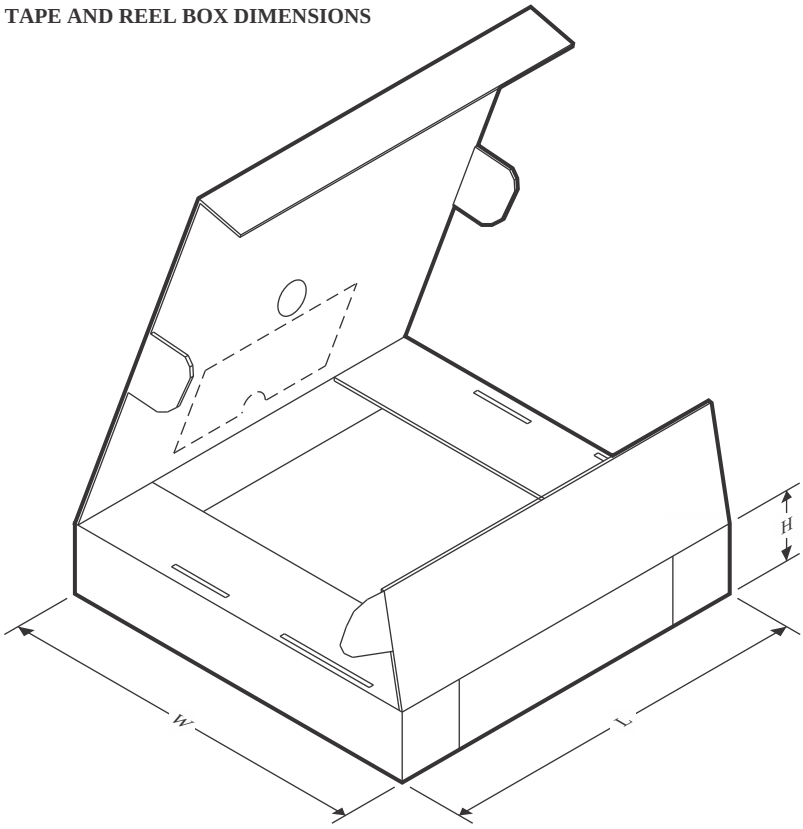
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLV4051ATDWRG4Q1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN74LV4051AQDYYRQ1	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74LV4051AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051ATDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN74LV4051ATPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

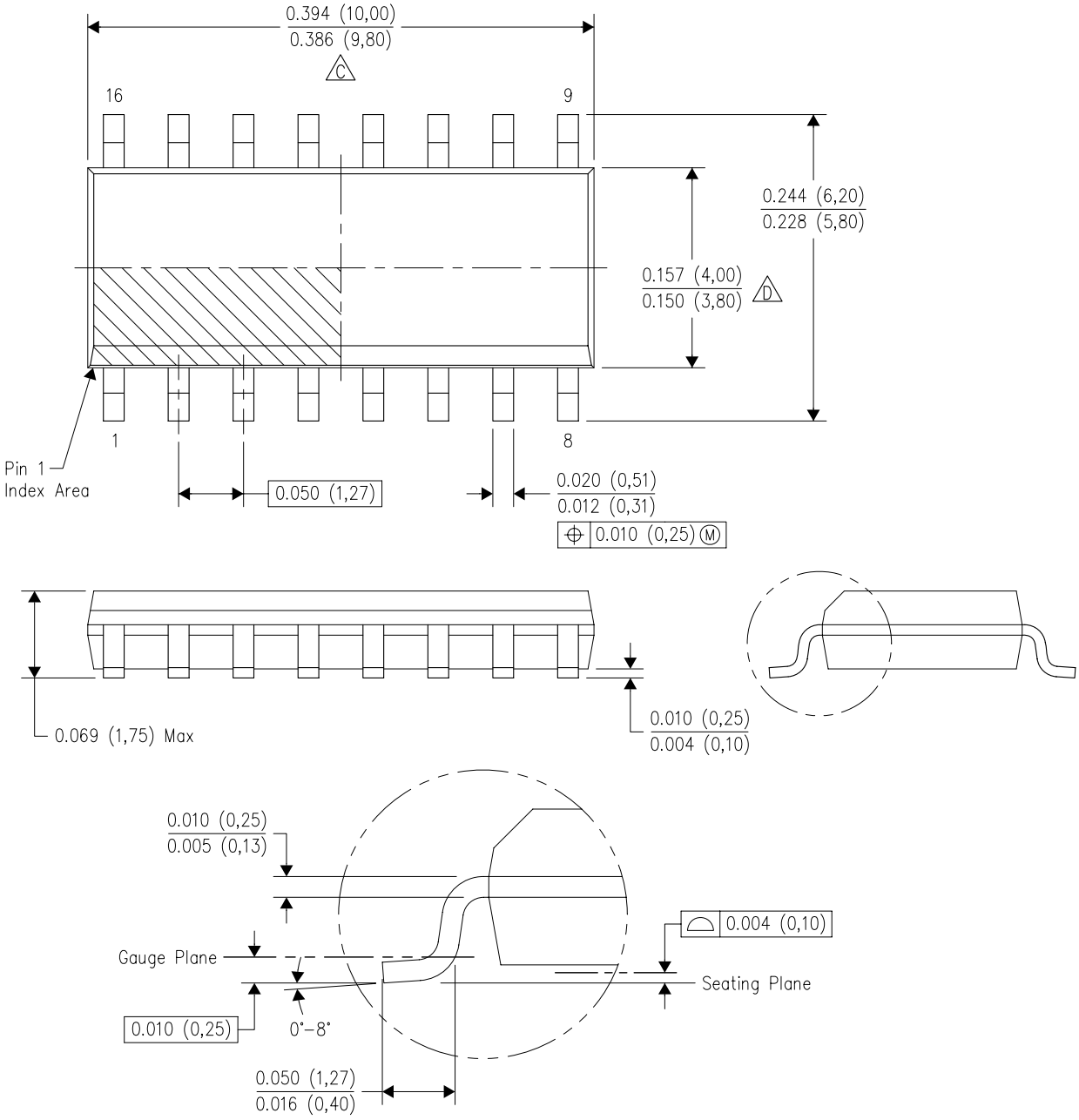
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLV4051ATDWRG4Q1	SOIC	DW	16	2000	350.0	350.0	43.0
SN74LV4051AQDYYRQ1	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74LV4051AQPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74LV4051ATDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
SN74LV4051ATPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



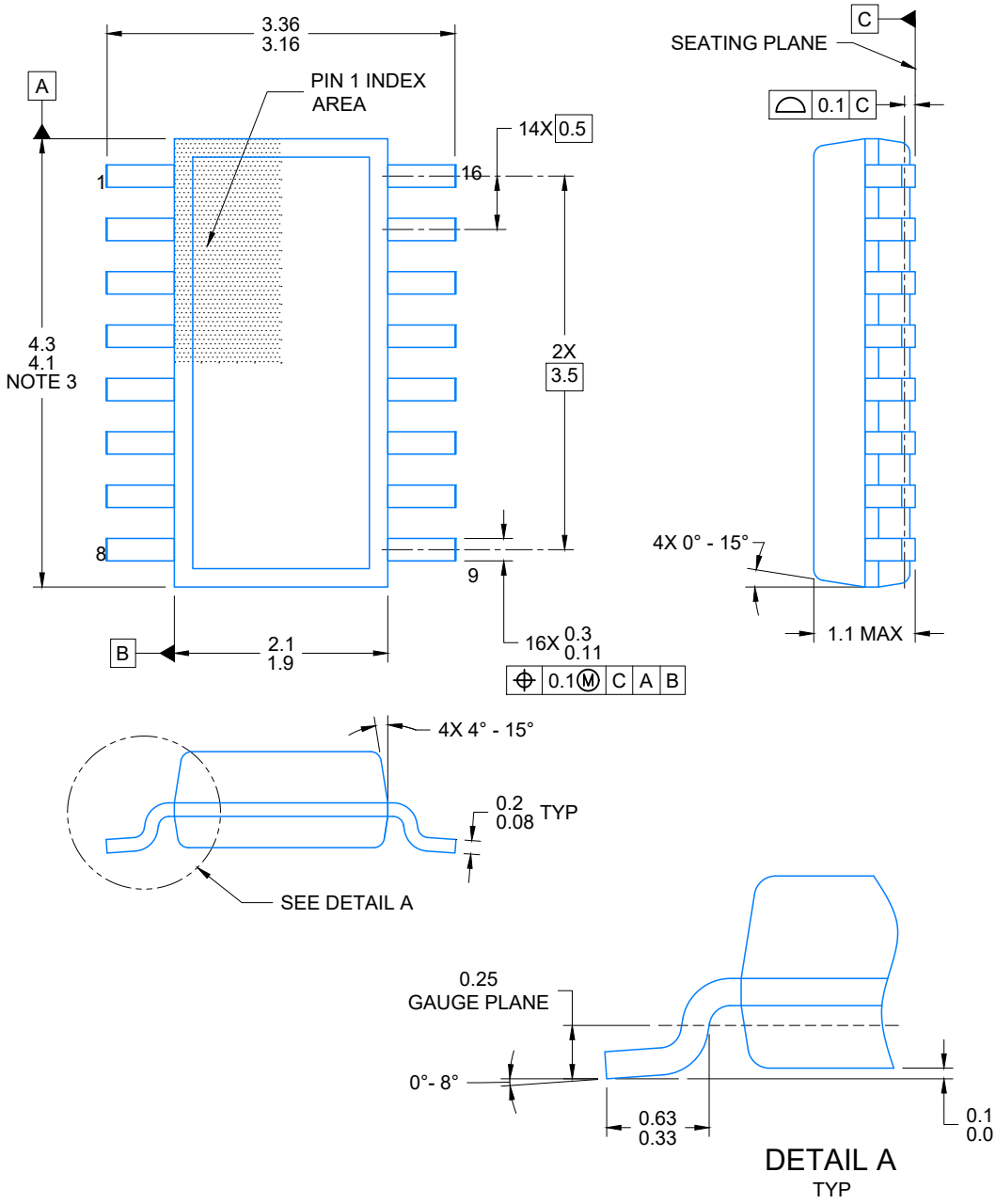
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DYY0016A

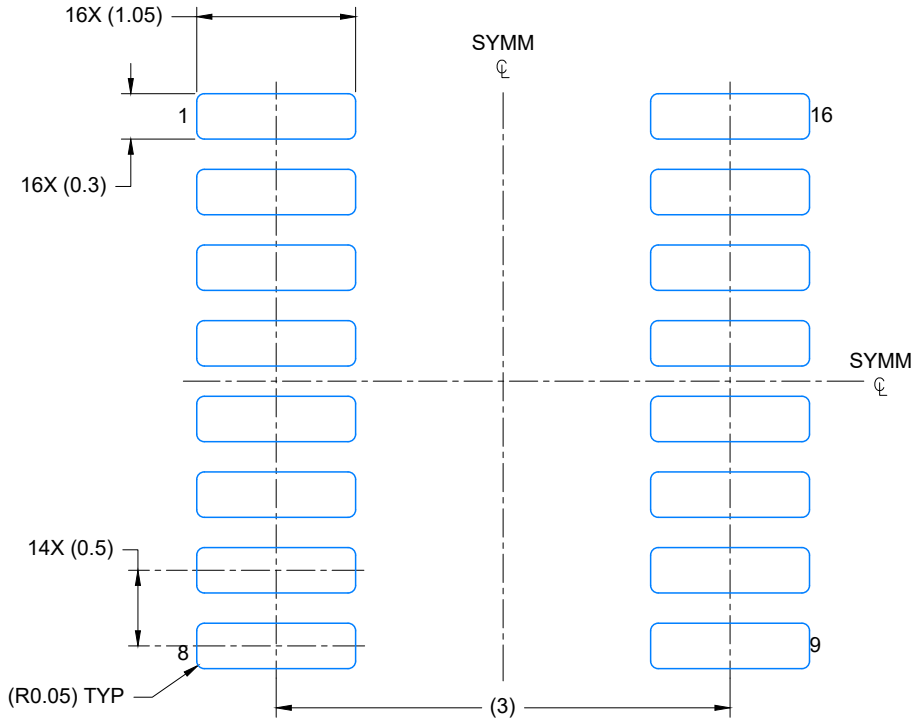
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

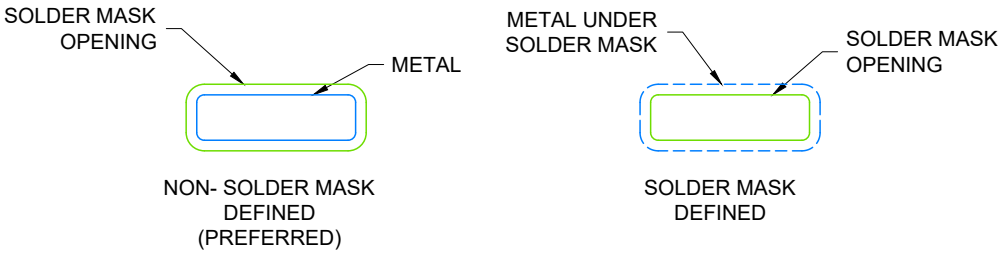


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

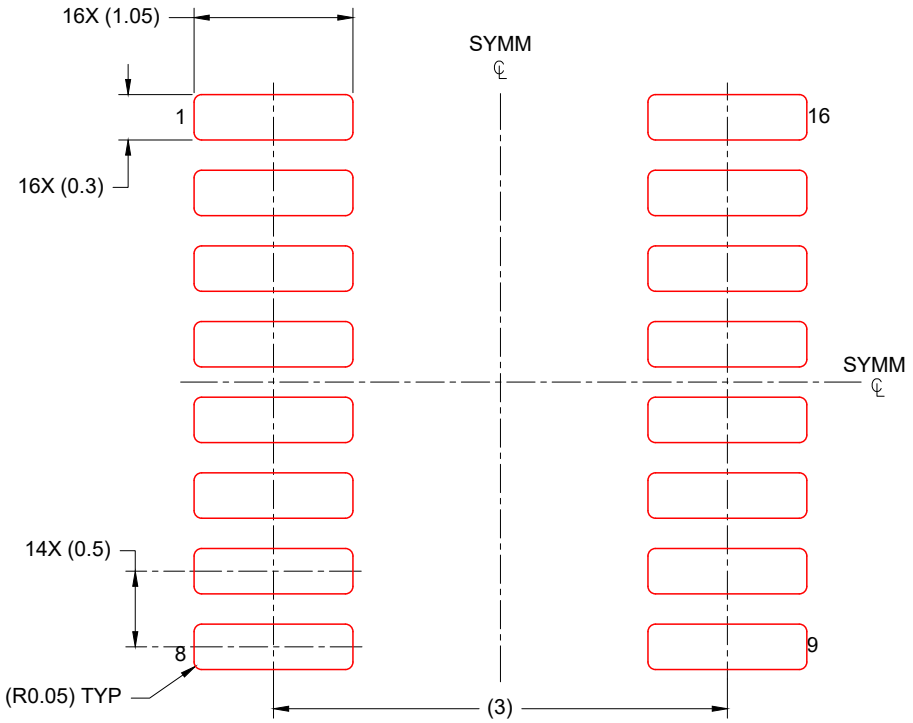
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

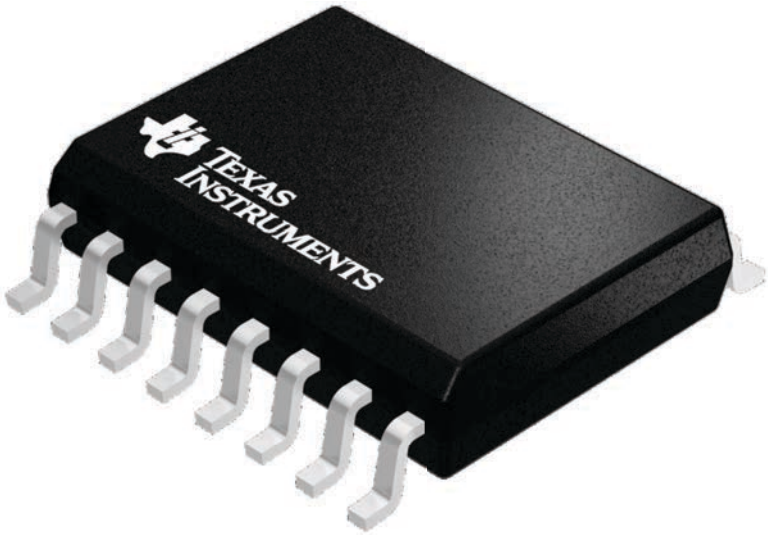
DW 16

SOIC - 2.65 mm max height

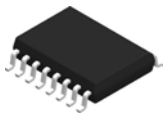
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

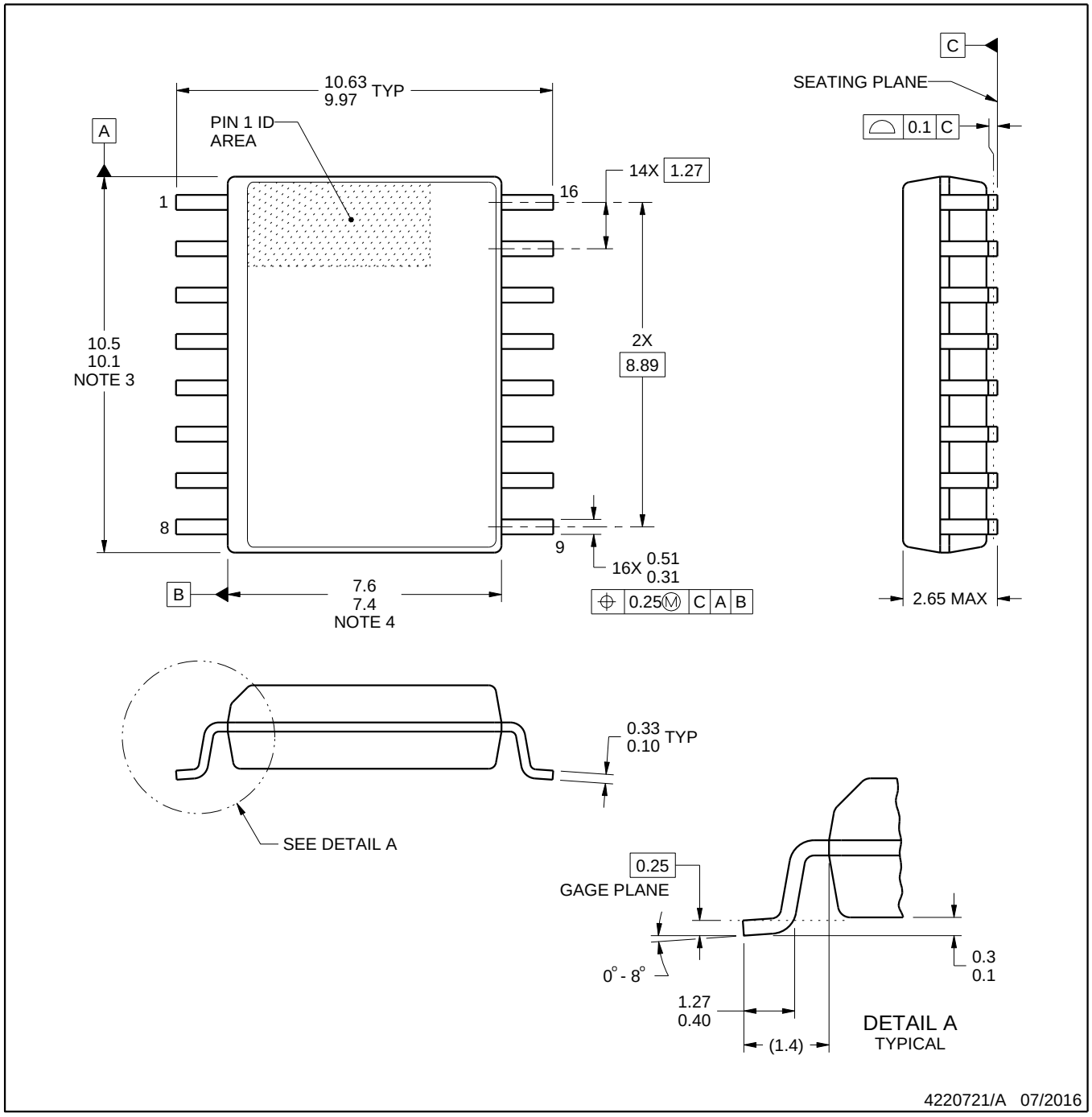


PACKAGE OUTLINE

DW0016A

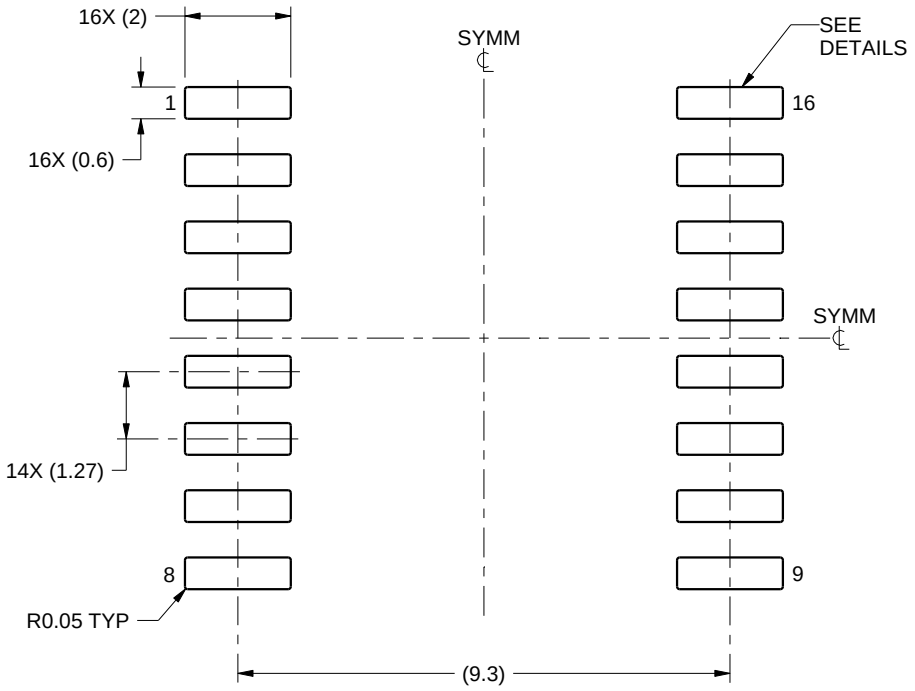
SOIC - 2.65 mm max height

SOIC

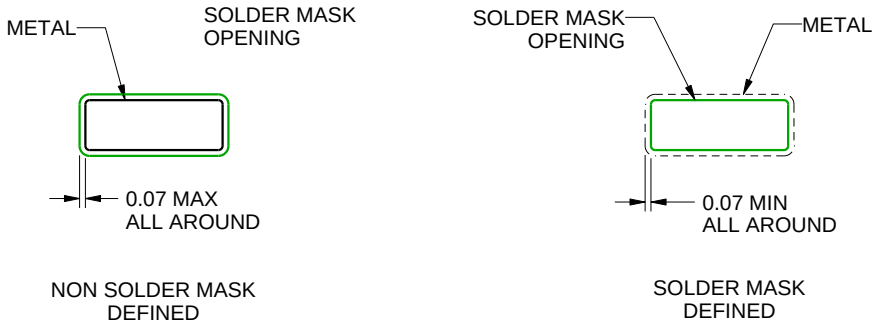


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

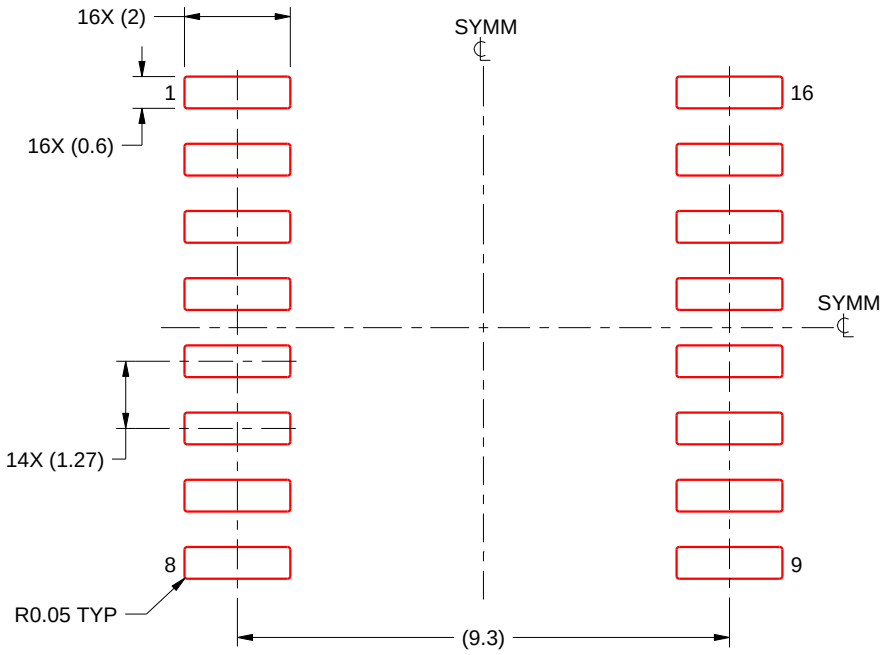


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

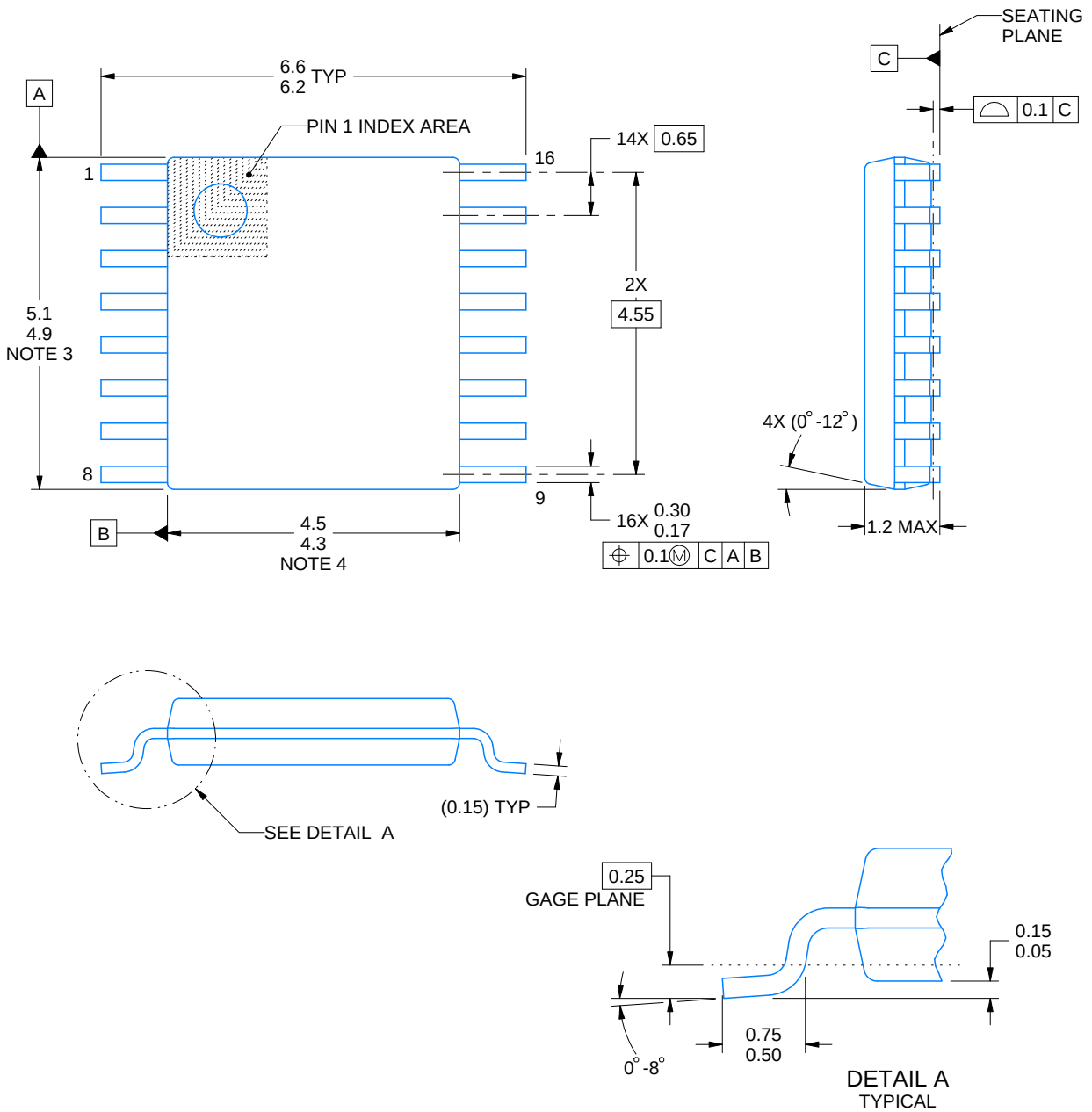
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

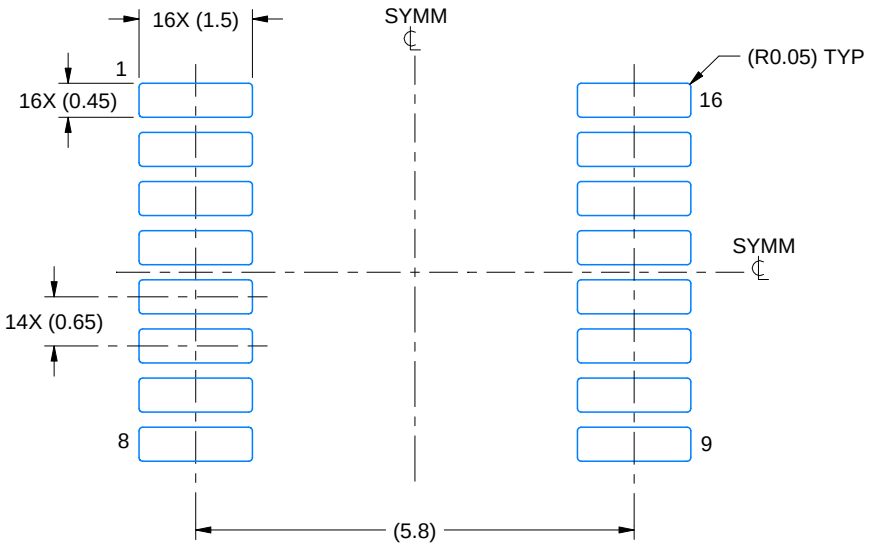
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



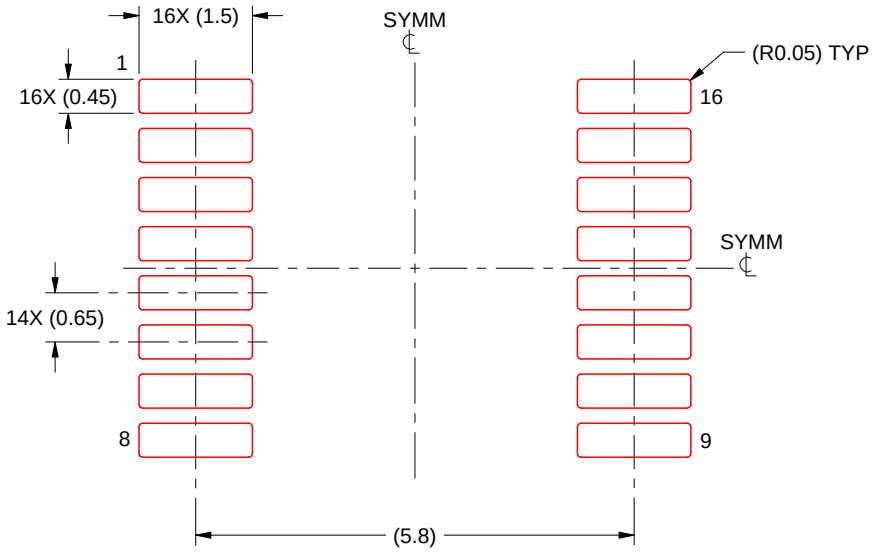
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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