SN74LV4040A 12-Bit Asynchronous Binary Counters

1 Features

- 2V to 5.5V V_{CC} operation
- Typical V_{OLP} (output ground bounce) <0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) 2.3V at V_{CC} = 3.3V, T_A = 25°C
- Support mixed-mode voltage operation on all ports
- High on-off output-voltage ratio
- Low crosstalk between switches
- Individual switch controls
- Extremely low input current
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, class II

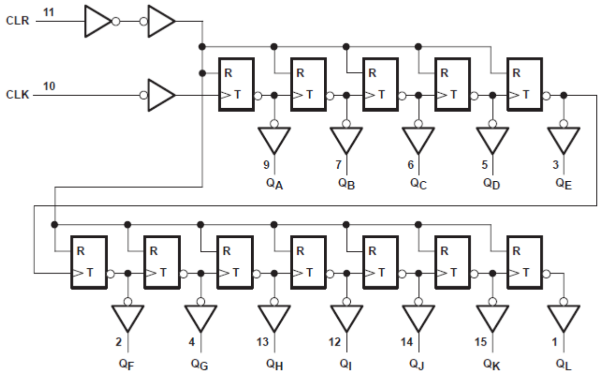
2 Description

The ’LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LV4040A	N (PDIP, 16)	19.3mm x 9.4mm	19.3mm x 6.35mm
	D (SOIC, 16)	9.9mm x 6mm	9.9mm x 3.9mm
	NS (SOP, 16)	10.2mm x 7.8mm	10.2mm x 5.3mm
	DB (SSOP, 16)	6.2mm x 7.8mm	6.2mm x 5.3mm
	PW (TSSOP, 16)	5mm x 6.4mm	5mm x 4.4mm
	DGV (TVSOP, 16)	3.6mm x 6.4mm	3.6mm x 4.4mm
	RGY (VQFN, 16)	4mm x 3.5mm	4mm x 3.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

Table of Contents

3 Pin Configuration and Functions

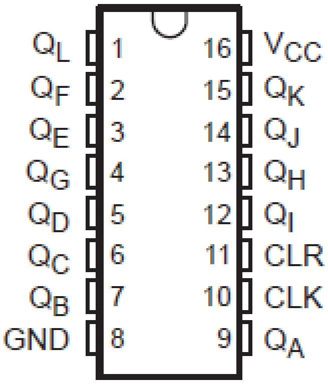
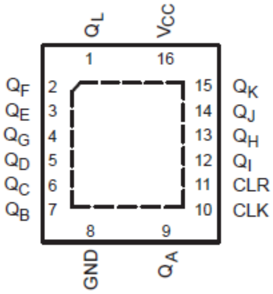


Figure 3-1. SN74LV4040A D, DB, DGV, N, NS, or PW Package (Top View)



A. NC - no internal connection

Figure 3-2. SN74LV4040A RGY Package (Top View)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
Q_L	1	O	Q_L output
Q_F	2	O	Q_F output
Q_E	3	O	Q_E output
Q_G	4	O	Q_G output
Q_D	5	O	Q_D output
Q_C	6	O	Q_C output
Q_B	7	O	Q_B output
GND	8	-	Ground
Q_A	9	O	Q_A output
CLK	10	I	Clock, falling edge triggered
CLR	11	I	Clear, active high
Q_I	12	O	Q_I output
Q_H	13	O	Q_H output
Q_J	14	O	Q_J output
Q_K	15	O	Q_K output
V_{CC}	16	-	Positive supply

(1) I = input, O = output

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range		-0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	7	V
V_O	Output voltage range		−0.5 V to V_{CC}	0.5	V
I_{IK}	Input clamp current(2)	(V_I < 0)		−20	mA
I_{OK}	Output clamp current(2)	(V_O < 0)		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		-65	150	℃

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		− 50	µA
		V_{CC} = 2.3 V to 2.7 V		− 2	mA
		V_{CC} = 3 V to 3.6 V		− 6	
		V_{CC} = 4.5 V to 5.5 V		− 12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	
		V_{CC} = 2.3 V to 2.7 V		2	
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	

4.3 Recommended Operating Conditions (continued)

over recommended operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Δt/Δv	Input transition rise/fall time	V_{CC} = 2.3 V to 2.7 V		200	ns
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		-40	85	℃

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC[1]		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.5	82	120	67	64	122.3	39	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics.*

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN74LV4040A MIN	SN74LV4040A TYP	SN74LV4040A MAX	UNIT
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC} − 0.1			V
	I_{OH} = −2 mA	2.3 V	2			
	I_{OH} = −6 mA	3 V	2.48			
	I_{OH} = −12 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4	
	I_{OL} = 6 mA	3 V			0.44	
	I_{OL} = 12 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		1.9		pF

4.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

			T_A = 25℃ MIN	T_A = 25℃ MAX	SN74LV4040A MIN	SN74LV4040A MAX	UNIT
t_w	Pulse duration	CLK high or low	7		7		ns
		CLR high	6.5		6.5		
t_{su}	Setup time	CLR inactive before CLK↓	6.5		6.5		

4.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

			T_A = 25℃		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t_{su}	Setup time	CLR inactive before CLK↓	5		5		

4.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			T_A = 25℃		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t_{su}	Setup time	CLR inactive before CLK↓	5		5		

4.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25℃			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	50 [1]	115 [1]		40 [1]		MHz
			C_L = 50 pF	40	95		35		
t_{PLH}	CLK	Q_A	C_L = 15 pF		8.7 [1]	19.4 [1]	1 [1]	23 [1]	ns
t_{PHL}					8.7 [1]	19.4 [1]	1 [1]	23 [1]	
t_{PHL}	CLR	Any Q	C_L = 15 pF		9.3 [1]	19.9 [1]	1 [1]	24 [1]	
t_{PLH}	$\overline{\text{CLK}}$	Q_A	C_L = 50 pF		10.5	24.1	1	28	
t_{PHL}					10.5	24.1	1	28	
t_{PHL}	CLR	Any Q	C_L = 50 pF		11.7	24.5	1	28	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		1.7	5.9		7	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 (unless otherwise noted) (Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25℃			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	75 [1]	160 [1]		75		MHz
			C_L = 50 pF	55	130		50		
t_{PLH}	CLK	Q_A	C_L = 15 pF		6.1 [1]	11.9 [1]	1	14	ns
t_{PHL}					6.1 [1]	11.9 [1]	1	14	ns
t_{PHL}	CLR	Any Q	C_L = 15 pF		7.1 [1]	12.8 [1]	1	15	ns
t_{PLH}	$\overline{\text{CLK}}$	Q_A	C_L = 50 pF		7.5	15.4	1	17.5	ns
t_{PHL}					7.5	15.4	1	17.5	ns
t_{PHL}	CLR	Any Q	C_L = 50 pF		9	16.3	1	18.5	ns

4.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V (continued)

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 (unless otherwise noted) (Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25℃			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		1.2	4.4		5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25℃			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	150 [1]	235 [1]		125		MHz
			C_L = 50 pF	95	185		80		
t_{PLH}	CLK	Q_A	C_L = 15 pF		4.2 [1]	7.3 [1]	1	8.5	ns
t_{PHL}					4.2 [1]	7.3 [1]	1	8.5	ns
t_{PHL}	CLR	Any Q	C_L = 15 pF		5.3 [1]	8.6 [1]	1	10	ns
t_{PLH}	$\overline{\text{CLK}}$	Q_A	C_L = 50 pF		5.3	9.3	1	10.5	ns
t_{PHL}					5.3	9.3	1	10.5	ns
t_{PHL}	CLR	Any Q	C_L = 50 pF		6.8	10.6	1	12	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		0.8	3.1		3.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.12 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER(1)		SN74LV4040A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		− 0.5	− 0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

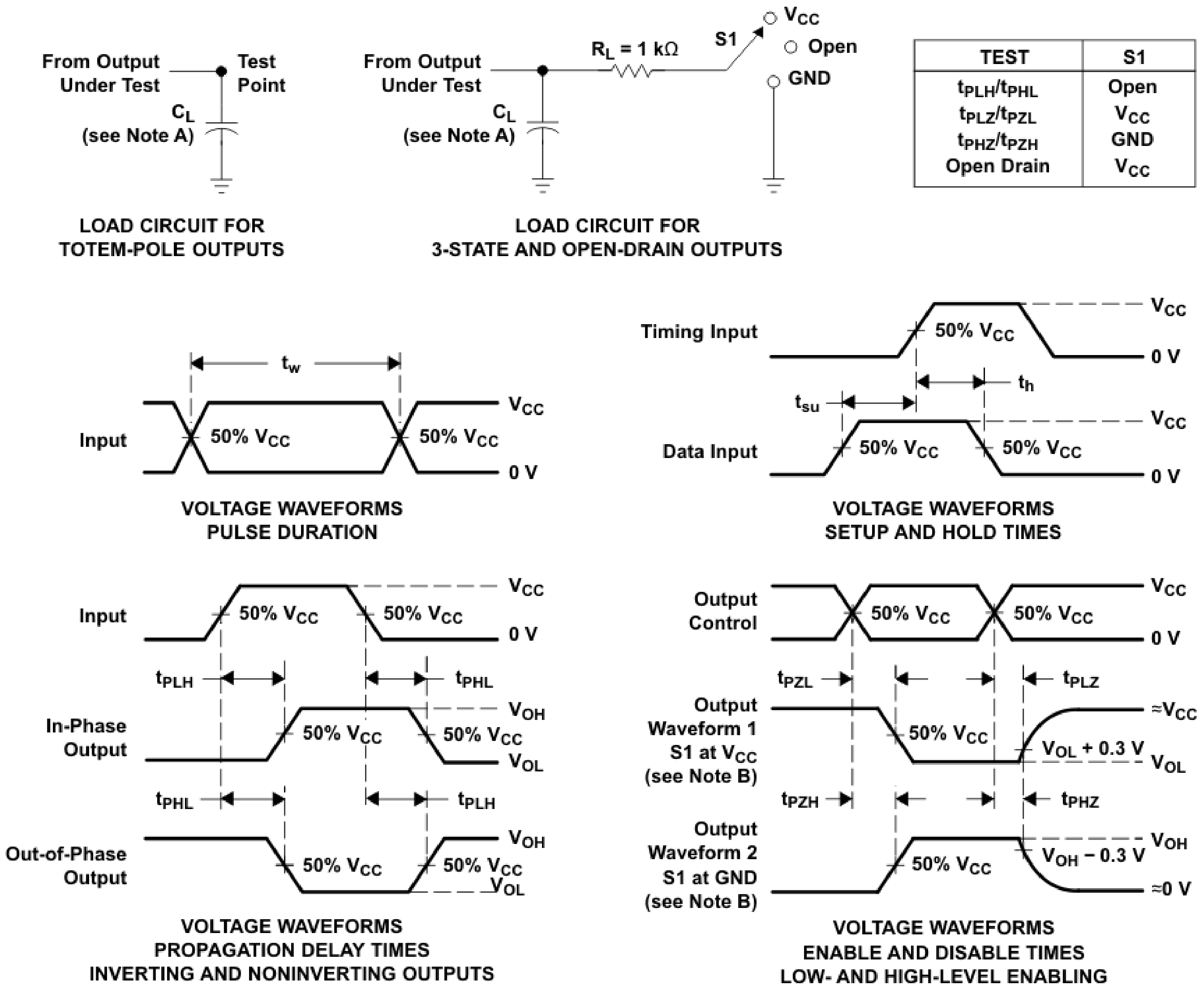
(1) Characteristics for surface-mount packages only.

4.13 Operating Characteristics

T_A = 25℃

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	11.9	pF
				5 V	13.1	

5 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.

D. The outputs are measured one at a time, with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PHL} and t_{PLH} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

The ’LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

6.2 Functional Block Diagram

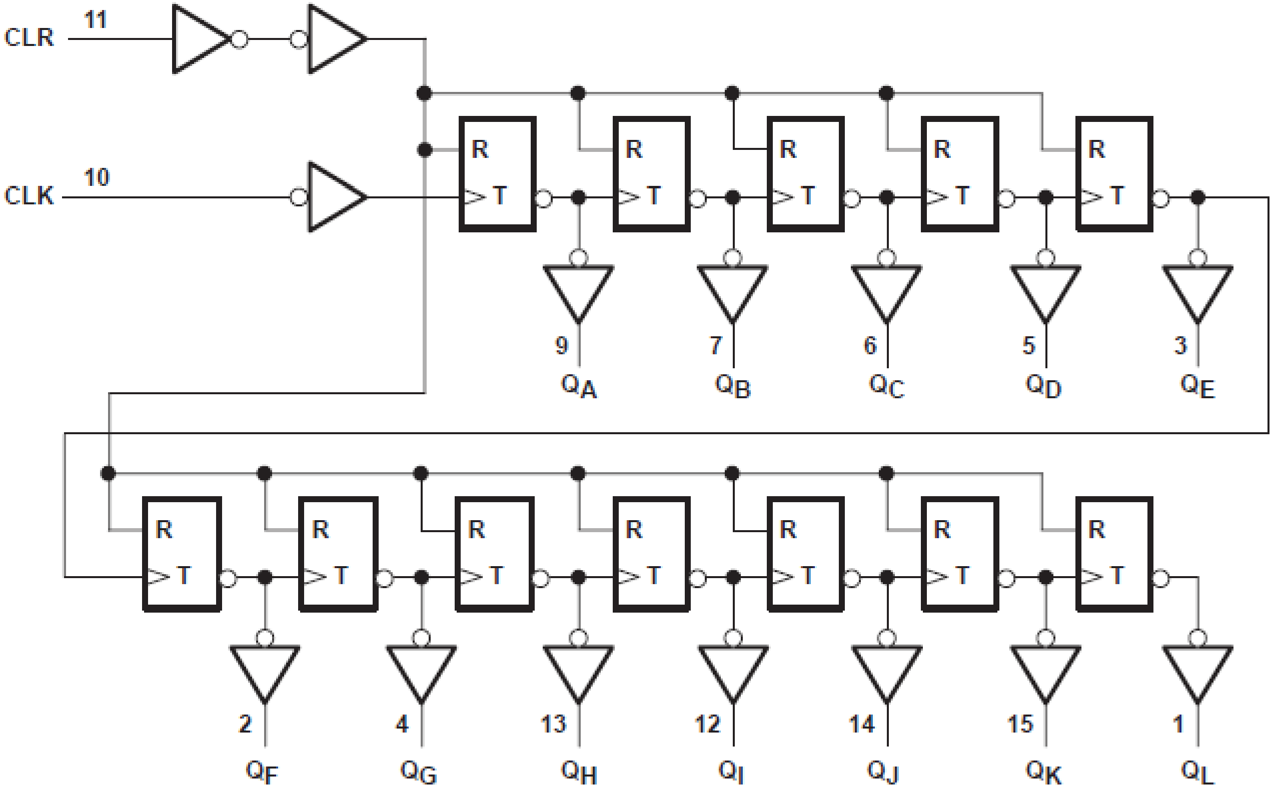


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table (Each Buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV4040A	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (July 2023) to Revision K (September 2024) **Page**

- Added body size to *Package Information* table.. 1
- Updated *Pin Functions* table.. 3
- Added *Application and Implementation* section...10

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4040AD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	LV4040A
SN74LV4040ADBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ADBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ADGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ADGVR.A	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4040A
SN74LV4040ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4040A
SN74LV4040AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4040AN
SN74LV4040AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4040AN
SN74LV4040ANSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4040A
SN74LV4040ANSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4040A
SN74LV4040APW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	LW040A
SN74LV4040APWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040APWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040APWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040APWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040APWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	LW040A
SN74LV4040ARGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ARGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ARGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ARGYRG4.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

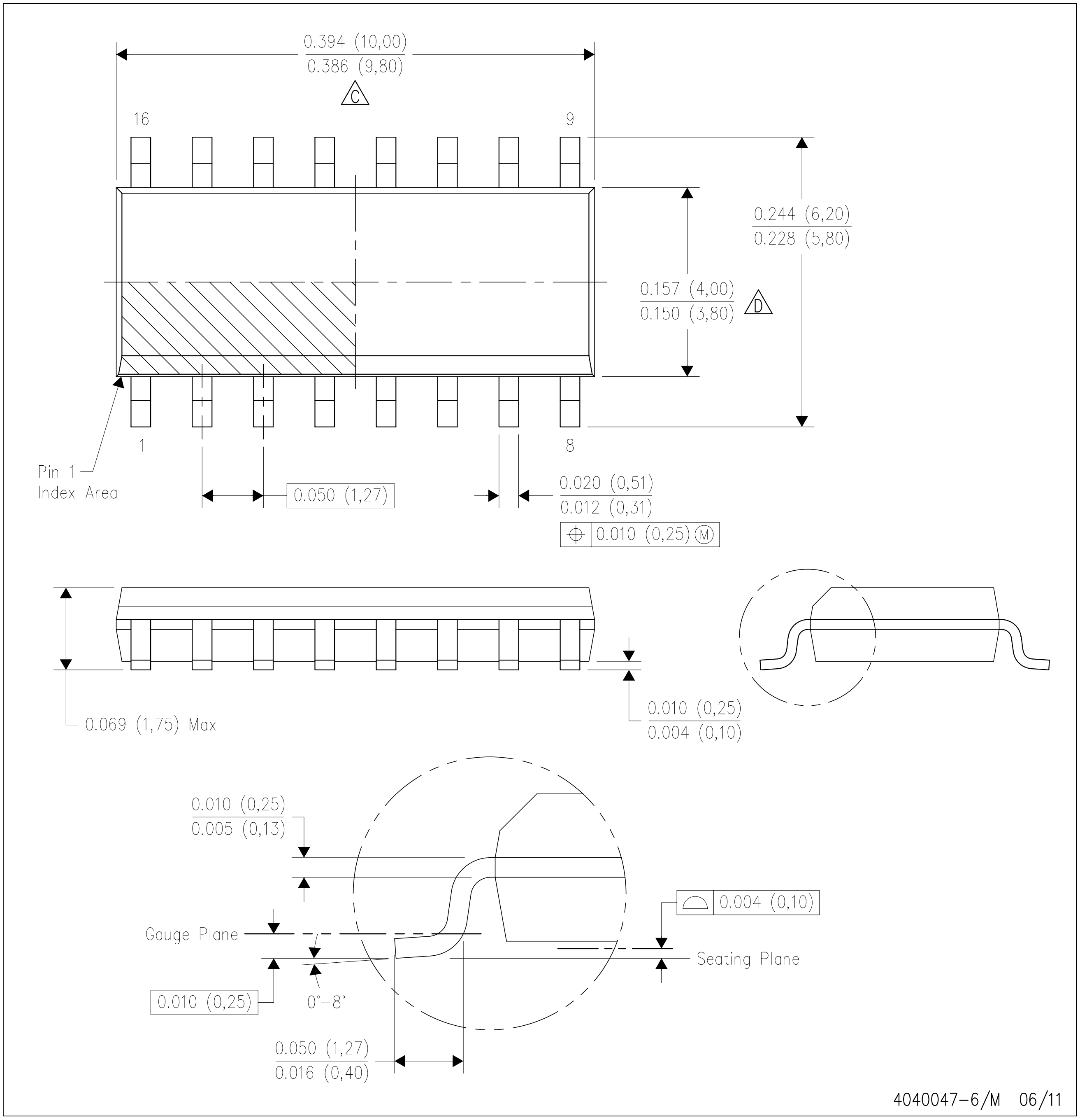
OTHER QUALIFIED VERSIONS OF SN74LV4040A :

- Enhanced Product : SN74LV4040A-EP

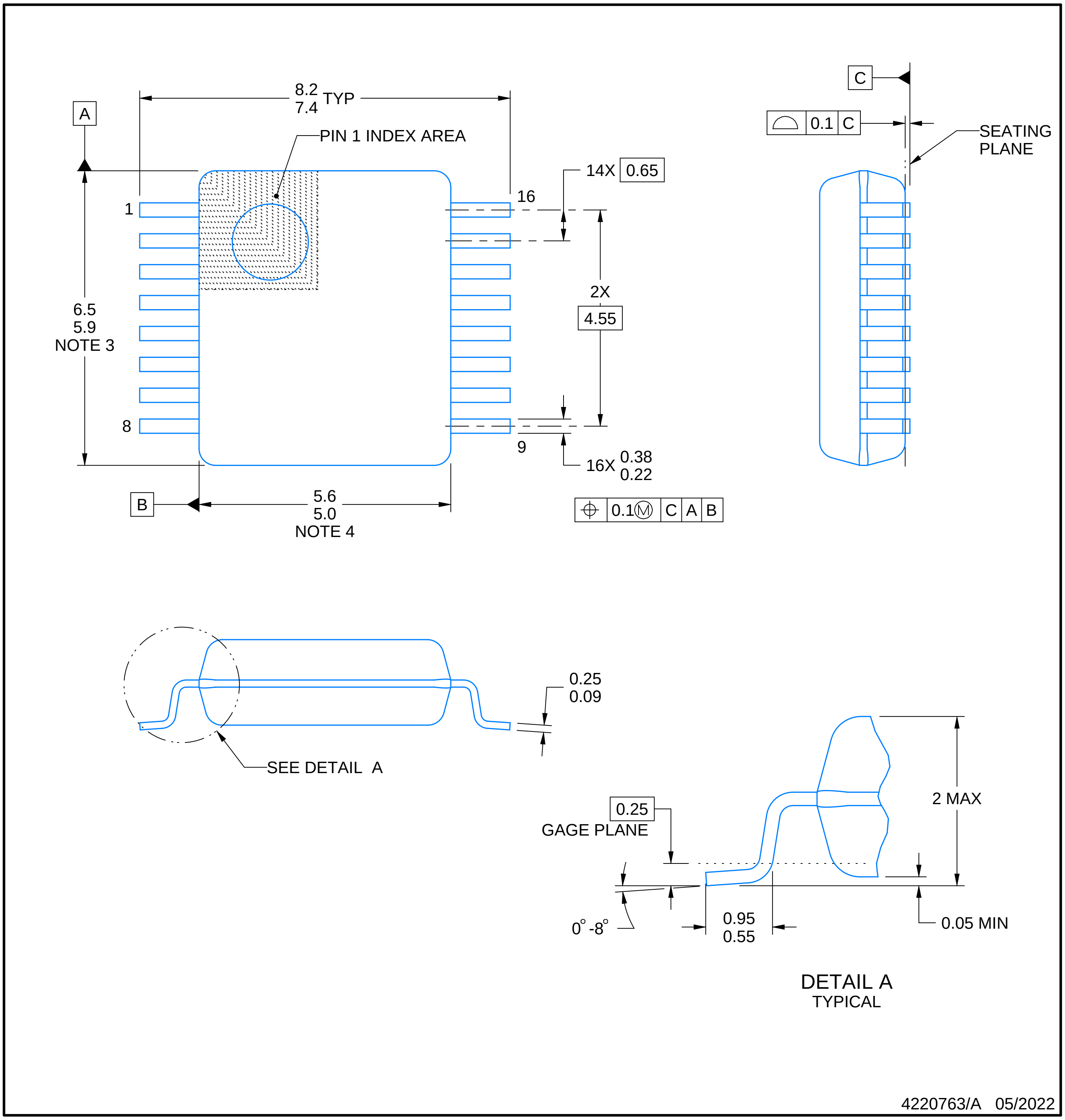
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

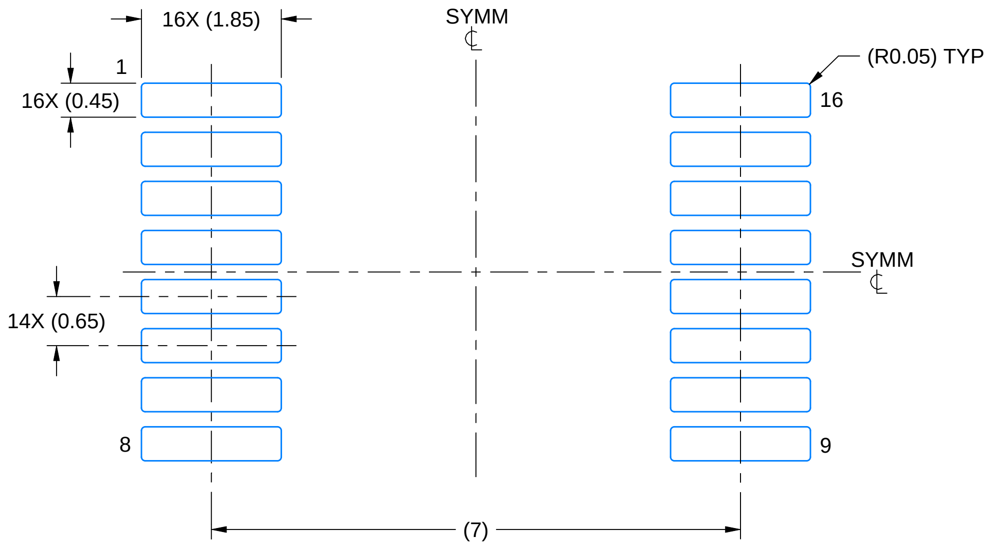


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.

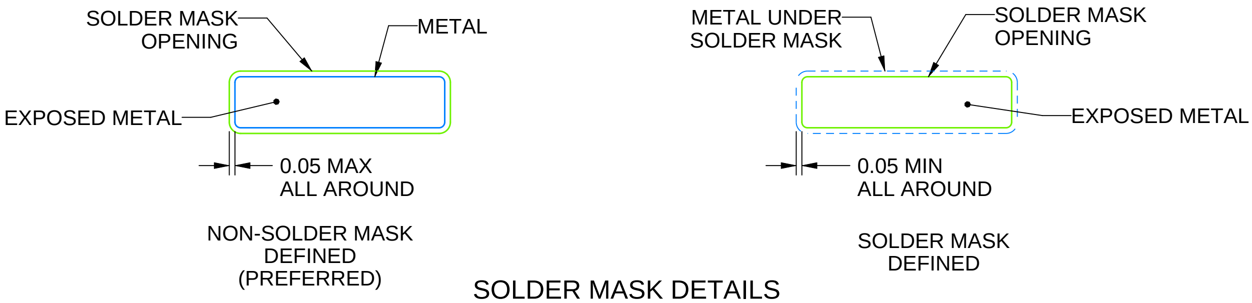


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

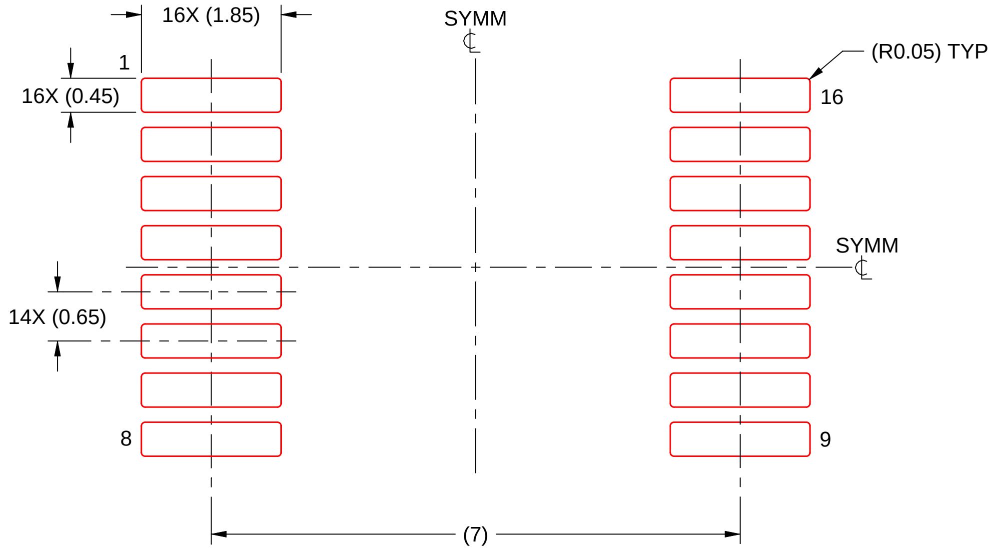


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

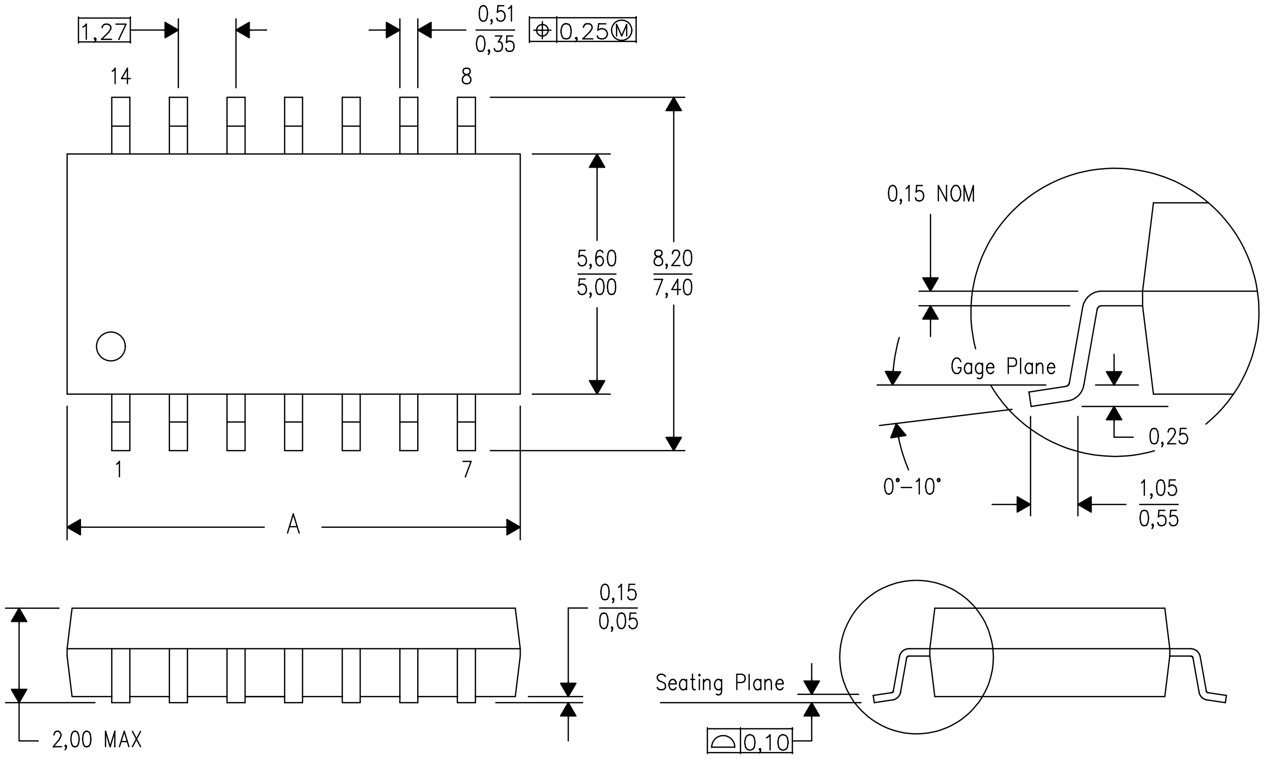
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



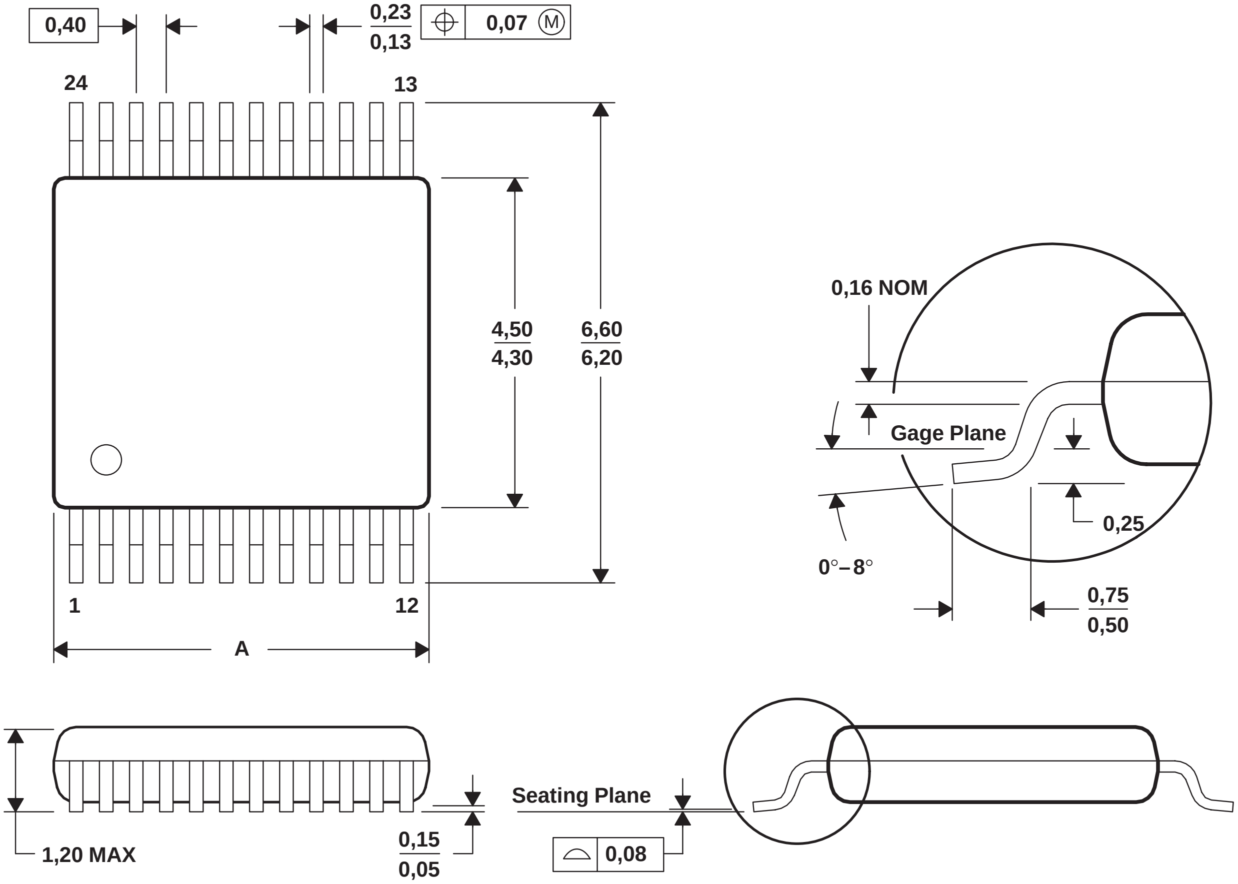
PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN

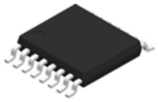


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

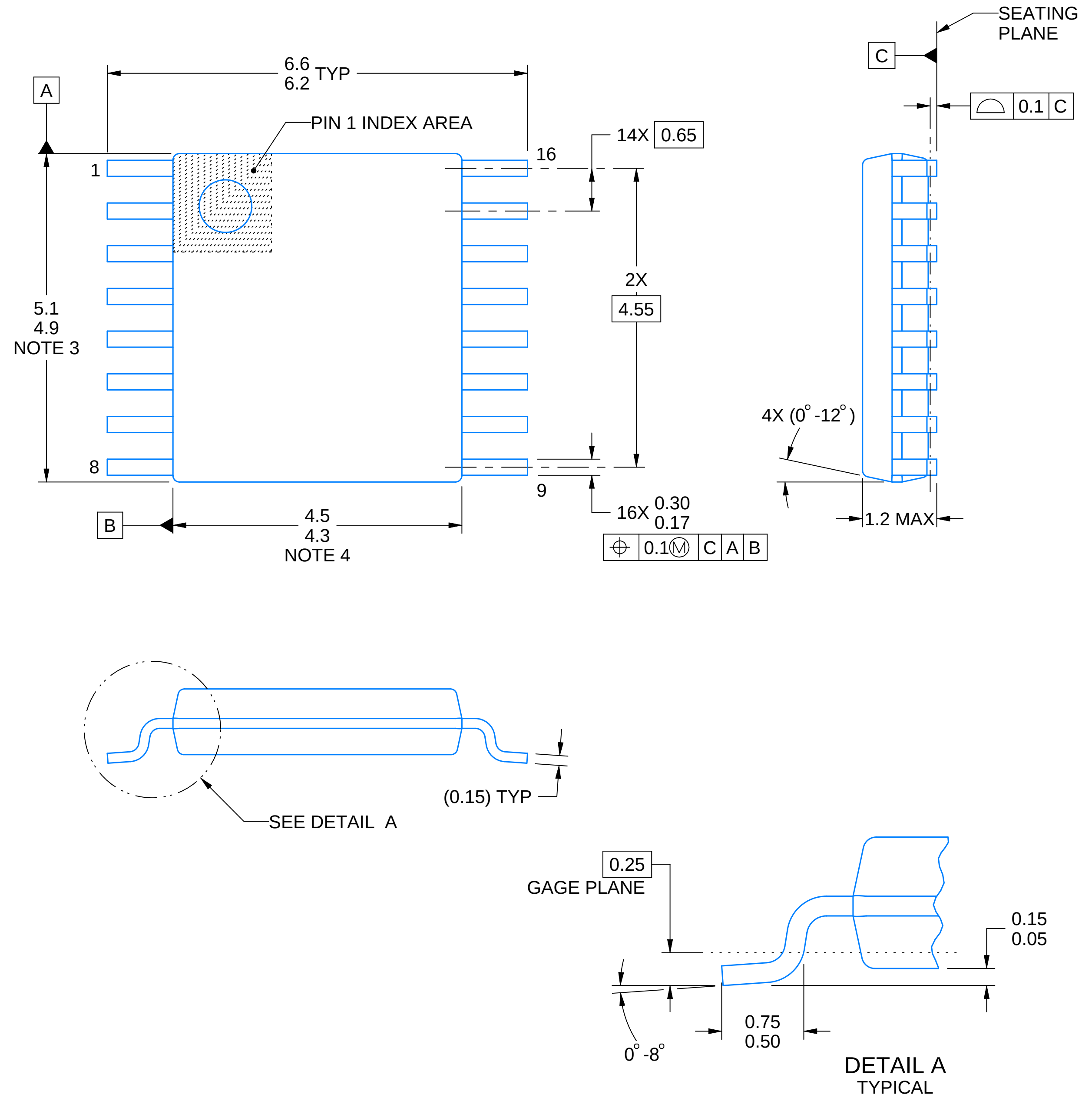
PACKAGE OUTLINE



PW0016A

TSSOP - 1.2 mm max height

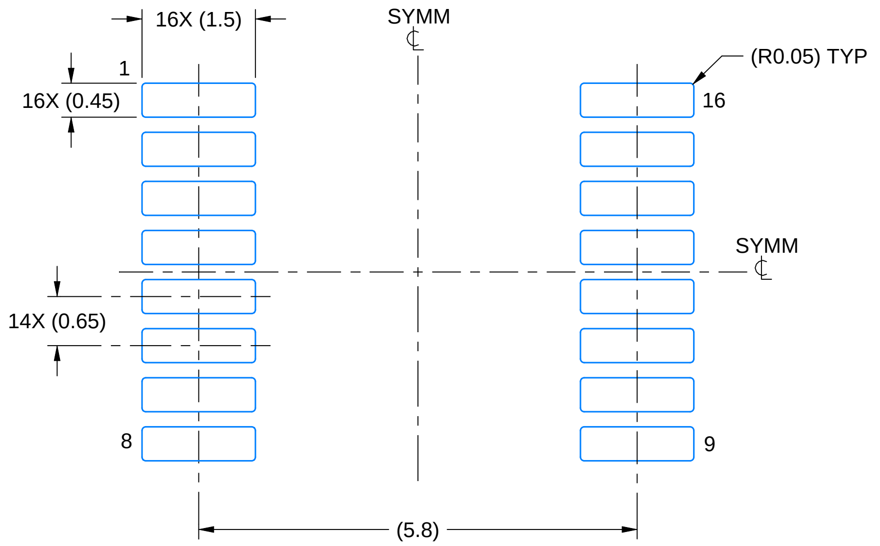
SMALL OUTLINE PACKAGE



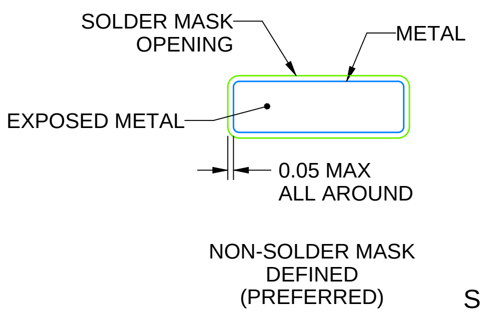
4220204/B 12/2023

NOTES:

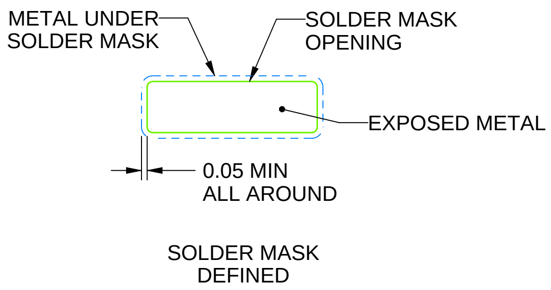
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)



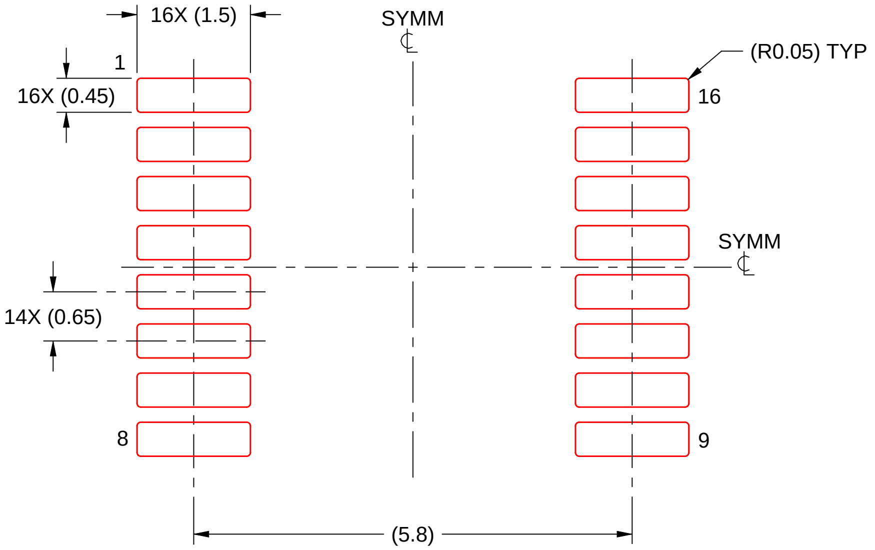
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

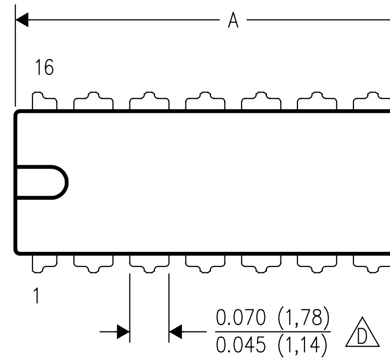
4220204/B 12/2023

NOTES: (continued)

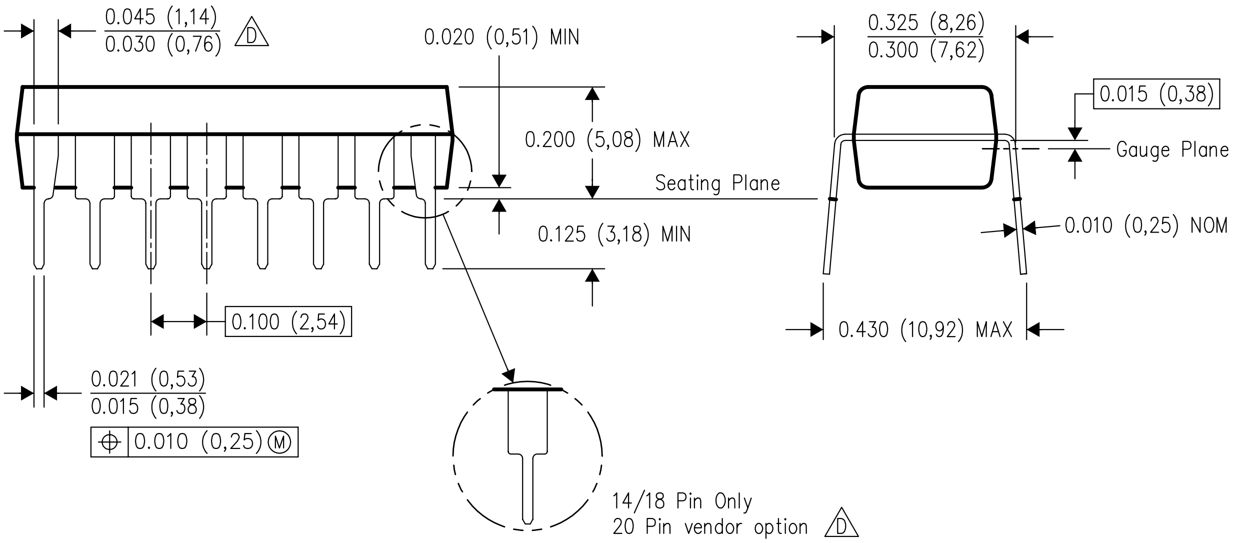
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



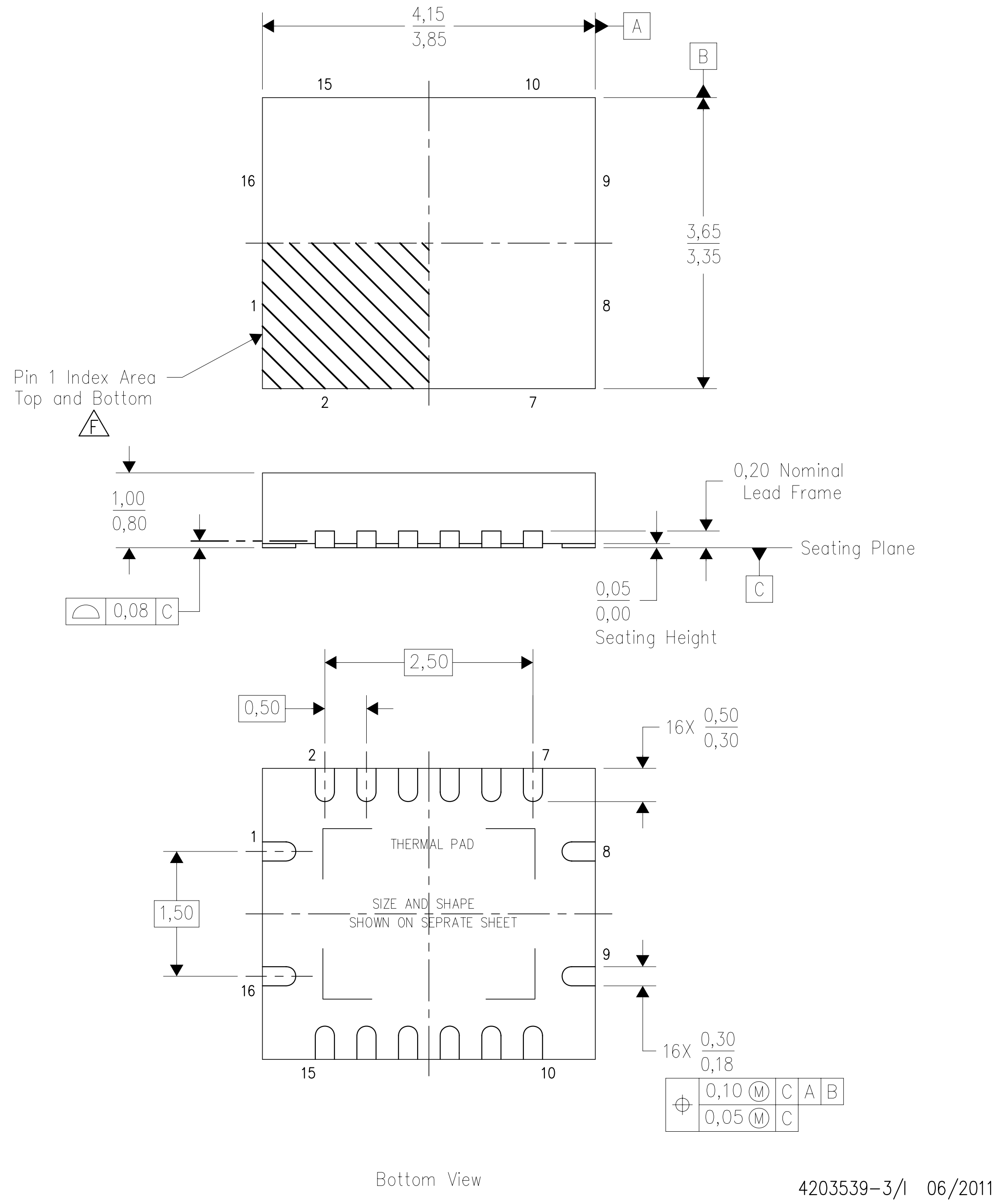
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

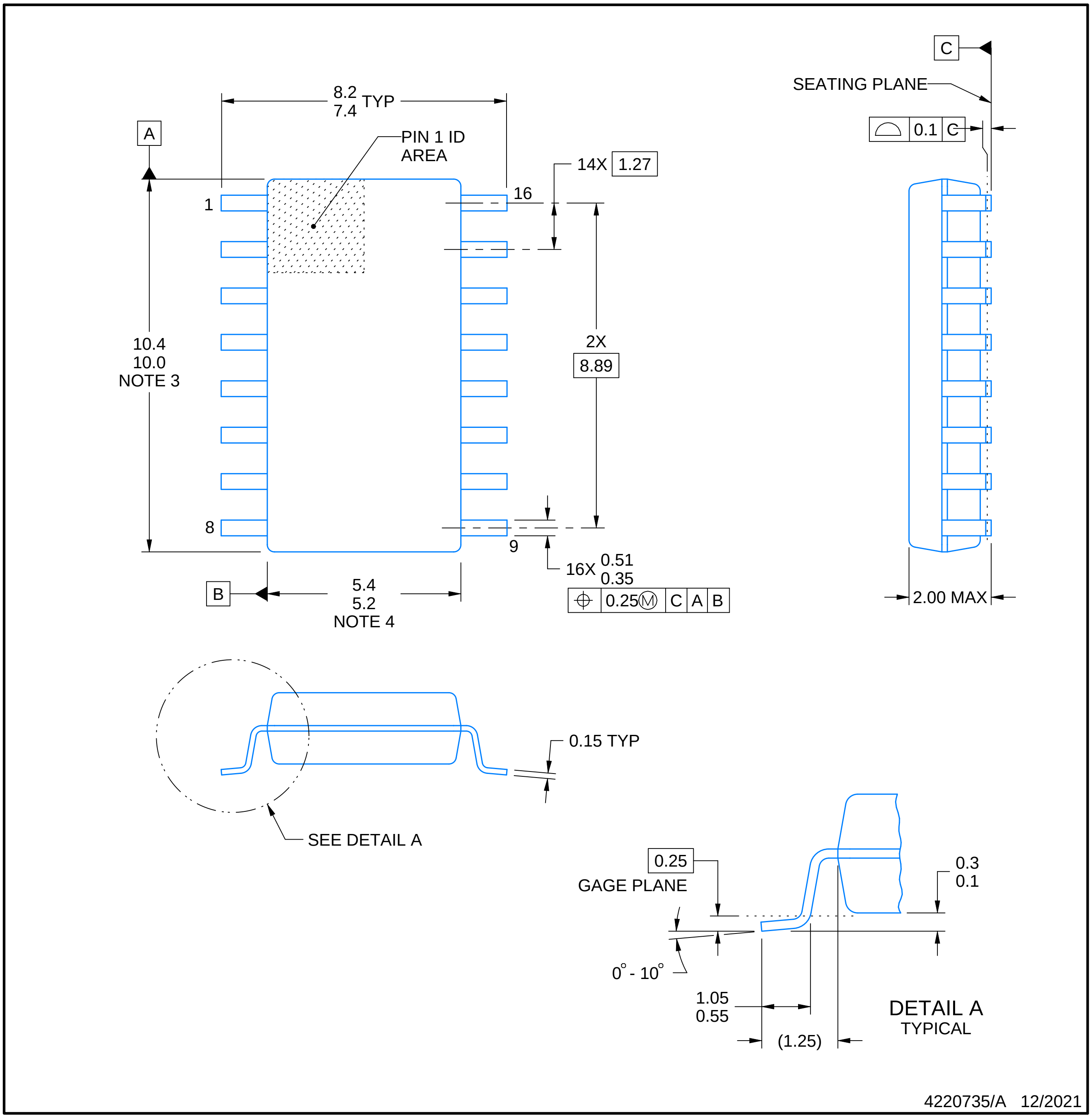


NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO–241 variation BA.

PACKAGE OUTLINE

SOP - 2.00 mm max height

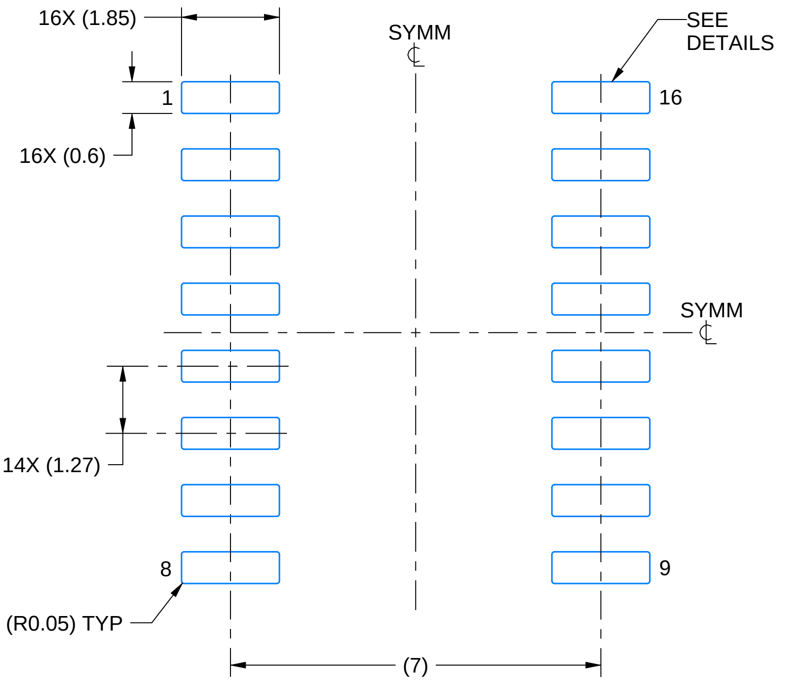
SOP



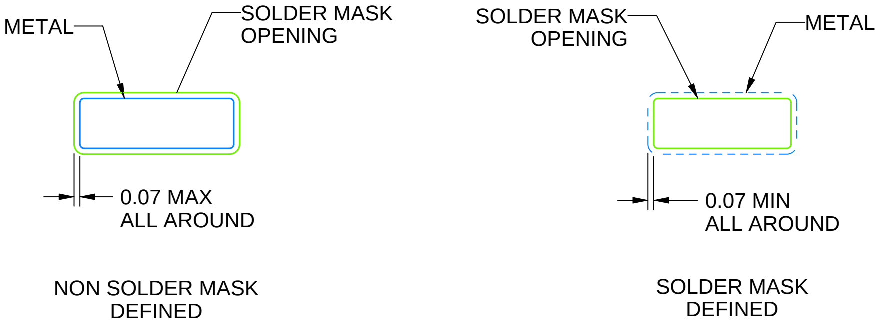
4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

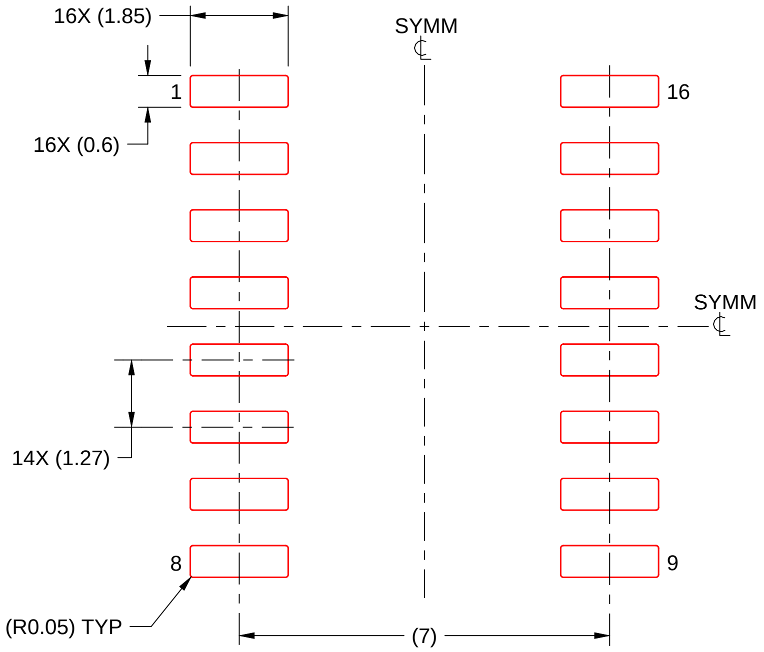


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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